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Spotlight on Applications

Printed 1T1R Arrays for Next-Generation Electronics

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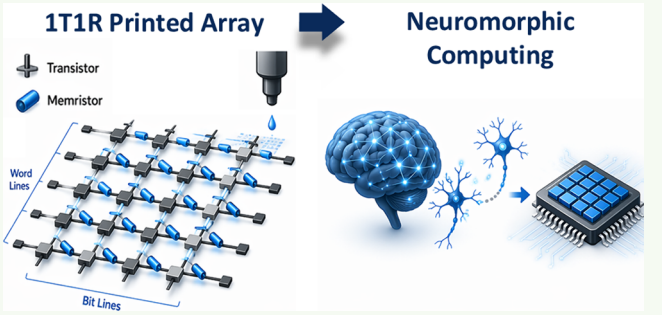
ABSTRACT: The increasing demand for energy-efficient and high-density hardware driven by artificial intelligence and the Internet of Things has exposed the limitations of conventional computing systems based on the von Neumann architecture. Consequently, neuromorphic computing has emerged as a promising paradigm, enabling in-memory data processing inspired by biological systems. The memristive array is one of the most promising hardware solutions for implementing various neuromorphic algorithms. Among the different unit cell configurations constituting a memristive array, the 1T1R architecture, combining a transistor and a memristor, has demonstrated significant potential due to its ability to provide controllable operation and reduced crosstalk. At the same time, printed electronics has gained attention as a low-cost and scalable fabrication approach, compatible with flexible substrates and low-temperature processing. However, the implementation of 1T1R structures using printing techniques introduces several challenges, including ink formulation, interfacial compatibility between printed layers, and multilayer alignment. This perspective provides an overview of 1T1R architectures with a particular focus on their fabrication through printing-based methods. The device structure, electrical performance, and integration strategies are discussed, along with the main challenges associated with printed techniques. The potential of 1T1R structures for applications in neuromorphic hardware, analog computing, and flexible IoT platforms is highlighted, outlining future directions toward scalable and low-power printed electronic systems.



KEYWORDS: *printed electronics, thin-film transistor, memristor, 1T1R, printed arrays*

1. INTRODUCTION

Currently, the rapid growth of artificial intelligence is driving demand for devices that combine low power consumption with high integration density.[1] Conventional computing systems based on the von Neumann architecture are becoming progressively less efficient for data-intensive tasks. In this architecture, the physical separation of the processor and the memory unit leads to frequent data transfers between these two blocks, creating a communication bottleneck that limits processing speed and increases energy consumption.[2]

To overcome these limitations and address the growing technological demands, alternative computing paradigms have been explored, where neuromorphic computing has gained significant attention, illustrated in the schematic in Figure 1a.[3] This approach aims to emulate the operational principles of the human brain, which can process large volumes of information with remarkable speed while maintaining extremely low power consumption. In neuromorphic systems, memory and processing functionalities are co-located within the same physical hardware, enabling more efficient data handling by reducing both latency and energy consumption during computation.[4]

Neuromorphic algorithms can be implemented using CMOS technology. However, in conventional CMOS architectures, memory and processing are still physically separated. As a result, synaptic weights must be stored in memory and continuously transferred during computation (e.g., inference). Therefore, replicating neuronal and synaptic functions using CMOS is resource-intensive, often requiring large numbers of transistors, capacitors, and other components.[5] Memristors have emerged as promising candidates for neuromorphic hardware.[6] These devices generally consist of a simple metal−insulator−metal (MIM) structure and exhibit intrinsic resistive switching behavior, enabling them to store information in a non-volatile manner.[7] Memristive devices offer several advantages for neuromorphic systems, including non-volatile weight storage, fast parallel matrix multiplication, and ultrahigh

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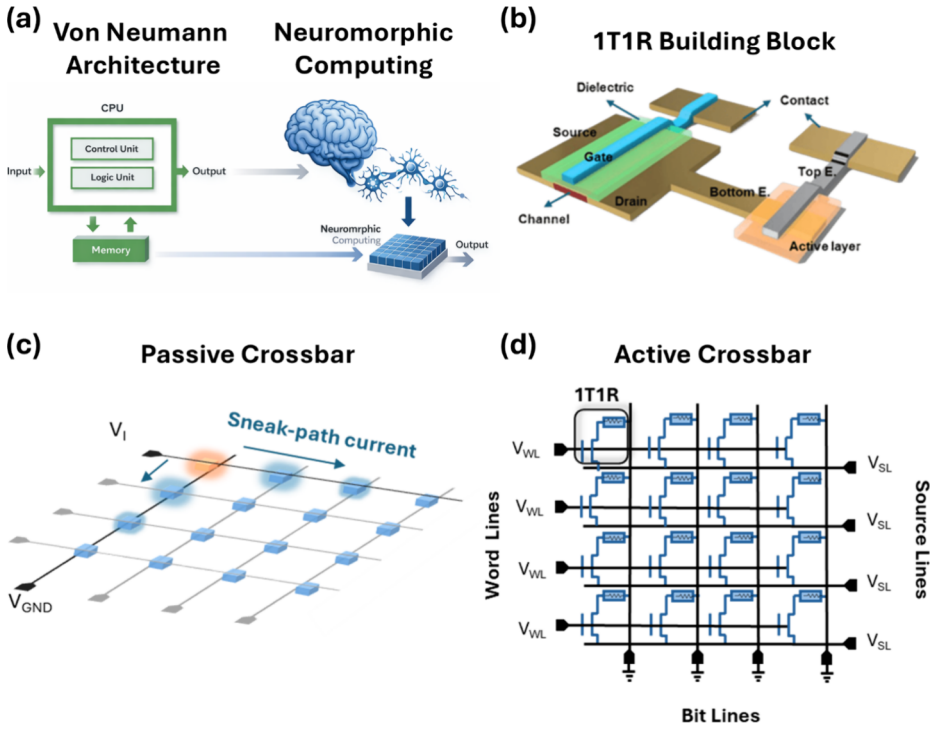

Figure 1. Schematic of (a) Von Neumann architecture compared with the neuromorphic computing approach; (b) 1T1R device building block schematic with a top gate thin-film transistor (TFT); (c) passive 4 x 4 crossbar; and (d) active 4 x 4 crossbar.

integration density.[8] Furthermore, their electrical characteristics allow them to emulate biological synapses and neurons, meaning they can simultaneously perform information storage and processing.[9]

For large-scale neuromorphic systems, memristors are typically arranged in crossbar architectures to achieve high device density and enable efficient vector−matrix operations (passive crossbars). However, when addressing a specific device in a crossbar array, the applied voltage can propagate through shared lines and unintentionally affect neighboring cells. This phenomenon, referred to as crosstalk, may lead to undesired switching events or over-programming of adjacent devices and is currently blocking large area integration of crossbars.[10,11] To mitigate this issue, a common strategy is to integrate a transistor in series with each memristor, forming a 1-transistor−1-memristor (1T1R) configuration, represented in Figure 1b.[12] The transistor acts as a selector device, allowing the targeted cell to be electrically addressed while isolating unselected cells from the applied voltage. This approach effectively suppresses crosstalk between neighboring devices and improves the reliability of crossbar-based neuromorphic systems by reducing the energy wasted on unintentional leakage, as demonstrated in Figure 1c,d.[13,14] Furthermore, the addiction of a transistor allows precise current control within each memory cell. This is essential for achieving accurate multilevel conductance states (synaptic weights) and it is particularly advantageous in large-scale arrays.[15]

Printed 1T1R architectures have emerged as promising candidates for next-generation electronic systems by enabling the integration of sensing, memory, and signal processing within a single platform. In contrast to conventional CMOS technologies, which are primarily optimized for digital computation, 1T1R systems are particularly attractive for analog signal processing and neuromorphic functionalities, where local data storage and in-memory computing are essential.[16] Furthermore, while printing techniques in traditional CMOS fabrication are generally restricted to interconnects or auxiliary processes, fully printed 1T1R architectures enable the fabrication of all device components using compatible printing-based methodologies. This approach may simplify integration processes, improve material compatibility, and reduce fabrication complexity and cost. Furthermore, printing technologies allow device fabrication on unconventional substrates, including flexible, lightweight, stretchable, and disposable materials, thereby expanding the range of potential applications beyond those accessible with conventional microfabrication technologies.[17] Such characteristics make printed 1T1R systems particularly attractive for emerging applications in healthcare, wearable electronics, agriculture, environmental monitoring, and distributed IoT platforms.[18] By combining sensing, memory, and processing capabilities within the same architecture, printed 1T1R systems also offer the possibility of reducing data transfer requirements, lowering power consumption, and enabling compact and autonomous edge-computing hardware.

Several studies have demonstrated the potential of printing techniques for the fabrication of high-performance devices for neuromorphic applications.[19,20] Recently, Zhong et al.[21] proposed an ambipolar transistor architecture for the implementation of a physical echo-state network (ESN). In this study, the semiconductor layer, based on Poly(3-hexylthiophene) (P3HT)−zinc oxide (ZnO) heterostructures, was deposited by spin-coating. These transistors operated simultaneously as synaptic and neuronal elements within the ESN reservoir, enabling the generation of high-dimensional reservoir states from electrical inputs. The proposed system demonstrated high performance in recognition tasks, achieving accuracies of

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96.98% on MNIST and 86.67% on Fashion-MNIST. Another recent study reported fully patterned ZTO memristors with printed active layers and top electrodes exhibiting stable operation, high reproducibility, and low device variability, demonstrating strong potential for printed neuromorphic systems and physical reservoir computing applications.[22] Owing to their volatile switching behavior, the devices were successfully programmed using the MNIST handwritten dataset, achieving recognition accuracies of 89.4 and 86.5% for 4-bit and 5-bit temporal sequences, respectively. Although fully printed approaches are currently mostly limited to device-level implementations, the combination of printing techniques with conventional fabrication processes already enables the realization of more complex neuromorphic architectures and neural-network-based systems.

The integration of a transistor with a memristor already represents a significant technological challenge due to the electrical requirements needed to achieve stable and efficient operation.[23] When such structures are fabricated using printing techniques, these challenges become even more pronounced, such as controlling layer uniformity, interface quality, different annealing temperatures between layers and multiple printing techniques.[24] Hence, stable and reproducible 1T1R structures are considerably harder to achieve through printing technologies.

In this perspective, the focus is on 1T1R arrays with particular emphasis on fabrication through printing techniques. The discussion covers 1T1R architectures, their electrical performance and the several strategies reported for the development of crossbar architectures, together with the associated challenges and limitations when printing is employed as the primary fabrication method. Throughout this work, the transistor component of the 1T1R architecture is assumed to be a thin-film transistor (TFT).

2. 1T1R ARCHITECTURES AND ELECTRICAL PERFORMANCE

By adding a memristor in series with a transistor through the drain node, in case of n-type TFTs, a 1T1R structure is formed, which allows the transistor to function as a selector device to the memristor (active cell). Moreover, the memristor can be trained by the output current of the transistor, effectively imposing a current compliance, controlled by gate and drain voltage, within the structure itself. These structures are commonly fabricated using monolithic integration, where both components are fabricated in the same substrate for higher density and easier integration. In many cases, 1T1R devices are implemented within the BEOL (back-end-of-line) process, where memristors are integrated on top of CMOS technology using vacuum-based deposition techniques, directly connected to the transistor drain through metallic interconnects, as represented in Figure 2a. With such approach, it is possible to integrate memristors with conventional technology, as has been reported with CMOS technology nodes of 130,[3,25,26] 350,[27] 0.18,[28,29] 1.2,[30,31] and 2 μm[32,33] sizes. Furthermore, the implementation of vertically stacked 1T1R crossbar arrays using monolithic 3D integration has already been reported, enabling multi-layer architectures suitable for artificial neural networks (ANN).[3] In fact, the progress of the 1T1R architecture is reflected in the consistency of scientific publications over recent years (Figure 2b).

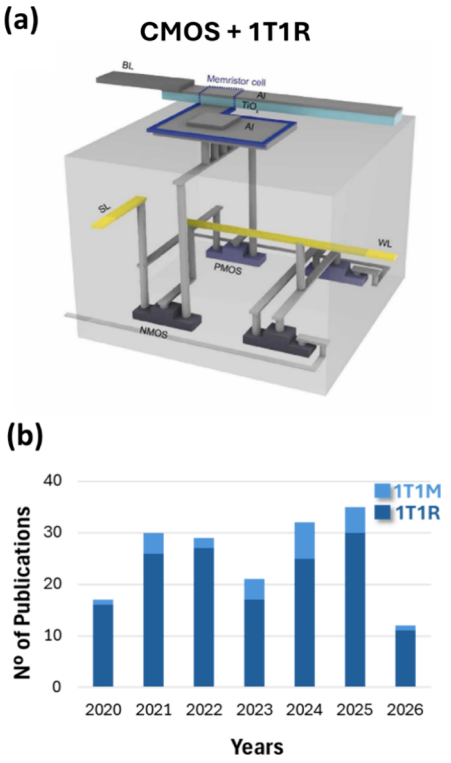

Figure 2. (a) Conventional CMOS integration of 1T1R. Reproduced with permission ref 34. Copyright 2025, Elsevier. (b) Publications on 1T1R devices from 2020 to March 2026 (search engine: Web of Science, accessed on March 2026; keywords:1T1R;1T1M.

When the 1T1R architecture is fabricated at the same level using a common fabrication approach for both the transistor and the memristor, it is essential to ensure compatibility between materials and fabrication processes. In this case, three main architectures have been reported in the literature (shown in Figure 3) using TFTs as the selector device. One architecture was reported by Sivan et al.,[35] where it was fabricated a TFT based on mechanically exfoliated tungsten diselenide (WSe_2) flakes, followed by the fabrication of a memristor on the same substrate using aerosol jet printing (AJP). The two devices were then connected in series, and the electrical results highlighted the critical role of the on-state resistance of the transistor, which increased the memory switching voltage, as depicted in Figure 3a.

The most common configuration consists of a planar transistor combined with a vertical memristor, where its bottom electrode is shared with the drain of the transistor. In this architecture, the transistor is typically fabricated first, followed by the integration of the memristor (Figure 3b). In some cases, parts of the fabrication process can be carried out simultaneously, allowing partial process integration. Indium gallium zinc oxide (IGZO) is a semiconductor widely used in TFTs industry and has also been employed as active layer in memristors. The use of IGZO in 1T1R structures has enabled a reduction in fabrication steps,[23] while also supporting implementation on flexible substrates.[10,36] However, the IGZO-TFT has to be meticulously optimized in regard to channel dimensions and annealing conditions, in order to provide the required output to switch the memristor and, at the same time, guarantee low standby power.[37] 2D materials have been also employed using this architecture. Ma et al.[38] demonstrated a 1T1R device by combining $CuCrP_2S_6$

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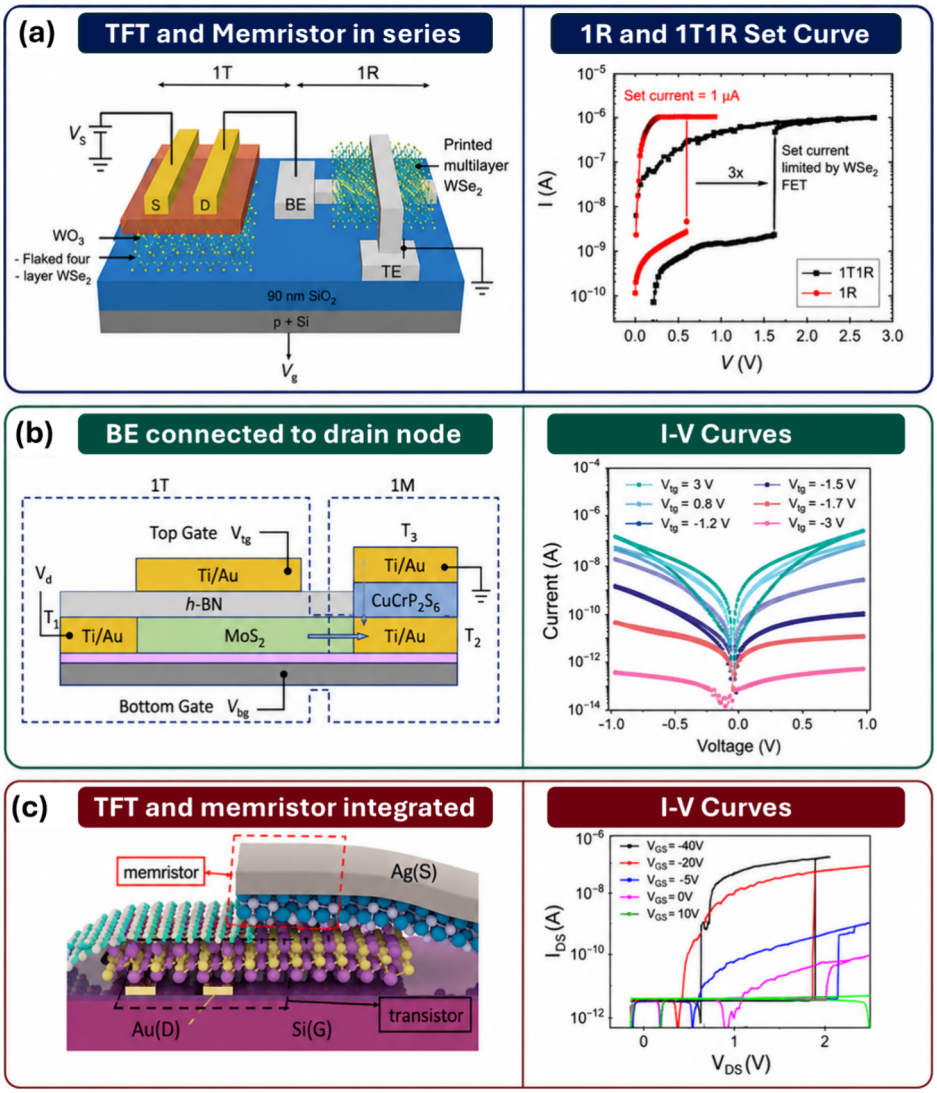

Figure 3. (a) 3D schematic view of the 1T1R structure with flaked WSe2 transistors and printed WSe2 memristors; representation of the I-V set curve of the memristor and the 1T1R. Reproduced from ref 35 Available under a CC-BY 4.0 License. Copyright 2019, Springer Nature. (b) Cross-sectional schematic of the 1T1R structure; hysteretic $I-V$ curves for the 1T1R with V_{tg} varied from −3 to 3 V. Reproduced from ref 38. Available under a CC-BY 4.0. Copyright 2025, American Chemical Society. (c) 3D structural diagram of the Au/WSe_2/Al_xO_y/Ag 1T1R device. Variation of the memristor window under different gate voltages. Reproduced with permission ref 39. Copyright 2025, American Chemical Society.

as the memristive active layer, hexagonal boron nitride as dielectric and MoS_2 as transistor channel. This structure exhibited high resistance tunability and ultralow sneak path current, as depicted in Figure 3b $I-V$ curves. However, Zhao et al.[39] reported a different approach using 2D materials, in which a memristor is integrated with a WSe_2-based transistor, where the same WSe_2 acts both as the selector and as the transistor channel controlled by gate voltage. This configuration reduces the fabrication steps and the cell size (Figure 3c). Moreover, the device operates through a combination of oxygen and metal ion[38] migration mechanisms, resulting in lower threshold voltage, high switching ratio and stable retention.

Regarding the overall electrical performance, the addition of a transistor enhances the device performance by introducing active control and electrical isolation.[12] As already mentioned, one of the main advantages is the suppression of sneak-path currents, which are very common in passive crossbar arrays and greatly decrease the accuracy of ANNs tasks.[10,40] Also, the transistor ensures effective current compliance, limiting the current during switching events and preventing device degradation. This control reduces variability and improves device reliability, leading to more stable operation over multiple cycles.[11] In neuromorphic applications, the transistor also enables precise tuning of the memristor conductance through gate or drain voltage modulation, allowing gradual and more linear switching behavior, which is essential for synaptic functionality and multilevel data storage.[41]

3. FABRICATION OF PRINTED 1T1R STRUCTURES

Both transistors and memristors are composed of multiple layers, where each one plays a role in the operation of the device. Therefore, multiple materials, including conductors, semiconductors, and insulators, are involved in the realization

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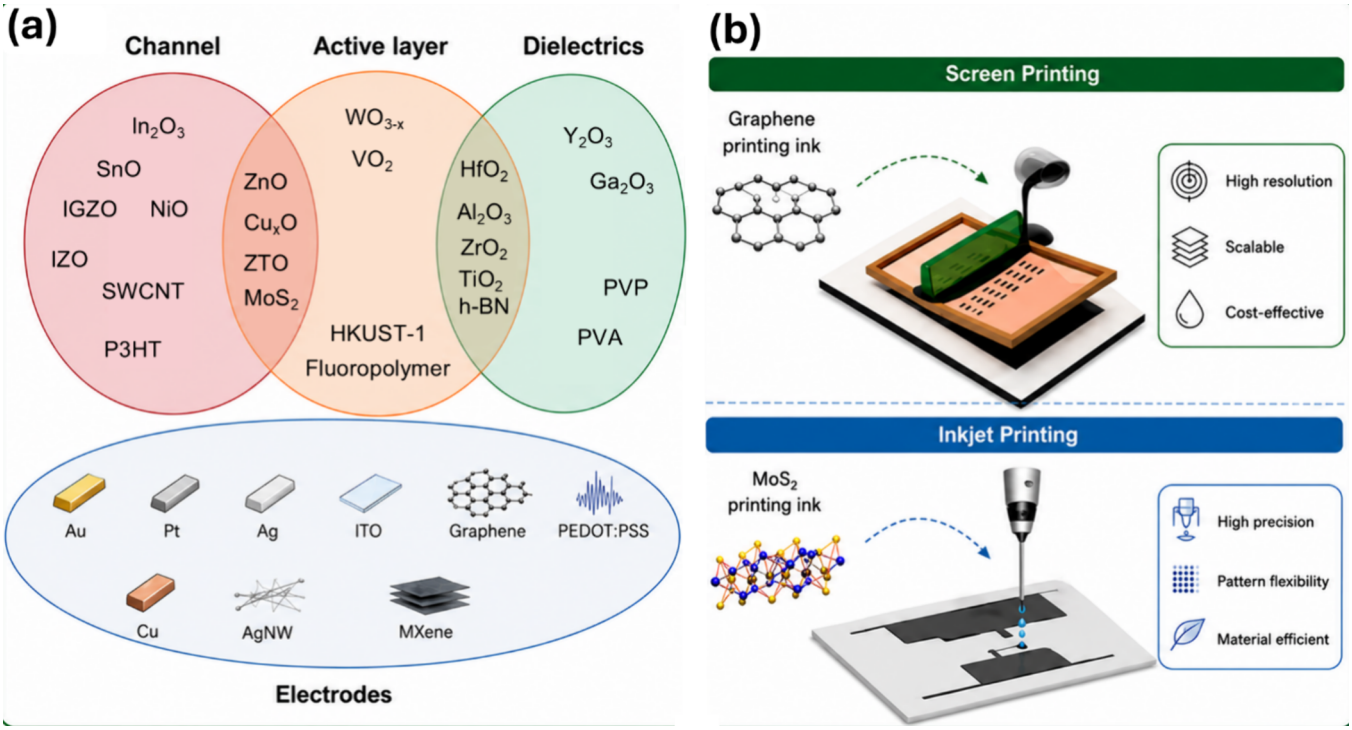

Figure 4. (a) Materials reported for the different layers (channel, active layer, dielectric, and electrodes) in printed TFTs and memristors. (b) Printing techniques that can be used for memristor fabrication. Reproduced from ref 45. Available under a CC-BY 4.0 License. Copyright 2024, Springer Nature.

of a 1T1R structure. A diverse spectrum of materials has been reported as printable for constructing TFTs[42] and memristors,[43] which are summarized and categorized in the diagram in Figure 4a. These materials span from metals, oxides, 2D compounds, and polymers. Some of the channel materials and gate dielectrics of printed TFTs are also used as the active layer in printed memristors, creating overlaps in the diagram in Figure 4a. These material selection intersections are an advantage in designing a 1T1R structure, as they reduce printing complexity and improve material compatibility, which will be addressed further. 2D materials are emerging as outstanding candidates for printable electronics, representing a significant advancement in the development of high-performance printed devices due to their atomically thin structure, excellent electrical properties, and compatibility with low-temperature fabrication processes.[44]

The printing of a 1T1R structure requires several material deposition steps, in which different types of inks and diverse printing techniques are employed. Therefore, the fabrication sequence requires special consideration based on the properties of the concerned material and its corresponding ink, as well as the printing techniques used.

First, different printing techniques[46−48] have distinct features and are suitable for fabricating specific components of the 1T1R structure. According to the deposition method, printing techniques are categorized into two groups, contact printing (such as screen printing or gravure printing) and non-contact printing (such as inkjet, EHD, and aerosol printing).[46] Table 1 exhibits the main characteristics of the printing techniques for electronic devices and also the ink requirements for each. Contact printing techniques can provide large-scale and high-speed operation; however, they have limited capability in terms of lateral resolution and alignment accuracy.[49,50] Therefore, contact printing techniques are ideal for patterning structures that are less size/dimension critical but require a large amount of material deposition, such as the TFT electrode (Figure 4b) and crossing wires in memristor crossbar arrays. When the structure dimensions directly affect device performance, for instance, thickness of the memristor active layer and width of the memristor electrodes, non-contact printing techniques become advantageous due to their superior resolution. Moreover, a 1T1R structure consists of multiple layers stacked one on top of another, such as the dielectric layer of the TFT and the active layer of the memristor. To deposit these layers, non-contact printing techniques are then preferred, as they exert minimal impact on layers patterned in earlier steps and allow more precise alignment between layers. The ideal fabrication of 1T1R structure will most likely involve multiple printing techniques in a hybrid manner.

Therefore, the process needs to be optimized across several aspects (such as fabrication cost, speed, and resolution requirements) to fully leverage the advantages of each printing technique. To provide a comprehensive reference for the design of 1T1R structures using printing techniques, the reported printable materials and their processing conditions employed as components of printed TFTs and memristors are summarized in Table S1 (see Supporting Information). Inkjet printing is one of the most widely reported techniques and one of the most promising for printing 1T1R, as it is highly compatible with other printing methods and offers high resolution and alignment accuracy (Figure 4b). Additionally, it enables the deposition of a wide range of materials, if particle size is suitable. However, ink viscosity must be carefully controlled, as it needs to fall within a specific range defined by the dimensionless Z

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Table 1. Main Characteristics of Printing Technologies and Ink Requirements for Electronic Devices (Adapted from ref 19)

	non-contact techniques			contact techniques			
	aerosol jet printing (AJP)	inkjet printing	electrohydrodynamic printing inkjet (EHD)	screen printing	gravure printing	flexographic printing	reverse offset
printing resolution (μm)	10–100	15–100	0.04–500	20–100	5–200	30–100	1–50
layer thickness (μm)	0.1–5	0.01–0.5	0.01–0.5	3–30	0.1–8	0.1–3	0.04–2
film roughness	low	low	low	high	low	low	low
printing speed (m min^{-1})	0.6–1.2	0.02–5	0.1–3	0.6–100	20–1000	20–600	0.06–15
alignment accuracy (μm)	10–20	10–15	10–15	<50; 250[a]	<100	<100	1–2.5
max particle size (μm)	1/10 of the nozzle diameter			1/10 of mesh opening	15	20	10
viscosity (cP)	1–2500	5–50	1–10,000	100–1,000,000	10–1000	10–1000	20,000–100,000

[a]In case of a manual screen printer.

parameter[51] to ensure stable jetting. Different types of ink generally require different post-treatment conditions[52,53], particularly the temperature of the post-thermal treatment after printings.[60,61] The inks commonly used in printing are generally categorized into two types according to the form of the solutes in the solvent: dispersion inks and precursor inks.[54] The dispersion ink[46] is developed by dispersing the target functional material from micrometer to nano-meter scale (such as nanoparticle or nanosheet) in an appropriate solvent. The post thermal treatment is mainly used to remove the solvent, therefore, requiring a heating process of relatively low temperature, generally around 100 °C which corresponds to the boiling point of the solvent used. This low-temperature routine is generally applied to printing electrode materials for memristor (such as Ag nano particle dispersion ink) or metal oxide semiconductor as the channel material for a printed transistor. Precursor ink[55] is developed by completely dissolving the precursor of target materials in a solvent that is optimal for printing. After the printing, the target functional material is formed via a chemical transformation, such as sol-gel or combustion process,[56] requiring a post-treatment of higher temperature (above 400 °C in some cases). In addition, different material species must be processed within different temperature ranges to avoid damage (such as oxidation or burnout) during post-thermal treatment. For instance, polymers[57,58] generally require much lower processing temperatures than metal oxides.

Furthermore, the ink formulation must be carefully tailored to meet the requirements of the selected printing techniques. As summarized in Table 1, parameters such as viscosity and particle size are particularly critical to ensure stable behavior and high-quality printed patterns.[55] Another important aspect to consider is the choice of substrate, as it can significantly influence device performance, from surface roughness to the tolerable processing temperature range. This is particularly critical for flexible substrates, where the thermal expansion coefficient must be considered, since the annealing temperatures required for printed layers may alter the substrate's properties.[59] To mitigate these effects, a common strategy is to perform a pre-treatment step at a temperature slightly higher than the maximum temperature used during the fabrication process, thereby stabilizing the substrate and ensuring more reliable device performance.

Overall, the design of a 1T1R architecture and its fabrication process should follow a temperature hierarchy in which all post-treatment temperatures are arranged in descending order, i.e., the printing steps that require higher processing temperatures should be prior to those performed at lower temperatures. To ensure proper device fabrication, careful selection of inks is also essential. The chosen formulations must minimize interaction with underlying layers and suppress common printing artifacts such as the coffee-ring effect, which can compromise film uniformity and device performance. Furthermore, accurate multilayer alignment is critical for device performance. The use of alignment marks facilitates the layer printout in the right place, improving reproducibility, while also ensuring compatibility between different printing techniques in terms of resolution and pattern definition.

4. CHALLENGES IN SCALING 1T1R STRUCTURES

As for the challenges in scaling 1T1R structures, the first encounter is the increase in the unit area, which consequently reduces the integration density.[2] The incorporation of a transistor typically leads to an increase in power consumption, not necessarily due to higher voltages, but as a result of the additional control element and its bias conditions. Moreover, the transistor generally dominates the device footprint, resulting in a larger cell area compared to a passive crossbar configuration, which can limit integration density and contribute to increased device-to-device variation. Monolithic 3D vertical integration can be a solution for reducing the area; however, the local thermal management must be considered.[60] Also, parasitic capacitances are present which can introduce transient effects that can impact the readout accuracy and the operating speed. All these challenges are scaled with the size of the crossbar array; as the array grows, parasitic effects become more significant and the overall area increases.

From a printing perspective, not only electrical performance is a challenge but also the fabrication process itself. One of the main limitations is the compatibility between different printing techniques, as each layer of the device requires distinct processing conditions and resolution.[19] Material and solvent compatibility is crucial, once the successive deposition layers can lead to the dissolution or even degradation of the previous printed layers. Also, multilayer alignment remains a challenge, which directly impacts array scaling due to the higher device variability. Regarding the electrical performance of printed transistors

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and memristors, achieving high yield and low variability is a key milestone that would enable less complex integration of printed 1T1R structures.[61]

Since these structures are compatible with CMOS technology, the main challenge shifts to economic cost and yield improvement. Nevertheless, the ongoing research on printing electronics, the use of emerging materials and advanced device architectures, aim to reduce the footprint while maintaining the electrical benefits of the 1T1R configuration.

5. APPLICATIONS

1T1R architecture has demonstrated great potential for neuromorphic computing applications, especially for hardware implementation of ANNs, due to its capability of emulating synapses and neurons functionalities.[62] Also, the reduced cell area and their compatibility with monolithic 3D stacking and hybrid CMOS integration enables high integration density on-chip which allows the development of scalable neuromorphic architectures without increasing the chip area.[15] Figure 5 represents

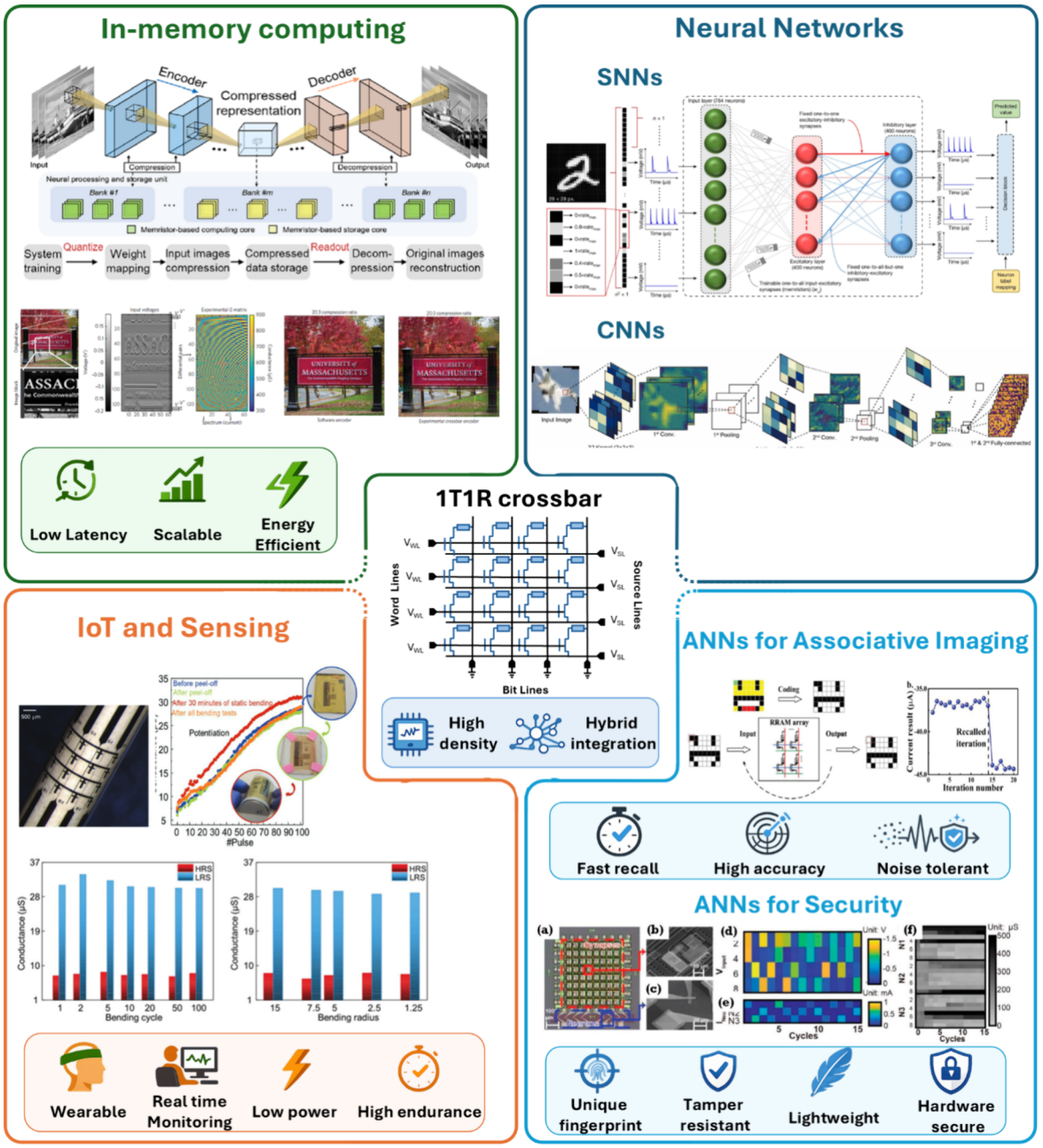

Figure 5. Schematical representation of the main applications of 1T1R crossbars. ANN applications include SNNs (Reproduced from ref 63. Available under a CC-BY 4.0 License. Copyright 2023, Springer Nature), CNNs (Reproduced with permission ref 34. Copyright 2025, Elsevier), and other neural networks that can be used for associative imaging (Reproduced with permission ref 30. Copyright 2019, John Wiley and Sons) or hardware security (Reproduced from ref 64. Available under a CC-BY 4.0 License. Copyright 2020, MDPI). Signal and imaging processing were demonstrated with in-memory computing systems. (Reproduced with permission ref 65. Copyright 2017, Springer Nature. Reproduced with permission ref 16. Copyright 2025, John Wiley and Sons). Flexible 1T1R crossbars for IoT applications. (Reproduced from ref 10. Available under a CC-BY 4.0 License. Copyright 2022, John Wiley and Sons).

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a schematic of the main applications and advantages of 1T1R crossbars.

Therefore, 1T1R arrays have been widely explored as hardware for ANNs, including conventional neural networks (CNN) and spiking neural networks (SNN), enabling significant improvements in energy efficiency compared to conventional computing systems.[16,63] These architectures also support associative memory functions, allowing the reconstruction of incomplete or noisy data,[30] and have been applied in emerging fields such as brain−computer interfaces for real-time signal processing.[66]

Still within neuromorphic systems, 1T1R architectures are suitable for in-memory computing, where data storage and processing occur within the same physical location. Particularly, crossbar arrays enable vector-matrix multiplication operations (also used in ANNs), which are fundamental to machine learning algorithms, by using Ohm's and Kirchhoff's laws, offering high speed operations and also low power consumption.[65] The analog tunability and reconfigurability of 1T1R devices allows their application in real time image processing the sensor. In this context, 1T1R crossbars can be integrated with optoelectronic memristors to realize near-sensor and in-sensor computing architectures, where sensing, processing, and data storage are closely coupled within the same platform.[67,68] These capabilities have been demonstrated for reconstruction of images, smoothing noisy images[65] and even process real-time video tasks like foreground-background separation.[16] In this matter, 1T1R systems are highly relevant for IoT applications and edge computing, where low-power, local data processing is required.[10,362,65] They can be integrated into smart sensors to perform tasks such as signal filtering, pattern recognition, and unsupervised learning without the need for complex external circuitry.[2,65]

Finally, 1T1R structures also show strong potential in hardware security and advanced memory technologies.[64] The intrinsic variability of memristors can be exploited for applications such as true random number generation and physical unclonable functions, while their non-volatile behavior makes them promising candidates for storage-class memory, bridging the gap between volatile and non-volatile memory technologies.

6. CONCLUSIONS AND FUTURE PERSPECTIVES

The 1T1R architecture has emerged as a key component for next-generation computing systems, by offering a robust solution to the limitations of conventional von Neumann architecture. By combining a transistor with a memristor, 1T1R building blocks enable precise control of switching dynamics, effective suppression of sneak-path currents, and reliable operation in large-scale crossbar arrays, positioning them as a strong candidate for neuromorphic computing and analog in-memory processing hardware.

The fabrication of printed 1T1R systems is currently constrained by several technological challenges that directly influence device performance, reproducibility, and large-scale integration capability. Limited printing resolution restricts the achievable integration density of crossbar architectures, particularly when feature sizes remain above 1 μm. The development of advanced high-resolution printing techniques is expected to significantly improve device miniaturization and array scalability. Furthermore, insufficient multilayer alignment accuracy can induce substantial device-to-device variability due to misaligned printed layers. Such limitations may be mitigated through comprehensive optimization of each printing process, equipment offset calibration, and the implementation of alignment mark strategies to improve registration precision between successive layers. Ink and material compatibility also represent critical concerns, since solvent interactions and interfacial instability between deposited layers may promote interface degradation and compromise electrical performance. The optimization of ink formulations combined with solvent compatibility engineering is therefore essential to preserve interface integrity during multilayer fabrication. Moreover, the development of high-performance conductive ink formulations and with low annealing temperatures will be critical to overcome the performance gap with conventional technologies. Electrical variability associated with non-uniform printed features can negatively affect reliability, endurance, and device yield. Consequently, process standardization and encapsulation strategies are considered fundamental approaches to improve fabrication reproducibility, environmental stability, and long-term operational reliability. Collectively, these mitigation strategies constitute key technological routes toward the realization of scalable, high-density, and high-performance printed 1T1R systems. Table 2 summarizes the main current limitations, their impact and the solutions to overcome those challenges:

The future development of printed 1T1R systems is strongly dependent on overcoming the current fabrication challenges associated with printed electronics. At present, most reported 1T1R arrays are based on vacuum-processed devices combined with partially printed fabrication approaches. In parallel, several demonstrations of printed TFTs and memristors for neuromorphic applications have already been reported, highlighting the growing potential of printed electronic technologies. Although fully printed 1T1R systems are still at an early stage of development, the continuous evolution of printing techniques, materials, and device engineering indicates that proof-of-concept fully printed 1T1R devices are becoming increasingly achievable.

Table 2. Challenges, Impact, and Mitigation Strategies in Printed 1T1R Arrays

challenges	impact	perspective
limited printed resolution (>1 μm)	reduced integration density	advanced printing technologies (resolution < 1 μm) deep study on each technique
accuracy in multilayer alignment (>1 μm)	device variability	offset of the equipment marks alignment
material compatibility	interface degradation	optimizing inks (constant) consider solvents compatibility
conductive inks variability	fully printed devices constraints	develop new conductive inks laser ablation of commercial conductive substrates
electrical variability	reliability instability	process standardization encapsulation

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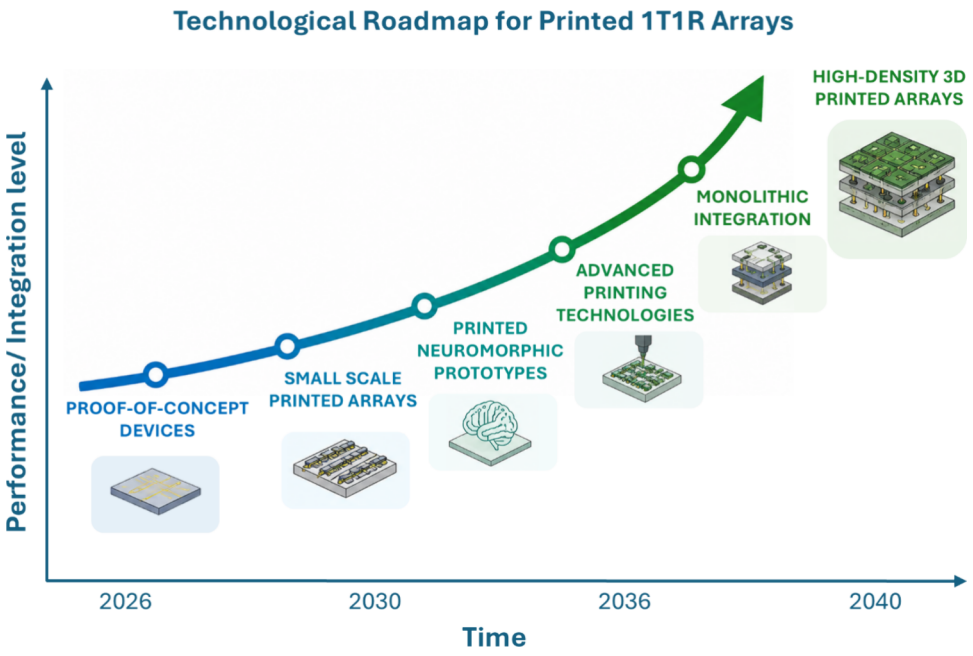

Figure 6. Trend chart illustrating the expected development of printed 1T1R arrays, including advances in printing technologies, neuromorphic prototypes, monolithic integration, and high-density 3D architectures.

The technological roadmap presented in Figure 6 illustrates the projected evolution of printed 1T1R systems from initial proof-of-concept demonstrations toward high-density monolithically integrated 3D architectures. As highlighted before, advances in printing resolution, multilayer alignment precision, material compatibility, and process reliability are expected to support the emergence of printed neuromorphic prototypes and more advanced system-level integration. In the longer term, the convergence of optimized materials, high-precision printing technologies, and hybrid fabrication strategies may enable monolithic integration and high-density 3D printed arrays, representing a major step toward scalable and energy-efficient hardware platforms.

The integration of printed 1T1R systems into emerging applications such as neuromorphic computing, IoT devices, and flexible electronics will drive the development of next-generation low-power and autonomous systems. The combination of sensing, memory, and computation within a single platform represents a route toward fully integrated and energy-efficient hardware for edge computing applications.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsaelm.6c00778.

Reported materials in solution-processed memristors and transistors (Table 1) (DOCX)

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