Reliable Emerging Electronics in Wearable and Implantable Healthcare Applications

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***Abstract*—Flexible electronics (FE) are enabling a new generation of wearable and implantable healthcare systems; however, ensuring reliable operation remains challenging due to process variability, mechanical deformation, and harsh physiological environments. In implantable settings, long-term exposure to bodily fluids a nd p ressure v ariations a ccelerates d evice degradation, while strict constraints on power and integration make the use of batteries and active electronics undesirable. This work presents a cross-layer approach to reliability in flexible h ealthcare systems by combining passive implantable sensing with robust wearable electronics. At the circuit level, we introduce *ReFlex-LDO*, a gain-boosted IGZO-TFT low-dropout regulator designed for capacitor-light operation and integrated with a structural delay-based built-in self-test (BIST) scheme, achieving $\sim 95\%$ fault coverage with minimal overhead. For signal acquisition, we develop a hierarchical fault modeling and mitigation framework for IGZO-based Flash ADCs, enabling up to 98% single-fault and 91% multi-fault coverage through targeted design enhancements. At the system level, we propose a passive RF-based sensing mechanism for monitoring fluid fl ow in im plantable bi omedical devices, eliminating the need for on-board power and improving long-term reliability. By pairing passive implantable sensing elements with flexible w earable p rocessing u nits, t he p roposed a pproach enables continuous health monitoring while mitigating risks associated with device degradation in the body.**

***Index Terms*—flexible e lectronics, L DO, a nalog a nd mixed-signal testing, structural fault, fault coverage**

I. Introduction

Flexible electronics (FE) are enabling a new class of wearable, implantable, and large-area healthcare systems due to their lightweight form factor, mechanical flexibility, and compatibility with low-cost fabrication processes. Among emerging technologies, indium gallium zinc oxide (IGZO) thin-film transistors (TFTs) have gained significant attention for implementing analog and mixed-signal circuits on flexible substrates. These systems are particularly attractive for biomedical applications, where conformability and continuous monitoring are essential.

However, ensuring reliable operation in FE remains a fundamental challenge. Compared to mature CMOS technologies, IGZO-based circuits exhibit higher process variability, lower intrinsic gain, increased parasitics, and sensitivity to temperature and mechanical bending. In implantable environments, these challenges are further exacerbated by harsh physiological conditions, including fluid exposure, pressure variations, and long-term material degradation, which can significantly impact device performance and lifetime.

A key challenge in such systems is the lack of reliable, low-power mechanisms to monitor device functionality in situ. While implantable sensors are critical for patient health monitoring, their degradation over time can lead to undetected failures. This motivates a hybrid approach in which passive implantable sensing elements are paired with flexible, wearable electronic units that provide power-efficient processing, monitoring, and fault detection capabilities.

At the circuit level, stable power delivery is critical, as fluctuations directly degrade the performance of analog front-ends and sensing interfaces. Similarly, data conversion blocks such as analog-to-digital converters (ADCs) must operate reliably despite device-level faults and variability. Together with system-level monitoring, these components form a cross-layer reliability challenge that must be addressed holistically.

In this work, we present a cross-layer approach to reliability in flexible electronics for healthcare applications, spanning power management, signal conversion, and system-level monitoring. First, we introduce *ReFlex-LDO*, a gain-boosted IGZO-TFT low-dropout regulator (LDO) designed for capacitor-light operation and integrated with a structural delay-based built-in self-test (BIST) scheme, enabling efficient fault detection and in-field monitoring. Second, we develop a hierarchical fault analysis and mitigation framework for IGZO-based Flash ADCs, allowing efficient identification of vulnerable circuit elements and improved fault tolerance through targeted design modifications. Finally, we propose a passive, chipless sensing approach for monitoring fluid flow in implantable biomechanical systems, enabling reliability assessment without requiring on-board power, and facilitating integration with wearable flexible electronics for continuous health monitoring.

The main contributions of this work are as follows:

- A gain-boosted IGZO-TFT LDO (*ReFlex-LDO*) with integrated structural delay-based BIST, achieving up to $\sim 95\%$ fault coverage with minimal hardware overhead.
- A hierarchical fault modeling and simulation framework for IGZO-based Flash ADCs, enabling up to 98% single-fault and 91% multi-fault coverage, along with fault-tolerant comparator designs.
- A passive RF-based sensing mechanism for monitoring fluid pressure and flow in implantable biomedical devices, eliminating the need for on-chip power.
- A unified cross-layer reliability framework combining implantable passive sensing with wearable flexible elec-

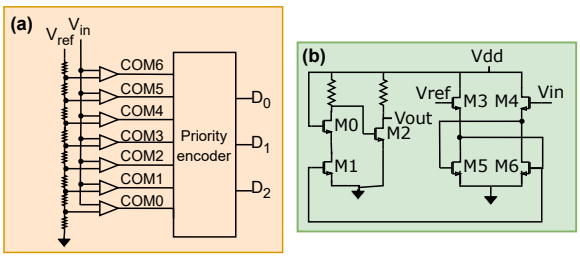


Fig. 1: 3-bit architecture of (a) Flash ADC (b) Comparator in IGZO-TFTs.

tronics for robust, long-term healthcare monitoring.

II. Background and Challenges in Flexible Healthcare Electronics

A. Flexible Electronics and IGZO TFTs

Flexible electronics (FE) offer unique advantages such as mechanical flexibility, lightweight, and compatibility with various flexible substrates including plastics, metals, and polymers. Unlike conventional rigid silicon-based electronics, FE can conform to dynamic or curved surfaces, making them suitable for wearable health monitors, medical devices, smart packaging, and IoT [1, 2]. Due to material and process constraints, a-IGZO TFT is unipolar (only n-type devices), which requires the use of resistor–transistor logic (RTL) for the circuit realization and imposes restrictions on its design complexity. The integration density is also limited to a few thousand devices, with feature sizes in the μm range, leading to prominence on compact, application-specific bespoke designs [3]–[6].

B. Reliability Challenges in Implantable and Wearable Systems

Flexible electronic systems for healthcare must operate reliably in both wearable and implantable environments, each imposing distinct constraints. While wearable devices benefit from accessibility and relaxed environmental conditions, implantable systems are exposed to harsh physiological environments, including bodily fluids, pressure variations, and long-term biochemical interactions. These conditions accelerate material degradation and can significantly impact the performance and lifetime of embedded electronics.

A critical challenge in implantable systems is the integration of power sources and active circuitry. The use of batteries and complex electronics within the body introduces risks related to leakage, degradation, and long-term reliability, while also increasing system complexity and limiting device lifetime.

To address these challenges, passive sensing approaches are highly desirable for implantable applications. By eliminating the need for on-board power and minimizing the amount of active electronics within the body, passive sensors improve reliability, reduce risk, and enable long-term operation. In this paradigm, sensing elements embedded within the implant can be interrogated externally by a wearable unit, which performs signal processing, monitoring, and fault detection. This separation between passive implantable components and active wearable electronics provides a robust and scalable solution for continuous health monitoring in harsh environments.

C. Analog and Mixed-Signal Blocks in FE

Analog and mixed-signal circuits form the critical interface between the physical environment and digital processing in flexible electronic systems. Key building blocks such as low-dropout regulators (LDOs) and analog-to-digital converters (ADCs) are essential for enabling stable power delivery and accurate signal acquisition, respectively. In wearable units, LDOs provide regulated supply rails for sensing and processing blocks, while ADCs convert physiological signals into the digital domain for further analysis.

However, the implementation of these circuits in IGZO-based flexible technologies introduces significant challenges. Reduced intrinsic gain, higher parasitics, and increased susceptibility to process variations degrade key performance metrics such as power-supply rejection ratio (PSRR), linearity, and noise. Moreover, structural defects and parameter shifts can propagate through these circuits, leading to system-level failures. These limitations highlight the need for integrated design and testing methodologies that enhance fault tolerance and enable reliable operation of analog and mixed-signal blocks within flexible healthcare systems.

III. Cross-Layer Reliability Framework for Implantable–Wearable Systems

This work demonstrates a cross-layer reliability framework for flexible healthcare systems by combining circuit-level robustness with system-level monitoring. The proposed ReFlex-LDO ensures stable power delivery for wearable processing units, while the fault-tolerant Flash ADC enables reliable signal acquisition under device-level variability and defects. Complementing these, the passive implantable sensor provides a mechanism for monitoring system functionality in harsh physiological environments without requiring on-board power.

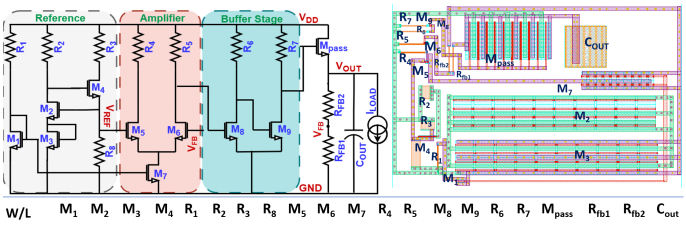
By pairing passive implantable sensing with flexible wearable electronics, the proposed approach enables continuous and reliable health monitoring while mitigating the effects of device degradation over time. This integration highlights the importance of co-design across power management, signal processing, and sensing layers in flexible electronic systems.

IV. Reliable Power Delivery for Wearable Units: ReFlex-LDO

Reliable power delivery is a fundamental requirement for wearable flexible electronics, as supply variations directly impact the performance and stability of downstream analog and digital blocks. In this section, we present the proposed ReFlex-LDO, a gain-boosted IGZO-TFT low-dropout regulator designed for capacitor-light operation. To address reliability challenges, we further integrate a structural delay-based built-in self-test (BIST) mechanism that enables efficient fault detection and in-field monitoring under process and mechanical variations.

A. Proposed ReFlex-LDO Architecture

The ***ReFlex-LDO*** is an all-NMOS low-dropout regulator designed in a flexible oxide-TFT process, addressing the challenges of reduced intrinsic gain, high process variation, and the



W/L	M_1	M_2	M_3	M_4	R_1	R_2	R_3	R_8	M_5	M_6	M_7	R_4	R_5	M_8	M_9	R_6	R_7	M_{pass}	R_{fb1}	R_{fb2}	C_{out}
W(μm)	12	200	200	20	0.6	15	15	10	2	2	100	0.6	0.6	18	18	1	1	1000	1	1	14
L(μm)	1.2	1.2	1.2	0.6	30	9	9	30	1.2	1.2	1.2	30	30	1.2	1.2	30	30	1.2	30	30	15

Fig. 2: Schematic and layout of the proposed gain-boosted *ReFlex-LDO*, showing the reference, amplifier, buffer, and output stages, with design specifications.

absence of PMOS devices in FE. The architecture retains the key stages of a classical LDO but adapts them for IGZO TFTs. The design includes four main stages:

Error Amplifier: The loop begins with the differential input pair (M5–M6), which senses the difference between the reference voltage V_{REF} and the divided feedback voltage V_{FB}. The amplified error signal drives the next stages of the LDO.

Second Gain Stage: The error signal is fed into the second stage (M8–M9), which boosts both the voltage gain and output swing to drive the large pass transistor (M_{pass}) efficiently. This stage compensates for the limited intrinsic gain of IGZO TFTs and maintains regulation, even with a pF-scale output capacitor.

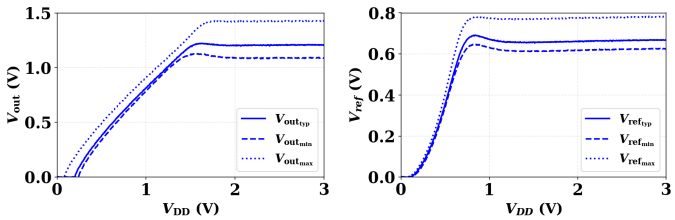
Pass Device and Feedback Network: The pass transistor M_{pass} provides the load current and regulates the output voltage V_{out}. A resistive feedback divider (R_{FB1}–R_{FB2}) samples V_{out} and generates the feedback signal V_{FB}, which is compared against V_{REF} in the error amplifier, closing the regulation loop.

Stability and Compensation: The design employs an output-capacitor-dominant-pole compensation strategy using a small on-chip capacitor C_0 at V_{out}. This ensures loop stability by creating dominant pole and improves noise filtering and PSRR, without relying on ESR-zero compensation.

The *ReFlex-LDO* is optimized to achieve a low dropout voltage, minimal quiescent current, and robustness against bending-induced variations. It demonstrates excellent line regulation, load regulation, PSRR (34 dB at 10 kHz), and transient response, with settling times of 30 µs and 120 µs. The low quiescent current of 31 µA ensures energy efficiency, making the LDO suitable for wearable and biomedical applications where power consumption is critical. The LDO design is both energy-efficient and robust across temperature and process variations, providing reliable power management for FE.

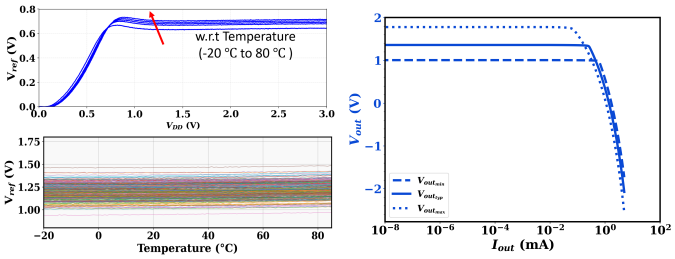
B. Structural Delay-based BIST in ReFlex-LDOs

We adopt a structural Built-In Self-Test (BIST) approach inspired by [7, 8] that perturbs the circuit at an *injection node* and observes the resulting response at an *observation node* as a digitally measurable *time delay*. Injection is performed using ON/OFF keying, such as shorting a passive or pulling a bias node, with a single observation circuit shared across multiple injection points. A chain of inverters converts the analog response to a 1-bit digital signal, which is then measured using a counter. Non-sensitive nodes such as bias rails and feedback ladders are selected for injection, and V_{out} is used



(a) Line regulation at the output stage: V_{out} across PVT corners. (b) Line regulation of the internal reference: V_{ref} across PVT.

Fig. 3: Line regulation of the proposed gain-boosted ReFlex-LDO. The left plot illustrates the regulated output voltage V_{out}, while the right plot highlights the stability of the internal reference voltage V_{ref} across process corners after **post-layout**.



(a) Line regulation of reference: V_{ref} versus V_{DD} and MC of 5000 runs for V_{ref} with temperature. (b) Load regulation at the output stage: V_{out} versus I_{out} across process corner.

Fig. 4: Regulation characteristics of the proposed gain-boosted ReFlex-LDO. The left plot shows the line regulation of the internal V_{ref} and 5000 monte-carlo simulation across PVT corners while the right plot shows load regulation by showing variation of V_{out} with I_{load}.

as the observation node, providing a clean, digitally detectable transition when a feedback resistor is bypassed.

To generate the perturbation, two injection methods are used: bypassing passive components, like resistors or capacitors, with a pass transistor, and bypassing active components by pulling a bias device's gate with a pass transistor, which perturbs multiple stages simultaneously. Both methods require minimal hardware, with each injection point adding only one pass device and a digital enable. The delay is measured by timing the response at the observation node, where a fault that shifts the DC point can be detected due to the change in delay.

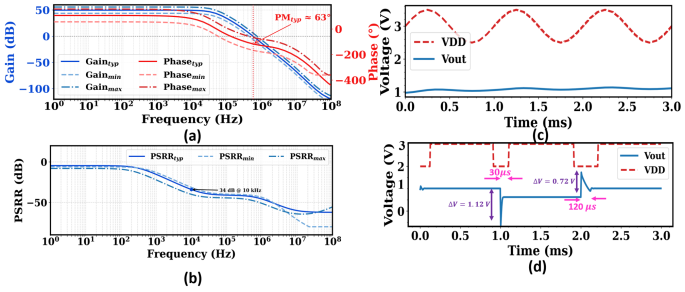


Fig. 5: (a) Loop gain and phase response across frequency for stable operation after **post-layout**, (b) power-supply-rejection ratio (PSRR) in dB (c) V_{out} under supply ripple V_{DD}, (d) line transient response of the LDO under varying V_{DD}.

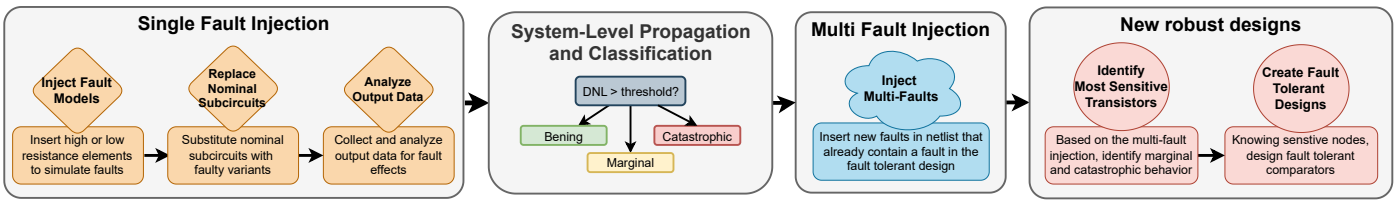


Fig. 6: End-to-end hierarchical fault injection flow. The methodology begins with single-fault injection and device-level characterization, followed by system-level fault propagation and classification based on DNL degradation. Multi-fault scenarios are then constructed using the sensitivity information extracted from single-fault analysis. Finally, the identified weak points guide the development of fault-resilient comparator designs for IGZO-TFT Flash ADCs.

C. Evaluation Under PVT and Mechanical Variations

We evaluate *ReFlex*-LDO using a structural delay–based BIST following the methodology in [7]. Transient SPICE simulations are run with mismatch-enabled Monte Carlo and PVT sweeps appropriate for the FE process. V_{DD} is swept over its operating range (e.g., $\pm 10\%$), load current over $I_{\text{load,min}} \rightarrow I_{\text{load,max}}$, and temperature over the qualified range (e.g., $-20°\text{C}$ to $80°\text{C}$). The on-chip output capacitor is $C_0 = 0.95\ pF$.

a) Simulation flow: All simulations are run in Cadence Spectre[1] with *Ocean scripts* after **post-layout** extractions using *PragmatIC's FlexIC-Gen3* PDK [9]. We evaluate: (i) **process corners** using the model sections `max/typ/min`; (ii) **Monte-Carlo** using the model's `mc` section; (iii) **mechanical corner** for minimum bend radius $R = 5$ mm by overlaying an empirical bend model. For each condition we sweep V_{DD} and load current I_{LOAD} across the specified range and run N Monte-Carlo samples (*e.g.*, $N = 5000$).

b) Fault list and injection: Catastrophic faults are modeled as resistive opens/shorts on transistor terminals and passives: opens in $[1\,\text{M}\Omega,\ 1\,\text{G}\Omega]$, shorts in $[1,\ 100]\,\Omega$. For each fault and each point, a transient run records t_d. Fault-free runs (across PVT and bend) form the nominal delay distribution.

c) Thresholding decision rule and fault simulation: Delays for each injection/observation pair are characterized by 5000 Monte Carlo (MC) samples to obtain μ_{t_d} and σ_{t_d}; For each point, the FAIL window is a two-sided guardband

$$G = \left[\mu_{t_d} - 3\sigma_{t_d} - T_{clk},\ \mu_{t_d} + 3\sigma_{t_d} + T_{clk}\right],$$

computed from fault-free MC at each corner; production FAIL uses the intersection of guardbands across corners and bends. Faults are detected when t_d falls outside the guardband.

d) FE mechanical corners: Bending is modeled by perturbing the TFT parameters according to [10, 11]. For each radius r, we modify the nominal models as follows:

$$\mu \leftarrow \kappa_\mu(r)\,\mu_0,\ R_{\text{sw1}} \leftarrow \kappa_R(r)\,R_{\text{sw1},0},\ V_{\text{th}} \leftarrow V_{\text{th},0} + \Delta V_{\text{th}}(r),$$

At circuit level this implies $g_m \rightarrow \kappa_\mu g_m$ and increased series resistance along the affected paths; r_o follows from perturbed device model. Monte-Carlo runs are drawn around each radius by adding small zero-mean spreads to κ_μ, κ_R, and ΔV_{th}.

[1] https://www.cadence.com/en_US/home.html

1) ReFlex-LDO Results and Discussion: Tab. I summarizes the fault coverage of the proposed *ReFlex*-LDO under structural delay-based testing. A total of 140 structural and parametric faults were injected (73 in the LDO core, 62 in the BIST circuitry, and 5 parametric variations), of which 121 were detected, resulting in 86.42% overall coverage. The LDO core achieved 82.19% coverage (64/73), while the BIST circuitry reached 91.94% (57/62). Parametric variations showed 80% detectability. These results show that delay-based methodology effectively captures the majority of open and short defects across both analog and digitally assisted blocks.

Tab. II analyzes the effect of increasing injection points ($N_{\text{tot}} = 140$). Coverage improves from 86.4% with a single injection node to 91.4% with three nodes, and gradually saturates at 95.7% for seven to eight injection points. The diminishing improvement beyond five nodes indicates that most structural faults are observable through a limited set of strategically placed injection locations, highlighting a favorable trade-off between coverage and test overhead.

TABLE I: Fault coverage for *ReFlex*-LDO

type	simulated faults			detected faults			coverage
	total	shorts	opens	total	shorts	opens	
LDO	73	36	37	60	28	32	82.19%
BIST	62	30	32	57	28	29	91.94%
param	5	NA	NA	4	NA	NA	80%
Total	140	66	69	121	56	61	86.42%

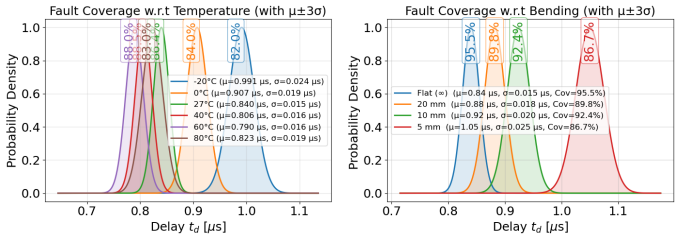
2) Area Overhead and Test Time: Tab. II shows that the proposed BIST adds only **4.2% area overhead** and consumes **1.8 mW** during test, which is almost 5.5% using multiple injection points, with a per-point time of **12 µs** and total test time of just **≈1.84 ms**. This shows that delay-based BIST achieves high fault coverage at negligible cost in area, power, and time, making it practical for integration in *ReFlex*-LDOs.

3) Fault Coverage under PVT and Bending: Fig. 7b shows the impact of mechanical bending on the delay distributions and fault coverage of the proposed *ReFlex*-LDO. At the flat condition, the coverage is 95.5%, which gradually decreases as the bending radius reduces due to mobility degradation and increased parasitics. At 20 mm radius, coverage falls to 89.8%, while at 10 mm it remains 92.4%, and at the extreme 5 mm radius it drops to 86.7%.

TABLE II: Impact of multiple injection points and corresponding BIST overhead ($N_{\text{tot}} = 140$).

Injection Points	1	2	3	4	5	6	7	8
Simulated	140	140	140	140	140	140	140	140
Detected	121	125	128	130	132	133	134	134
Coverage [%]	86.4	89.3	91.4	92.9	94.3	95.0	95.7	95.7
ΔArea [%]	1.56	2.54	3.25	3.96	4.11	4.23	4.23	4.24
ΔP_{test} [%]	1.42	1.45	2.73	3.92	4.85	5.50	5.53	5.56
ΔT_{tot} [ms]	1.11	1.12	1.24	1.36	1.48	1.60	1.72	1.84

1) Feedback-leg bypass (R_9/R_{10}), 2) EA tail-starve (M_7), 3) Pass-gate discharge (M_{pass}), 4) V_{ref} pull ($R_{8_{\text{shunt}}}$), 5) Driver-node clamp (M_6–M_9), 6) Load step at V_{out}, 7) Shared bias-rail pull, 8) V_{DD} micro-droop.



(a) Fault coverage vs. temperature: PDF of delay t_d at $-20\,^\circ$C, $0\,^\circ$C, $27\,^\circ$C, $40\,^\circ$C, $60\,^\circ$C, and $80\,^\circ$C. Coverage is computed over $\mu\pm3\sigma$; the $27\,^\circ$C is 86.4% respectively.

(b) Fault coverage under bending: PDF of path delay t_d for flat, 20 mm, 10 mm, and 5 mm; $\mu \pm 3\sigma$ windows yield 95.5%, 89.8%, 92.4%, and 86.7% respectively.

Fig. 7: Delay-based fault coverage of *ReFlex-LDO* under temperature and bending variation.

Temperature variation was also evaluated, as shown in Fig. 7a. Starting from the baseline 27°C coverage of 86.4%, the distributions shift with temperature due to the negative temperature coefficient of the flexible resistors. Coverage remains above 88% at -20°C and 0°C, but decreases towards 82.0% at 80°C. Overall, the results indicate that while both bending and temperature variations affect fault coverage, the structural delay-based BIST maintains coverage above 95% without bending and 86.4% across nominal temperature.

V. Reliable Signal Acquisition: Fault-Tolerant Flash ADCs

In addition to stable power delivery, reliable signal acquisition is essential for accurate sensing in flexible healthcare systems. However, analog-to-digital converters (ADCs) implemented in IGZO technologies are highly susceptible to process variations and structural defects.

A. Fault Modeling and Hierarchical Simulation Framework

We propose a hierarchical fault simulation framework for analyzing faults in IGZO-based Flash ADCs, focusing on fault-tolerant design. The methodology is composed of the following:
Fault Modeling: Faults are modeled at the transistor level using Spectre netlists, considering open circuits (high-value resistors, $500M\Omega$) and short circuits (low-value resistors, 10Ω). Each transistor is treated as a fault candidate, and comparator modules are replaced with faulty subcircuits for evaluation.

TABLE III: Transistor dimensions and resistor values used in the comparator and resistor ladder of the baseline flash ADC

Component	**Element**	**Size**
COM0:COM6	M0:M2 and M5:M6	W= 2μm L= 600nm
	M3:M4	W= 5μm L= 600nm
	R	r = 255$M\Omega$
Resistors in the resistor ladder r = 1.7$M\Omega$		

Multi-Level Simulation Flow:

- *Single-fault characterization:* Analog submodules (e.g., comparators) are simulated with OC/SC faults. Faulty characteristics are integrated into the ADC behavioral hierarchy for system-level analysis.
- *Fault classification:* The ADC output is analyzed to classify faults as catastrophic (incorrect outputs), marginal (degraded linearity), or benign (negligible impact).
- *Multi-fault injection:* Targeted multi-fault scenarios are constructed based on the single-fault analysis, ensuring realistic fault propagation and computational feasibility.

Automation and Simulation Framework: A Python-based framework automates netlist parsing, fault insertion, and simulation. Faulty netlists are processed in parallel using Spectre and Ocean, reducing simulation time. Key metrics (DNL, power, area) are computed through an automated post-analysis pipeline.

Fault-Resilient Comparator Designs:

- *Vulnerable element identification:* The simulation framework identifies transistors with high catastrophic or marginal behavior.
- *Design enhancement:* Redundancy and sizing adjustments are introduced to improve fault tolerance.
- *Validation:* Enhanced designs are validated under both single- and multi-fault conditions, quantifying improvements in robustness and hardware cost.

This streamlined methodology enables efficient fault analysis and fault-tolerant design in FE.

B. Fault Tolerant ADC Evaluation

1) Simulation Setup: All simulations are conducted using `Spectre` (Cadence), with analog netlists written in native Spectre syntax. The entire simulation workflow is automated using Python 3.9.18. The target technology is Pragmatic's second-generation FlexIC platform, which exclusively employs IGZO-based n-type TFTs and is optimized for low-frequency and low-power operation.

Flexible ADCs in FE applications typically range from 3 to 5 bits [12] for resource-constrained scenarios, though higher resolutions such as 8 bits [13] have also been reported. For validation purposes, we focus on the 3-bit Flash ADC design, although the methodology is applicable to larger bit lengths. The sizing of the baseline design, consistent with the simulations in [12], is detailed in Table III.

V_{dd} is 1V. The input signal is a 1V sine wave operating at a frequency of 5Hz. Each ADC design is evaluated under structural fault conditions. The faults are injected directly into the Spectre netlist at the device level. Over 220 fault

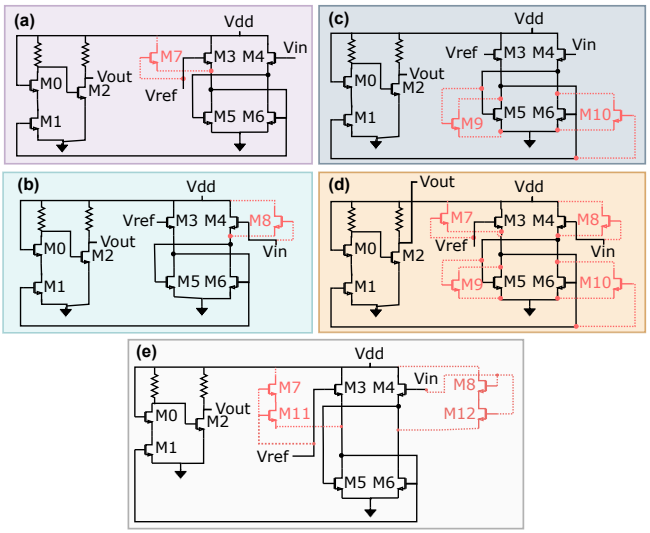


Fig. 8: Proposed comparator for enhanced fault tolerance in the flash ADC. (a) D1, (b) D2, (c) D3, (d) D4, and (e) D5.

scenarios are evaluated per design, covering all key devices and subcircuits in the ADC path. We measure the DNL, estimated from transition points in the digital output, to characterize static linearity errors.

2) Results for Single-Fault Injection: The results of the fault simulations for the Flash ADC architecture are summarized in Table IV. It can be observed that in approximately 95% of the simulated single-fault scenarios, the ADC maintains acceptable performance, with a DNL below 1. Furthermore, in more than 61% of the cases, the DNL remains below 0.5, which is considered a good margin.

After identifying the most vulnerable transistors in the baseline design, we developed several comparator variants incorporating redundant transistors to mitigate the effect of catastrophic faults. The first modification was to apply uniform resizing to the design. In this case, all transistors have the same size: W = 2 μm and L = 600 nm. This design corresponds to D0 in Table V, and the subsequent designs also use this sizing, as it provides better multi-fault tolerance than the original sizing. These designs are illustrated in Figure 8:

D1, D2: Each design includes a single redundant transistor in either M3 or M4, targeting the most critical locations identified in the fault analysis.

D3: Includes two redundant transistors in M5 and M6 to cover faults affecting the respective comparator stages.

D4: Integrates the redundancies of D1, D2, and D3 to provide comprehensive coverage across multiple vulnerable transistors.

D5: Represents a distinct comparator configuration, designed to further improve fault tolerance beyond the previous designs.

Introducing a single additional transistor increases the area by approximately 3% per comparator and by 1.6% when integrated with the Flash ADC's digital encoder. Adding two transistors results in an overall area increase of about 3%. This modest overhead is primarily due to the fact that, in FE, resistors dominate the area footprint, whereas transistors contribute comparatively little. As a result, incorporating additional transistors has a limited impact on the overall area. Changing the transistor sizing also has a negligible effect on the total area of the ADC, as the wiring and device distribution remain largely unchanged. Figure 9 shows the layout of the comparator and the full Flash ADC for both the baseline and D5 designs.

In terms of power, however, this modification provides a notable reduction of up to 11.2% compared to the baseline. It can also be observed that designs incorporating redundancy in M5 and M6 consume more power than those with redundancy in M3 and M4. This suggests that adding redundancy in the

TABLE IV: Flash ADC fault sensitivity map based on RMS DNL deviations under single-fault injection

Block	T-id[1]	OC_D[2]	OC_G[3]	OC_S[4]	SC_DG[5]	SC_GS[6]
ComFlash0	M0	0.00	0.00	0.00	0.00	0.00
	M1	0.00	0.00	0.00	0.00	0.00
	M2	0.27	0.66	0.22	0.00	0.61
	M3	0.30	0.29	0.28	1.82	0.62
	M4	0.26	0.00	1.32	0.29	0.13
	M5	0.28	2.58	0.24	1.02	0.00
	M6	0.28	0.24	0.31	1.02	0.25
ComFlash1	M0	0.61	0.62	0.65	0.61	0.61
	M1	0.65	0.59	0.64	0.56	0.59
	M2	0.26	0.60	0.27	0.62	0.59
	M3	0.29	0.42	0.61	1.46	0.56
	M4	0.58	0.60	0.59	0.29	0.34
	M5	0.39	2.06	0.35	0.63	0.59
	M6	0.25	0.62	0.41	0.63	0.64
ComFlash2	M0	0.68	0.59	0.69	0.64	0.60
	M1	0.69	0.58	0.64	0.73	0.61
	M2	0.21	0.51	0.22	0.64	0.57
	M3	0.41	0.60	0.37	1.11	0.49
	M4	0.55	0.65	0.73	0.29	0.55
	M5	0.30	1.61	0.33	0.25	0.61
	M6	0.34	0.53	0.37	0.25	0.58
ComFlash3	M0	0.51	0.44	0.57	0.57	0.53
	M1	0.57	0.46	0.56	0.59	0.45
	M2	0.35	0.49	0.39	0.51	0.45
	M3	0.47	0.81	0.59	0.87	0.49
	M4	0.50	0.54	0.49	0.29	0.61
	M5	0.31	0.53	0.33	0.43	0.45
	M6	0.49	0.54	0.53	0.43	0.57
ComFlash4	M0	0.37	0.41	0.41	0.44	0.41
	M1	0.41	0.35	0.49	0.49	0.40
	M2	0.32	0.46	0.31	0.51	0.48
	M3	0.42	1.06	0.50	0.84	0.51
	M4	0.41	0.36	0.39	0.29	0.53
	M5	0.30	0.41	0.35	0.48	0.40
	M6	0.45	0.57	0.54	0.48	0.55
ComFlash5	M0	0.24	0.27	0.27	0.23	0.38
	M1	0.27	0.21	0.52	0.34	0.25
	M2	0.34	0.43	0.40	0.26	0.45
	M3	0.56	1.32	0.51	0.64	0.43
	M4	0.45	0.31	0.27	0.29	0.49
	M5	0.34	0.33	0.36	0.45	0.25
	M6	0.49	0.52	0.48	0.45	0.56
ComFlash6	M0	0.23	0.22	0.23	0.23	0.24
	M1	0.23	0.21	0.23	0.20	0.25
	M2	0.29	0.44	0.47	0.26	0.46
	M3	0.50	1.62	0.52	0.37	0.30
	M4	0.32	0.28	0.23	0.29	0.51
	M5	0.31	0.23	0.35	0.48	0.25
	M6	0.44	0.51	0.51	0.48	0.50

Green cells indicate RMS DNL values below 0.5 (benign). Yellow cells represent values between 0.5 and 1.0 (marginal). Red cells exceed the defined 1.0 threshold (catastrophic). [1]Transistor ID. [2]OC fault at the drain terminal. [3]OC fault at the gate terminal. [4]OC fault at the source terminal. [5]SC fault between drain and gate. [6]SC fault between gate and source.

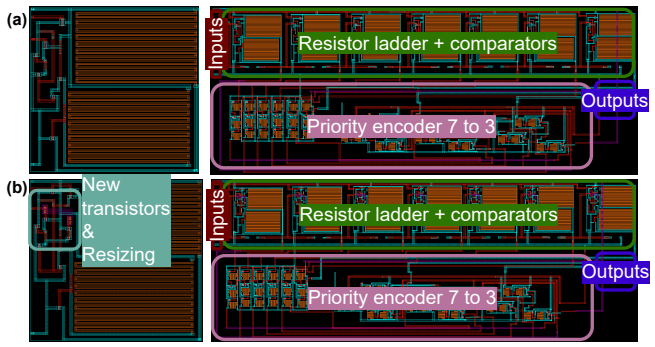


Fig. 9: (a) Layout of the baseline comparator (left) and full flash ADC (right). (b) Layout of the D5 comparator (left) and corresponding full flash ADC (right). Total area of the baseline is $0.484mm^2$, and D5 $0.5mm^2$.

TABLE V: Comparison of comparator configurations in terms of fault coverage, area, and power

Design	Single Injection		Multi Injection		A[1]	P[2]
	DNL (B/M/C)	(B+M)	DNL (B/M/C)	(B+M)		
Baseline	61.6 / 33.5 / 4.9	95.1	29.7 / 54.9 /15.4	84.6	-	-
D0	61.6 / 31.4 / 6.5	93.0	31.9 / 54.9 / 13.2	86.8	**0**	**-11.2**
D1	61.6 / 35.5 / 2.9	97.1	38.5 / 50.6 / 11.0	89.0	+1.6	-8.7
D2	**71.0** / 25.7 / 3.3	96.7	29.7/ 57.1 / 13.2	86.8	+1.6	-8.6
D3	38.8 / 49.8 / 11.4	88.6	22 / 63.7 / 14.3	85.7	+3.2	-3.3
D4	64.1 / 31.8 / 4.1	95.9	39.6 / 46.2 / 14.3	85.7	+3.2	+7.4
D5	69.8 / 27.8 / 2.4	**97.7**	**41.8** / 49.4 / 8.8	**91.2**	+3.1	-8

B (benign) = percentage of codes with DNL $<$ 0.5. M (marginal) = percentage of codes with 0.5 $\leq$ DNL $\leq$ 1. C (catastrophic) = percentage of codes with DNL $>$ 1. (B+M) = cumulative percentage of codes with DNL $\leq$ 1. [1] Area and [2] Power (%) are relative to the baseline design; positive values indicate an increase, and negative values indicate a reduction.

earlier stages of the circuit results in more efficient power consumption.

After implementing these redundant-transistor designs, the single-fault injection simulations were repeated. The results show an improvement of nearly 3% in total coverage (B+M) across the designs. In addition, the fraction of cells with DNL below 0.5 increases by more than 10%, which, as will be discussed in the multi-fault section, contributes to a more robust design under multiple simultaneous faults.

When separating the results by fault type, design D5 achieves a fault coverage of 99.3% for OC faults and 95% for SC faults. The higher OC coverage indicates that the redundant transistors effectively preserve circuit functionality when a single connection is broken, as alternative current paths remain available within the comparator structure. In contrast, SC creates low-resistance connections between nodes that should remain electrically isolated, causing multiple transistors to malfunction simultaneously.

These findings demonstrate that targeted transistor-level redundancy and resizing is an effective strategy to improve fault tolerance with minimal area overhead, setting the stage for improved multi-fault resilience in subsequent simulations.

3) Results for Multi-Fault Injection: The multi-fault simulation set was constructed by respecting the proportions of benign (B), marginal (M), and catastrophic (C) DNL values observed in single-fault simulations. For each design, we created 100 double-fault simulations that preserve these proportions. This approach guarantees that the multi-fault sample preserves the original distribution observed in single-fault injection, allowing a controlled evaluation of double-fault effects. The results are summarized in Table V. Two notable observations can be drawn. First, the total coverage remains high for several designs under multi-fault injection. For instance, design D5 shows the highest multi-fault coverage with 91.2% (B+M), compared to 97.7% in single-fault, indicating that the benign and marginal codes remain dominant even under multiple faults. Second, as expected, when extending the analysis from single- to multi-fault injection, the overall proportion of benign codes naturally decreases, as simultaneous faults impose greater stress on the circuit.

Several representative multi-fault scenarios illustrate the robustness improvements of the proposed architectures: a) *Benign + Marginal:* Combining `COM2_M3_OC_D` (benign) with `COM6_M3_OC_D` (marginal) produces a marginal DNL in the baseline and in D2 and D3, but reduced to benign in D1, D4 and D5. Similarly, `COM3_M3_SC_DG` (marginal) paired with `COM2_M3_OC_D` yields catastrophic DNL for the baseline and D3, yet remains marginal in D0, D1, D4, D5. These examples show the proposed designs suppress cross-fault amplification that otherwise leads to marginal/catastrophic codes. b) *Marginal + Marginal:* The combination `COM0_M3_SC_GS` and `COM6_M3_OC_S` produces catastrophic DNL in all designs except D5, where it is marginal. This confirms that interactions of moderate faults can still be mitigated. c) *Catastrophic + Benign:* The pair `COM5_M3_OC_G` (catastrophic) with `COM2_M3_OC_D` generates catastrophic DNL in the baseline and D1–D4, but is reduced to marginal in D5. d) *Catastrophic + Marginal:* The pair `COM0_M3_SC_GS` (marginal) with `COM6_M3_OC_G` (catastrophic) generates catastrophic DNL in the baseline and D1–D4, getting reduced to marginal in D5, improving resilience even for severe fault combinations.

Overall, the proposed comparator designs consistently prevent benign or marginal faults from escalating and, in some cases (notably D5), mitigate catastrophic contributors. This confirms that optimizing benign-DNL coverage under single-fault simulations translates directly into higher robustness under multi-fault scenarios.

Fault resilience can also be addressed at the algorithmic or architectural level via calibration, digital error correction, or adaptive thresholding; such approaches are outside the scope of this hardware-level study and are left for future work.

VI. System-Level Reliability Monitoring: Passive Implantable Sensor

While circuit-level techniques improve intrinsic robustness, system-level monitoring is critical for detecting failures in deployed implantable devices operating in harsh physiological environments. In this section, we introduce a passive, chipless sensing approach for monitoring fluid flow in implantable biomechanical systems. By leveraging RF-based interrogation, the proposed method enables reliable functionality assessment

without requiring on-board power, making it well-suited for long-term implantable applications.

A. Passive Monitoring Systems for Implantable Healthcare Applications

In-situ monitoring is particularly important for implanted shunt systems used in the management of the neurological disorder known as hydrocephalus, where impaired flow may indicate shunt failure, which could be life-threatening if left undetected. These shunt systems are often required to alleviate the intracranial pressure caused by the accumulation of cerebrospinal fluid (CSF) in the ventricles of the brain for the lifelong management of hydrocephalus [14, 15]. However, up to 40% of shunt systems fail within two years of implantation [16]. Due to the often nonspecific nature of clinical symptoms and the limited reliability of imaging modalities such as CT, MRI, X-rays, cranial ultrasound, and nuclear medicine shunt patency studies in detecting shunt malfunction, surgical exploration is frequently required for definitive diagnosis [14, 17].

Therefore, to circumvent these diagnostic challenges, several active approaches have been developed to diagnose shunt system failure, including thermal anemometry with wearable electronics [18, 19], implantable thermal flow sensors with onboard power [16], and intraluminal electrical sensing using actively stimulated electrodes [20]. While these methods are capable of measuring CSF flow, they require active power and added hardware, increasing complexity and limiting reliability. To address these limitations, a fully passive chipless monitoring approach is proposed that eliminates the need for onboard power or active electronics while enabling assessment of shunt system functionality.

The proposed monitoring approach (Figure 10(a)–(c)) uses a wearable RF transceiver to interrogate an implanted antenna-based sensor. The implanted antenna and its electrically connected bias line are fully integrated into the silicone catheter. A valve is interposed between a bias line pad at the end of a bias line and an end line pad. The bias line is able to be any arbitrary length. Accordingly, the monitoring system can be used in both adult and pediatric patients and can be positioned at different locations within a standard shunt system.

When integrated into the shunt system, the implanted antenna bias line and end line pad surfaces are directly exposed to the CSF within the catheter. The flow of CSF through the valve is primarily governed by hydrostatic pressure differences associated with patient position, and this valve-mediated flow determines the electrical connectivity between the sensing pads. The implanted antenna is designed such that this change in pad connectivity produces a corresponding shift in resonant frequency. This resonant frequency shift is detected by the external RF transceiver as a change in backscatter, allowing the passive monitoring system to function as a posture dependent connectivity sensor based on CSF flow through the valve.

Accordingly, when the valve is closed and CSF flow is absent (Figure 10(b)), as occurs in the supine position, the pads remain electrically disconnected and the antenna resonates at 915 MHz (ISM band) with suppression of the 405 MHz (MedRadio band) frequency. Conversely, when the patient is in the upright position and CSF flows through the valve (Figure 10(c)), gravitational effects promote CSF flow, and the intrinsic electrical conductivity of the CSF electrically connects the pads. This causes the resonance to shift to 405 MHz while suppressing the 915 MHz response. Persistence of a 915 MHz resonance during upright posture may therefore indicate shunt system malfunction, such as valve obstruction or impaired CSF flow.

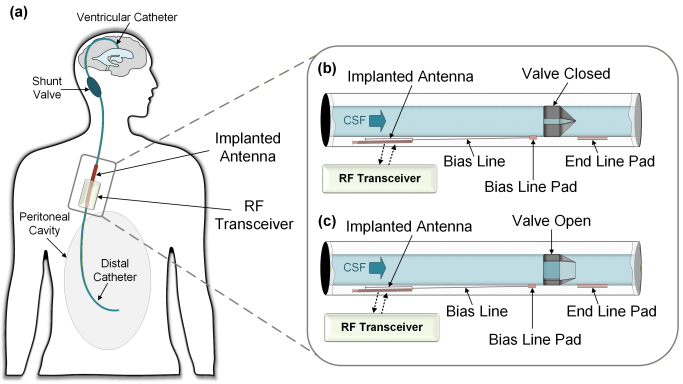


Fig. 10: (a) Passive monitoring system with an implanted antenna in a shunt system and an external wearable RF transceiver. (b) Valve closed, with disconnected sensing pads and antenna resonance at 915 MHz. (c) Valve open, with connected sensing pads and antenna resonance shifted to 405 MHz.

B. Prototype and Experimental Validation

To evaluate the proposed system's performance, prototypes of the implanted antenna (Figure 11(a)), the end line pad (Figure 11(b)), and the RF transceiver antenna (Figure 11(c)), were designed using ADS simulation software and milled using the LPKF S104. The dimensions of these antenna prototype designs are shown in Table VI.

Given that standard shunt system catheters have an inner diameter of approximately 1 mm and an outer diameter of approximately 2 mm, the maximum width of the implanted antenna, bias line, bias line pad, and end line pad was limited to approximately 1.6 mm to ensure compatibility within the catheter wall. The implanted antenna, bias line, and bias line pad were milled together as a single structure and fabricated on RO4003C substrate material with a dielectric thickness of 0.3 mm and 35 µm top copper cladding. The end line pad microstrip lines were fabricated from the same RO4003C substrate material as the implanted antenna.

The RF transceiver antenna was fabricated on RO4003C substrate material with a dielectric thickness of 0.2 mm and 17.5 µm copper cladding on both sides, with the copper layer on the back side serving as the ground plane. It was designed as a broadband antenna to enable interrogation at both operating frequencies. Measurements of the milled prototype RF transceiver antenna demonstrated return losses of approximately 19.3 dB and 22.8 dB at 405 MHz and 915 MHz, respectively, confirming adequate impedance matching across the frequency bands of interest.

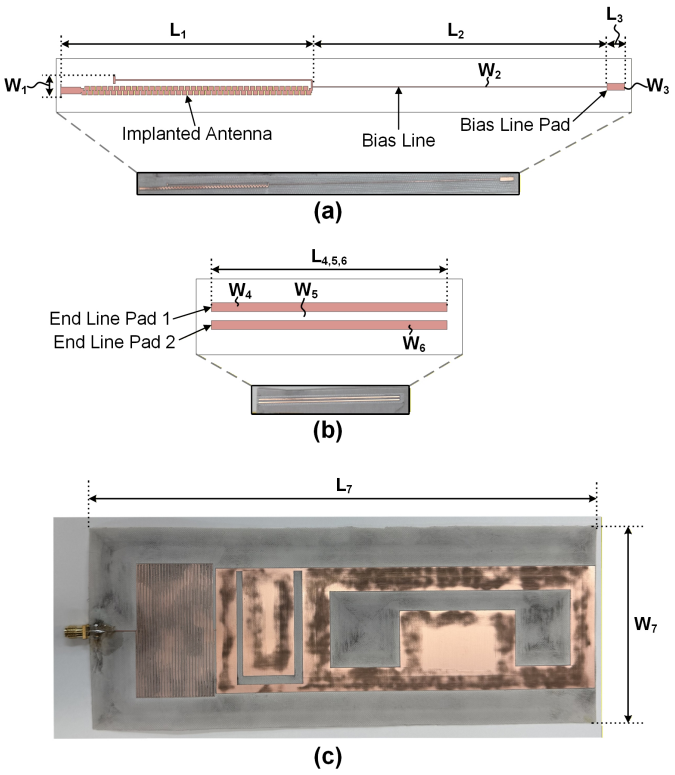


Fig. 11: (a) Implanted antenna, bias line, and bias line pad designed to resonate at 915 MHz, (b) end line pad that enables the implanted antenna to resonate at 405 MHz (while suppressing 915 MHz) when connected by CSF, and (c) milled transceiver antenna.

To emulate valve-mediated CSF conductivity responsible for electrically connecting the bias line and end line pads, a standard 0.9% saline solution was used during benchtop testing of the milled prototype antennas. Saline was used because it provides a physiologically relevant ionic medium with conductive properties similar to those of CSF. As such, the use of saline enabled emulation of the open and closed states of the shunt valve during benchtop testing. When applied across the pads, the saline established an ionic conduction pathway analogous to CSF flow through the valve, thereby electrically connecting the sensing pads.

Since saline is electrically conductive, it's electrical conductivity is frequency dependent. As such, its impedance was first characterized at the two operating frequencies (i.e., 405 MHz and 915 MHz). The measured impedance values were then

TABLE VI: Antenna Dimensions

Component	Length		Width	
	Label	Value (mm)	Label	Value (mm)
Implanted Antenna	L_1	51	W_1	1.58
Bias Line	L_2	100	W_2	0.1
Bias Line Pad	L_3	6	W_3	0.88
End Line Pad 1	L_4	52	W_4	0.5
End Line Pad 2	L_5	52	W_5	0.5
Spacing Between End Line Pads	L_6	52	W_6	0.4
Transceiver Antenna	L_7	237.5	W_7	93.8

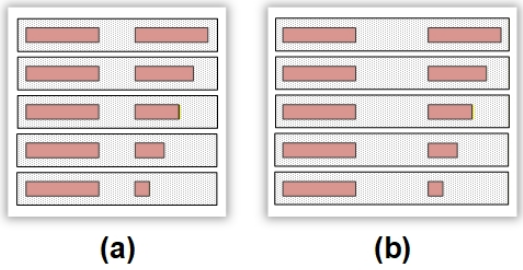


Fig. 12: Pad configurations used for saline impedance characterization. (a) Five pad pairs with a spacing of 2.5 mm. (b) Five pad pairs with a spacing of 5 mm. In each pair, the first pad was fixed at 1 mm by 5 mm, while the second pad had a fixed width of 1 mm and a length varying from 1 to 5 mm in 1 mm increments.

incorporated into the milled antenna prototype designs to ensure proper impedance matching and resonance of the implanted antenna when saline was present on the bias line and end line pads.

To characterize the impedance change caused by the introduction of saline on the pads at the two resonant frequencies, a series of experiments was conducted to isolate the saline's electrical behavior. Figure 12(a) and (b) shows the pad configurations used to evaluate saline-induced electrical connection between the pads. A total of ten pairs of pads were evaluated, with five pad pairs having a spacing of 2.5 mm (Figure 12(a)) and five pad pairs with a spacing of 5 mm (Figure 12(b)). The first pad in each pair was fixed at 1 mm by 5 mm, whereas the second pad had a fixed width of 1 mm and a length that varied from 1 to 5 mm in 1 mm increments. For each configuration, a baseline measurement of the pads without saline was first obtained and later used so that the shown impedance reflects only the saline contribution. Subsequently, 10 µL and 20 µL of saline were applied between the pads to electrically connect them, and the input reflection coefficient S_{11} was measured

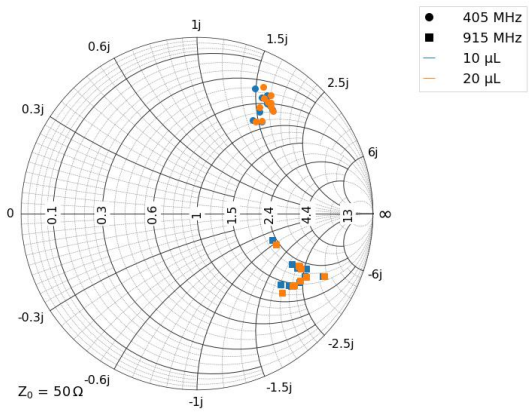


Fig. 13: Measured S_{11} of saline at 405 MHz and 915 MHz, where blue markers and orange markers represent 10 µL and 20 µL of saline, respectively.

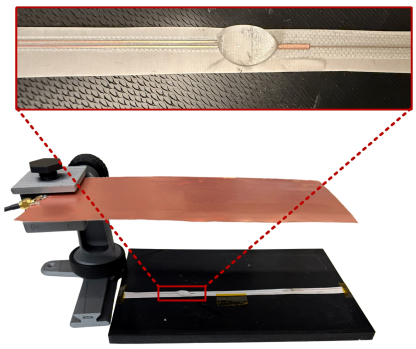


Fig. 14: Benchtop setup for wireless characterization of the implanted antenna system, with an inset showing the sensing region where saline was applied between the bias line and end line pads.

(Figure 13).

The results show distinct impedance clustering at the two frequencies. At 405 MHz, the average impedance was approximately $1.277 + j1.459$ (inductive), whereas at 915 MHz it shifted to $1.929 - j1.515$ (capacitive), indicating frequency dependent reactive behavior. Increasing the saline volume from 10 µL to 20 µL produced minimal change across all geometries and spacings, demonstrating that the response is primarily changed by the frequency and only weakly dependent on the volume of the saline.

Benchtop testing of the milled antennas was performed, as shown in Figure 14. The broadband RF transceiver antenna was connected to an RF signal generator and positioned approximately 5 inches above the implanted antenna assembly to enable wireless interrogation at 405 MHz and 915 MHz. The implanted antenna assembly was mounted on a non-conductive platform, and saline was placed between the bias line and end line pads to emulate CSF-mediated electrical connectivity corresponding to the open valve condition. For the closed valve condition, saline was placed only on the bias line pad.

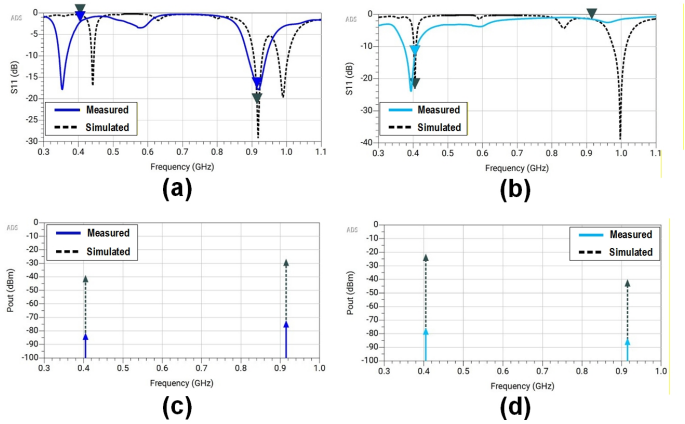


Fig. 15: Simulated and measured S_{11} and received output power for the valve closed and valve open states, showing distinct responses at 405 MHz and 915 MHz.

The simulated and measured S_{11} results for the valve closed and valve open states are shown in Figure 15(a) and Figure 15(b), respectively. For the valve closed state, resonance is observed near 915 MHz with suppression of the 405 MHz response, whereas for the valve open state, resonance shifts to 405 MHz with suppression of the 915 MHz response. The corresponding simulated and measured received output power levels are shown in Figure 15(c) and Figure 15(d). In both valve states, the simulated and measured S_{11} differences at 405 MHz and 915 MHz were sufficient to produce an observable ΔP_{out}. In particular, for the valve closed state, the simulated and measured ΔP_{out} values were approximately 12.3 dB and 9.1 dB, respectively, while for the valve open state, the simulated and measured ΔP_{out} values were approximately 18.7 dB and 7.6 dB, respectively. These results indicate that the two valve states can be differentiated through distinct resonance frequency responses that change the backscatter power responses at the two respective frequencies.

VII. Conclusion

This work addresses the critical challenge of reliability in flexible electronics for healthcare applications, particularly in the context of implantable and wearable systems operating under harsh physiological conditions. Device variability, mechanical stress, and long-term degradation necessitate design approaches that go beyond individual circuit optimization and instead consider reliability across multiple system layers.

To this end, we presented a cross-layer reliability framework spanning power delivery, signal acquisition, and system-level monitoring. At the circuit level, the proposed *ReFlex-LDO* provides robust and energy-efficient power regulation, augmented with a structural delay-based built-in self-test (BIST) for in-field fault detection. For signal acquisition, a hierarchical fault modeling and mitigation framework for IGZO-based Flash ADCs enables improved fault tolerance through targeted design enhancements. At the system level, a passive RF-based sensing approach allows monitoring of implantable biomedical devices without requiring on-board power, improving long-term reliability and safety.

By pairing passive implantable sensing elements with flexible wearable electronics, the proposed approach enables continuous and reliable health monitoring while mitigating the risks associated with embedding active electronics within the body. This integration highlights the importance of co-design across circuit and system levels in emerging flexible electronic platforms.

Future work will explore tighter integration between sensing, processing, and communication layers, as well as adaptive and self-healing mechanisms to further enhance the robustness and longevity of flexible healthcare systems.

Acknowledgments

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