Control and Loss Optimization of the HiLEM Topology - a PV Partial Power Converter

Marcus Becker*, Lukas Stefanski, Marc Hiller
Institute of Electrical Engineering, Karlsruhe Institute of Technology, Karlsruhe, Germany
*marcus.becker@kit.edu

***Abstract*—This paper presents an advanced control concept for a specialized Partial Power Converter (PPC) topology, specifically the High Efficiency Low Effort MPPT (HiLEM) circuit. A revised hardware architecture is introduced to enable a more systematic and robust control of the PPC. The results of the measurement and simulation validate the effectiveness of the proposed control strategy and highlight its potential for further functional enhancements. Beyond the novel control approach for the HiLEM topology, a loss-reduced operating method is also investigated. This method leverages the characteristic that identical input-side voltages can be generated at multiple operating points, thereby providing additional degrees of freedom for implementing an efficiency oriented operating strategy.**

***Index Terms*—DC/DC converter, Maximum Power Point Tracking, Partial Power Converter, photovoltaic system**

I. Introduction

In recent years, the newly installed capacity of photovoltaic (PV) systems has shown a consistent global growth trend, reaching a record annual rate of 32 % in 2024, resulting in an additional capacity of 451.94 GW [1]. This remarkable progress in the sector has fueled further research efforts aimed at reducing costs, increasing yields, and minimising losses in large-scale PV systems.

In large PV systems, two distinct methodologies are currently employed for connecting individual PV strings. In both variants, the modules are connected in series to form a string up to a predefined system voltage. One approach is to feed solar power into the public grid via single-stage PV systems, using a central inverter with parallel PV strings for single Maximum Power Point Tracking (single-MPPT) and grid connection. The central approach has lower investment costs and good power conversion efficiency under optimal system conditions [2]–[4].

However, when the PV system deviates from optimal conditions due to factors such as soiling, non-uniform shading, defects, string configuration, or system ageing, employing a two-stage approach with a multi Maximum Power Point Tracking (multi-MPPT) capability can significantly improve the overall system yield [3], [5]–[9]. The two-stage variant comprises a boost converter for each string, which enables a multi-MPPT mechanism with a single inverter. Using a Full Power Converter (FPC) as DC-to-DC converter (DC-DC converter) means that the entire power flow must be handled by the active switches, resulting in additional losses and reducing the overall system efficiency. Consequently, PPCs have emerged as a promising alternative for increasing system efficiency while ensuring precise MPPT [10], [11]. The PPC approach requires active processing of only a fraction of the generated system power, thus incurring a fraction of the losses, costs, and size associated with the traditional FPC [12].

In recent years, numerous topologies have been developed and studied for PPC DC-DC converters, all of which exhibit lower losses and less effort compared to conventional FPC DC-DC converters [11], [13]–[17].

One of the most promising approaches for multi-MPPT with PPC is the so-called HiLEM topology introduced in [15], [18] and further developed in [19]. The topology enables semiconductor losses to be lowered by reducing the necessary blocking voltages of the semiconductors, making it possible to use semiconductor technologies with lower voltage ratings, such as Gallium Nitride (GaN), even at high system voltages of 1000 V or even 1500 This paper presents a novel control strategy and a loss-reduced system control algorithm for the previously mentioned HiLEM topology. The paper is structured as follows:

First, Section II describes the structure and functionality of the HiLEM-2 topology, which is used in this paper and depicted in Fig. 1. Section III explains the structure and configuration of the developed control and demonstrates the system's capabilities through a simulation. The idea of the loss-optimised system controller of the converter that builds on the represented control is described in Section IV. Finally the preliminary measurement results of the controlled system with implemented Maximum Power Point Tracking (MPPT) are shown in Section V.

II. Partial Power Converter Topology - HiLEM

The PPC topology HiLEM-2, hereafter referred to as HiLEM, shown in Fig. 1 enables efficient multi-MPPT for large PV power plants.

The topology takes advantage of two important properties: On the one hand, it is not necessary to lower the converter input voltage of a string in its Maximum Power Point (MPP) down to 0 V. On the other hand, the voltage difference

$$u_{\mathrm{G,diff}} = u_{\mathrm{G,max}} - u_{\mathrm{G,min}} \tag{1}$$

between the MPP voltage of the string with the lowest voltage, $u_{\mathrm{G,min}} = \min\left(u_{\mathrm{G}x}\right)$, and the MPP voltage of the string with the highest voltage, $u_{\mathrm{G,max}} = \max\left(u_{\mathrm{G}x}\right)$, is usually low for

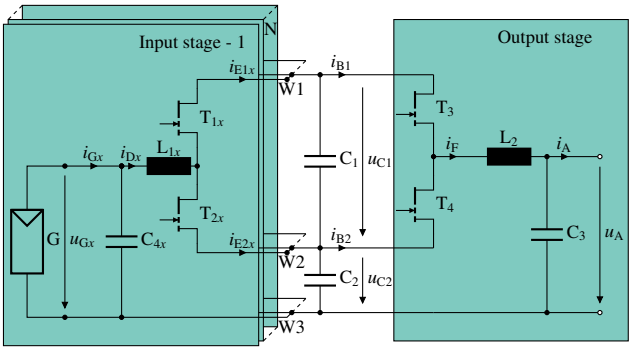

Fig. 1. Circuit design of the HiLEM-2 topology with one to N Input Stages and a single Output Stage

large PV plant applications. The reason for this is that in large PV plants, the string configuration is typically homogeneous across all strings, which means that their MPP voltages can only differ significantly due to soiling, heterogeneous shading, defects, different string orientation or ageing. Asymmetrical string configurations, meaning different number of PV modules per string, are uncommon in large PV systems. This leads to very low differential voltage between the individual strings of the system, which is utilised by HiLEM's special circuit arrangement, as it only needs to switch the differential voltage $u_{\mathrm{G,diff}}$ with its active semiconductors [15]. Furthermore, asymmetric string configurations can of course also be utilised with the HiLEM topology, as long as they do not exceed a limit defined by the design for voltage differences between the strings. However, higher differential voltages are switched by the active semiconductors, which increases switching losses.

As seen in Fig. 1, the DC link connecting the Input Stages with the Output Stage is split into an upper (W1 to W2) and lower (W2 to W3) part. This arrangement makes it possible to adjust the voltage at the Input Stage $u_{\mathrm{G}x}$ between u_{C2} and $u_{\mathrm{C2}} + u_{\mathrm{C1}}$. Fig. 2 shows this functionality of adjusting the input voltage $u_{\mathrm{G}x}$.

The hardware setup on which this paper is based was described in detail in [19]. It assigns each PV string its own Input Stage, enabling individual MPPT per string. It consists of an capacitor C_{4x}, an inductor L_{1x} and the GaN semiconductors T_{1x} and T_{2x}, with $x \in \{1 \ldots \mathrm{N}\}$. The right side of Fig. 1 is

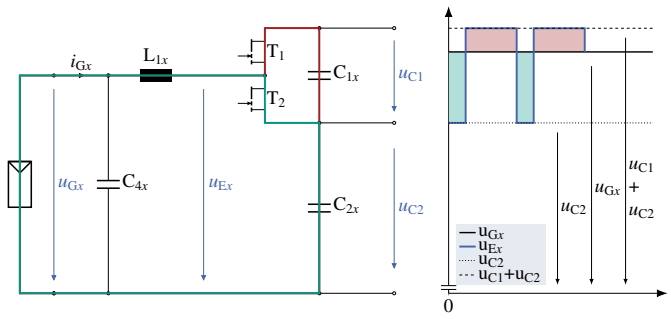

Fig. 2. Voltage adjustment for the Input Stage of the HiLEM topology

called the output stage and consists of the GaN semiconductors T_3 and T_4, a capacitor C_3 and the inductor L_2. The divided DC link with the capacitors C_1 and C_2 between W1, W2 and W3 connects the Input Stages with the single Output Stage. In the described hardware implementation, the capacitors C_1 and C_2 are allocated across the Input and Output Stages.

The following equations are based on the references [15], [19].

The Inputs Stage transistors T_{1x} and T_{2x} are driven by a Pulse Width Modulation (PWM) characterized by the duty cycle $d_{\mathrm{D}x}$ and the switching frequency f_{sw}. The corresponding conduction intervals within one switching period $T_{\mathrm{sw}} = 1/f_{\mathrm{sw}}$ are given by:

$$T_{\mathrm{T}_{1x}} = d_{\mathrm{D}x} \cdot T_{\mathrm{sw}}, \tag{2}$$

$$T_{\mathrm{T}_{2x}} = (1 - d_{\mathrm{D}x}) \cdot T_{\mathrm{sw}}. \tag{3}$$

The input current $i_{\mathrm{G}x}$ applied to each input stage is divided into the branch currents $\mathrm{i}_{\mathrm{E1}x}$ and $\mathrm{i}_{\mathrm{E2}x}$. In steady-state operation, the average values of these branch currents are:

$$\bar{i}_{\mathrm{E1}x} = d_{\mathrm{D}x} \cdot i_{\mathrm{G}x}, \tag{4}$$

$$\bar{i}_{\mathrm{E2}x} = (1 - d_{\mathrm{D}x}) \cdot i_{\mathrm{G}x}. \tag{5}$$

For simplification of the analytical framework, the N input stages are abstracted into a unified equivalent input stage. This equivalent representation is characterized by the aggregated input voltage u_{G} and the corresponding equivalent currents i_{G} and i_{D}. The total input current i_{G} is obtained as the sum of all individual input currents $i_{\mathrm{G}x}$, while the total inductor current i_{D} is defined as the sum of all individual inductor currents $i_{\mathrm{D}x}$. The total voltage u_{G} is constrained to the interval defined by the minimum string voltage $u_{\mathrm{G,min}}$ and the maximum string voltage $u_{\mathrm{G,max}}$. The equivalent quantities are determined under the assumption that the total power of all individual strings, given by $P_{\mathrm{G}x} = u_{\mathrm{G}x} \cdot i_{\mathrm{G}x}$, is equal to the equivalent aggregated power $P_{\mathrm{G}} = u_{\mathrm{G}} \cdot i_{\mathrm{G}}$. Accordingly, the equivalent voltage u_{G} is obtained by applying power-normalization to the aggregated input stage:

$$i_{\mathrm{G}} = \sum_{x=1}^{\mathrm{N}} i_{\mathrm{G}x}, \qquad i_{\mathrm{D}} = \sum_{x=1}^{\mathrm{N}} i_{\mathrm{D}x}, \tag{6}$$

$$u_{\mathrm{G}} = \frac{P_{\mathrm{G}}}{i_{\mathrm{G}}} = \frac{\sum_{x=1}^{\mathrm{N}} p_{\mathrm{G}x}}{i_{\mathrm{G}}} = \frac{\sum_{x=1}^{\mathrm{N}} u_{\mathrm{G}x}\, i_{\mathrm{G}x}}{i_{\mathrm{G}}}. \tag{7}$$

The Output Stage combines the currents i_{B1} and i_{B2} by the semiconductors T_3 and T_4. They are controlled using PWM with the duty cycle d_{F}. The corresponding conduction intervals within one switching period $T_{\mathrm{sw}} = 1/f_{\mathrm{sw}}$ are given by:

$$T_{\mathrm{T}_3} = d_{\mathrm{F}} \cdot T_{\mathrm{sw}} \tag{8}$$

$$T_{\mathrm{T}_4} = (1 - d_{\mathrm{F}}) \cdot T_{\mathrm{sw}} \tag{9}$$

Under steady-state conditions, the average output power $\overline{p_{\mathrm{F}}} = u_{\mathrm{A}} \cdot \overline{i_{\mathrm{D}}}$ corresponds to the input power $p_{\mathrm{G}} = u_{\mathrm{G}} \cdot i_{\mathrm{G}}$ minus the internal losses of the converter. The output current i_{A} corresponds to the mean inductor current $\overline{i_{\mathrm{D}}}$, due to current aggregation at the input stage, it is identical to the equivalent

input current i_{G}. If the internal losses are neglected, the output voltage u_{A} approximates the equivalent input voltage u_{G}:

$$i_{\mathrm{A}} = \overline{i_{\mathrm{D}}} = i_{\mathrm{G}}, \tag{10}$$

$$u_{\mathrm{A}} \approx u_{\mathrm{G}}. \tag{11}$$

Consequently, the inverter is supplied with an input voltage u_{A}, whose magnitude may vary within the admissible range defined by $u_{\mathrm{G,min}}$ and $u_{\mathrm{G,max}}$:

$$u_{\mathrm{G,min}} \leq u_{\mathrm{A}} \lesssim u_{\mathrm{G,max}}. \tag{12}$$

A voltage boost beyond $u_{\mathrm{G,max}}$ is not achievable with this topology. This restriction does not impose a practical limitation, since most inverter architectures are inherently designed to operate over a wide range of DC input voltages.

The previously mentioned hardware setup uses GaN semiconductors with a blocking voltage of 650 V, which limits the voltage level of the upper DC link u_{C1} to 400 V. This value also serves as the upper limit for the differential voltage $u_{\mathrm{G,diff}}$ between the input strings. This also represents the limitation for deviation in asymmetric string configurations. The voltage of the lower DC link u_{C2} is designed for a maximum voltage of 1000 V, which allows a system voltage of up to 1000 V to be set at the input, regardless of the current voltage level of u_{C1}.

In order to minimize switching losses, the most straightforward approach is to ensure the voltage u_{C1} is kept as low as possible while using the second voltage u_{C2} to ensure the necessary system voltage for the MPP at the Input Stage. A comprehensive elaboration of this control methodology is provided in Section IV.

III. Control Design for fast switching HiLEM Topology

The already mentioned new hardware design used for this paper allows a new straightforward strategy to control the HiLEM DC-DC converter. To get an overview of how the signal processing of the new hardware design works, Fig. 3 shows the connection and control diagram of the system that has been set up. The input and Output Stages have a Local Control Unit (LCU) based on a Field Programmable Gate Array (FPGA) from Altera's MAX10© series, communicating with the Central Control Unit (CCU) using an Fiber Optic Cable (FOC) interface. The CCU is a modular, highly performant and fully adaptable real-time signal processing platform containing a Zynq-7030 System on Chip (SoC) from Xilinx© as its central logic chip [20].

As shown in Fig. 2, the input voltage $u_{\mathrm{G}x}$ is driven by the PWM of T_1 and T_2. To determine the modulation duty cycle $d_{\mathrm{D}x}$), a cascaded control is implemented at the LCU of each single Input Stage. The two proportional integral controller (PI controller) forming the control structure of the input side, consisting of a voltage controller for $u_{\mathrm{G}x}$ and a subordinate current controller for $i_{\mathrm{D}x}$.

The subordinate current PI controller for $i_{\mathrm{D}x}$ is designed according to the optimum criteria. This means that the internal current control loop of $i_{\mathrm{D}x}$ behaves like a second-order element with an attenuation of $d = \sqrt{2}$. The voltage PI controller for $u_{\mathrm{G}x}$ results in the combination of an integrator and a first-order element, in which the parameters can be determined with the help of the symmetrical optimum. A better controller performance is achieved by using a back calculation anti-windup. To avoid saturation of the choke, the operating range of the choke L_1 is set as the control value limit.

To stabilize overshoot during setpoint changes of $u^*_{\mathrm{G}x}$, a first-order element is connected as an optional reference value filter before the controller's setpoint input.

The setpoint of $u_{\mathrm{G}x}$ is provided by a local MPPT algorithm, implemented in the LCU of each Input Stage. This MPPT is based on a Perturb and Observe algorithm (P&O algorithm) [21], that finds a local optimal operating point for the connected PV string by perturbing the input voltage and observing the behaviour. A comparison between the instantaneous power and that of the previous operating point enables a decision regarding whether the voltage trajectory should be further advanced in the current direction or whether the polarity of the voltage increment should be reversed.

The setpoints of the two remaining voltages of the divided DC link u_{C1} and u_{C2} are controlled by the LCU of the Output Stage.

Voltage u_{C2} is driven by the PWM of T_3 and T_4, with the modulation duty cycle d_{F} provided by a cascaded control structure at the LCU of the Output Stage. The control structure is similar to the Input Stage consisting of a voltage controller for u_{C2} and a subordinate current controller for i_{F}.

The current i_{F} is controlled by the subordinate PI controller which is designed according to the optimum criteria. Similar to the Input Stage, i_{F} behaves like a second-order element with an attenuation of $d = \sqrt{2}$. As with the Input Stage, the voltage PI controller for u_{C2} is also designed with the help of the symmetrical optimum. A better controller performance is achieved by using a back calculation anti-windup. Achieving better controller performance involves implementing a back-calculation anti-windup. To prevent the choke from saturating, the operating range of the choke L_2 is set as the control value limit.

Another PI controller, located at the Output Stage, controls the voltage of u_{C1} using the control variable u_{A}. To regulate the capacitor voltage u_{C1}, the approach is expressed in relation to the power. If losses are neglected, the difference of the powers in capacitor C_1 occurs as follows:

$$p_{\mathrm{C_1}} = \underbrace{u_{\mathrm{G}} \cdot i_{\mathrm{D}}}_{p_{\mathrm{D}}} - \underbrace{u_{\mathrm{A}} \cdot i_{\mathrm{F}}}_{p_{\mathrm{F}}} - \underbrace{u_{\mathrm{C2}} \cdot i_{\mathrm{C2}}}_{p_{\mathrm{C_2}}} \tag{13}$$

With u_{G} as the average value of the input voltages $u_{\mathrm{G}x}$ weighted over the current $i_{\mathrm{D}x}$. The average power $p_{\mathrm{C_2}}$ over capacitor C_2 is approximately 0 W and can therefore be neglected for further consideration. The output voltage u_{A}, provided by an arbitrary output-side circuit, for example a DC-to-AC converter (DC-AC converter) or a DC-DC converter, is a suitable degree of freedom to regulate the capacitor voltage u_{C1}. Considering the transfer function $G_{u_{\mathrm{A}}}(s)$ of the voltage

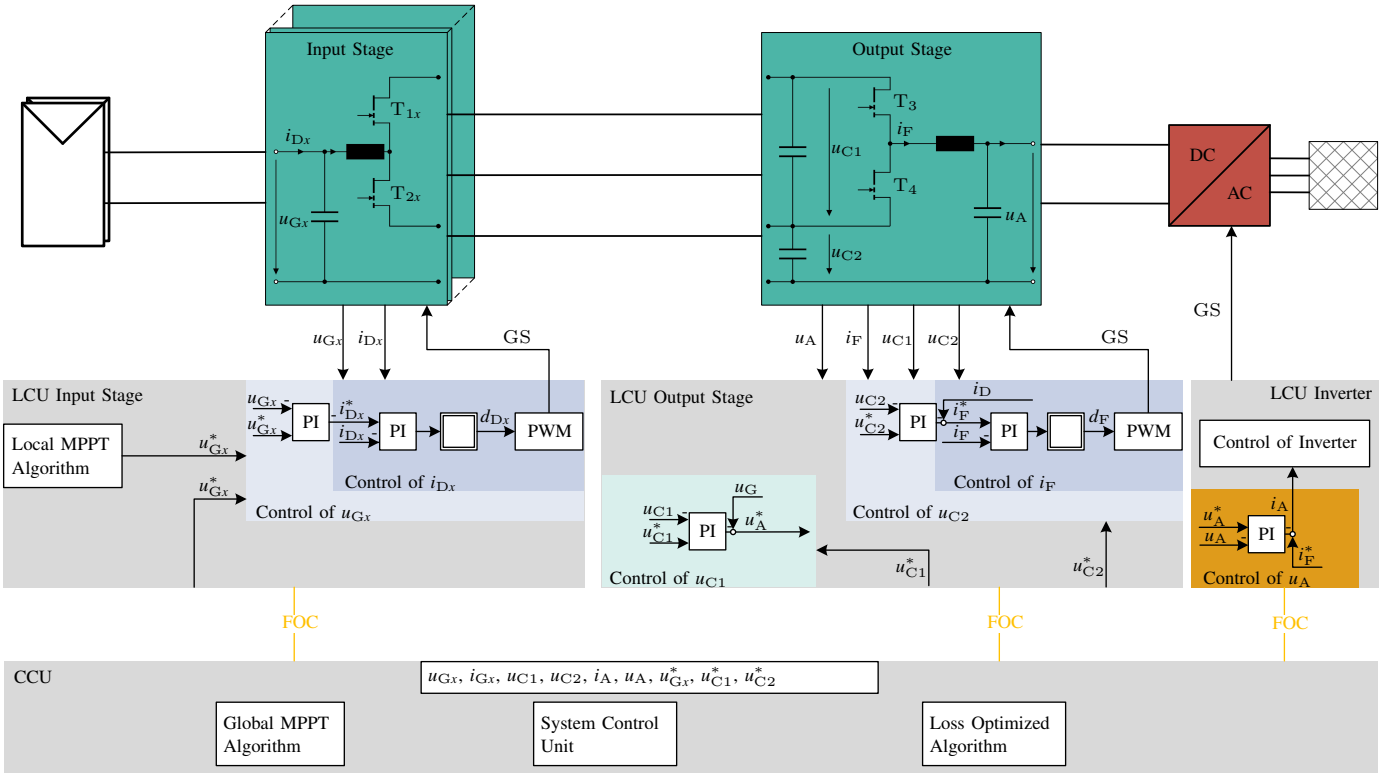

Fig. 3. Structure of the HiLEM Control System

control circuit and Eq. (13), it follows for p_{C_1} with the controller output variable u'_{C1}:

$$p_{C_1} = u_G \cdot i_D + G_{u_A}(s) \cdot u'_{C1} \cdot i_F - G_{u_A}(s) \cdot u_G \cdot i_F \quad (14)$$

The setpoints u^*_{C1} and u^*_{C2} are defined by the higher level CCU with a loss-reduced approach explained in Section IV. In Section V, the control behaviour will be presented using the control approach described above.

IV. Loss Reduced System Operation

The largest loss contributions in the HiLEM circuit are caused by the conduction and switching losses of the GaN High-Electron-Mobility Transistor (HEMT) employed in the Input and Output Stage. This is where the greatest potential for loss-reduced operation is available. With the HiLEM topology, it is possible to realise an input voltage u_{Gx} with different operating points of the voltages (u_{C1}, u_{C2}) of the divided DC link. The primary loss-minimisation strategy consists in regulating the upper DC-link voltage u_{C1} to the lowest feasible level, thereby reducing the semiconductor switching losses associated with high voltage stress. It must be ensured that u_{C1} is at least as high as $u_{G,diff}$ from Eq. (1), otherwise the voltage at the input cannot be set correctly. The lower DC link voltage u_{C2} must then be selected such that the remaining voltage difference for the input voltages u_{Gx} can be provided.

In addition, the following boundary conditions must be observed when regulating the DC-link voltages. The system-wide voltage constraints must be satisfied at all times, meaning that u_{C1} must not exceed $U_{C1,max} = 400\,\mathrm{V}$, and the combined DC-link voltage $u_{C1} + u_{C2}$ must remain below $U_{sys,max} = 1000\,\mathrm{V}$ to ensure electrically safe operation and prevent overstressing of insulation and semiconductor devices. Moreover, the input voltage control loop requires a defined voltage buffer U_{buf} on u_{C1} to avoid operation at the modulation boundaries corresponding to $u_{G,max}$ and $u_{G,min}$. This voltage buffer enables rapid compensation of minor variations in the input voltages u_{Gx} without necessitating continuous adjustment of the divided DC-link voltages u_{C1} and u_{C2}.

The algorithm scheme, with the specified boundary conditions, is illustrated in Fig. 4, calculating the voltage setpoints U^*_{C1} for the upper DC link and U^*_{C2} for the lower DC link. To illustrate this approach, a simulation was performed, which is shown in Fig. 10, whereby the input voltages u_{Gx} were varied. The simulation results are discussed in Section V. The loss-reduced algorithm from Fig. 4 selects an operation point with low switching losses, for the given input voltages u_{Gx}, but neglects the main value that actually needs to be optimised, namely the total system yield. This consists mainly of two components: the system losses and the solar PV yield from which the losses must be deducted to receive the total system yield. Therefore, in certain configurations, it may be more effective to discontinue operating the Input Stage in local MPP mode and instead reduce system losses in the HiLEM topology, thereby enhancing overall system performance. For this purpose, loss characteristic maps seen in Fig. 5 and Fig. 7 were generated for the HiLEM topology in order to be able to determine the losses of the current operating point during

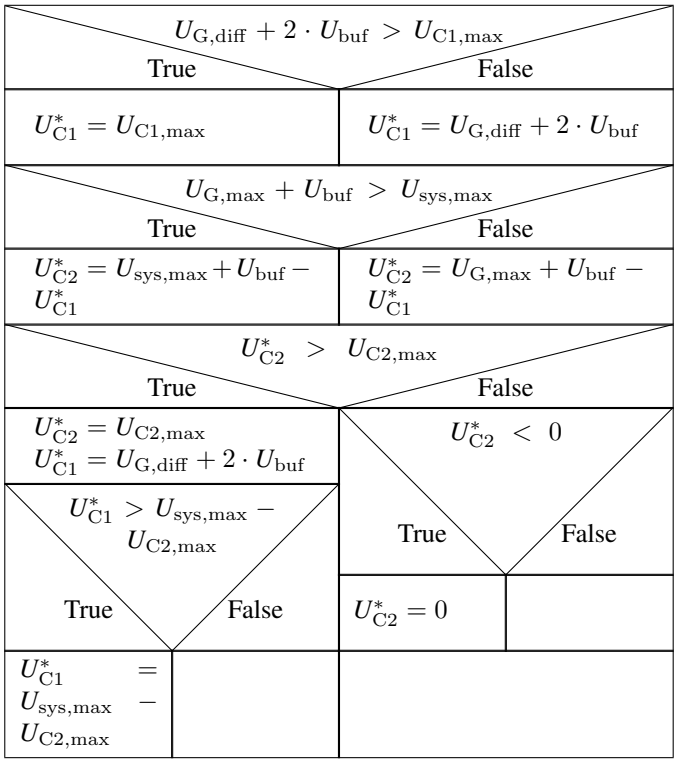

Fig. 4. Loss-reduced algorithm

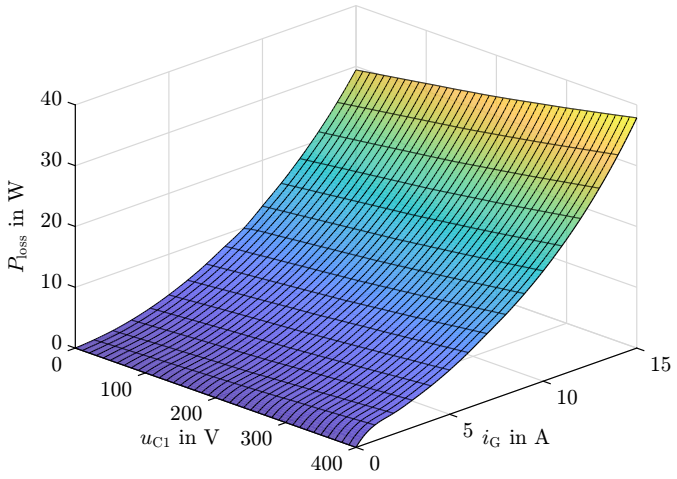

Fig. 5. Loss characteristic map of the Input Stage

runtime. A more advanced approach is now to compare the PV yield and the HiLEM system losses, provided by the loss characteristic maps at different operating points. Based on this comparison, an operating point for each Input and Output Stage can then be selected that maximises the overall system yield. More precisely, a global MPPT is implemented, which periodically cycles through certain voltage ranges of the strings. The specific PV power of the detected MPPs is determined, and then the system losses occurring at the respective operating point are to be subtracted, thereby obtaining the total system yield of the respective operating point.

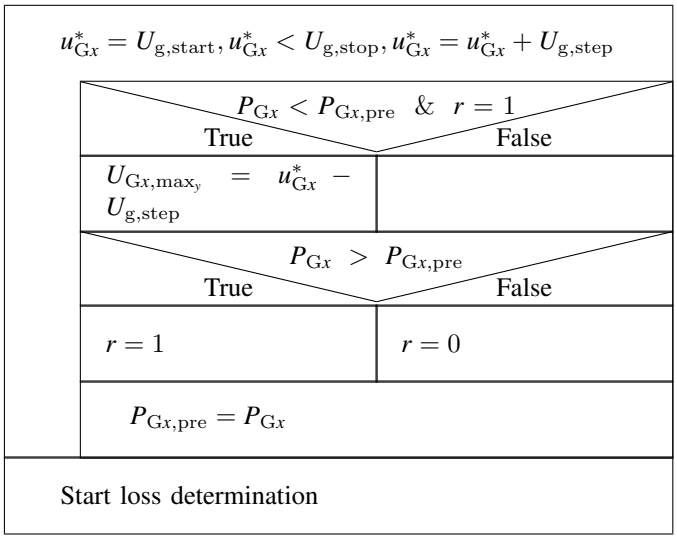

Fig. 6. Advanced system-power algorithm

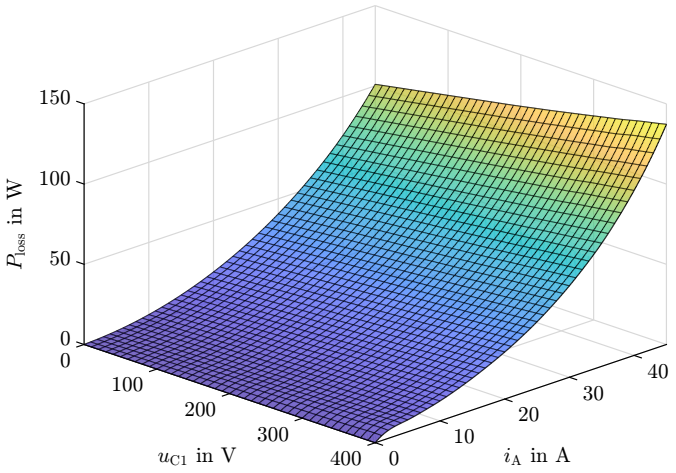

Fig. 7. Loss characteristic map of the Output Stage

The advanced system-power algorithm combines the continuous setpoint determination of u^*_{C1} and u^*_{C2} of the loss-reduced algorithm from Fig. 4 with a periodically executed global MPPT. The global MPPT is only performed periodically every 10 min to 30 min, whereby the periodic execution time can be adjusted to the configuration and conditions of the PV system. This results in voltage setpoints for the individual string voltages $u^*_{\mathrm{G}x}$ optimised for the overall system power, which are transmitted to the local MPPT of the input stages as initial values. The structural process of the algorithm is illustrated in Fig. 6. The loss evaluation then assigns the corresponding power-loss values to each local maximum, as illustrated in Fig. 5 and Fig. 7, and aggregates the individual loss components to obtain the total system losses at the respective operating point. The local maximum that achieves the highest total system output is then selected, meaning the PV power minus the losses within the topology.

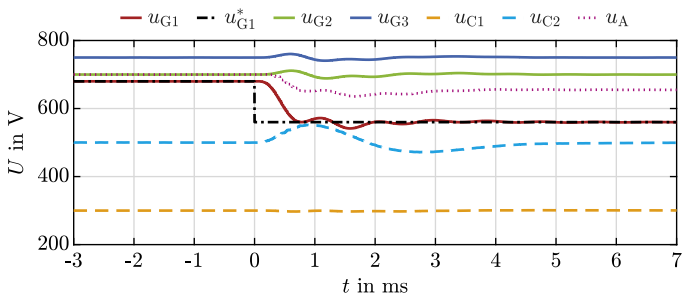

Fig. 8. Simulation of HiLEM control with a setpoint step of u_{G1}

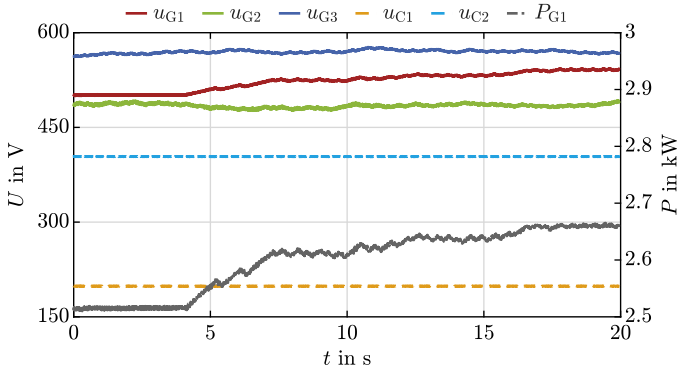

Fig. 9. Measurement of three HiLEM Input Stages with active MPPT

V. Simulations and Measurements

To demonstrate the behaviour of the control system presented in Section III, the simulation shown in Fig. 8 was prepared. A step change in the setpoint value u^*_{G1} of u_{G1} from 680 V to 560 V was performed to demonstrate the response behaviour of the implemented control system. A rapidly declining oscillation of the step response of u_{G1} with minor setpoint deviation can be observed. The output voltage u_A behaves as expected and corresponds to the weighted input voltages u_{G1} to u_{G3}, and the voltage u_{C2} deviates slightly from the setpoint during the change of u_{G1}.

Fig. 9 shows the measurement of the Input Stage control with activated local MPPT for three active input stages. The MPPT was ensured by the local P&O algorithm described in Section III. The three PV strings were emulated with a three-channel PV emulator (EA-PSB 20920-40 triple 4U) for this measurement. A MPP voltage of 490 V was set on string 2 and a MPP voltage of 580 V was set on string 3, which were adjusted appropriately by the control system of the Input Stages. For string 1, the MPP voltage was abruptly increased from 500 V to 550 V at $t = 4$ s. The controller then increased the voltage to the appropriate MPP value, which can also be seen from the power output of string 1 P_{G1}.

To demonstrate the loss-reduced algorithm shown in Section IV, the simulation displayed in Fig. 10 was performed. Initially, it can be seen that the voltages u_{C1} and u_{C2} adapt with the buffer voltage $U_{buf} = 30$ V to the total voltage and to the voltage difference $u_{G,diff}$ from u_{G1} to u_{G3}, as described in

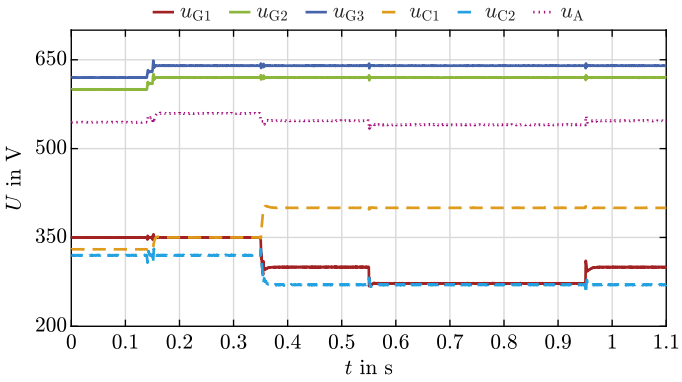

Fig. 10. Simulation of the loss-reduced algorithm

Section IV. From $T = 0.35$ s, the voltage of u_{G1} continues to decrease, so that u_{C1} reaches the specified limit of 400 V, but all voltages can still be set correctly. As soon as $T = 0.55$ s, a setpoint value of 250 V is requested for u_{G1}, which cannot be fully achieved due to the limitation of u_{C1}. Because the algorithm seeks the highest possible yield by favouring larger voltages, the voltages u_{G2} and u_{G3} are set at their target levels, whereas u_{G1} is intentionally limited in order to keep within system constraints.

The advanced system-power algorithm presented in Section IV uses the described loss-reduced algorithm in order to find the setpoints u^*_{C1} and u^*_{C2} that minimise losses for the specified operating points u_{Gx}. Second, it integrates a global MPPT, in which a defined voltage range is cycled through for each string in order to find the global MPP from several possible local MPPs, and to set the starting value for a local MPPT algorithm there. The advanced system-power algorithm presented here extends this global MPPT to include a loss analysis of the individual operating points. Although the global MPPT finds the operating points at which the highest PV yield can be achieved. These operating points need not necessarily be those with the highest total system yield, as the losses in the selected MPPs could be disproportionately high. To demonstrate the advantages of the advanced system-power algorithm presented in Section IV, it is compared in Fig. 12 and Fig. 13 with a standard global MPPT algorithm. The conditions for the PV strings are selected such that multiple local MPPs occur, in order to demonstrate real-world conditions affected by the factors mentioned in Section I, such as shading, soiling or uneven orientation. The power-voltage characteristics of the three simulated PV strings are shown in Fig. 11. The local MPPs can be obtained from Tab. I, and the voltage buffer was set to $U_{buf} = 20$ V. Particularly for local MPPs that lie in close proximity to one another, the advanced system-power algorithm is capable of identifying an operating point that yields higher net system power than the standard global MPP approach.

A comparison of Fig. 12 and Fig. 13 shows that the advanced system-power algorithm selects a different MPP for String 1. In contrast to the standard global MPPT, the

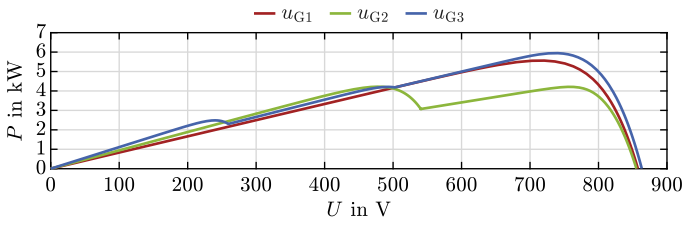

Fig. 11. Simulated current-voltage characteristics of the PV strings

TABLE I
VOLTAGE VALUES OF THE LOCAL MPPS

String 1	480 V	760 V	-
String 2	240 V	495 V	740
String 3	720 V	-	-

advanced algorithm targets maximization of the system output power and therefore selects for String 1 a MPP with a higher operating voltage. This allows u_{C1} to be controlled to a lower value, which in turn reduces conduction and switching losses in both the Input and Output stages.

In the operating scenario considered, the use of the advanced system-power algorithm yields a total of 17 W more system power to be achieved compared to the standard global MPPT algorithm, despite a reduction in gained PV power. This corresponds to an increase in overall system efficiency of just over 0.1 %, achieved solely by an optimized selection of the operating MPPs. By design, the algorithm guarantees that, in the worst case, the same performance as the global MPPT is obtained; thus, no penalty arises from deploying the advanced system-power strategy. In addition, the systematically reduced losses lower the thermal and electrical stress on the semiconductors, which is expected to have a positive impact on device reliability and operating lifetime.

VI. Conclusion and Outlook

This paper introduces a novel control scheme and operating strategy for loss reduction in a PV PPC based on the HiLEM topology. The control architecture, including the MPPT routine, is detailed in Section III and validated by both simulation and experimental results in Section V.

The HiLEM topology provides additional control degrees of freedom by enabling flexible adjustment of the input voltages u_{Gx} via independent setting of the split DC-link voltages u_{C1} and u_{C2} across the full operating range. This flexibility permits systematic selection of operating points that minimise conduction and switching losses.

To exploit this capability, a loss-reduced algorithm for computing the optimal setpoints of u_{C1} and u_{C2} was introduced in Section IV and its performance evaluated in Section V. In addition, an advanced system-power algorithm was introduced in Section IV, which incorporates a topology-specific loss model to evaluate efficiency over a wide range of operating conditions and to compare overall system efficiency with alternative strategies. The algorithm was then compared with a

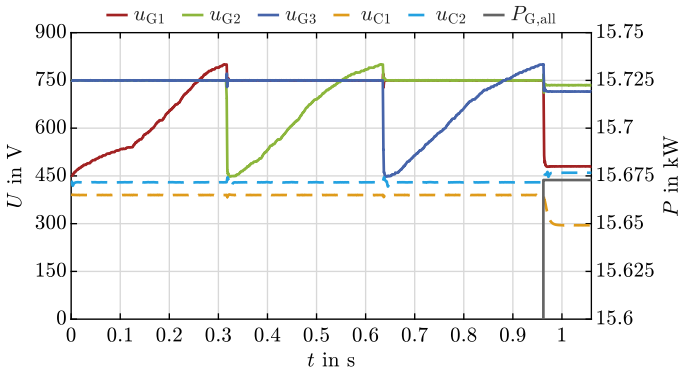

Fig. 12. Simulation of the standard global MPPT algorithm

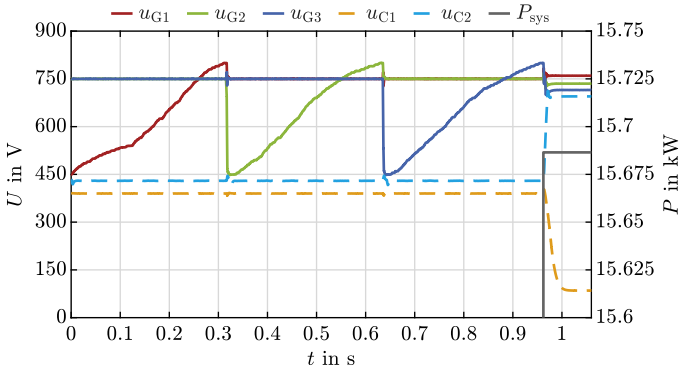

Fig. 13. Simulation of the advanced system algorithm

standard global MPPT under challenging string conditions and serves as the basis for yield maximization through loss-aware operating point selection.

Future work on the advanced system-power algorithm includes integrating more efficient search strategies to accelerate the identification of local MPPs and extending the analysis of device stress reduction enabled by loss-optimized operating points. The extension of the advanced system-power algorithm to the subsequent DC-AC converter is also a promising strategy for fully enhancing overall system efficiency.

Compared to a conventional boost converter, which requires semiconductor devices rated for the full DC-link voltage, the divided DC-link topology of HiLEM enables the use of semiconductors with a lower blocking voltage than the system voltage. As a result, power semiconductors, such as GaN HEMT shown here, can be used with significantly lower blocking voltages. Such devices typically feature lower conduction losses and lower switching energies while being considerably more cost-efficient than high-voltage counterparts required in traditional boost converter topologies.

Although the HiLEM topology necessitates a larger semiconductor count due to the additional output stage, this drawback is offset by the higher conversion efficiency and comparable, or potentially lower, overall system cost relative to a conventional boost-converter-based solution.

REFERENCES

[1] J. Prime, I. A. Ahmed, D. Akande, N. Elhassan, Y. Melnikov, and A. Whiteman, "Renewable Capacity Statistics 2025," IRENA, Abu Dhabi, Tech. Rep., Mar. 2025.

[2] A. Hensel, L. Probst, and B. Burger, "Study on the possbile yield gain by Inverters with Multi-MPPT compared to Single-MPPT Inverters for different solar system configurations and locations," Fraunhofer ISE, Freiburg, Study, Sep. 2021.

[3] S. Leva, F. P. Yu Hu, and E. Lamanna, "Performance and Economic Comparison of String and Central Inverter Systems," in *2023 IEEE International Conference on Environment and Electrical Engineering and 2023 IEEE Industrial and Commercial Power Systems Europe (EEEIC / I&CPS Europe)*, Jun. 2023, pp. 1–6.

[4] N. Foureaux, A. Machado, É. Silva, I. Pires, J. Brito, and B. C. F, "Central inverter topology issues in large-scale photovoltaic power plants: Shading and system losses," in *2015 IEEE 42nd Photovoltaic Specialist Conference (PVSC)*, Jun. 2015, pp. 1–6.

[5] B. Atasoy and S. S. Tezcan, "Comparison of String and Central Inverter for 10MW PV Plant," in *2021 5th International Symposium on Multidisciplinary Studies and Innovative Technologies (ISMSIT)*, Oct. 2021, pp. 182–186.

[6] K. M. Paasch, M. Nymand, and S. B. Kjær, "Long term energy yield measurements of a string- vs. central inverter concept tested on a large scale PV-plant," in *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, Sep. 2015, pp. 1–9.

[7] M. Alawadhi, H. Albeshr, A. Husnain, A. Almarzooqi, A. Sahoo, and S. K. Sadanandan, "Techno-Economic Analysis of String vs Central Inverter Fed on a Large-Scale PV Plant," in *2022 IEEE PES 14th Asia-Pacific Power and Energy Engineering Conference (APPEEC)*, Nov. 2022, pp. 1–6.

[8] A. Desai, I. Mukhopadhyay, and A. Ray, "Performance Analysis of String and Central Inverter based Ideally Designed Utility scale Solar PV Plant," in *2020 47th IEEE Photovoltaic Specialists Conference (PVSC)*, Jun. 2020, pp. 2412–2417.

[9] B. Dumnić, E. Liivik, B. Popadić, F. Blaabjerg, D. Milićević, and V. Katić, "Comparative Analysis of Reliability for String and Central Inverter PV Systems in Accordance with the FMECA," in *2020 IEEE 11th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, Sep. 2020, pp. 591–596.

[10] J. W. Zapata, S. Kouro, G. Carrasco, H. Renaudineau, and T. A. Meynard, "Analysis of Partial Power DC–DC Converters for Two-Stage Photovoltaic Systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 1, pp. 591–603, Mar. 2019.

[11] J. Zhao, K. Yeates, and Y. Han, "Analysis of high efficiency DC/DC converter processing partial input/output power," in *2013 IEEE 14th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Jun. 2013, pp. 1–8.

[12] N. Weldt, J. Espinoza, D. Sbárbaro, L. Morán, and S. Kouro, "Topologies and Control Strategies of Partial Power DC/DC Converters for Photovoltaic Systems," in *IECON 2021 – 47th Annual Conference of the IEEE Industrial Electronics Society*, Oct. 2021, pp. 1–6.

[13] J. W. Zapata, S. Kouro, G. Carrasco, and H. Renaudineau, "Step-Up Partial Power DC-DC Converters for Two-Stage PV Systems with Interleaved Current Performance," *Energies*, vol. 11, no. 2, p. 357, Feb. 2018.

[14] J. Rojas, H. Renaudineau, S. Kouro, and S. Rivera, "Partial power DC-DC converter for electric vehicle fast charging stations," in *IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society*, Oct. 2017, pp. 5274–5279.

[15] M. Gommeringer, A. Schmitt, F. Kammerer, and M. Braun, "An ultra-efficient maximum power point tracking circuit for photovoltaic inverters," in *IECON 2015 - 41st Annual Conference of the IEEE Industrial Electronics Society*, Nov. 2015, pp. 001 704–001 709.

[16] A. Morrison, J. W. Zapata, S. Kouro, M. A. Perez, T. A. Meynard, and H. Renaudineau, "Partial power DC-DC converter for photovoltaic two-stage string inverters," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2016, pp. 1–6.

[17] B. Chen, Y. Wang, Y. Tian, and S. Wei, "Current Sharing/Voltage Sharing Control Strategy for Cascaded DC/DC Converter in Photovoltaic DC Collection System," in *2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia)*, May 2018, pp. 1397–1402.

[18] M. Gommeringer, "Neue effiziente und aufwandsarme Schaltungen zum individuellen Maximum Power Point Tracking mehrerer Solarmodulstränge / von Dipl.-Ing. Mario Gommeringer," Ph.D. dissertation, Karlsruher Institut für Technologie (Elektrotechnisches Institut), 2016.

[19] M. Becker, L. Stefanski, and M. Hiller, "Design of a GaN-Based DC-DC Converter with HiLEM Topology for Efficient MPP-Tracking," in *2024 Energy Conversion Congress & Expo Europe (ECCE Europe)*, Sep. 2024, pp. 1–8.

[20] B. Schmitz-Rode, L. Stefanski, R. Schwendemann, S. Decker, S. Mersche, P. Kiehnle, P. Himmelmann, A. Liske, and M. Hiller, "A modular signal processing platform for grid and motor control, HIL and PHIL applications," in *2022 International Power Electronics Conference (IPEC-Himeji 2022- ECCE Asia)*, May 2022, pp. 1817–1824.

[21] M. A. G. de Brito, L. Galotto, L. P. Sampaio, G. d. A. e Melo, and C. A. Canesin, "Evaluation of the Main MPPT Techniques for Photovoltaic Applications," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 3, pp. 1156–1167, Mar. 2013.