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Full Length Article

LF-MightyPix: A second HV-MAPS prototype for the LHCb Mighty-Tracker☆

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ABSTRACT

For the future high-luminosity operation of the LHCb experiment, the downstream tracker will be upgraded to the Mighty-Tracker. A key part of this upgrade is the introduction of silicon pixel detectors, MightyPix, in the central region of the tracker. We have developed MightyPix prototype chips using High-Voltage Monolithic Active Pixel Sensors fabricated in a commercially available CMOS process on high-resistivity wafers. The second prototype chip, LF-MightyPix, is fabricated in the LFoundry 150 nm CMOS process. LF-MightyPix has a chip size of 3.5 mm × 4.0 mm and a pixel size of 100 µm × 100 µm. For each pixel hit, both the time of arrival and the time over threshold are recorded to ensure correct bunch-crossing identification at 40 MHz. The results presented in this paper confirm compatibility with the MightyPix requirements.

1. Introduction

The Large Hadron Collider beauty (LHCb) experiment [1] at CERN after its Upgrade II, scheduled for 2034–2035, is expected to achieve an instantaneous luminosity of up to $10^{34}\,\mathrm{cm^{-2}\,s^{-1}}$ and to collect a total integrated luminosity of $300\,\mathrm{fb^{-1}}$ [2]. To operate under this high-luminosity condition, the downstream tracker currently based on scintillating fibers will be upgraded to the Mighty-Tracker, whose central region will be based on silicon pixel detectors named MightyPix [3]. MightyPix is based on High Voltage Monolithic Active Pixel Sensors (HV-MAPS) [4] since the monolithic design simplifies construction compared to hybrid sensors, which is advantageous for large-scale detector systems such as the Mighty-Tracker.

Due to the complexity of MAPS design, both the sensor and the readout electronics require careful optimization. The full development of MightyPix is expected to take more than ten years from initial planning to final installation. The discontinuation of the CMOS process during the development could delay the project schedule. Therefore, evaluating alternative CMOS processes as potential backup options is important to ensure long-term feasibility.

In this paper, we describe the prototype LF-MightyPix, which was ported to an alternative CMOS process technology. The suitability of this technology is evaluated in terms of sensor depletion and timing performance at the target power consumption.

2. MightyPix

2.1. Requirements and prototype development

Requirements for the MightyPix, derived from the physics goals of the LHCb Upgrade II, are described in earlier studies [2,3]. These requirements are summarized in Table 1. The MightyPix development includes three prototype chips prior to Mighty-Tracker production: MightyPix1, MightyPix2, and MightyPix3. MightyPix1 is the first prototype dedicated to the Mighty-Tracker and implements the basic LHCb control and data-acquisition interfaces. The chip has been fabricated and tested [5]. MightyPix2, with a chip size of 20.1 mm × 18.7 mm, integrates nearly all functions foreseen for the final design [6]. The chip has been submitted for fabrication. MightyPix3 will be the final full-reticle pre-production prototype and will include improvements based on the results of the previous prototypes.

The structure of HV-MAPS is shown in Fig. 1. A charge-collection well is implemented as a deep n-well, the deepest n-well available in the process. A p–n junction forms between the collection well and the p-type substrate, where a reverse bias voltage will be applied. Multi-well structures enable CMOS readout electronics to be inside the collection well and isolated from the substrate. Thus, the HV-MAPS design allows a high bias voltage to be applied to the substrate.

To meet the MightyPix requirements, CMOS processes are selected based on the following criteria: (1) support for multi-well structures, (2)

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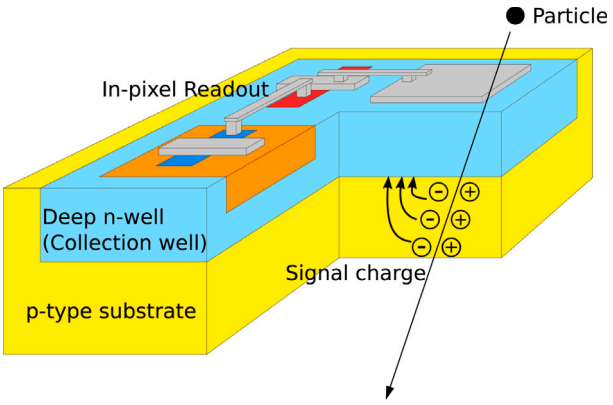

Fig. 1. Simplified diagram of HV-MAPS structure.

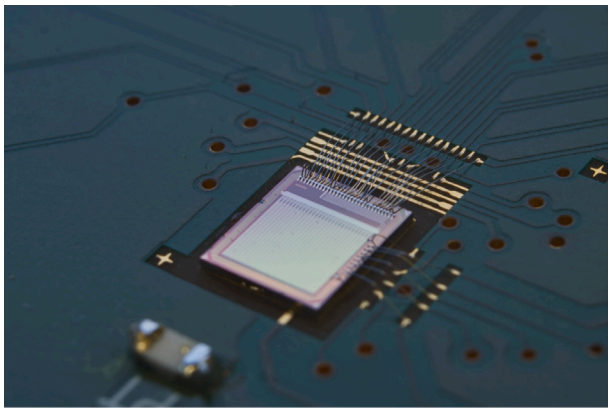

Fig. 2. LF-MightyPix on a PCB for the GECCO system.

Table 1
Requirements of the MightyPix.

Parameter	Value
Area to be covered	~18 m^2
Pixel size	≤100 µm × ≤300 µm
Chip thickness	<200 µm
Maximum hit rate	34 Mhit/s/cm^2
Overall detection efficiency	>96 % including inactive areas (e.g. chip gaps)
In-time detection efficiency	>99 % within 25 ns for the active area
NIEL (End of Life)	3×10^{14} (1MeV)n_{eq}/cm^2
TID (End of Life)	40 Mrad
Power consumption	<150 mW cm^{-2}
Data transmission rate	1.28 Gbps per port

availability of high-resistivity wafers, (3) sufficient production capacity for the Mighty-Tracker, and (4) demonstrated radiation hardness in previous projects. Criterion (2) is necessary to achieve the required radiation tolerance. A sufficiently large depletion region, formed by the high substrate resistivity and a high bias voltage, enables fast charge collection by drift before radiation-induced charge trapping occurs [7]. The TSI/AMS 180 nm CMOS technology [8,9] used for MightyPix1 and MightyPix2 satisfies all these criteria, including a substrate resistivity of >280 Ω cm and demonstrated radiation hardness [10].

In parallel, LF-MightyPix has been developed as a prototype using the LFoundry 150 nm CMOS technology [11]. It also meets the previous criteria, including wafers with resistivity above 2 kΩ cm and proven radiation hardness [12]. LF-MightyPix has been designed taking into account the differences between the two CMOS processes, such as the wafer resistivity (>2 kΩ cm and >280 Ω cm), feature size (150 nm and 180 nm), and the well structure details.

2.2. LF-MightyPix

LF-MightyPix has been fabricated (Fig. 2) as a small prototype chip with dimensions of 3.5 mm × 4.0 mm and a thickness of 280 µm. It consists of three main components (Fig. 3a). The largest component is the pixel matrix, which has 28 columns and 23 rows. The pixel size is 100 µm × 100 µm.

The in-pixel readout electronics include n-well biasing circuits, a chargesensitive amplifier (CSA), and a comparator (Fig. 3b) [13]. The n-well biasing circuits apply a voltage of approximately 1.8 V to the collection well. A capacitor connected to the collection well (C_{inj}) enables test-pulse injections. The CSA amplifies the collected charge and converts it into a voltage signal. A high-pass filter between the CSA and the comparator shapes the signal before discrimination. Each pixel includes a 4-bit trim DAC (TDAC) and a 1-bit switch, and their configuration bits are stored in a 5-bit RAM. The TDAC adjusts the comparator threshold, and the switch enables or disables the comparator output.

The comparator output is sent to the hit buffers, which are located between the pixel matrix and the chip periphery as shown in Fig. 3a. To reduce power consumption and minimize crosstalk, the output signal amplitude is controlled by a voltage called V_{minus} in Fig. 3b. Each pixel has one corresponding hit-buffer cell that stores the timestamps of the leading and trailing edges of the comparator output in DRAM. The time of arrival (ToA) and time over threshold (ToT) are calculated from these timestamps outside the chip. The ToT reflects the signal amplitude, which can be estimated after applying an appropriate calibration. The hit buffers use a column-drain architecture. Each column includes an end-of-column circuit that mediates communication between the buffer cells in that column and the finite state machine (FSM) in the chip periphery.

The chip periphery is the third main component of the chip. It contains peripheral function blocks such as the FSM, a timestamp counter, and a newly implemented serializer. The timestamp counter value is distributed to the hit buffers. It is a dual-edge counter, which improves the ToA resolution. The serializer encodes the data and reformats it into 32-bit packets [14], and sends it out at the maximum speed of 1.28 Gbps. It operates as expected and has been integrated into the digital periphery of MightyPix2 [6].

3. Measurement results

The LF-MightyPix has been evaluated using a test system based on the GECCO system [15,16] and the Basil framework [17]. Fig. 4 shows the leakage current as a function of the sensor bias voltage. The leakage current begins to significantly rise at bias voltages around −195 V. This increase suggests that the depletion region extends to the back-side of the chip, where the surface is non-uniform due to wafer thinning. Assuming that the front-side inactive region, i.e., from the surface to the deep n-well, and the back-side surface non-uniformity together amount to 20 µm, the effective sensitive thickness of the sensor diode is estimated to be 260 µm. Using this assumption and a simple planar diode model, in which the depletion depth is $0.3\sqrt{V_{bias}\,[V] \cdot R_{wafer}\,[\Omega\,cm]}\,[\mu m]$ [7], the wafer resistivity is estimated to be 4 kΩ cm,

which is higher than the resistivity guaranteed by the foundry and is consistent with a previous study [18]. Since the required chip thickness for MightyPix is <200 µm (Table 1), the results demonstrate that full depletion of the sensor is achievable below −195 V.

TDAC tuning is performed by injecting test pulses pixel-by-pixel via C_{inj}, while lowering the comparator threshold in each pixel using the TDAC. The tuned value is taken as the TDAC value at which the pixel first detects the test pulse during the threshold scan. Fig. 5 shows the intrinsic threshold distribution and the distribution after applying the TDAC tuning. After tuning, the threshold uniformity reaches a standard deviation of 32 e^-, and the mean threshold is approximately 1.8 ke^-.

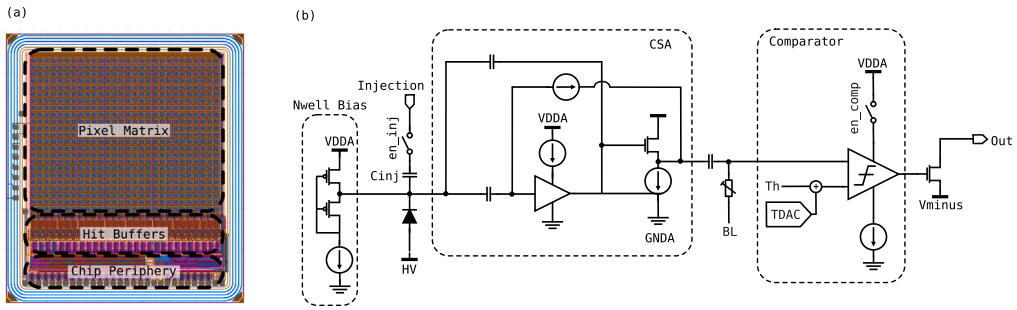

Fig. 3. Chip layout (a) and in-pixel readout circuit (b) of LF-MightyPix.

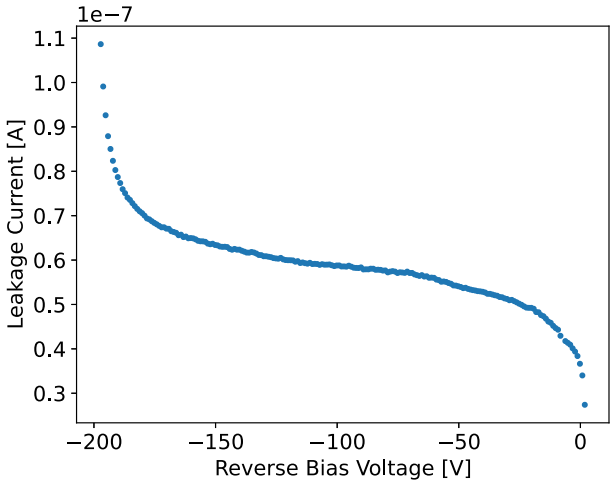

Fig. 4. Leakage current of LF-MightyPix as a function of the reverse bias voltage.

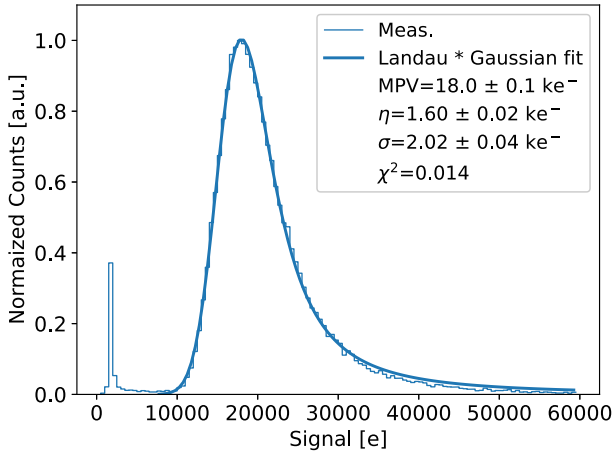

Fig. 6. ^{90}Sr spectrum measured at a bias voltage of −150 V. The spectrum was fitted with an approximate Landau function convoluted with a Gaussian function, and fitting parameters are shown in the legend. η and σ are the Landau width parameter and the Gaussian standard deviation, respectively.

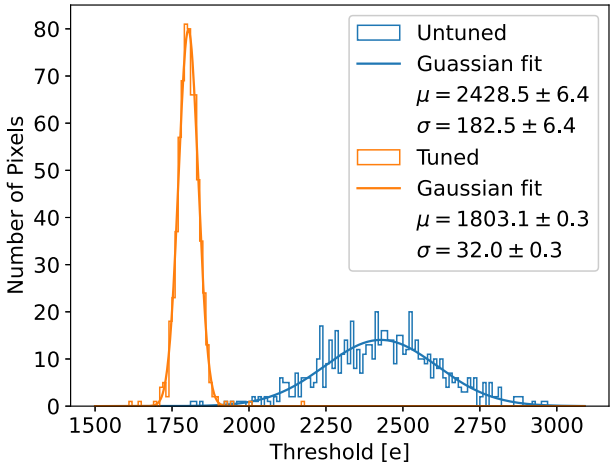

Fig. 5. Threshold distributions of LF-MightyPix before and after TDAC tuning. Each distribution is fitted with a Gaussian function, and the mean and standard deviation are indicated in the legend as μ and σ, respectively. The uncertainties correspond to the fitting errors.

Fig. 6 shows the ^{90}Sr spectrum at a bias voltage of −150 V, measured with all pixels enabled and using the tuned TDAC values. To mitigate the low-energy component of ^{90}Sr, a polyethylene terephthalate filter has been inserted between the ^{90}Sr source and the LF-MightyPix chip, and a scintillator has been placed behind the chip as a timing reference. Particles occasionally produce hits that spread over multiple pixels, which typically indicates that the particle entered the sensor at a non-perpendicular angle. To remove such cases, the hit data are clustered by grouping hits that are contiguous in rows or columns, and only events with a cluster size of one, i.e., single-pixel hits, are selected. The ToT values of these single-pixel hits are then converted into signal charge. To perform this conversion, a calibration curve is obtained for each pixel individually by injecting test pulses with varying amplitudes into C_{inj} and recording the corresponding ToT response. The measured ToT–charge relation for each pixel is subsequently used to convert the ToT values into charge in a pixel-by-pixel manner.

The most probable value (MPV) is obtained as 18.0 ± 0.1 ke$^-$ by fitting the spectrum with a Landau function convoluted with a Gaussian (Fig. 6). The small structure near 0 e$^-$ in the figure is excluded from the fit because it is an artifact caused by baseline and cross-talk noise. At a bias voltage of −150 V, using a wafer resistivity of 4 kΩ cm from the leakage current measurement, the approximate depletion depth is 230 μm. Assuming that β-particles emitted from ^{90}Sr are minimum ionizing particles, producing 80 e$^-$/μm in silicon [7], the expected MPV of the collected charge is about 18.4 ke$^-$. Considering the approximations and assumptions, the expected and measured MPVs show good agreement.

To evaluate the timing performance of LF-MightyPix, the chip has been configured to the designed power consumption of 11 μW/pixel (110 mW cm^{-2}), as the time resolution depends on the power consumption. This value is chosen to leave margin for the power consumption in the hit buffers and chip periphery to meet the requirement (Table 1). The timestamp clock of LF-MightyPix is operated at 80 MHz. As the leading-edge timestamp is generated by a dual-edge counter, the least significant bit (LSB) corresponds to 6.25 ns. The measurement was performed using the same setup as for the ^{90}Sr spectrum. The

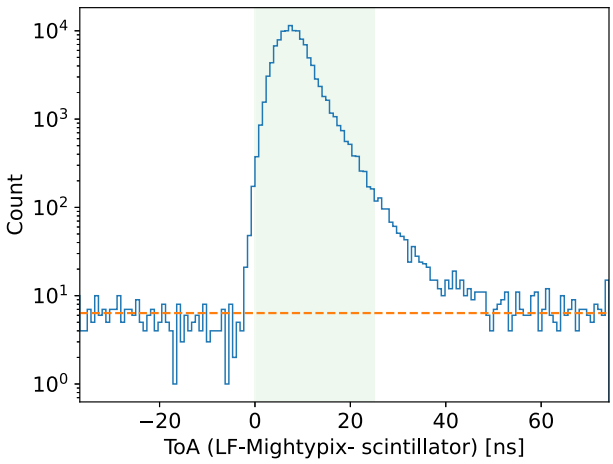

Fig. 7. ToA difference between LF-MightyPix and the scintillator measured using a ^{90}Sr source. The light green hatched region indicates the 25 ns bin used to determine the in-time percentage, defined as the fraction of events falling within this bin. The averaged background level is shown as an orange dashed line.

scintillator signal is measured using an external comparator and a time-to-digital converter operating at a sampling rate of 1.28 GHz.

Fig. 7 shows the ToA difference for LF-MightyPix at a bias voltage of −150 V, measured relative to the scintillator signal, after subtracting a fixed offset. The hit data are clustered, and the ToA of the seed pixel, defined as the pixel with the largest ToT value in each cluster, is used as the ToA of LF-MightyPix. A uniform background is observed in Fig. 7. The average value in the region where the ToA difference is less than −25 ns is subtracted as background in the analysis, as it originates from mismatches between scintillator hits and LF-MightyPix hits. The scintillator is larger than the LF-MightyPix and has no spatial resolution, while its comparator threshold is strictly set to enhance timing performance. As a result, some scintillator events do not have corresponding LF-MightyPix hits, and some LF-MightyPix hits do not have corresponding scintillator events.

The ToA distribution shows different slopes on its left and right sides, with the right side falling more slowly. This asymmetry originates from time walk of the in-pixel readout. Because delay of the small signals are larger than that of the large signals, ToT-based corrections are expected to improve the timing performance. However, even without the ToT timing correction, the percentage of hits within a 25 ns bin has been measured as high as 99.1 ± 0.2 %. This result confirms that LF-MightyPix can achieve a good time resolution at the designed power consumption.

4. Summary

In this work, we present the development and evaluation of the second prototype chip of MightyPix, LF-MightyPix, designed using the LFoundry 150 nm CMOS process for the Mighty-Tracker after the LHCb Upgrade II. A sufficient depletion depth of the sensor (>200 µm) has been confirmed by IV measurements and the ^{90}Sr spectrum. A pixel-by-pixel threshold standard deviation of 32 e^- is achieved after tuning, and 99.1 ± 0.2 % of hits are in-time of 25 ns bin at the pixel power consumption of 11 µW/pixel (110 mW cm^{-2}). These results show that this alternative process is a feasible option for MightyPix and also future HV-MAPS developments. Detection efficiency studies after irradiation are planned as a further study, as well as the development of the next prototype using this CMOS process with additional features for MightyPix.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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References

[1] The LHCb Collaboration, The LHCb detector at the LHC, J. Instrum. 3 (08) (2008) S08005, http://dx.doi.org/10.1088/1748-0221/3/08/S08005.
[2] The LHCb Collaboration, LHCb Framework TDR for the LHCb Upgrade II Opportunities in flavour physics, and beyond, in the HL-LHC era, Tech. Rep.CERN-LHCC-2021-012, 2022.
[3] The LHCb Collaboration, LHCb Upgrade II Scoping Document, Tech. Rep., CERN, Geneva, 2024.
[4] I. Peric, A novel monolithic pixelated particle detector implemented in high-voltage CMOS technology, Nucl. Instr. Meth. A 582 (2007) 876–885, http://dx.doi.org/10.1016/j.nima.2007.07.115.
[5] S. Scherl, Development of a Silicon Detector in HV-CMOS Processes for the LHCb Mighty Tracker (Ph.D. thesis), University of Liverpool, 2025, http://dx.doi.org/10.17638/03190258.
[6] N. Striebig, et al., MightyPix – A novel high voltage monolithic active pixel sensor for the proposed LHCb Mighty-Tracker, J. Instrum. 21 (04) (2026) C04059, http://dx.doi.org/10.1088/1748-0221/21/04/C04059.
[7] H. Kolanoski, N. Wermes, Particle Detectors: Fundamentals and Applications, Oxford University Press, 2020, http://dx.doi.org/10.1093/oso/9780198858362.001.0001.
[8] TSI Incorporated, TSI. URL https://tsi.com/.
[9] ams-OSRAM AG, ams OSRAM. URL https://ams-osram.com/.
[10] M. Benoit, et al., Testbeam results of irradiated ams H18 HV-CMOS pixel sensor prototypes, J. Instrum. 13 (02) (2018) P02011, http://dx.doi.org/10.1088/1748-0221/13/02/P02011.
[11] LFoundry S.r.l, LFoundry. URL https://ams-osram.com/.
[12] M. Barbero, et al., Radiation hard DMAPS pixel sensors in 150 nm CMOS technology for operation at LHC, J. Instrum. 15 (05) (2020) P05013, http://dx.doi.org/10.1088/1748-0221/15/05/P05013.
[13] I. Peric, et al., High-Voltage CMOS active pixel sensor, IEEE J. Solid-State Circuits 56 (8) (2021) 2488–2502, http://dx.doi.org/10.1109/JSSC.2021.3061760.
[14] S. Scherl, et al., MightyPix at the LHCb Mighty Tracker — verification of an HV-CMOS pixel chip's digital readout, J. Instrum. 19 (04) (2024) C04045, http://dx.doi.org/10.1088/1748-0221/19/04/C04045.
[15] R. Schimassek, Development and Characterisation of Integrated Sensors for Particle Physics (Ph.D. thesis), Karlsruher Institut für Technologie, 2021, http://dx.doi.org/10.5445/IR/1000141412.
[16] F.M. Ehrler, Characterization of monolithic HV-CMOS pixel sensors for particle physics experiments (Ph.D. thesis), Karlsruher Institut für Technologie, 2021, http://dx.doi.org/10.5445/IR/1000133748.
[17] SiLab, University of Bonn, Basil. URL https://github.com/silab-Bonn/basil.
[18] T. Hirono, et al., CMOS pixel sensors on high resistive substrate for high-rate, high-radiation environments, Nucl. Instr. Meth. A 831 (2016) 94–98, http://dx.doi.org/10.1016/j.nima.2016.01.088.