A 2 × 2 240–270-GHz Transmitter Array With 33 dBm of EIRP in a 0.13-μm SiGe Technology

Kaan Balaban, *Graduate Student Member, IEEE*, Max Vöhringer, Matthias Möck, *Graduate Student Member, IEEE*, Marius Kretschmann, Thomas Zwick, *Fellow, IEEE*, John Jelonnek, *Senior Member, IEEE*, and Ahmet Çağrı Ulusoy, *Senior Member, IEEE*

***Abstract*—This work presents a 240–270-GHz transmitter array implemented in a 0.13-μm SiGe BiCMOS process. The transmitter array comprises two J-band ×6 frequency multipliers, four J-band four-way combined power amplifiers (PAs), and an on-chip 2 × 2 antenna array. The system is driven by an external continuous-wave (CW) signal generator, and each four-way combined PA delivers a peak output power of 16.7 dBm at 250 GHz with a 3-dB bandwidth of 50 GHz. The integrated antenna array consists of four differential dipoles with a reflector layer beneath the silicon substrate to enhance radiation efficiency. The fabricated transmitter array achieves an equivalent isotropically radiated power (EIRP) of 33 dBm and estimated total radiated power ($P_{\text{tot,rad}}$) of 21 dBm at 264 GHz with a 3-dB bandwidth of 30 GHz while consuming 4 W of DC power and occupying a silicon area of 13 mm^2. Compared to prior works at similar frequencies, the proposed transmitter array achieves a 9-dB higher EIRP than previously reported silicon-based transmitters without the use of external lens-based gain enhancement.**

***Index Terms*—Integrated circuits (ICs), J-band, millimeter-wave (mm-wave), SiGe BiCMOS, transmitter array.**

I. Introduction

SUB-TERAHERTZ and millimeter-wave frequencies have gained attention for a wide range of applications, including high-resolution radar, high-data-rate wireless communications, and molecular-scale material characterization. Electron paramagnetic resonance (EPR) and nuclear magnetic resonance (NMR) spectroscopy, in particular, rely on high-frequency electromagnetic (EM) excitation to probe material properties. In particular, dynamic nuclear polarization (DNP) serves to enhance NMR sensitivity through the transfer of polarization from electron spins to nuclear spins utilizing microwave excitation at millimeter-wave frequencies. Since DNP-NMR systems operate at high magnetic flux densities, the electron spin resonance frequency scales linearly with the applied field; for instance, a 9.4-T field necessitates microwave excitation at approximately 263 GHz. Conventional DNP systems employ gyrotrons to generate 10–100-W output power in this frequency range; however, these sources exhibit limited bandwidth [1]. In this work, a gyrotron traveling-wave tube (gyro-TWT) can serve as a broadband high-power source, and a silicon-based solid-state power amplifier (PA) is introduced, serving either as a driver stage for the gyro-TWT or as a standalone source for low-power DNP experiments [2].

Using silicon-based technologies with high yield and high integration capability enables achieving higher output power levels through parallelization. However, as the operating frequency approaches f_{max}, the limited transistor gain becomes the primary bottleneck in designing high-power transmitters. Reported silicon-based PAs at these frequencies deliver a maximum output power of about 50 mW [3], [4], [5], [6]. These results indicate that the desired high-level output power can only be attained by parallelizing multiple amplifiers. On the other hand, losses in the power-combining structures and detuning of impedance matching during combining impose a fundamental limit on the maximum achievable output power. Moreover, the relatively low efficiency of the transistor introduces severe thermal issues, making heat management increasingly difficult. Although the lossy nature of the silicon substrate presents significant challenges at J-band frequencies, integrating antennas on-chip and employing spatial power combining across multiple channels offers a promising solution [7]. The proposed architecture employs transmission-line-based power combining within each PA–antenna unit, while the overall array-level power combining is achieved spatially through the antenna array. Compared to fully centralized transmission-line or transformer-based combining schemes, this approach reduces the passive routing and insertion loss associated with combining high-power signals at J-band frequencies. In addition, the proposed architecture enables the parallelization of multiple PA–antenna units, each operating at thermally manageable power levels, thereby improving scalability and alleviating the excessive parasitic and thermal challenges associated with single large-PA implementations. Furthermore, both the DC and RF inputs are provided from one side of the chip, facilitating scalable multichip array implementations.

Abdo et al. [8] present a 1×4 chip array, where each element consists of a CMOS transmitter (TX) chip packaged with an

Received 10 April 2026; revised 13 June 2026; accepted 3 July 2026. This work was supported by the Deutsche Forschungsgemeinschaft (DFG, German Research Foundation)—SFB 1527/1 under Project 454252029. *(Corresponding author: Kaan Balaban.)*

Kaan Balaban, Matthias Möck, Thomas Zwick, and Ahmet Çağrı Ulusoy are with the Institute of Radio Frequency Engineering and Electronics (IHE), Karlsruhe Institute of Technology, 76131 Karlsruhe, Germany (e-mail: kaan.balaban@kit.edu).

Max Vöhringer and John Jelonnek are with the Institute for Pulsed Power and Microwave Technology (IHM), Karlsruhe Institute of Technology, 76344 Karlsruhe, Germany.

Marius Kretschmann was with the Institute of Radio Frequency Engineering and Electronics (IHE), Karlsruhe Institute of Technology, 76131 Karlsruhe, Germany. He is now with VEGA Grieshaber KG, 76137 Karlsruhe, Germany.

Digital Object Identifier 10.1109/TMTT.2026.3711721

InP chip containing PAs and on-chip antipodal Vivaldi antennas. Such integration introduces challenges in maintaining array uniformity due to the packaging interface between the CMOS and InP chips. In [9], a 1×4 phased array integrating on-chip differential double-folded dipole antennas using local backside etching (LBE) is reported. However, LBE requires an additional postmicromachining step that is not available in all technologies. In [10], a 2×2 phased array implemented in a SiGe technology is demonstrated, where oscillators serve as the core TX components and on-chip patch antennas act as the radiating elements. In [11], a 1×2 phased array integrating an off-chip bow-tie antenna through a novel packaging solution in a SiGe technology is presented. However, the use of off-chip antennas introduces challenges in alignment accuracy and repeatability, which can degrade array uniformity and phase coherence, particularly in multichip-array implementations. Although promising results have been reported, most prior works rely either on specialized postmicromachining steps that are not available in all technologies or on packaging-based antenna solutions that degrade the array uniformity and limit the practicality of multichip-array implementations. Therefore, a scalable transmitter architecture that avoids additional postprocessing steps and complex packaging remains highly desirable.

In this work, a scalable, single-chip transmitter array with 2×2 elements is presented, achieving an equivalent isotropically radiated power (EIRP) of 33 dBm and an estimated $P_{\text{tot,rad}}$ of 21 dBm at 264 GHz with a 3-dB bandwidth of 30 GHz, surpassing the output power of previously reported silicon-based transmitters at the similar frequencies. A single-tone continuous-wave (CW) signal is supplied to the transmitter array, which relaxes the strict linearity requirements in this work.

The remainder of this article is organized as follows: Section II presents the architecture of the proposed transmitter array, including the design considerations for scalability and individual building blocks. Section III details the on-chip integrated antenna and its array implementation. Section IV presents the board design and discusses the packaging solutions with emphasis on thermal considerations. Section V describes the experimental setup and results, highlighting the achieved output power, bandwidth, and EIRP performance. Finally, Section VI presents the comparison of this work with the state of the art and concludes this article.

II. Transmitter Array Architecture

The block diagram and chip micrograph of the 2×2 transmitter array are shown in Fig. 1(a) and (b), respectively. The proposed architecture integrates a 2×2 dipole antenna array with four PAs, with each pair of PAs driven by a $\times 6$ frequency multiplier.

In antenna array implementation, array uniformity is critical for controlling main lobe width and sidelobe levels. For off-chip configurations, achieving uniformity depends heavily on the board tolerance and reproducibility of bondwire characteristics, such as width, length, and landing angle, introducing significant challenges in packaging and assembly. On-chip

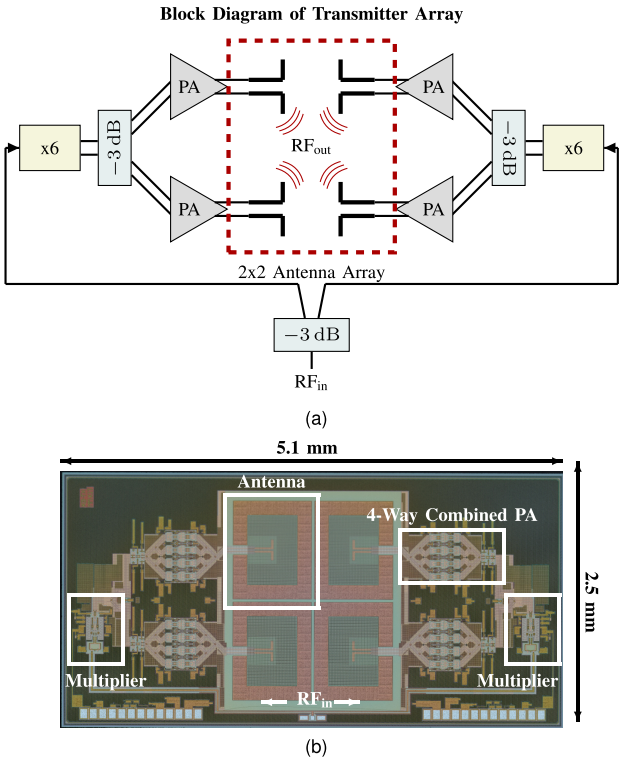


Fig. 1. (a) Block diagram and (b) chip micrograph of the transmitter array.

antenna arrays, however, benefit from precise lithographic definition, ensuring highly consistent physical dimensions and electrical performance. The intrinsic uniformity of the design supports reliable operation of the array and enhances system-level performance when implemented on a single chip [12], [13], [14], [15]. In array antenna design, the spacing between array elements is one of the critical parameters to determine. An interelement distance of $0.5 \cdot \lambda$ is optimal, as it suppresses side lobes while maximizing radiation in the main-beam direction.

At J-band, transmission line lengths approach a significant fraction of the wavelength, leading to high insertion loss and increased sensitivity to impedance transformations. Moreover, compensating for these losses is challenging due to the limited transistor gain available at J-band [16], [17]. To address these limitations, each branch drives a $\times 6$ frequency multiplier. Each component in the transmitter array is matched to 100 Ω for differential input/output ports and 50 Ω for single-ended input/output ports to facilitate integration between the circuit blocks.

The transmitter array chip is fabricated in IHP's 130-nm SiGe BiCMOS technology (SG13G3). This technology features heterojunction bipolar transistors (HBTs) with f_t/f_{max} = 470/650 GHz. The collector–emitter (BV_{CEO}) and collector–base (BV_{CBO}) breakdown voltages are specified with BV_{CEO} = 1.5 V and BV_{CBO} = 3.8 V, respectively. The back-end of line (BEOL) stack integrates eight metal layers, comprising four thin copper layers (M1–M4), two 3.2-μm-thick copper layers (ThCu1, ThCu2), one thin aluminum layer (ThinAl), and a 2.8-μm-thick top aluminum layer (ThAl) as shown in Fig. 2(a).

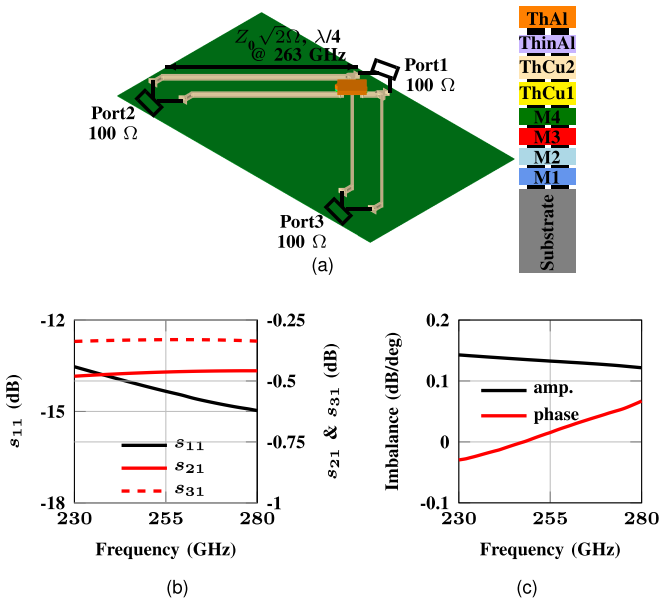


Fig. 2. J-band power divider. (a) Layout image and stack-up of SG13G3. (b) Simulated s_{11} and s_{21}. (c) Amplitude and phase imbalances between differential outputs.

A single-ended 39–46-GHz input signal is applied through a GSG RF pad. A single-ended two-way transmission-line power divider is designed to distribute the input signal from the RF pad to the ×6 multipliers, aiming for low insertion loss. The power divider layout is optimized for compact integration within the transmitter array. The power divider achieves an insertion loss of 1.15 dB at 43 GHz. The output amplitude and phase imbalance achieve 0.01 dB and 0.05°.

The ×6 frequency multiplier consists of a bootstrapped Gilbert cell (BGC) followed by a driver amplifier and upconverts the signal to the 234–276-GHz range while simultaneously converting the single-ended input into a differential output. Within the frequency range of interest, all harmonics other than the sixth harmonic are suppressed by more than 20 dBc, ensuring high spectral purity of the output signal. A detailed discussion can be found in [18].

A differential J-band two-way power divider is designed to split the output signal of the ×6 frequency multiplier to the PAs. The power divider is implemented using ThCu2 and M4 as the RF line and ground plane, respectively, and incorporates a quarter-wavelength ($\lambda/4$) section at 263 GHz with a characteristic impedance of $Z_0\sqrt{2}$. The layout is optimized for compact integration with the multipliers and PAs. The layout of the power divider and stack-up of SG13G3 are shown in Fig. 2(a), while the simulated reflection coefficients and the amplitude and phase imbalances between the differential output ports are shown in Fig. 2(b) and (c). The power divider exhibits an insertion loss of approximately 0.4 dB across J-band, with amplitude and phase imbalances within 0.12–0.14 dB and 0°–0.08°, respectively.

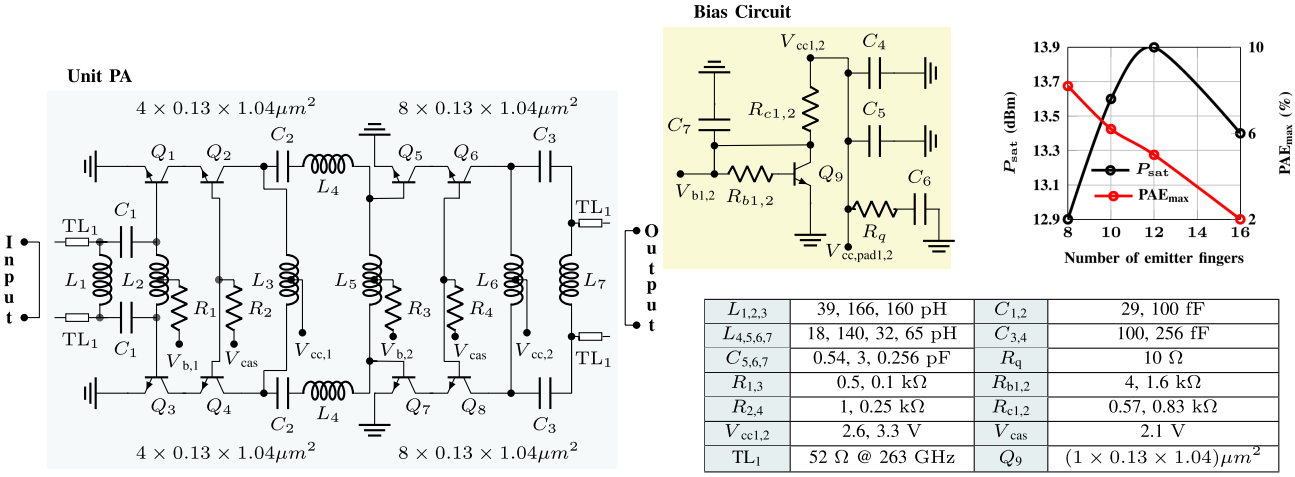
The signal from the power divider is fed into the J-band four-way combined PAs. Each PA consists of a driver amplifier, a four-way power divider, four unit PAs, and a four-way power combiner [3]. The schematic of the two-stage cascode unit PA and its bias circuitry are shown in Fig. 3. As the operating frequency approaches f_{max}, the limited transistor power gain becomes the main bottleneck for achieving higher output power. To maximize the maximum available gain (MAG), the PA is biased in class-A operation at 2.94 mA per emitter finger. Although high output power is desirable for maximizing EIRP, the emitter finger configuration is selected based on a tradeoff among output power, efficiency, and thermal reliability. The saturated output power (P_{sat}) and maximum power-added efficiency (PAE_{max}) versus the number of emitter fingers, each having a size of $0.13 \times 1.04\ \mu m^2$, are plotted in Fig. 3. Increasing the number of emitter fingers from 8 to 12 improves P_{sat} by approximately 1 dB while reducing the PAE by nearly a factor of two; further increases in the number of emitter fingers degrade P_{sat} due to layout parasitics. The number of emitter fingers is selected as 8 to compromise between output power, efficiency, and thermal reliability. A diode-connected bias circuit is implemented at the base of each common-emitter (CE) device to enhance thermal stability. This scheme suppresses thermal runaway and maintains stable PAE performance with increasing temperature.

Fig. 4 illustrates the conceptual layout for a scalable $2 \times N$ chip array implementation. The number of rows N can be scaled according to the required output power. Since the chips in the right column are horizontally flipped, the RF signal is distributed with a 180° phase shift relative to the left column to enable constructive power combining. To facilitate chip placement, both the DC supply and RF input signals are provided from only one side of each chip. The DC supply and RF input lines are routed with identical electrical lengths to each PA to ensure uniform biasing and consistent RF signal distribution across the array. In addition, a bypass network is implemented to suppress potential low-frequency instabilities.

III. On-Chip Integrated Array Antenna Design

In the BEOL stack of the SiGe process employed in this work, the small separation between the ground and top metal layers, combined with the high-loss silicon substrate (50 Ω·cm), constrains antenna efficiency. Furthermore, required filler densities degrade performance by inducing eddy currents and altering the effective substrate permittivity. These limitations necessitate novel design strategies to enhance radiation efficiency [19].

Several techniques have been investigated to address these issues. Backside etching has been used to mitigate substrate losses [9], while the deposition of a dielectric superstrate has been proposed to improve efficiency [20]. Although effective, such methods often require postmicromachining steps or impose strict packaging constraints. In this work, an alternative approach is adopted in which the substrate itself with a backside reflector is exploited as part of the antenna structure, following the methodology in [21]. This strategy offers distinct advantages: the high permittivity of silicon (ϵ_r = 11.9) reduces the wavelength within the substrate by a factor of 3.45, enabling a compact design; radiation efficiency is enhanced by incorporating a reflector at the backside.



$L_{1,2,3}$	39, 166, 160 pH	$C_{1,2}$	29, 100 fF
$L_{4,5,6,7}$	18, 140, 32, 65 pH	$C_{3,4}$	100, 256 fF
$C_{5,6,7}$	0.54, 3, 0.256 pF	R_q	10 Ω
$R_{1,3}$	0.5, 0.1 kΩ	$R_{b1,2}$	4, 1.6 kΩ
$R_{2,4}$	1, 0.25 kΩ	$R_{c1,2}$	0.57, 0.83 kΩ
$V_{cc1,2}$	2.6, 3.3 V	V_{cas}	2.1 V
TL_1	52 Ω @ 263 GHz	Q_9	$(1 \times 0.13 \times 1.04)\mu m^2$

Fig. 3. Schematic of the PA unit, the bias circuit, and simulated P_{sat} and PAE_{max} versus number of emitter fingers. From [3].

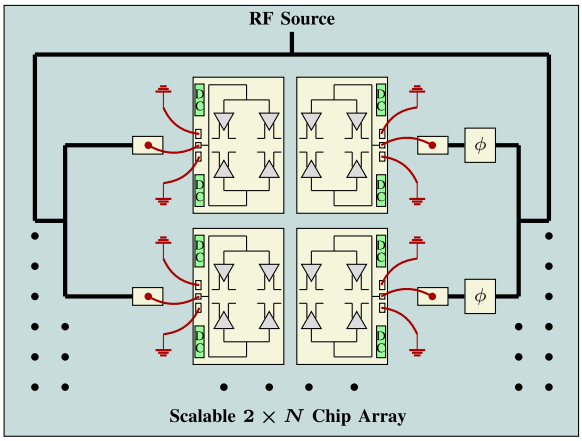


Fig. 4. Conceptual layout for a 2 × N chip array.

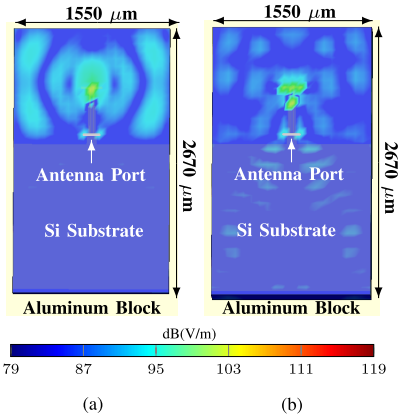


Fig. 5. Simulated E-field of dipole antenna at 263 GHz with (a) 80 and (b) 330 μm of silicon substrate thickness.

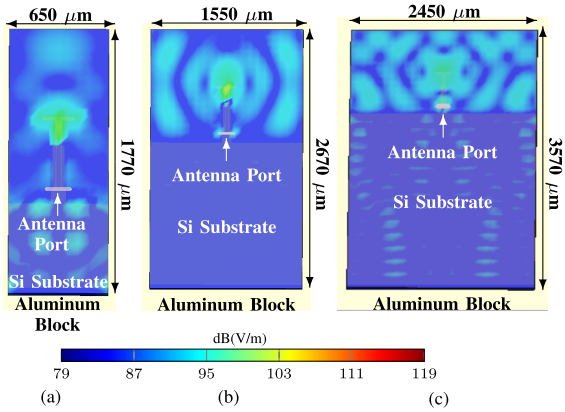


Fig. 6. Simulated E-field of dipole antenna at 263 GHz with 80 μm of silicon substrate thickness and (a) x = 650 μm, y = 1770 μm, (b) x = 1550 μm, y = 2670 μm, and (c) x = 2450 μm, y = 3570 μm of silicon substrate lateral dimensions.

Setting the antenna–reflector spacing to $\lambda/4$ introduces an additional 180° phase shift in the reflected wave, which, combined with the reflection-induced 180° phase shift, results in constructive interference with the direct radiation, thereby enhancing radiation efficiency and gain. The final wafer thickness is thinned to 100 μm using an available foundry option. The resulting silicon substrate thickness of 80 μm corresponds to approximately $\lambda/4$ at 263 GHz (λ = 330 μm in silicon).

The high permittivity of silicon leads to undesired wave propagation within the substrate with increasing frequency of operation [22], [23]. A grounded dielectric substrate supports both transverse magnetic (TM) and transverse electric (TE) modes, where the TM_0 mode has no cutoff frequency, and the TE_1 mode exhibits a cutoff frequency given by

$$f_{c,TE1} = \frac{c_0}{4z\sqrt{\epsilon_r - 1}} \quad (1)$$

with c_0 denoting the speed of light in vacuum, z the substrate thickness, and ϵ_r the relative permittivity of silicon [24]. These modes result in two radiation contributions: direct radiation from the antenna and parasitic radiation from the substrate edges, which may distort the radiation pattern and affect the antenna gain depending on the substrate dimensions due to the superposition of both components [25]. Fig. 5 shows the simulated electric-field (E-field) distributions of the dipole antenna, whose dimensions are selected to achieve optimal radiation characteristics at 263 GHz, as detailed in Fig. 7. The shielding ring is not included in these simulations. The

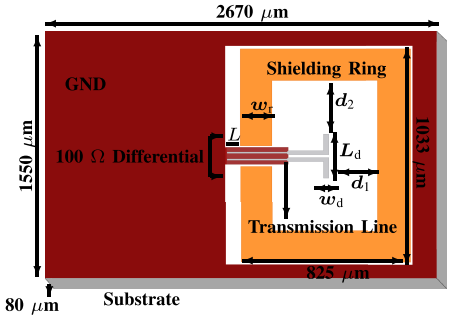


Fig. 7. Layout of unit antenna.

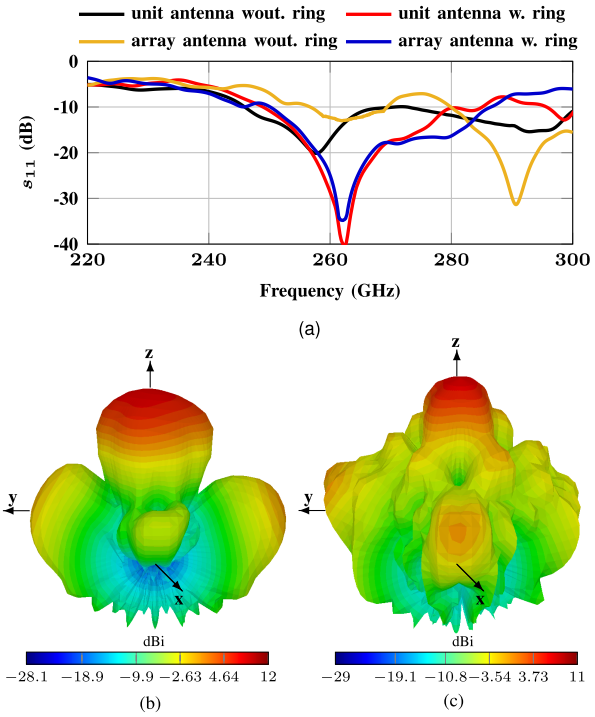


Fig. 8. (a) s_{11} of unit antenna without shielding ring and array antenna with and without shielding ring, 3-D radiation pattern cuts (b) at 263 GHz of array antenna with shielding ring and (c) at 290 GHz of array antenna without shielding ring.

simulations are carried out for fixed substrate lateral dimensions (x = 1550 μm and y = 2670 μm) and substrate thicknesses of 80 and 330 μm. A substrate thickness of 80 μm increases the TE_1 cutoff frequency to 284 GHz [see (1)], suppressing parasitic radiation at 263 GHz. Fig. 6 presents the corresponding E-field distributions for a fixed substrate thickness of 80 μm and varying substrate lateral dimensions. The combination x = 1550 μm and y = 2670 μm achieves the strongest suppression of parasitic radiation. Therefore, a substrate with x = 1550 μm, y = 2670 μm, and a thickness of 80 μm is selected, as it minimizes parasitic radiation, maximizes radiation performance, including gain, and enables integration of the remaining circuit blocks within the available substrate area.

A dipole antenna topology is adopted to achieve a broader impedance bandwidth and to facilitate integration with the PA feedlines. Fig. 7 illustrates the structure of the on-chip

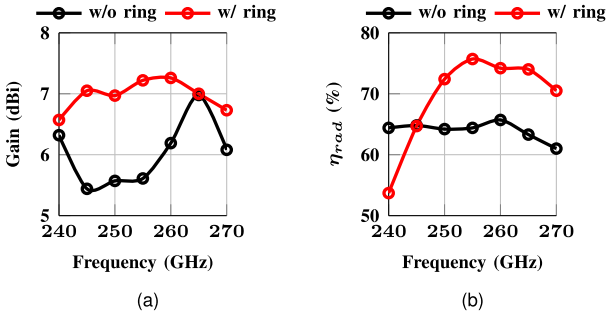


Fig. 9. (a) Simulated unit antenna gain with and without shielding ring and (b) unit antenna radiation efficiency with and without shielding ring versus frequency.

dipole-type antenna. The antenna is realized on the ThCu2 metal layer, which also accommodates the transmission lines connecting the PA to the antenna. A shielding ring is implemented around the antenna, spanning from the bottom to the top metal layers through vertical vias. The antenna is designed to achieve optimal radiation characteristics at 263 GHz, with a dipole length of L_d = 213 μm and width w_d = 25 μm.

Fig. 8(a) compares the simulated s_{11} of a single antenna with and without a shielding ring and a 2 × 2 array with and without a shielding ring. For the array configurations, only one port is shown, as the remaining ports exhibit similar responses. In the array implementation, the absence of a shielding ring leads to a shift of the resonant frequency toward higher frequencies due to increased interelement coupling. To mitigate this effect, a shielding ring is placed around each unit antenna, ensuring that the resonant frequency of the unit element is maintained at 263 GHz. As a result, interelement coupling is suppressed in the array configuration, and the desired resonance at 263 GHz is preserved. Fig. 8(b) shows the radiation patterns of the 2 × 2 array with and without the shielding ring at 263 and 290 GHz, respectively. For the case without the shielding ring, the shifted resonance at 290 GHz is considered. The shielding ring suppresses parasitic surface waves, thereby reducing pattern distortion and improving the main-beam directivity [27]. Placement of the shielding ring is critical: it introduces additional coupling to the antenna and extends the differential 100 Ω transmission line from the PA. Full-wave EM simulations determine the parameters needed to achieve a 100 Ω input impedance at 263 GHz: d_1 = 250 μm, d_2 = 260 μm, transmission line length (L) = 65 μm, and w_r = 150 μm. The design achieves a peak gain of 7 dBi and a maximum radiation efficiency of 74% at 263 GHz. The simulated half-power beamwidths are approximately 37° and 25° in both ϕ = 0° and ϕ = 90° planes, respectively. Fig. 9(a) and (b) presents a comparison of the unit antenna performance with and without the shielding ring in terms of gain and radiation efficiency as a function of frequency.

For the array implementation, achieving strong main-beam radiation is aimed. Owing to the shielding ring surrounding each antenna element, the minimum achievable interelement spacing in Fig. 1(a) is limited to $0.93 \cdot \lambda$ between adjacent antenna rows and $0.74 \cdot \lambda$ between adjacent antenna columns. The increased interelement spacing of $0.93 \cdot \lambda$ and $0.74 \cdot \lambda$

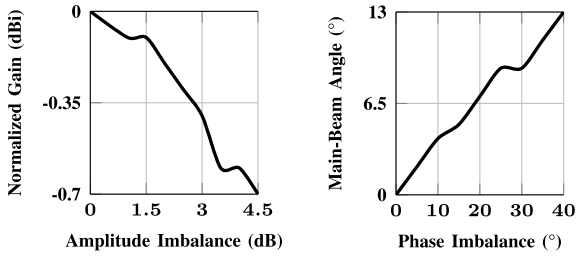


Fig. 10. (a) Simulated normalized antenna array gain versus amplitude imbalance and (b) antenna array main-beam angle versus phase imbalance introduced between adjacent antenna columns.

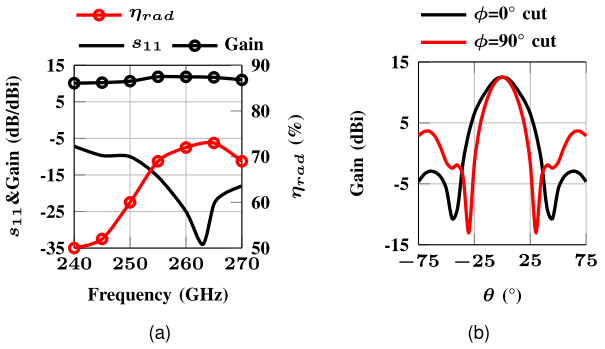


Fig. 11. (a) Simulated s_{11}, gain and radiation efficiency versus frequency and (b) 2-D radiation pattern cuts at 263 GHz of 2×2 antenna array.

reduces the sidelobe suppression level from approximately 20–10 dB compared to the ideal $0.5 \cdot \lambda$ spacing condition; however, this degradation is not critical for the intended system application, since only the main beam is directed toward the gyro-TWT system. In addition, only a slight degradation in radiation efficiency is observed due to the increased spacing between the antenna elements. Due to the symmetric layout and identical routing of the array branches, channel-to-channel amplitude and phase mismatches are expected to remain limited. Amplitude imbalance mainly reduces the coherent combining efficiency and consequently lowers the achievable antenna array gain, whereas phase imbalance primarily causes a slight shift in the main-beam angle. Fig. 10(a) and (b) illustrates these effects, where amplitude and phase imbalances are introduced between adjacent antenna columns.

The simulated s_{11}, gain and radiation efficiency of the 2×2 array are presented in Fig. 11(a). The design achieves a peak gain of 12 dBi and a maximum radiation efficiency of 72% at 263 GHz. The corresponding 2-D simulated radiation patterns at 263 GHz in the $\phi = 0°$ and $\phi = 90°$ planes are shown in Fig. 11(b). The simulated half-power beamwidths are approximately 20° in both the $\phi = 0°$ and $\phi = 90°$ planes.

IV. Board Design and Package

Fig. 12 shows the complete board layout and its layer stack. The board integrates a 1.85 mm RF connector, DC connectors, and surface-mount devices (SMDs). A grounded coplanar waveguide (GCPW) routes the RF signal from the connector to the chip. Parallel grounding stubs compensate for

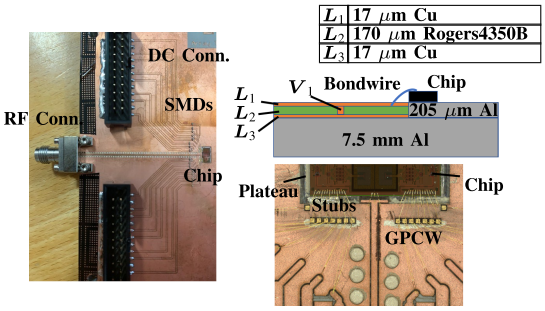


Fig. 12. Board and its stack cross section.

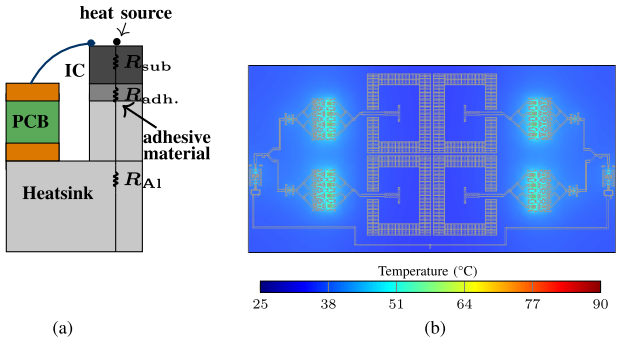


Fig. 13. (a) Basic thermal model of packaging and (b) on-chip temperature distribution after electrothermal simulation.

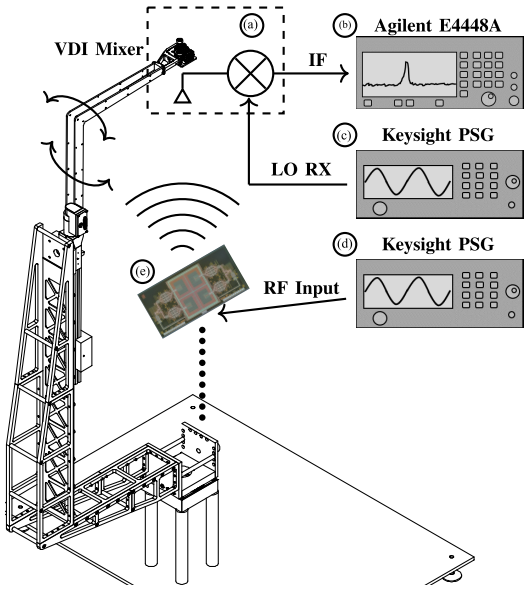


Fig. 14. Block diagram of measurement setup. (a) Receiver. (b) Spectrum analyzer. (c) LO signal source for subharmonic down-conversion mixer. (d) RF signal generator. (e) DUT. From [26].

the inductance of the RF wirebond, improving the board-to-chip transition. The board includes a cavity beneath the chip, which is mounted on an aluminum plateau of 205 μm height within a 7.5-mm-thick aluminum block as shown in Fig. 12. The chip is centered on the plateau with 100 μm clearance to each edge. The aluminum block functions both as a heat sink and as a reflector for the antenna.

With a total DC power consumption of 4 W, efficient heat dissipation is required to prevent performance degradation.

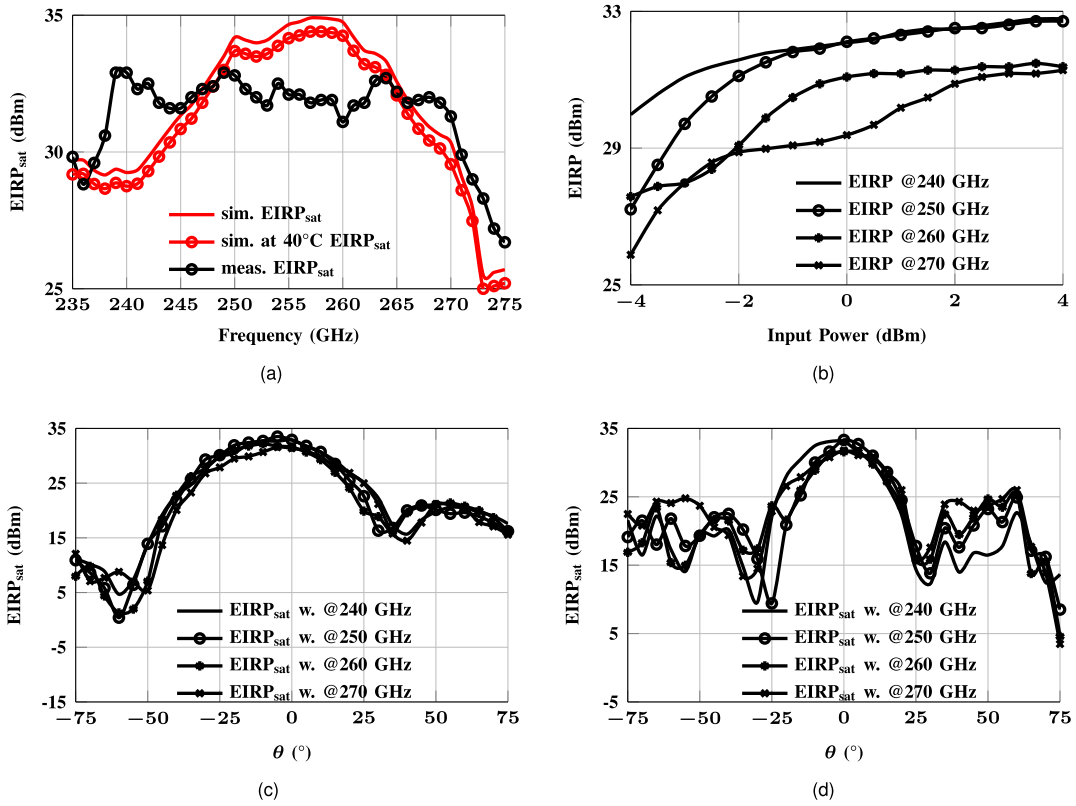


Fig. 15. (a) Measured and simulated EIRP$_{sat}$ versus frequency at room temperature and 40 °C. (b) Measured EIRP versus input power. (c) Measured EIRP$_{sat}$ versus θ for $\phi = 0°$ and (d) for $\phi = 90°$ at different frequencies.

The heat-transfer path is modeled using a thermal resistance, R_{th}. Off-chip interfaces, such as the die-adhesive material layer and heatsink, are assumed to provide ideal thermal contact without voids. Under these assumptions, R_{th} can be expressed as

$$R_{\text{th}} = \frac{h}{Ak} \tag{2}$$

where (h), (A), and (k) denote the thickness, interface area, and thermal conductivity of the corresponding material, respectively. Fig. 13(a) shows the thermal model employed in this work. Owing to the high thermal conductivity of silicon (k_{Si}) of 145 (W/mK) [28] and the reduced substrate thickness of 80 μm, the substrate thermal resistance, R_{sub}, is negligible for the chip area of 12.75 mm^2. The die-adhesive material layer must provide both high thermal conductivity and reliable mechanical adhesion. Although an In–Ag alloy was initially considered, its application over a large chip area and adhesion to an aluminum heatsink are challenging. Therefore, Ag-epoxy (EPO-TEK H20S) is adopted as the die-adhesive material. Assuming a thickness of 15 μm and a thermal conductivity of 3.3 (W/mK) [29], the corresponding thermal resistance, $R_{\text{adh.}}$, is estimated to be 0.35 K/W. The thermal resistance of the aluminum heatsink is neglected due to its high thermal conductivity and large volume. The thermal resistance through the bottom side of the chip is estimated as 0.45 K/W, while the top side is modeled by a thermal resistance of 1e6 K/W to account for negligible heat dissipation. These values are incorporated into the electrothermal simulation in Keysight ADS. Fig. 13(b) shows the simulated temperature distribution under saturated operating conditions. The substrate temperature surrounding the active devices is estimated to be approximately 40 °C and is subsequently used in the circuit-level simulations to evaluate the impact of temperature on transmitter performance, as shown in Fig. 15(a).

V. Measurement

The transmitter array chip is characterized using an antenna measurement system consisting of a two-axis rotating arm that moves the receiver around the device under test (DUT). The block diagram of the measurement setup is shown in Fig. 14. The DUT is driven with an RF input signal generated by a Keysight performance signal generator (PSG) operating in the 39–46 GHz range, while DC bias signals are supplied via a National Instruments (NI) source measure unit (SMU). The measurements are performed in free space. The transmitted signal is received by a Virginia diodes (VDIs) J-band horn antenna, down-converted to an intermediate frequency (IF) of 1 GHz using a VDI J-band subharmonic down-conversion mixer, and measured with an Agilent E4448A spectrum analyzer. To enhance thermal management, an air fan is suspended beneath the aluminum heat sink. Calibration of the receiver chain is performed using a reference transmitter setup consisting of a Keysight performance network analyzer (PNA) driving a VDI J-band transmit module connected to a VDI J-band horn antenna. The transmitter RF signal is swept across 235–275 GHz by fixing the IF signal at 1 GHz. The output of this reference transmitter chain is measured with the same

TABLE I
PERFORMANCE COMPARISON OF STATE-OF-THE-ART SILICON-BASED J-BAND TRANSMITTERS

	[9]	[30]	[11]	[8]	[31]	[32]	**This**
Tech.	130 nm SiGe	130 nm SiGe	130 nm SiGe	65 nm CMOS + 250 nm InP	50 nm GaN HEMT	250 nm InP	**130 nm SiGe**
$f_{\max}$ (GHz)	450	450	500	-	420	700	**650**
Frequency (GHz)	240	240	246	253	224	230	**264**
TX config.	1x4 4 elem./chip	1x1 1 elem./chip	1x2 1 elem./chip	1x4 1 elem./chip	1x32 1 elem./chip	1x32 1 elem./chip	**2 × 2 4 elem./chip**
TX EIRP (dBm)	24	27	12	8.4	n.a.	n.a.	**33**
$P_{\mathrm{tot,rad}}$ (dBm)	12*	3	7.48+	n.a.	31.8-	28.5-	**21***
Antenna type	on-chip LBE dipole	on-chip bow-tie+sil. lens	off-chip bow-tie	on-chip vivaldi	WG°	WG°	**on-chip dipole**
Antenna spacing (λ)	1	-	0.5	3	-	-	**0.7**
DC power (W)	4.38	0.9	0.82	2.64	160[a]	56	**4**
Efficiency[t] (%)	0.36	0.22	0.68	n.a.	0.94	1.26	**3.14**
Chip size (mm^2)	25	2.7	2.3	-	n.a.	1.53[b]	**13.8**

* calculated based on theoretical antenna gain. + estimated from the plot. - received power at the waveguide output.
° waveguide combining. [a] calculated based on reported efficiency. [b] without chip to waveguide transition.
[t] Efficiency = $P_{\mathrm{tot,rad}}$ / DC power.

receiver setup used for the DUT. The absolute output power of the VDI WR3.4 transmit module is determined separately with an Erickson PM4 calorimetric power meter, while the gain of the horn antenna is obtained from its datasheet. EIRP of the reference transmitter chain is calculated as the sum of the transmit module output power and the horn antenna gain. The EIRP of the DUT is then obtained by adding the measured difference between the DUT and the reference transmitter chain to the EIRP of the reference transmitter chain. This calibration procedure also de-embeds the frequency response of all cables, antennas, free path loss, and active components in the measurement path.

During the measurement, a sinusoidal RF input signal generated by a signal generator in the 39–46 GHz range with an output power of 15 dBm is applied. After accounting for the losses in the input network, including 4 dB cable loss, 1-dB RF connector loss, 4-dB RF routing loss on the PCB, and 2-dB wire-bond loss, approximately 4 dBm is delivered to the integrated circuit (IC) to saturate the DUT. Fig. 15(a) compares the measured EIRP with simulated results at room temperature and 40 °C over the 235–275-GHz frequency range. The measured and simulated results are in good agreement, confirming the accuracy of the design and modeling approach. Fig. 15(b) presents the measured EIRP of the DUT at different frequencies as a function of the RF input power after embedding the input network losses. To characterize the on-chip antenna array, the rotating arm with receiver chain is swept around the DUT in both $\phi = 0°$ and $\phi = 90°$ planes over a range of $-75°$ to $+75°$. The resulting radiation patterns are shown in Fig. 15(c) and (d) at different frequencies. The observed 4° main-beam tilt at $\phi = 0°$ is consistent with the effect of interchannel phase mismatch predicted in Fig. 10(b). The half-power beamwidths are within 15°–20° range in the $\phi = 0°$ and $\phi = 90°$ planes across J-band frequencies.

VI. CONCLUSION

This work presents a scalable, single-chip 2×2 transmitter array operating in the 240–270-GHz band. An on-chip dipole antenna array with a backside reflector is integrated with the PAs. The silicon substrate is thinned to $\lambda/4$ at 263 GHz, enabling direct and reflected signals to add constructively, thereby improving the radiation efficiency and gain of the antenna while suppressing undesired substrate wave propagation. To minimize interelement coupling and further reduce substrate waves, a shielding ring is implemented around each unit antenna. The PA design targets maximized output power with thermally manageable efficiency. To overcome high insertion loss and impedance transformation challenges at J-band frequencies, a $\times 6$ frequency multiplier drives each PA pair. The chip is mounted on an aluminum heatsink using Ag-epoxy conductive adhesive and actively cooled by an air fan to enhance heat dissipation. Overall, these design choices yield a high-performance 2×2 transmitter array.

Table I compares the proposed transmitter with state-of-the-art J-band transmitters. The proposed 2×2 array achieves an EIRP of 33 dBm, corresponding to an estimated $P_{\text{tot,rad}}$ of 21 dBm after accounting for the theoretical antenna gain while consuming 4 W of DC power. In comparison, [9], [11] report EIRP values of 24 and 12 dBm with DC power consumptions of 4.38 and 0.82 W, respectively. In addition, [30] achieves an EIRP of 27 dBm with 0.9 W of DC power consumption through the use of an external silicon lens. To the best of the authors' knowledge, the proposed work demonstrates the highest reported EIRP among silicon-based J-band transmitters to date. Although the works in [31] and [32], implemented in compound semiconductor technologies (GaN and InP), report measured output powers of 31.8 and 28.5 dBm, respectively, these results rely on the combination of multiple chips using a waveguide power combiner. Consequently, their overall efficiency is limited by interface losses between the chips and the waveguide, and scalability is inherently limited.

These results demonstrate that the proposed scalable, single-chip 2×2 transmitter array is a promising RF source for applications such as DNP-NMR systems.

ACKNOWLEDGMENT

The authors acknowledge the support of their colleagues Andreas Lipp, Thorsten Fux, and Andreas Gallego in the design of the board, heatsink, and SMD components assembly, as well as chip bonding. They would like to thank the German Research Foundation (DFG) for its funding within the Collaborative Research Center "SFB 1527 High Performance Compact Magnetic Resonance (HyPERiON)."

REFERENCES

[1] M. Blank, P. Borchard, S. Cauffman, K. Felch, M. Rosay, and L. Tometich, "High-frequency CW gyrotrons for NMR/DNP applications," in *Proc. IVEC*, Monterey, CA, USA, Apr. 2012, pp. 327–328.

[2] K. R. Thurber, W.-M. Yau, and R. Tycko, "Low-temperature dynamic nuclear polarization at 9.4 t with a 30 mW microwave source," *J. Magn. Reson.*, vol. 204, no. 2, pp. 303–313, Jun. 2010.

[3] K. Balaban, I. K. Aksoyak, and A. Ç. Ulusoy, "A 16.7-dBm 245-to-295-GHz power amplifier with a four-way power combiner in 0.13-μm SiGe," *IEEE Microw. Wireless Technol. Lett.*, vol. 35, no. 9, pp. 1348–1351, Sep. 2025.

[4] E. Mohamed, G. Fischer, T. Mausolf, H. Ruecker, A. Malignaggi, and G. Kahmen, "220–320-GHz J-band 4-way power amplifier in advanced 130-nm BiCMOS technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 32, no. 11, pp. 1335–1338, Nov. 2022.

[5] J. Yu et al., "A 211-to-263-GHz dual-LC-tank-based broadband power amplifier with 14.7-dBm PSAT and 16.4-dB peak gain in 130-nm SiGe BiCMOS," *IEEE J. Solid-State Circuits*, vol. 58, no. 2, pp. 332–344, Feb. 2023.

[6] M. H. Eissa, A. Malignaggi, and D. Kissinger, "A 13.5-dBm 200–255-GHz 4-way power amplifier and frequency source in 130-nm BiCMOS," *IEEE Solid-State Circuits Lett.*, vol. 2, no. 11, pp. 268–271, Nov. 2019.

[7] M. P. DeLisio and R. A. York, "Quasi-optical and spatial power combining," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 3, pp. 929–936, Mar. 2002.

[8] I. Abdo et al., "300-GHz-band four-element CMOS-InP hybrid phased-array transmitter with 36circ steering range," *IEEE Microw. Wireless Technol. Lett.*, vol. 33, no. 6, pp. 887–890, Jun. 2023.

[9] M. H. Eissa et al., "A fully integrated modular 2×4 220–260 GHz beamforming transmitter and receiver with 50 Gbps wireless transmission in SiGe: C BiCMOS," *IEEE Trans. THz Sci. Technol.*, vol. 15, no. 5, pp. 805–820, Sep. 2025.

[10] H. Jalili and O. Momeni, "A 0.34-THz wideband wide-angle 2-D steering phased array in 0.13-μM SiGe BiCMOS," *IEEE J. Solid-State Circuits*, vol. 54, no. 9, pp. 2449–2461, Sep. 2019.

[11] J. Hebeler, L. Steinweg, F. Ellinger, and T. Zwick, "Wideband BPSK transmitter phased array operating at 246 GHz with ±30° steering range," *IEEE Access*, vol. 12, pp. 51130–51137, 2024.

[12] W. Shin, B.-H. Ku, O. Inac, Y.-C. Ou, and G. M. Rebeiz, "A 108–114 GHz 4×4 wafer-scale phased array transmitter with high-efficiency on-chip antennas," *IEEE J. Solid-State Circuits*, vol. 48, no. 9, pp. 2041–2055, Sep. 2013.

[13] Y. Yang, O. D. Gurbuz, and G. M. Rebeiz, "An eight-element 370–410-GHz phased-array transmitter in 45-nm CMOS SOI with peak EIRP of 8–8.5 dBm," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 12, pp. 4241–4249, Dec. 2016.

[14] A. Karakuzulu, W. A. Ahmad, D. Kissinger, and A. Malignaggi, "A four-channel bidirectional D-band phased-array transceiver for 200 Gb/s 6G wireless communications in a 130-nm BiCMOS technology," *IEEE J. Solid-State Circuits*, vol. 58, no. 5, pp. 1310–1322, May 2023.

[15] B. Yu et al., "A 200-GHz phased-array wireless communication system using HTCC system-in-package technology," *IEEE Trans. THz Sci. Technol.*, vol. 15, no. 1, pp. 45–60, Jan. 2025.

[16] R. Hasan, M. H. Eissa, W. A. Ahmad, H. J. Ng, and D. Kissinger, "Wideband and efficient 256-GHz subharmonic- based FMCW radar transceiver in 130-nm SiGe BiCMOS technology," *IEEE Trans. Microw. Theory Techn.*, vol. 71, no. 1, pp. 59–70, Jan. 2023.

[17] C. Mangiavillano, A. Kaineder, T. Wagner, and A. Stelzer, "A 240-GHz 4-TX 4-RX 2-D-MIMO FMCW radar transceiver in 130-nm SiGe BiCMOS," *IEEE Microw. Wireless Technol. Lett.*, vol. 33, no. 8, pp. 1239–1242, Aug. 2023.

[18] M. Möck, K. Balaban, and A. Ç. Ulusoy, "A compact 238–278-GHz frequency sextupler based on a single bootstrapped Gilbert cell," *IEEE Trans. Microw. Theory Techn.*, vol. 73, no. 7, pp. 3836–3846, Jul. 2025.

[19] S. Yuan, "SiGe BiCMOS circuits and system demonstrators for high range resolution mm-wave radars," *Ph.D. dissertation, Fac. Eng. Comput. Sci., Universität Ulm*, Ulm, Germany, 2018.

[20] A. Haag, T. Li, K. Disch, A. Ç. Ulusoy, and T. Zwick, "Efficient D-band on-chip antennas in silicon germanium technologies," in *Proc. 54th Eur. Microw. Conf. (EuMC)*, Paris, France, Sep. 2024, pp. 888–891.

[21] S. Yuan, A. Trasser, and H. Schumacher, "56 GHz bandwidth FMCW radar sensor with on-chip antennas in SiGe BiCMOS," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Tampa, FL, USA, Jun. 2014, pp. 1–4.

[22] D. M. Pozar, "Microstrip antennas," in *Proc. IEEE*, 1992, vol. 80, no. 1, pp. 79–91.

[23] C. A. Balanis, *Antenna Theory: Analysis and Design*. Hoboken, NJ, USA: Wiley, 2005.

[24] D. M. Pozar, *Microwave Engineering*. Hoboken, NJ, USA: Wiley, 2011.

[25] V. Lammert, M. Leyrer, M. Hamouda, R. Weigel, and V. Issakov, "Dual-mode substrate wave cancellation in a 120 GHz 2×2 on-chip dipole array," *IEEE Trans. Antennas Propag.*, vol. 70, no. 8, pp. 6683–6691, Aug. 2022.

[26] J. Hebeler, L. Steinweg, F. Ellinger, and T. Zwick, "Performance evaluation of ultra-wideband 246-GHz BPSK transmitters on an organic substrate with external chip and substrate antenna," *IEEE Trans. Microw. Theory Techn.*, vol. 72, no. 10, pp. 6153–6163, Oct. 2024.

[27] M. Stocchi et al., "Gain enhancement of BiCMOS on-chip sub-THz antennas by mean of meta-cells," *Sci. Rep.*, vol. 12, no. 1, p. 3946, Mar. 2022.

[28] I. J. Bahl, *Fundamentals of Rf and Microwave Transistor Amplifiers*. Hoboken, NJ, USA: Wiley, 2009.

[29] Epoxy Technology Inc. (2019). *EPO-TEK H20S Technical Data Sheet*. [Online]. Available: https://www.rikei.co.jp/wp/wp-content/uploads/solution/H20S.pdf

[30] E. Turkmen et al., "A 223–276-GHz cascadable FMCW transceiver in 130-nm SiGe BiCMOS for scalable MIMO radar arrays," *IEEE Trans. Microw. Theory Techn.*, vol. 71, no. 12, pp. 5393–5412, Dec. 2023.

[31] W. Wang et al., "Design of G-band watt-level GaN power amplifier with multiband large-signal impedance correction and circuit-package co-design technique," *IEEE J. Solid-State Circuits*, vol. 60, no. 12, pp. 4600–4616, Dec. 2025.

[32] D. Gritters, K. Brown, and E. Ko, "200–260GHz solid state amplifier with 700 mW of output power," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Phoenix, AZ, USA, May 2015, pp. 1–3.

Kaan Balaban (Graduate Student Member, IEEE) received the B.Sc. degree in electrical and electronics engineering from Boğaziçi University, Istanbul, Türkiye, in 2017, and the M.Sc. degree in electronics engineering from Politecnico di Milano, Milan, Italy, in 2019. He is currently pursuing the Ph.D. degree at the Institute of Radio Frequency Engineering and Electronics, Karlsruhe Institute of Technology (KIT), Karlsruhe, Germany.

His research interests include silicon-based transceivers, components for millimeter-wave systems, high-power SiGe amplifiers, and millimeter-wave on-chip antennas.

Max Vöhringer received the B.Eng. degree from Reutlingen University, Reutlingen, Germany, in 2020, and the M.Sc. degree from Karlsruhe Institute of Technology (KIT), Karlsruhe, Germany, in 2022, where he is currently pursuing the Ph.D. degree at the Institute for Pulsed Power and Microwave Technology (IHM) and the Institute of Radio Frequency Engineering and Electronics.

His research interests include high-power vacuum tube amplifiers and components for millimeter-wave applications.

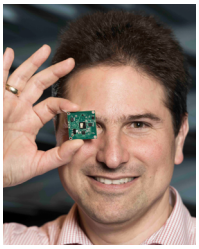
Matthias Möck (Graduate Student Member, IEEE) received the B.Eng. degree in mechatronics/microelectronics from Reutlingen University, Reutlingen, Germany, in 2018, and the M.Sc. degree in electrical engineering from Karlsruhe Institute of Technology (KIT), Karlsruhe, Germany, in 2020, where he is currently pursuing the Ph.D. degree at the Institute of Radio Frequency Engineering and Electronics.

His research interests include silicon-based signal generation circuits for millimeter-wave systems, including voltage-controlled oscillators, frequency multiplication circuits, and phase-locked loops.

Mr. Möck was a recipient of the Best Student Paper Award (second place) from IEEE Radio and Wireless Week in 2024.

Marius Kretschmann received the master's degree in electrical engineering from Karlsruhe Institute of Technology (KIT), Karlsruhe, Germany, in 2019. His Ph.D. thesis at the Institute of Radio Frequency Engineering and Electronics (IHE), KIT, was focusing on packaging, antenna design, and antenna characterization in the submillimeter frequency range.

He is currently working as an RF Engineer at VEGA Grieshaber KG, Karlsruhe.



Thomas Zwick (Fellow, IEEE) received the Dipl.-Ing. and Dr.-Ing. degrees from Karlsruhe Institute of Technology (KIT), Karlsruhe, Germany, in 1994 and 1999, respectively.

In February 2001, he joined IBM as a research staff member at IBM T. J. Watson Research Center, Yorktown Heights, NY, USA. From October 2004 to September 2007, he was with Siemens AG, Lindau, Germany, managing the RF development team for automotive radars. In October 2007, he became a full Professor at KIT, where he is the Director with the Institute of Radio Frequency Engineering and Electronics.

Dr. Zwick has been a member of the Heidelberg Academy of Sciences and Humanities since 2017. In 2019, he became the Editor-in-Chief of IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS. Since 2019, he has been a member of Acatech (German National Academy of Science and Engineering). In 2022, he was awarded an Honorary Doctorate of the Faculty of Electrical Engineering and Informatics at Budapest University of Technology and Economics in Hungary.

John Jelonnek (Senior Member, IEEE) received the Dipl.-Ing. and Dr.-Ing. degrees in electrical engineering from Hamburg University of Technology (TUHH), Hamburg, Germany, in 1991 and 2000, respectively.

At TUHH, he developed rigorous self-consistent analyses for gyrotron oscillators with a particular focus on rigorous time-domain simulation at mismatched conditions and injection locking. From 1997 to 2011, he was working in several different positions in industry. Since 2011, he has been the Director with the Institute for Pulsed Power and Microwave Technology (IHM), Karlsruhe Institute of Technology (KIT), Karlsruhe, Germany. He is a Professor for high-power microwave technologies at KIT. Both research and development of high-power microwave sources, with particular focus on megawatt-class gyrotrons, and applications of microwaves to energy-efficient industrial processes using dielectric heating and microwave plasmas are in focus.

Ahmet Çağrı Ulusoy (Senior Member, IEEE) received the B.Sc. degree in electrical engineering from Istanbul Technical University, Istanbul, Türkiye, in 2006, and the M.Sc. and Ph.D. degrees in electrical engineering from Ulm University, Ulm, Germany, in 2008 and 2012, respectively.

From 2012 to 2015, he was with Georgia Institute of Technology, Atlanta, GA, USA, as a Research Engineer. From 2015 to 2016, he was the Team Leader of the Broadband Mixed-Signal ICs Group, Innovations for High Performance Microelectronics (IHP), Frankfurt (Oder), Germany. From 2016 to 2019, he was an Assistant Professor with Michigan State University, East Lansing, MI, USA. In January 2019, he became a Full Professor with Karlsruhe Institute of Technology (KIT), Karlsruhe, Germany, and the Director of the Institute of Radio Frequency Engineering and Electronics (IHE). He has authored or co-authored more than 150 publications in his research field. His research interests include the broad area of high-frequency integrated circuits and systems.

Dr. Ulusoy is a member of the Microwave Theory and Techniques Society and the Chair of Technical Committee 14. He was a recipient and a co-recipient of several Best Paper Awards. His dissertation received the Südwestmetall Young Scientist Award. He served as the Chair for IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems and IEEE International Conference on Microwaves for Intelligent Mobility. He served as an Associate Editor for IEEE MICROWAVE WIRELESS COMPONENT LETTERS.