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The RFSoC-based electronics readout system for the BULLKID-DM experiment: sub-GeV dark matter detection with MKIDs

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Abstract: We present the readout and data acquisition (DAQ) system for BULLKID-DM, a cryogenic dark-matter experiment employing Kinetic Inductance Detectors (KIDs) to probe below 1 GeV dark matter candidates. The system is built around an AMD RFSoC (ZCU216) platform that synthesizes densely spaced probe tones, performs frequency demultiplexing and amplitude demodulation, and executes real-time triggering and background suppression across up to 16 readout lines with 145 resonators per line in the 700 MHz to 950 MHz band. A fully automated calibration flow integrates vector-network-analyzer (VNA) functionality, resonator-circle acquisition with in-firmware phase rotation for maximum trigger sensitivity, and an energy calibration scheme based on LED illumination via a mezzanine board on the FMC+ connector. We summarize architecture, firmware, preliminary phase-noise studies, and the status of the detector demonstrator. The system is ready for scale-up to the full BULLKID-DM detector at the Laboratori Nazionali del Gran Sasso (LNGS).

Keywords: Data acquisition concepts; Detector control systems (detector and experiment monitoring and slow-control systems, architecture, hardware, algorithms, databases); Trigger algorithms; Cryogenic detectors

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1 Introduction

The BULLKID-DM experiment aims to search for Weakly Interacting Massive Particles (WIMPs) with masses around 1 GeV/c^2 or lower, which are compelling candidates for dark matter. Detecting such low-mass particles presents a significant challenge, as it requires nuclear recoil detectors with both large target mass and energy thresholds around 200 eV, capabilities that surpass those of conventional liquid gas or semiconductor-based technologies. BULLKID-DM addresses these requirements by employing cryogenic microwave kinetic inductance detectors (MKIDs), which combine high multiplexing capability with excellent sensitivity at sub-keV energies [1].

The detector concept is based on an array of silicon absorber dice, each $(5.4 \times 5.4 \times 5)$ mm^3 and weighing roughly 0.3 g, individually coupled to kinetic inductance detectors (KIDs) with an active area of approximately (2×2) mm^2 [1, 2]. Each wafer exhibits 145 frequency-multiplexed KIDs on a single readout line covering a 250 MHz band between 700 MHz and 950 MHz. Sixteen of such lines instrument a tower of 16 wafers diced from 100 mm diameter silicon substrates, corresponding to a total target mass of approximately 800 g. To minimize environmental backgrounds, the detector is

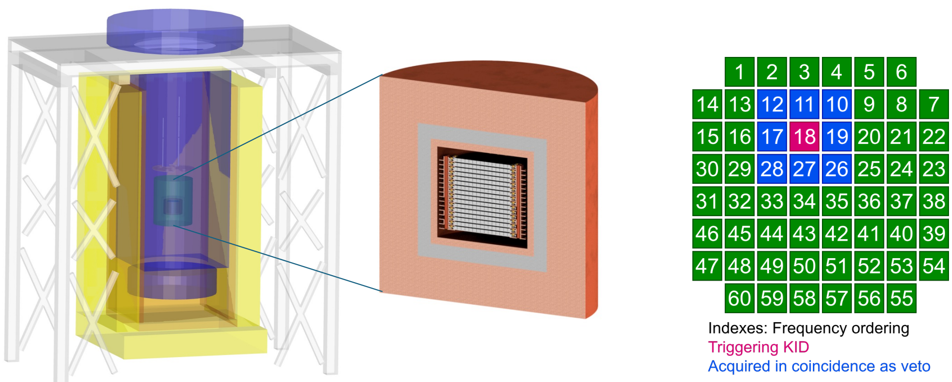

Figure 1. Left: preliminary room-temperature external shielding. From outside to inside: lead (yellow), copper (light brown), and polyethylene (blue). Middle: cryogenic payload composed of outer copper shield, middle B_4C, inner copper, and the detector stack. For integration of the active veto system, portions of the copper shielding will be removed. Right: frequency map of a single 3-inch wafer illustrating the topological trigger concept, with KID 18 shown as an example [5]. Reproduced with permission from [5].

enclosed within a multi-layer shield composed of high-purity copper, lead, polyethylene, and borated materials, and will be operated in the low-radiation environment of the LNGS underground laboratory. In addition to passive shielding, the collaboration is also investigating a cryogenic active veto system based on scintillating crystals read out with phonon-mediated KIDs [3]. This approach further suppresses backgrounds from ambient gamma rays and neutrons in the 200 eV–2 keV energy region of interest. Furthermore, an active topological trigger is being developed, in which selected KIDs act as primary sensors while adjacent pixels serve as veto channels to suppress coincident background events [4]. The overall detector layout, shielding configuration, and trigger concept are illustrated in figure 1. This contribution focuses on the design and characterization of the room-temperature data acquisition (DAQ) system that interfaces with the cryogenic detector array.

2 Data acquisition electronics system

The room-temperature readout electronics are currently based on the AMD ZCU216 RFSoC evaluation board, which integrates sixteen 14-bit DACs operating at sampling rates up to 5 GS/s and sixteen 14-bit ADCs operating at up to 2.5 GS/s. A custom-designed analog front-end [6] provides differential-to-single-ended conversion through broadband baluns, followed by low-pass filtering, and high-density signal fanout to the cryogenic interface. Probe tones are generated within the firmware by precomputing tone samples and initializing the transmit-side memory, enabling precise placement of excitation frequencies within the 250 MHz band of interest.

System operation and monitoring are performed over Ethernet via a gRPC-based control interface, with Jupyter notebooks serving as the user-facing graphical environment for configuration, calibration, and data acquisition.

The firmware components within the FPGA handle all real-time digital signal processing tasks, including tone generation, frequency demultiplexing, demodulation, event triggering, and automatic resonator search using a built-in vector network analyzer. As part of the calibration strategy, the detector stack is illuminated with an external LED signal. A dedicated FMC+ mezzanine board is currently being developed to interface with the LANTERN LED illumination system [7], providing control and synchronization trigger signals. Alternative calibration strategies are also under investigation [8], including methods based on movable radioactive sources to provide localized and reproducible excitation of the detector array.

In the BULLKID system, the chosen method for frequency demultiplexing is the polyphase channelization [9], which is performed as the first stage of the digital signal processing chain. This stage separates the modulated excitation tones to ensure optimal noise performance and minimize cross-talk while maintaining low resource usage within the FPGA. It does so by dividing the wideband input spectrum into multiple equidistant sub-bands that can be further processed in a time-division multiplexing (TDM) scheme. For a critically sampled polyphase channelizer, the sampling rate $f_{s,out}$ of each channel (equivalent to its bandwidth) is given by

$$f_{s,out} = \frac{f_{s,in}}{N}, \tag{2.1}$$

where $f_{s,in}$ is the sampling rate of the wideband input signal and N is the number of output channels (chosen as a power of two for algorithm efficiency). In the BULLKID-DM data acquisition system, the complex input signal $f_{s,in}$ has a bandwidth of 250 MHz and is divided into $N = 64$ channels.

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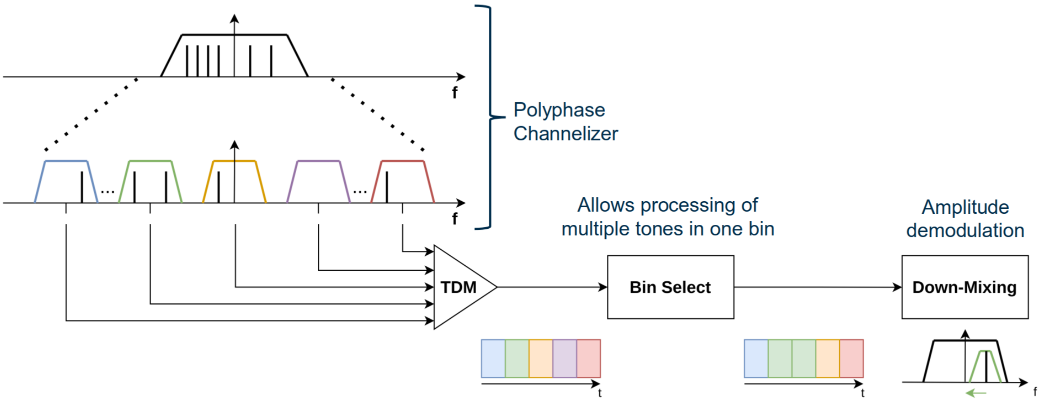

Figure 2. Implementation of frequency demultiplexing. This processing stage is responsible for reconstructing the individual detector signals from the wideband frequency comb.

To eliminate the spectral gaps between adjacent output channels, a second polyphase channelizer is applied to a frequency-shifted copy of the input signal. This shift aligns the output bins of the second channelizer with the stop bands of the first. A subsequent interleaving block combines the two TDM signals into a single data stream with 500 MHz and 128 individual bands.

Since the excitation tones are not uniformly spaced, some channels may contain multiple tones while others remain empty. To address this, a bin-selection module dynamically forwards the relevant channels of the TDM stream. Channels containing multiple tones are buffered and processed sequentially.

Finally, the fine downmixing stage compensates for residual frequency offsets caused by tones not being centered within their respective channels. Each tone is multiplied by its corresponding correction frequency and low-pass filtered, thereby fully downconverting the carrier frequencies and recovering the raw detector signals. The complete architecture of the frequency demultiplexing stage is illustrated in figure 2.

In addition to the downmixing process, both the polyphase channelizer and the fine downmixing stage employ finite impulse response (FIR) filters to suppress unwanted spectral leakage and reduce crosstalk. The polyphase channelizer utilizes a filter with a cutoff frequency of approximately 1.1 MHz and a stopband attenuation of about 90 dB, while the subsequent fine downmixing stage employs a FIR filter with a 100 kHz cutoff and 80 dB stopband attenuation.

3 Prototype detector demonstrator

A partially assembled four-channel analog front-end is currently coupled to a prototype detector demonstrator consisting of three 3-inch wafers, each containing 60 readout channels (see figure 3 (Left)), operated at Sapienza University of Rome. This setup enables continuous firmware development, validation of the automated calibration workflow, and early performance characterization under representative operating conditions. The demonstrator incorporates a fully automated calibration and energy reconstruction framework integrated into the room-temperature readout electronics [6]. During operation, an on-board vector network analyzer (VNA)-like sweep identifies the resonance frequencies of all channels without requiring external instrumentation. The sweep parameters, such as frequency span, step size, integration time, and output power, are tunable at runtime to ensure robust operation

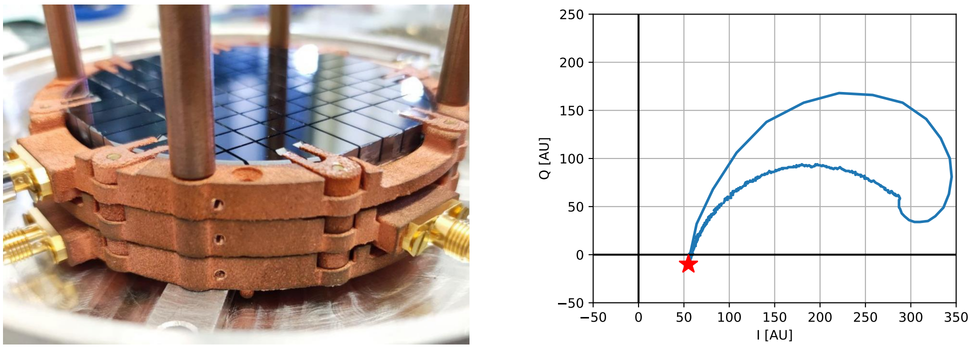

Figure 3. Left: three-wafer detector demonstrator stack, each 3-inch wafer containing 60 KIDs, mounted on a copper holder equipped with SMA connectors for interfacing the feedline of the multiplexer. Reproduced with permission from [5]. Right: representative detector signal acquired and reconstructed by the readout platform. The baseline operating point is marked by a red star. Following energy absorption, the detector signal exhibits a hysteretic trajectory in the IQ plane.

across different detector configurations. Resonance peaks are automatically detected in software, and the resulting frequency list is used to generate the corresponding excitation comb using the direct digital synthesis (DDS) approach mentioned in section 2. On the receive path, after polyphase channelization, each resonator is fine-tuned to baseband by adjusting its local numerically controlled oscillator (NCO) to the measured residual offset. The firmware subsequently acquires resonator circles for all channels by incrementally stepping the mixing frequency, reusing identical settings in the receive chain to avoid reconfiguration overhead. To maximize the signal-to-noise ratio of the trigger, the tangent at resonance circle's operating point is determined, and the phase of the corresponding channel is rotated accordingly. This approach aligns the sensitive quadrature without additional hardware requirements.

Energy calibration is achieved through a synchronized LED illumination system coupled via optical fibers to the detector wafer stack. The LED driver is phase-aligned with the RFSoC timing chain through an FMC+ extension interface, ensuring precise trigger correlation and enabling absolute calibration of pulse amplitudes and energy reconstruction, an event captured by the platform can be seen in figure 3 (Right).

4 System characterization

A key design requirement of the room-temperature readout electronics is that its intrinsic noise must remain below the detector noise level, ensuring that the measurement is not limited by the readout chain. For the BULLKID-DM experiment, a phase noise of less than -100 dBc/Hz in the frequency range from 100 Hz to 10 kHz is targeted. System phase noise was determined by downconverting a single, unmodulated excitation tone through the complete readout path. This tone was either generated internally in loopback mode or provided by external laboratory signal sources. The noise of the resulting DC signal was analyzed by computing its Power Spectral Density (PSD) as shown in figure 4 (Left).

The dominant contribution to the PSD originates from the clock jitter of the high-speed data converters. In the default configuration, the DAC (5 GHz) and the ADC (2.5 GHz) clocks are generated by the CLK104 mezzanine board included with the ZCU216 evaluation board. The clock distribution network on this board, consisting of an LMK04828 and two LMX2594 synthesizers, introduces additional phase noise that degrades the overall signal quality. Significantly improved performance, by

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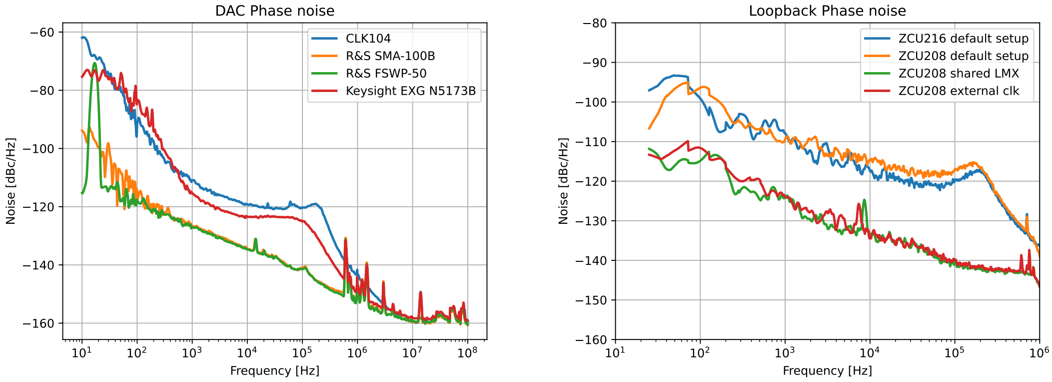

Figure 4. PSD of a single unmodulated excitation tone obtained using different clocking options. Left: phase noise of the DAC measured with the R&S FSWP-50 using various signal synthesizers. The R&S FSWP-50 provides a high-stability signal generator output (hardware option B4). The R&S SMA-100B is equipped with the B711 hardware option for ultra-low phase-noise (PNO). The use of external frequency synthesizers improves the DAC output phase noise by 20 dB within the frequency range of interest (100 Hz-10 kHz). Right: phase noise of the complete system in loopback operation. Employing a common LMX chip both for DAC and ADC yields comparable performance to that achieved with an external reference clock. However, this configuration is only possible when operating both converter types with the same sampling frequency.

more than 10 dB in phase noise, was achieved using high-purity external synthesizers such as the R&S SMA100-B. Using this setup, the targeted system phase noise of -100 dBc/Hz at 100 Hz to 10 kHz is achieved. Comparable results can be obtained when both converters share a single LMX2594 source on the CLK104, which allows common-mode phase noise cancellation in loopback mode. However, this configuration requires identical sampling frequencies for the DAC and ADC, limiting the DAC sampling rate to 2.5 GHz on the ZCU216. This reduction leads to a degraded Spurious-Free Dynamic Range (SFDR) due to insufficient suppression of image frequencies in the second Nyquist zone.

An alternative configuration employs the ZCU208 evaluation board, which supports simultaneous DAC and ADC operation at 5 GHz. Apart from the converter interface, the ZCU208 is fully compatible with the existing firmware and represents a cost-effective migration path with improved performance. Full readout of the 16-wafer detector tower could be achieved with only two ZCU208 evaluation boards.

5 Conclusion

A room-temperature readout system based on the AMD RFSoC evaluation boards (ZCU2016 or ZCU208) and a custom analog front-end has been developed for the BULLKID-DM experiment. The firmware integrates direct digital synthesis, polyphase channelization, and real-time demodulation, together with automated calibration. Characterization measurements in loopback confirm that the readout system meets the targeted noise specifications and is therefore not expected to limit the overall detector sensitivity. Operation of the three-wafer detector demonstrator at Sapienza University has been essential for validating the firmware functionality and accelerating the development of the automated calibration workflow under realistic experimental conditions. Future work will focus on adapting the firmware and signal processing parameters to support the 100 mm diameter wafers foreseen for the final detector configuration, preparing the system for operation at the LNGS underground laboratory, and integrating the topological trigger logic within the FPGA for real-time background suppression.

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