

Power Hardware-in-the-Loop Modeling and Stability Analysis

Zur Erlangung des akademischen Grades eines

DOKTORS DER INGENIEURWISSENSCHAFTEN (Dr.-Ing.)

von der KIT-Fakultät für Elektrotechnik und Informationstechnik des
Karlsruher Instituts für Technologie (KIT)

angenommene

DISSERTATION

von

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geb. in Sary

Tag der mündlichen Prüfung:

Hauptreferent:

Korreferent:

03.07.2026

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Acknowledgment

I would like to sincerely thank Prof. Giovanni De Carne for giving me the opportunity to experience some of the most meaningful years of my life. I am deeply grateful for his trust, his belief in my abilities, and for the chance to learn, grow, and develop, both professionally and personally.

I would like to thank Prof. Noe for his guidance and valuable insights. My sincere thanks also go to Dr. Shahab Karari for his support at the very beginning of my PhD journey and for helping me take my first steps with confidence.

I am grateful to the lab team, Mr. Christian Lange, Mr. Frank Gröner, and Mr. Dieter Riegel, for their technical support and for always being there when it mattered.

I would like to thank my colleagues at the RTS group for creating such a dynamic, supportive, and inspiring environment. It has truly been a privilege to be part of this team.

I am deeply thankful to the families of Zarei, Hamzeh, Daheshvar, Pourghasem, Kholghi, Bernoon, and Azizzadeh for welcoming me so warmly. Throughout these years, I never felt alone, and that meant more than words can express.

This thesis is dedicated to: Zohreh, the love of my life, for her patience, her strength, and for enduring these years with grace, so that we could finally begin our journey together.

Agaah, my brother, my first teacher, supervisor, mentor, and unwavering supporter.

Sarafraz and Ali, my parents, who sacrificed so much so that I could have a better life, even across the distance. Your love will always be a part of me.

Kurzfassung

Power Hardware-in-the-Loop PHIL Testing kombiniert die Flexibilität numerischer Simulationen mit der hohen Genauigkeit von Hardware-Experimenten und ermöglicht die Validierung elektrischer Systeme unter realistischen und kontrollierbaren Laborbedingungen. Ein PHIL-System verbindet ein simuliertes Model-of-Interest MoI, das in einem Digital Real-Time Simulator DRTS ausgeführt wird, mit physischer Hardware, dem Hardware-of-Interest HoI, über Schnittstellenkomponenten und -algorithmen. Obwohl PHIL erhebliche Vorteile hinsichtlich der Reduzierung von Entwicklungszeit, -kosten und der Abhängigkeit von Feldtests bietet, führt das Vorhandensein von Schnittstellenkomponenten zu grundlegenden Herausforderungen in Bezug auf Systemstabilität und -genauigkeit, die in der bestehenden Literatur nicht systematisch oder einheitlich behandelt werden.

Diese Arbeit adressiert diese Lücke durch die Entwicklung einer umfassenden Methodik zur Modellierung, Analyse und Validierung von PHIL-Systemen, mit Beiträgen in vier miteinander verbundenen Bereichen.

Erstens wird der Einfluss wesentlicher Schnittstellenkomponenten, nämlich Zeitverzögerungen, Filterstufen und Leistungsverstärker, auf die PHIL-Stabilität und -Genauigkeit mittels Übertragungsfunktionsanalyse charakterisiert, und konventionelle Schnittstellenalgorithmen (IAs) werden systematisch hinsichtlich ihrer Anwendbarkeit und Einschränkungen verglichen.

Zweitens wird, um dem hybriden Charakter von PHIL-Systemen aus Kontinuierlicher Zeit CT und Diskreter Zeit DT gerecht zu werden, ein neuartiger Mehrfachabtastrate-Diskrete-Zeit MDT Modellierungsansatz vorgeschlagen, um die PHIL-Modellierungsgenauigkeit zu verbessern. Quantitative Genauigkeitsmetriken werden eingeführt und durch Simulations- und experimentelle Studien validiert, wobei Messunsicherheiten berücksichtigt werden.

Drittens wird die Wechselwirkung zwischen PHIL-Schnittstellendynamik und einem aktiven HoI, nämlich einem dreiphasigen netzgekoppelten Umrichter, analysiert, wobei gezeigt wird,

wie die Regelungsdynamik des Umrichters sowohl die Stabilitätsgrenzen als auch die Testgenauigkeit entscheidend beeinflusst. Dies verdeutlicht die Notwendigkeit einer koordinierten Abstimmung zwischen Schnittstellenparametern und Umrichterregelungsdynamik und führt einen Modellierungsrahmen ein, der die Regelungsdynamik des HoI explizit in die PHIL-Kreisanalyse einbezieht.

Viertens wird ein impedanzbasierter Stabilitätsanalyserahmen entwickelt und über die klassische Annahme passiver Lasten hinaus erweitert, um die dynamischen Regler netzgekoppelter Umrichter als aktive HoIs einzubeziehen. Der Rahmen umfasst netzfolgende GFL und netzbildende GFM Umrichter, Auswirkungen der Sensorplatzierung, Zwischenkreisdynamik sowie Rücken-an-Rücken-Umrichterkonfigurationen in Mehrport-PHIL-Aufbauten.

Abschließend werden die theoretischen Erkenntnisse in praktische Leitlinien für die Auslegung und den Betrieb von PHIL-Systemen überführt, die Stabilität, Genauigkeit und Skalierbarkeit adressieren und zur Entwicklung standardisierter Methoden für zukünftige PHIL-Implementierungen beitragen.

Abstract

Power Hardware-in-the-Loop PHIL testing combines the flexibility of numerical simulations with the high fidelity of hardware experiments, enabling the validation of electrical systems under realistic and controllable laboratory conditions. A PHIL system interfaces a simulated Model-of-Interest MoI, running in a Digital Real-Time Simulator DRTS, with physical Hardware-of-Interest HoI via interface components and algorithms. While PHIL offers significant advantages in reducing development time, costs, and reliance on field testing, the presence of interface components introduces fundamental challenges related to system stability and accuracy that are not systematically or uniformly addressed in the existing literature.

This thesis addresses this gap by developing a comprehensive methodology for modeling, analyzing, and validating PHIL systems, with contributions spanning four interconnected areas.

First, the impact of key interface components, time delays, filtering stages, and power amplifiers on PHIL stability and accuracy is characterized through transfer-function-based analysis, and conventional Interface Algorithms (IAs) are systematically compared with respect to their applicability and limitations.

Second, to address the hybrid Continuous-Time CT and Discrete-Time DT nature of PHIL systems, a novel Multi-rate Discrete-Time MDT modeling approach is proposed to improve the PHIL modeling accuracy. Quantitative accuracy metrics are introduced and validated through simulation and experimental studies, accounting for measurement uncertainties.

Third, the interaction between PHIL interface dynamics and an active HoI, namely a three-phase grid-connected converter, is analyzed, demonstrating how converter control dynamics critically influence both stability margins and testing accuracy. This establishes the necessity of coordinated tuning between interface parameters and converter control dynamics, and introduces a modeling framework that explicitly incorporates HoI control dynamics into the PHIL loop analysis.

Fourth, an impedance-based stability analysis framework is developed and extended beyond the classical passive-load assumption to incorporate the dynamic controllers of grid-connected converters as active HoIs. The framework encompasses Grid-Following GFL and Grid-Forming GFM

converters, sensor placement effects, dc-link dynamics, and back-to-back converter configurations in multi-port PHIL setups.

Finally, the theoretical insights are translated into practical guidelines for the design and operation of PHIL systems, addressing stability, accuracy, and scalability, and contributing toward the development of standardized methodologies for future PHIL implementations.

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Acronyms and symbols

Acronyms

A/D	Analog-to-Digital
AFE	active front end
B2B	Back-to-Back Converter
C-ITM	Current-type Ideal Transformer Method
CHIL	Controller Hardware-in-the-Loop
CT	Continuous-Time
D/A	Digital-to-Analog
DER	Distributed Energy Resource
DIM	Damping Impedance Method
DRTS	Digital Real-Time Simulator
DT	Discrete-Time
EG	Emulated Grid
EM	Emulated Model
EMS	Energy Management System
FT	Fourier Transform
GFL	Grid-Following
GFM	Grid-Forming
GTO	Gate Turn-Off Thyristors
HoI	Hardware-of-Interest
IA	Interface Algorithm
IGBT	Insulated Gate Bipolar Transistor
ITM	Ideal Transformer Method
LPF	Low-Pass Filter
LTI	Linear Time-Invariant
MaxDev	Maximum deviation error
MDT	Multi-rate Discrete-Time

MIMO	Multi-Input Multi-Output
MMC	Modular Multi-level Converter
MMSH	Multi-Model, Single-Hardware Architecture
MoI	Model-of-Interest
nRMSE	normalized root-mean-square error
PA	Power Amplifier
PCC	Point of Common Coupling
PCD	Partial Circuit Duplication
PHIL	Power Hardware-in-the-Loop
PLL	Phase-Locked Loop
RHP	Right Half Plane
ROCOF	Rate of Change of Frequency
SDT	Single-rate Discrete-Time
SISO	Single-Input Single-Output
SMMH	Single-Model, Multi-Hardware architecture
SST	Solid-State Transformer
TFA	Time variant First order Approximation
TLM	Transmission Line Method
V-ITM	Voltage-type Ideal Transformer Method
VSC	Voltage-Source Converter
ZOH	Zero-Order-Hold

Variables and Symbols

A	A compact form transfer function
$A(\omega)$	Amplitude of error
$A^\circ(\omega)$	Phase error
AVG	Average error
B	A compact form transfer function
C	A compact form transfer function
C_f	Capacitor of LCL filter
C_{dc}	DC link capacitor
C_{HoI}	Capacitor in the hardware-of-interest section
C_{LCL}	Capacitor of LCL filter
C_{LC}	Capacitor of LC filter
D	Damping ratio of the linear power amplifier, voltage mode

δ_P	Damping ratio of the linear power amplifier, current mode
E	A compact form transfer function
F	A compact form transfer function
f_c	Cut-off frequency of the low-pass filter
G_s	Transfer function of simulated system
$G_{A/D}$	Transfer function of analog-to-digital converter
$G_{D/A}$	Transfer function of digital-to-analog converter
G_{DRTS}	Transfer function of digital real-time simulator
G_{fb}	Feed-back transfer function
G_{fw}	Forward path transfer function
G_{HoI}	Transfer function of hardware-of-interest
G_{LPF}	Transfer function of Low-pass filter
G_{model}	Model transfer function
G_{cl}	Closed-loop transfer function
G_{ol}	Open-loop transfer function
G_{PA_i}	Transfer function of power amplifier in current mode
G_{PA_v}	Transfer function of power amplifier in voltage mode
$G_{PI,V_{dc}}$	Transfer function of the voltage controller
G_{PI_i}	Transfer function of the current controller
G_{PI_v}	Voltage PI controller transfer function
G_{PI}	Transfer function of PI controller
G_{ref}	Reference transfer function
G_{Sens}	Transfer function of sensor
$G_{T_{fb}}$	Transfer function of delays in feedback path
$G_{T_{fw}}$	Transfer function of delays in forward path
G_{ZOH}	Zero-order-hold transfer function
H	Auxiliary transfer function
H_i	Current transfer function
$H_{i_{GFL}^*}$	Current source transfer function
H_v	Voltage transfer function
H_{v^*}	Voltage source transfer function
$H_{V_{Cs}^*}$	Voltage source transfer function
H_{EG}	Emulated grid source transfer function
H_{GFL}	Grid-following source transfer function
H_{i_s}	A compact form transfer function
i	Current at PCC

i_d	d-axis current
i_{dc}	DC current
$\hat{i}$	Small-signal current
$i_p(f_p)$	Current perturbation source
I_s	Current source current
i_s	Simulated output current
I_{GFL}	Current source model of grid-following converter
I_L	DC load current
k	Scaling factor
K_{I_i}	Integral gain of the current controller
K_{I_v}	Integral gain of the voltage PI controller
$K_{I_{dc}}$	Integrator gain of DC voltage controller
K_{P_i}	Proportional gain of the current controller
K_{P_v}	Proportional gain of the voltage PI controller
$K_{P_{dc}}$	Proportional gain of DC voltage controller
$L(f)$	Inductor as a function of frequency
L_{fc}	Converter side inductor of LCL filter
L_{fg}	Grid side inductor of LCL filter
L_g	Grid inductance
L_s	Simulated inductance
L_{HoI}	Inductor in the hardware-of-interest section
L_H	Hardware inductance
L_{LCL_c}	Converter side inductor of LCL filter
L_{LCL_g}	Grid side inductor of LCL filter
L_{LC}	Inductor of LC filter
N	Number of Nyquist encirclements around critical point
ω_0	Natural angular frequency of the linear power amplifier
ω_c	Cut-off frequency of the Low-pass filter
ω_P	Pole angular frequency of the linear power amplifier
ω_Z	Zero angular frequency of the linear power amplifier
P	Number of open-loop right-half-plane poles
$r(f)$	Resistor as a function of frequency
R_f	LCL filter resistance
r_{fc}	Internal resistor of converter side inductor of LCL filter
r_{fg}	Internal resistor of grid side inductor of LCL filter
R_g	Grid resistance

R_s	Simulated resistance
R_{dc}	DC link resistor
R_{HoI}	Resistor in the hardware-of-interest section
R_H	Hardware resistance
r_{LCL_c}	Internal resistor of converter side inductor of LCL filter
r_{LCL_g}	Internal resistor of grid side inductor of LCL filter
R_{LCL}	Series damping resistor of LCL filter
R_{LC}	Resistor of LC filter
r_{LC}	Resistance of inductor of LC filter
T_d	Transfer function of the PI controller delay
T_f	Time constant of the low-pass filter
$T_{d,A/D}$	Analog-to-digital delay
$T_{d,D/A}$	Digital-to-analog delay
$T_{d,DRTS}$	Digital real-time simulator delay
$T_{d,Sens}$	Sensor delay
T_{d_i}	Transfer function of current controller delay
T_{dT}	Total delay in the loop
T_{d_v}	Transfer function of voltage controller delay
T_{dPI_i}	Delay of current controller
T_{dPI_v}	Delay of voltage controller
T_{dPI}	The PI controller delay
T_s	Time-step of the digital real-time simulator
$ TF_{PHIL} $	PHIL transfer function gain
$\angle TF_{PHIL}$	PHIL transfer function phase
$ TF_{RC} $	Real coupling transfer function gain
$\angle TF_{RC}$	Real coupling transfer function phase
V	Voltage at PCC
V_d	d-axis voltage
$\hat{V}$	Small-signal voltage
$V_p(f_p)$	Voltage perturbation source
V_s	Voltage of the simulated source
V_{Cs}	Output voltage of the simulated grid
V_{Cs}^*	Voltage setpoint of the grid-forming converter
V_c	Voltage over capacitor
V_{dc_n}	DC link voltage nominal value
V_{dc}	DC link voltage

V_{dc}^*	DC link voltage setpoint
V_{EG}	Voltage source model of emulated grid
V_{GFM}	Output voltage of grid forming converter
V_n	Nominal PCC voltage
$WAVG$	Weighted average error
Y	A transfer function in the form of admittance
Y_{EG}	Admittance of emulated grid
Y_{GFL}	Admittance of grid-following converter
$Y_{LCL,V_{GFL}}$	Admittance of LCL seen from grid-following converter
$Y_{LCL,V}$	Admittance of LCL seen from grid
$Y_{LCL_{HoI}}$	A transfer function in the form of admittance
Y_{LCL}	Admittance of LCL filter
$Y_{R_{LC}}$	Admittance of capacitor of LC filter
$Y_{r_{LC}}$	Admittance of inductor of LC filter
Y_s	Admittance of simulated model
Z^*	Damping impedance as an interface
Z_C	Capacitor impedance
Z_c	Converter side's impedance
Z_{Cf}	Impedance of capacitor of LCL filter
$Z_{L_{fc}}$	Impedance of converter side inductor
$Z_{L_{fg}}$	Impedance of gridside inductor of LCL filter
Z_{BLT}	Discrete transformation using bilinear transform method
$Z_{C_{LCL}}$	Impedance of capacitor of LCL filter
Z_{dc}	Impedance of DC link
Z_g	Small-signal voltage
Z_{HoI}	Impedance of hardware-of-interest
Z_{L_c}	Impedance of converter side inductor
Z_{L_g}	Impedance of grid side inductor
Z_{LCL_c}	Impedance of converter side inductor of LCL filter
Z_{LCL_g}	Impedance of grid side inductor of LCL filter
Z_{LC}	LC filter impedance
Z_L	Impedance of inductor
$Z_{R_{LC}}$	Impedance of capacitor of LC filter
$Z_{r_{LC}}$	Impedance of inductor of LC filter
Z_{SH}	Linking impedance as an interface
Z_s	Impedance of simulated system

Z_{EGref}	Reference values for emulated grid impedance
Z_{GFLref}	Reference values for grid-following converter impedance

1 Introduction, Motivation and Scope of Work

1.1 PHIL Motivation

A wide range of new energy solutions for power systems is proposed each year, including energy storage systems, renewable energy sources, and components for transportation infrastructure. The fast pace of these developments challenges system operators to validate new technologies before their adoption. While compliance with grid codes can be easily assessed with standard laboratory testing, the real system-level performance can be validated only in the field. For some consolidated technologies (e.g., photovoltaics), the learning curve is already advanced, and only limited testing is needed. However, for less mature technologies (e.g., electrolyzers, new battery chemistries), relatively limited information is available about their field performance and overall system impact.

Setting up a full-scale demonstrator is the only current practice for increasing operational know-how. However, this may lead to several issues: *(i)* high testing costs associated with long installation time and the need for specialized workforce on the field; *(ii)* low testing flexibility due to the limited possibilities to change the demonstrator configuration and its properties, and the need to extend the testing campaign duration until all desired scenarios are covered; *(iii)* liability issues because the Hardware-of-Interest (HoI) is still at prototype stage and could eventually provoke large disturbances in the grid or at local customers. This could require insurance policies to cover unexpected damage to adjacent equipment.

Having a test bench that the actual HoI interacts with a simulation model (e.g., a power grid model), known as a Model-of-Interest (MoI), provides the flexibility of simulation scenarios and the fidelity of working with the actual power hardware (Fig. 1.1a). Therefore, the concept of Power Hardware-in-the-Loop (PHIL) was introduced in the early 2000s [1] to reduce testing costs, time, and risk while maintaining high assessment accuracy, and has continued to gain traction since then [2–4]. As shown in Fig. 1.1b, a PHIL setup combines the fidelity of full-power

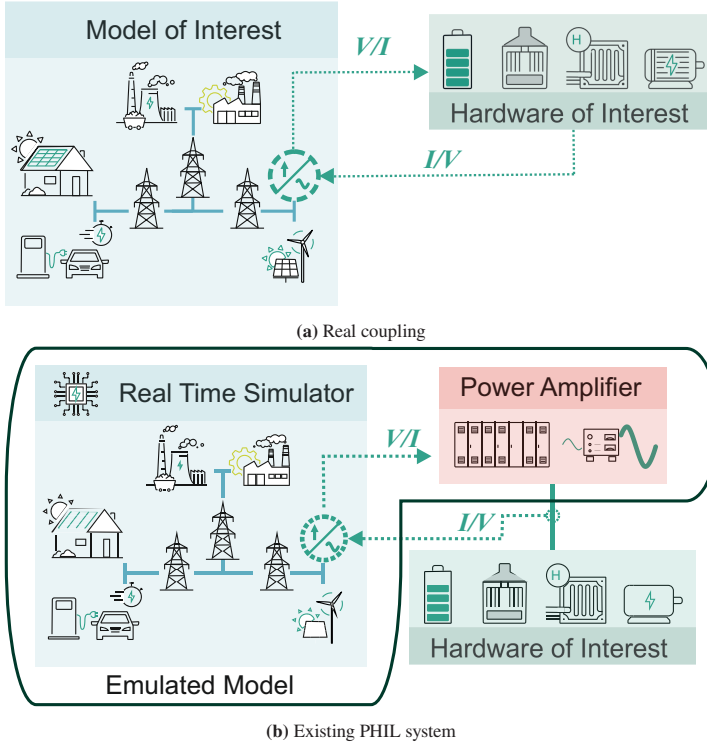


Figure 1.1: PHIL concept

hardware tests with the flexibility of numerical simulations by interfacing HoIs, via specialized power amplifiers (PA), with a real-time model of its operational environment. The MoI is running in a digital real-time simulator (DRTS). The DRTS provides the PA setpoints (typically in digital form), which are converted to the corresponding voltages and currents in the physical system.

The presence of a PA as an interface between the MoI and the HoI is a distinct feature of PHIL systems, and compared to Control Hardware-In-the-Loop (CHIL), as depicted in Fig. 1.1, a PHIL system intends to preserve the real coupling with the real power exchange [5]. A PA enables the flow of instantaneous power at the interface point as in the real system, thus reproducing the real coupling case between the HoI and its operational environment. This operational environment comprises DRTS and PA, which are collectively referred to in this thesis as the Emulated Model (EM). Any HoI that respects the voltage and current ratings of the PA can be connected at its output. Moreover, a chosen variable (e.g., current or voltage) should be measured and fed back to the simulator [6], closing the loop. This approach allows assessment of HoI performance by applying equivalent test conditions to those used in field testing.

1.1.1 PHIL Evolution

In the academic world, there is a clear increasing trend of using PHIL systems for experimental validation of electrical components, as shown in Fig. 1.2. Initial works on PHIL are dated at the beginning of the 2000s. Currently, papers with PHIL as the main topic have grown to more than 40 per year in 2024, with a linear increase. As Table 1.1 shows, the focus changed greatly over time. The initial focus was on motors and electric drives applications, targeting the performance validation of machines under external disturbances [1, 7–9, 23, 24] while even earlier works [1, 25] introduced the concept and focused more on the basic aspects. However, as global attention shifts to renewable energy production and integration, the focus of PHIL-related research has shifted toward grid-connected components. For example, the validation under realistic conditions of energy storage systems has been performed to counteract the higher power variations caused by renewable resources [10–13]. Finally, in the most recent years, the results of more complicated and accurate real-time-based simulations using the PHIL approach have been published mostly in the domain of electric power grids and power electronics-based control approaches [14–16, 18–22].

Table 1.1: Evolution of the PHIL applications in literature from 2007

References	Year	Application	Simulation time step	Time frame of interest	Size of simulated grid	Hardware power scale factor	Hardware voltage scale factor
[7]	2007	Super Conducting Motor	1.5 & 50 μ s	minutes	756 nodes	1	1
[8]	2008	Electric Drives	50 μ s	hundreds ms	1 Bus	1	1
[9]	2010	Large Motor Drives	50 μ s	hundreds ms	1 Bus	1	1
[10]	2013	Unintentional islanding		hundreds ms	Small	1	1
[11]	2017	Frequency response of Energy Storage	50 μ s	hundreds ms	24 Buses	5-50e3	500
[12]	2017	Flywheel Energy Storage	50 μ s	minutes	24 Buses	1	1
[13]	2018	Heat Pump and Energy Storage Systems	50 μ s	minutes	1 Bus	1	1
[14]	2018	Distribution Voltage Regulation		minutes	14 Buses	10	1
[15]	2019	Solid State Transformers Primary frequency support		hundreds ms	Small	100	1
[16]	2020	Flywheel Frequency Response	24 μ s	hundreds ms	18 Buses	1	1
[17]	2021	Power electronics grid integration	50 μ s	ms	1 Bus	1	1
[18]	2021	Energy Storage Integration	50 μ s	minutes	1 Bus	3 & 7	5 & 8
[19]	2021	Variable Speed Diesel Generator with Supercapacitor	50 μ s	hundreds ms	Small	1	1
[20]	2021	Virtual Motors	15 μ s	seconds	Small	1	1
[21]	2024	Asynchronous Grids	24 μ s	hundreds ms	18 Bus	10	1
[22]	2024	Virtual Synchronous Machine validation in flywheels	24 μ s	hundreds ms	Small	1	1

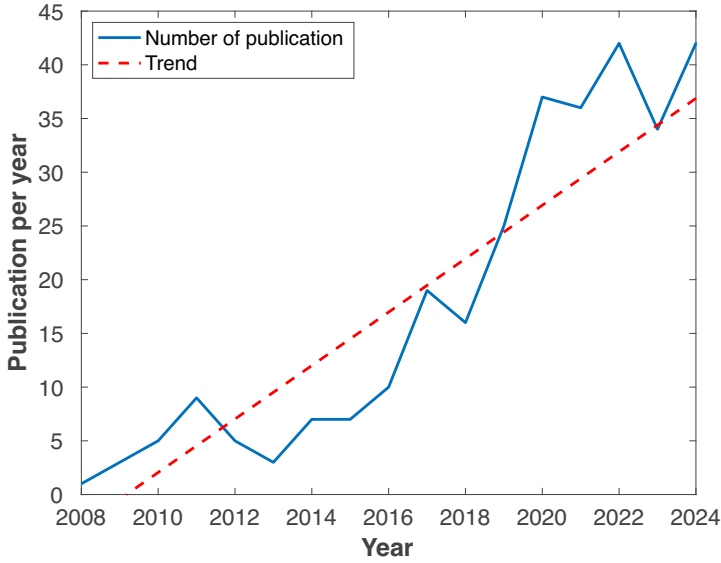


Figure 1.2: Number of published papers for each year from 2008 using Web of Science database. Research performed in Web of Science with the query $TS=(\text{"power hardware in the loop"} \text{ OR } \text{"power-hardware-in-the-loop"})$

1.1.2 Challenges of PHIL Testing

A PHIL is a multi-component system, and the communication between components and the method to interconnect them can change the dynamics of PHIL results, affecting the functionality and accuracy of PHIL tests. Therefore, users should be aware of factors that challenge PHIL testing. The key aspects of these challenges are discussed below.

1.1.2.1 Modeling Approach

A PHIL system is made of coupling software (DRTS) and HoI (analog device). The DRTS operates in the discrete domain, whereas, on the other side of PA, real-world hardware operates continuously. To achieve a dynamic model of the PHIL systems, the loop transfer functions are required. While choosing continuous-time domain transfer functions makes it easier to understand the dynamic behavior of each component, modeling the entire PHIL in the continuous domain ignores the actual behavior of DRTS, and vice versa. Additionally, in many studies, the model of interface components is neglected, and delays are understated; for example, Padé approximations are used. Finally, on the hardware side, the HoI model is often uncertain, further complicating loop modeling.

Open points: A modeling approach that mimics PHIL's hybrid discrete/continuous nature is required. Also, to analyze the loop transfer functions, a general methodology must be adopted that accounts for interface dynamics and delays. Hence, for PHIL modeling, a general approach must be adopted, considering the possibility of inaccuracies in the HoI or interface model.

1.1.2.2 Stability vs. Accuracy

As mentioned above, the PHIL introduces elements for interfacing the MoI and HoI that do not exist in reality (real coupling scheme): DRTS, PAs, sensors, etc. As a consequence, these elements impose delays in the software-hardware communication and limit the PHIL bandwidth. The stability and accuracy of the PHIL systems are, therefore, affected [3, 4].

To solve this issue, two approaches have been followed:

1. Varying the interface method, which is given in [26] and will be illustrated in the next chapter.
2. Inserting a feedback (or feed-forward) filter to damp the high-frequency system dynamics, and thus stabilize the loop [27].

Both approaches help to stabilize the PHIL systems. However, they also modify the loop plant by introducing transfer functions that do not exist in reality, deteriorating the PHIL accuracy, mostly at the high-frequency range. Therefore, a trade-off emerges between accuracy and stability in PHIL testing. Furthermore, as noted earlier, in many cases the behavior of the HoI is unknown; therefore, its detailed model has yet to be verified via PHIL itself. This complicates the stability of PHIL even more.

Open points: In the literature, the stability of PHIL is mostly analyzed when passive loads are employed as HoI. A methodology for analyzing the stability of PHIL regardless of the HoI (e.g., grid converters) prior to laboratory experiments is lacking. A general approach applicable to a wide range of HoIs can help operators choose better stabilizers for interface components and interface algorithms (the method of coupling HoI to EM), thereby optimizing the stability-accuracy trade-off.

1.1.2.3 Scalability

The PHIL testing is mainly limited by the PA sizing, which is typically limited to several MVA in low-voltage applications (1 kV RMS or 1.5 kV DC). However, higher-voltage and higher-power applications are currently of great interest to the academic and industrial communities. The results of PHIL tests performed using reduced-scale prototypes connected to simulated networks of significantly larger size are presented in several papers. This approach is typically used to test wind power plants [28, 29], HVDC systems [30–32], and high-power electric drives [33].

Although some performance characteristics can be easily captured, the main concern with this trend is the fidelity of testing due to power converter scaling-up. Improper scaling can introduce significant inaccuracies in test results because some converter properties, such as switching characteristics, dynamic and thermal properties, cannot be accurately scaled.

Open points: The fidelity of tests based on scaled-down HoI with respect to the full-scale hardware needs to be verified. Using reduced-scale PHIL system components may neglect certain phenomena or dynamics, leading to an incorrect performance assessment. In some cases, a well-built simulation or CHIL testing could produce more accurate results.

1.1.2.4 Experimental Dynamics

PAs in PHIL systems are used as an interface between the MoI and the HoI. PAs used in PHIL systems can be either linear PAs, or switched-mode PAs [34]. Due to their operating principle, linear PAs can achieve very high bandwidths but suffer from low efficiency and cannot regenerate energy into the input power source. On the contrary, switched-mode PAs offer significantly higher energy efficiency (above 90%), bidirectional power flow, and smaller size and weight. Furthermore, Chapter 2 shows that choosing the interface algorithm alters the PHIL dynamics.

All these aspects need to be taken into account during PHIL testing (especially when testing phenomena involving fast transients), because the amplifier's limited bandwidth and the interface algorithm can compromise test accuracy in several cases.

Open points: Additional research is needed to characterize the effects of PA limitations and interface algorithm methods on simulation testing accuracy of highly dynamic systems and phenomena (e.g., faults). There is a need for new PA technologies capable of operating at high frequencies and high power levels (e.g., for testing medium-frequency transformers).

1.2 PhD Research Question

Given that the first two issues also occur across all the other challenges discussed above, the research framework of this thesis is developed to address the PHIL modeling and stability challenges. To be concise, this thesis is structured around the following core research questions:

1. How can a PHIL system be modeled to accurately capture the effects of interface components and time delays in closed-loop operation?
2. How can the stability of PHIL systems with active HoIs, e.g., grid converters, be assessed using prior experimental testing?
3. How can PHIL stability be evaluated when the internal dynamics of the HoI are partially unknown?
4. How do the control dynamics of active HoIs influence PHIL stability and accuracy?
5. What practical design guidelines can be derived for selecting PHIL configurations and controller parameters to ensure stable and accurate operation?

1.3 Scope of the Work and Thesis Structure

To address the research questions, this thesis examines PHIL modeling techniques, considers the modeling domain and interface components, and proposes an impedance-based approach suitable for active HoIs in PHIL systems modeling and stability analysis. Various converters are examined using the selected approach and verified through simulations and laboratory experiments. The structure of the thesis is shown graphically in Fig. 1.3, and the main contribution of each chapter is given as follows:

- **Chapter 2** provides an overview of the PHIL concept, its components and their impact, classic methods to couple the EM and HoI, and the most recent studies on the PHIL.
- **Chapter 3** proposes a modeling approach that considers the hybrid continuous/discrete nature of PHIL setups, and the closed-loop response is verified via simulations and experiments.

- **Chapter 4** takes a grid-following converter as an active HoI in a PHIL and investigates its impact on the stability and accuracy of the PHIL considering the converter controller loop.
- **Chapter 5** proposes Impedance-based stability analysis to study the stability of a PHIL for grid-converter testing, with the advantage of stability verifications for uncertain HoIs. The impact of control variables on the stability of PHIL is studied. The approach is further developed for an active front-end converter with a dynamic DC link.
- **Chapter 6** compares the current and voltage mode of the commonly-used interface algorithm, Ideal Transformer Method (ITM), for Grid-following and Grid-forming converter testing in a PHIL setup.
- **Chapter 7** expands the methodology of the impedance-modeling and stability analysis to a double-PHIL, required for back-to-back converter testing.
- **Chapter 8** provides testing guidelines on PHIL testing, highlighting the importance of various scenarios.
- **Chapter 9** concludes the thesis by summarizing the key findings, identifying open research questions in the field, and outlining directions for future work.

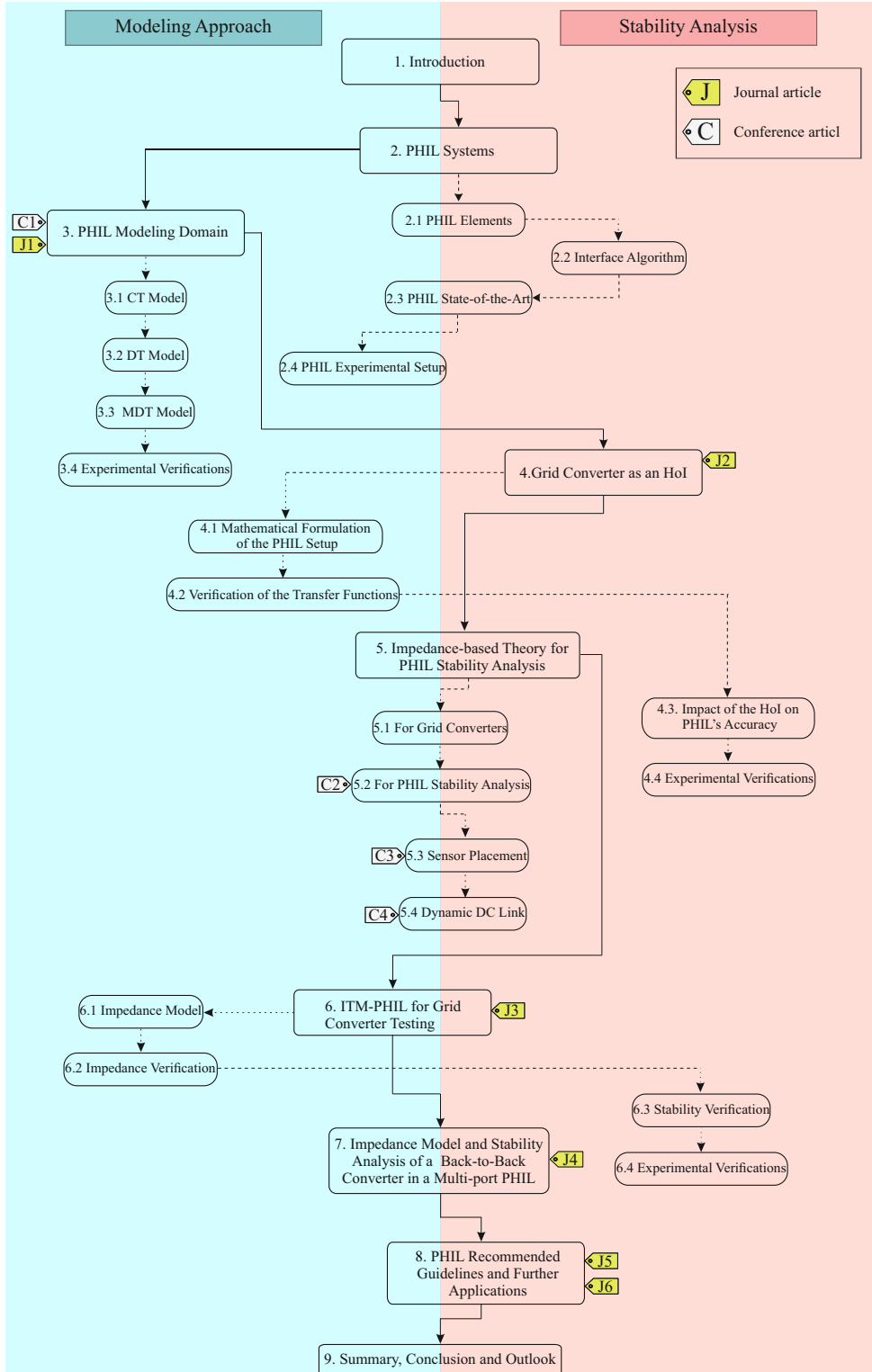


Figure 1.3: This thesis structure

2 Power Hardware-in-the-Loop Systems: Elements, Interface Algorithms, and State-of-the-Art Review

The main components of the PHIL used in this thesis are introduced here before going to the modeling details. The impact of each component on PHIL stability and accuracy is then shown through simulations. The common interface algorithm for connecting MoI to the HoI is reviewed and compared with respect to stability and accuracy. Finally, the selected PHIL setups for experimental verification in the thesis are presented in the last section.

2.1 PHIL Elements

As shown in the Fig. 2.1, a PHIL setup combines DRTS with a physical HoI through a power interface, enabling the evaluation of power devices under realistic operating conditions. The PHIL setup chosen in this section employs the Voltage-type Ideal Transformer Method (V-ITM) as its interface algorithm, meaning that the output voltage of the MoI is measured and sent to the amplifier to be reproduced and applied to the HoI, and the current of the HoI is measured and sent back to the DRTS. Detailed explanations of different interface algorithms, including V-ITM, are provided later in this chapter.

A typical PHIL setup consists of several key components whose dynamic characteristics determine the stability and accuracy of the closed-loop system. The main components are described in the following subsections.

① Digital Real-Time Simulator

The DRTS constitutes the computational core of a PHIL system. It executes a numerical model of the simulated power system with a fixed and deterministic time step to ensure real-time operation. The simulator calculates electrical quantities, such as voltages and currents, that represent the virtual network connected to the HoI. These calculated quantities are provided as reference signals to the power interface, while measured feedback signals from the hardware are incorporated into the simulation model to close the loop. The achievable simulation bandwidth and fidelity are limited by the selected time step, solver structure, and model complexity. As will be shown in the next section, excessive computational delay or insufficient time resolution can introduce phase lag, negatively affecting PHIL stability and accuracy. The delays imposed by DRTS due to the computational time can be described as follows:

$$G_{DRTS} = e^{-(T_{d,DRTS})s} \quad (2.1)$$

where $T_{d,DRTS}$ is normally equal to the time step chosen for the DRTS, and its typical range is from hundreds of ns to around a few μs for power electronics switching simulations and between $10\text{-}50 \mu s$ for power system analysis. It is important to note that this delay occurs at least once in both sending and receiving the data.

② D/A and A/D Converters

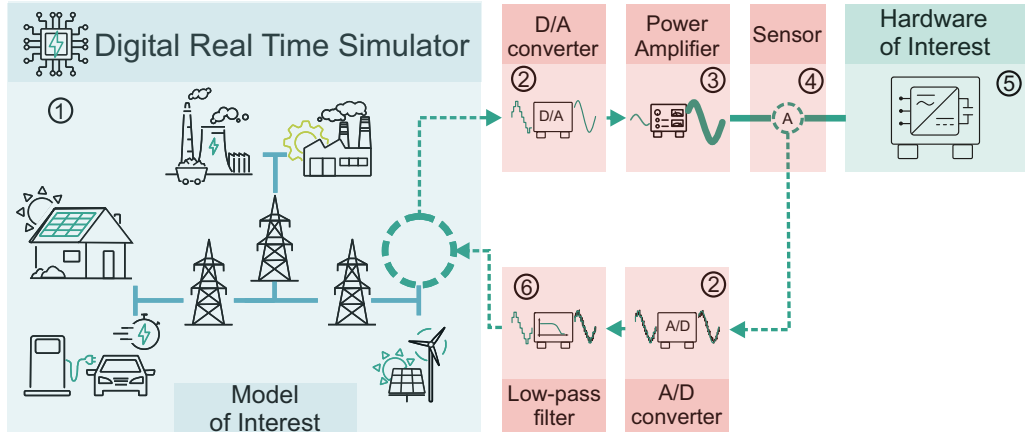


Figure 2.1: Structure of a PHIL

Digital-to-analog (D/A) and analog-to-digital (A/D) converters form the signal-level interface between the DRTS and the physical components of the PHIL system. The D/A converters transform the simulator-generated digital reference signals into analog signals suitable for operating PA. However, depending on the PA technology, communication between DRTS and PA can be digital-to-digital, and then the PA itself converts it to analog. Therefore, D/A section may be part of the DRTS, e.g, add-on card, or within the PA. Conversely, A/D converters sample the measured analog feedback signals and convert them into digital form for processing within the simulator. The resolution, sampling frequency, and conversion latency of these converters directly affect the quality of the signals exchanged. Quantization effects, sampling delays, and limited bandwidth contribute to inaccuracies and phase shifts in the PHIL loop. These effects must be accounted for when analyzing the system's closed-loop dynamics via modeling signal conversion exchange as:

$$G_{A/D} = e^{-(T_{d,A/D})s} \quad (2.2)$$

$$G_{D/A} = e^{-(T_{d,D/A})s} \quad (2.3)$$

which $T_{d,A/D}$, and $T_{d,D/A}$ are signal conversion delays and their typical range is around $5 \mu s$.

③ Power Amplifier The PA is a defining element of a PHIL setup, as it enables the exchange of real power between the DRTS and the HoI. Its role is to reproduce the electrical quantities calculated by the simulator at appropriate voltage and current levels. Different PA technologies are employed in PHIL applications [35]:

A. Linear Power Amplifiers The linear amplifier is designed to operate in the linear range of transistors, resulting in lower efficiency but higher bandwidth. They offer wide bandwidth, high voltage ramp rate, and low distortion, making them suitable for applications that require accurate reproduction of fast transients. However, operating in the linear region results in low efficiency and limited power-scalability, limiting their use to low- and medium-power PHIL experiments.

B. Switching Power Amplifiers The switching-mode amplifiers are based on multiple conversion stages from input to output, including AC/DC, DC/DC, and DC/AC (or DC/DC, depending on the application) converter topologies. The amplifier consists of a front-end rectifier and a back-end inverter, enabling operation in either current or voltage mode. Moreover, by selecting the control type, filter topology, and switching frequency, the amplifier bandwidth can be tuned [3]. Their high efficiency and scalability make them suitable for medium- and high-power PHIL systems.

However, switching dynamics, internal control loops, and modulation processes introduce finite bandwidth and time delays that can significantly affect PHIL stability and accuracy.

C. Motor/Generator Sets A generator-type amplifier operates by employing a DC motor that drives a synchronous generator. They represent an electromechanical approach to power amplification, in which a motor driven by a conventional power source supplies mechanical power to a generator connected to the HoI. While these systems provide electrical isolation and high overload capacity, their large mechanical inertia limits dynamic performance. Consequently, motor/generator sets are generally unsuitable for PHIL applications involving fast power-electronic dynamics.

Independent of the underlying technology, PAs may operate as voltage sources or current sources. In voltage-source operation, the amplifier enforces a specified output voltage waveform, whereas in current-source operation, it regulates the injected current. The selected operating mode must be compatible with the interface algorithm and the HoI characteristics, as it directly affects the PHIL loop's stability.

In this thesis, primarily the linear amplifier model is used for simulations, modeling, and experiments, whose dynamic impact and delay can be described:

$$G_{PA_V} = \frac{e^{-(T_{d,PA})s}}{((1/\omega_0^2)s^2 + (2 \cdot D/\omega_0)s + 1)} \quad (2.4)$$

$$G_{PA_i} = \frac{(1 + \frac{s}{\omega_Z})e^{-(T_{d,PA})s}}{1 + \frac{2 \cdot \delta_P}{\omega_P} \cdot s + \frac{s^2}{\omega_P^2}} \quad (2.5)$$

where G_{PA_V} is the transfer function of the amplifier in voltage mode, $T_{d,PA}$ is the amplifier's delay, and ω_0 and D are the natural frequency and damping factor, with the values of $2 \cdot \pi \cdot 180000$ Rad/s and 0.9, respectively. G_{PA_i} is the amplifier's transfer function in current mode, ω_P , and ω_Z are pole and zero angular frequency, and δ_P is the damping ratio. The typical delay of the linear amplifier is around $1.5 \mu s$ in the voltage mode and $1.6 \mu s$ in the current mode [36].

④ Sensor

Sensors measure physical quantities at the interface between the PA and the HoI. Typical measurements include voltages and/or currents, which are fed back to the DRTS to close the PHIL

loop. Sensor performance is characterized by bandwidth, accuracy, noise level, and inherent delay. Insufficient bandwidth or excessive noise can distort the feedback signals, while measurement delays can introduce additional phase lag into the closed-loop system. As a result, sensor selection and placement are critical for maintaining PHIL stability and accuracy. Similar to signal converter modeling, the sensors' delay can be modeled as:

$$G_{Sens} = e^{-(T_{d,Sens})s} \quad (2.6)$$

and the typical range for sensor delay, $T_{d,Sens}$ is less than $5 \mu s$.

⑤ Hardware-of-Interest

Evaluating the HoI behavior is the main purpose of the PHIL experiments. Therefore, in many cases, the HoI model is uncertain or even unknown. PHIL systems can be differently developed for various HoIs as given in Table 1.1. In this thesis, passive loads and grid converters are employed as HoIs. For passive loads, HoI modeling is straightforward; however, when a digital controller is added, e.g., in grid converters, HoI modeling becomes more challenging. In Chapter 4, it is shown that even HoI can affect the stability and accuracy of PHIL systems.

⑥ Low-Pass Filter

LPFs are commonly applied to measured feedback signals in PHIL systems to attenuate high-frequency noise, and switching harmonics effects introduced by sensors and PAs. Filtering improves signal quality and prevents numerical issues within the DRTS. However, LPFs introduce additional phase delay, which reduces the stability margin of the PHIL loop. Therefore, the filter cutoff frequency must be carefully selected to balance noise attenuation against dynamic performance. Improper filter design may significantly degrade the stability and accuracy of PHIL experiments. The dynamic impact of the LPF can be depicted via the following transfer function:

$$G_{LPF} = \omega_c / (s + \omega_c) \quad (2.7)$$

in which the ω_c is the cut-off angular frequency of the LPF. To maintain a balance between noise rejection and capturing the important dynamics of grid/converter interaction, the typical range for the cut-off frequency is around 2 kHz.

2.2 Elements Impact on PHIL Stability and Accuracy

PHIL faces stability and accuracy challenges compared to real coupling due to the presence of interfaces. Each interface element employed in PHIL alters the outputs compared to real coupling, potentially affecting accuracy and compromising the setup's stability. The aim of this section is to analyze and demonstrate how interface elements impact PHIL results using a simplified example.

For time-domain simulations, a PHIL system and its real coupling based on [26] is modeled in MATLAB/Simulink as shown in Fig. 2.2, where the HoI is chosen as an RL load, and the Thévenin equivalent of the grid is chosen as MoI. In addition to time-domain simulations, the models of the real coupling and PHIL systems are obtained from their transfer functions for frequency-domain analysis. For simplicity of representation, the transfer functions are given without (s). The transfer functions of the HoI and the grid impedance can be described as follows:

$$G_{HoI} = \frac{1}{R_H + L_H \cdot s} \quad (2.8)$$

$$G_s = R_s + L_s \cdot s \quad (2.9)$$

where, G_{HoI} is the transfer function of the RL load as HoI and G_s is the transfer function of the grid model as MoI. According to Fig. 2.3a, open-loop and closed-loop transfer functions for real coupling can be described as, $G_{ol,RC}$, and $G_{cl,RC}$:

$$G_{ol,RC} = G_s \cdot G_{HoI} \quad (2.10)$$

$$G_{ol,RC} = \frac{1}{1 + G_{ol,RC}} \quad (2.11)$$

and for PHIL system, the open-loop:

$$G_{ol,PHIL} = e^{-T_{dT}s} \cdot G_{PA} \cdot G_{HoI} \cdot G_{LPF} \cdot G_s \quad (2.12)$$

where T_{dT} is the total delay of the setup, excluding $T_{d,PA}$ which is included in G_{PA} , is as follows:

$$T_{dT} = 2 \cdot T_{d,DRTS} + T_{d,D/A} + T_{d,Sens} + T_{d,A/D} \quad (2.13)$$

Lastly, the closed-loop transfer function, G_{cl} , can be defined as follows:

$$G_{cl,PHIL} = \frac{G_{fw}}{1 + G_{ol,PHIL}} \quad (2.14)$$

$$G_{fw} = e^{-(T_{d,DRTS} + T_{d,D/A})s} \cdot G_{PA} \quad (2.15)$$

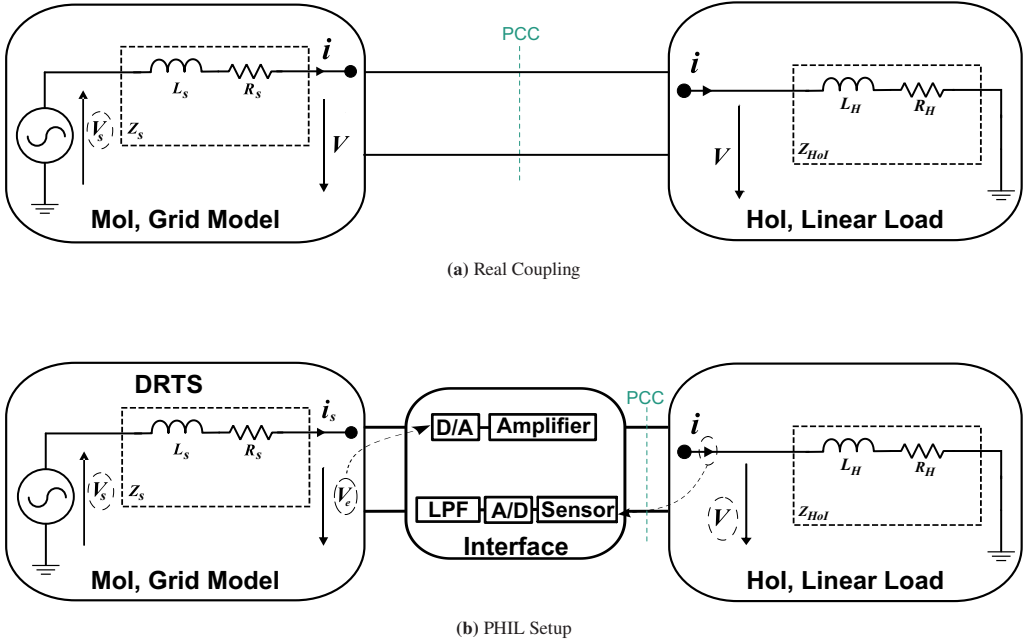


Figure 2.2: Benchmark for interface elements impact analysis: a) Real Coupling, which shows the connection in the real field without the interfaces of PHIL, b) PHIL setup, which shows the interfaces needed to couple the DRTS to the actual HoI

To illustrate the overall impact of the interfaces, a time-domain simulation is performed in addition to the closed-loop frequency response (using the parameters in Table 2.1), and the results are shown in Fig. 2.4 and Fig. 2.5, respectively. The results show that the voltage at the PCC in the PHIL lags that in the real coupling setup.

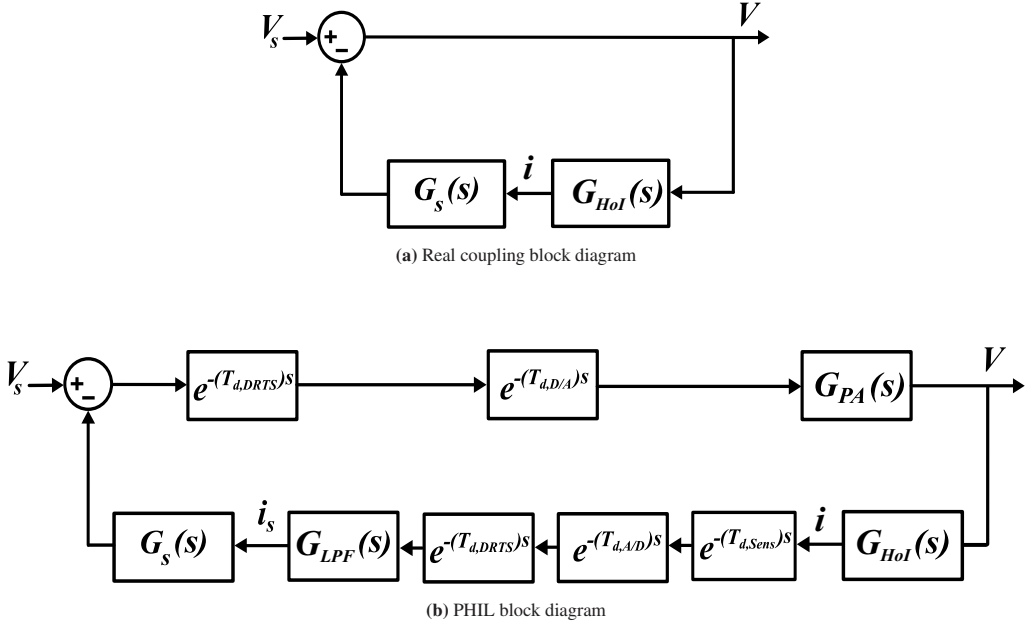


Figure 2.3: Block diagram comparison of real coupling and PHIL system

Then open-loop transfer functions of the real coupling and PHIL systems are compared and shown in Fig. 2.5. The observable differences in the frequency response are the result of the difference in (2.10) and (2.12), namely the term $G_{PA} \cdot G_{LPF} \cdot e^{-T_{dT}s}$.

The results show that the phase difference increases with frequency due to the term $e^{-T_{dT}s}$. Moreover, a gain difference can also be seen in the Fig. 2.5. This difference stems from the PA and the LPF. Therefore, the interface elements' impacts are divided into three sections, namely, time delays, PA, and LPF. To understand how each interface component contributes to this difference (i.e., inaccuracy), the impact of each element is explained next.

Table 2.1: PHIL Benchmark parameters

$T_{d,DRTS}$	$T_{d,Sens}$	$T_{d,A/D}$	$T_{d,D/A}$	$T_{d,PA}$	T_{dT}	V_s	R_H	L_H	R_s	L_s
$[\mu s]$	$[\mu s]$	$[\mu s]$	$[\mu s]$	$[\mu s]$	$[\mu s]$	$[V]$	$[\Omega]$	$[mH]$	$[\Omega]$	$[mH]$
50	3	3	3	1.5	110.5	310	0.5	5	1.25	6.25

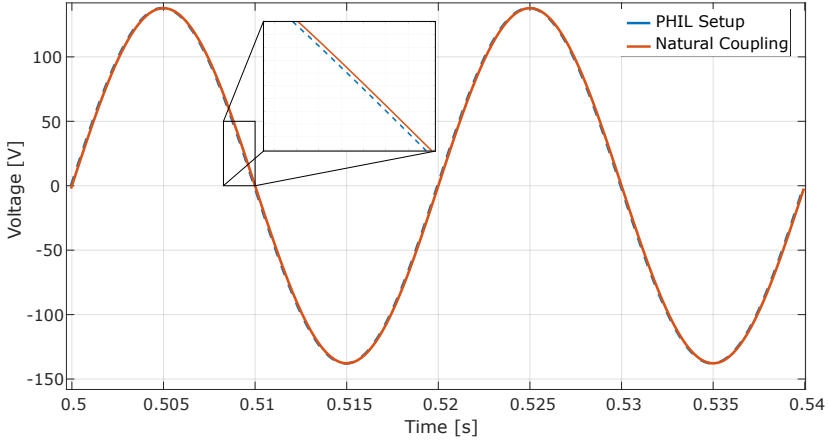


Figure 2.4: Time domain comparison: PCC voltage

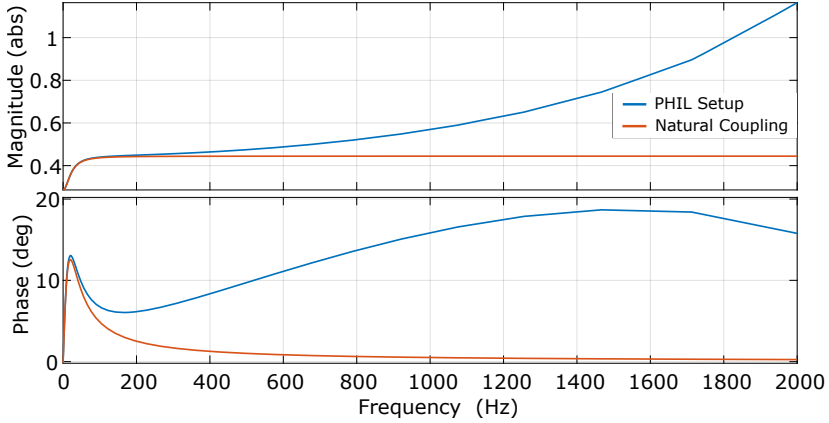


Figure 2.5: Closed-loop Bode plot results

2.2.1 Time Delays Impact

A PHIL system, regardless of the interface algorithm applied, will experience time delays. A full characterization of these delays is presented in [37]. Accordingly, the delays could be divided into simulation delay, communication delay, and PA delay. The simulation delay is the delay resulting from the DRTS or digital controllers. As noted in the previous section, where the PHIL elements and their equations are given, besides PA and DRTS, the A/D and D/A converters, and the sensors introduce delays into the loop. It is worth mentioning that, in most power system studies, the dominant loop delay is the DRTS delay, which is twice the DRTS time step (i.e., 10-50 μ s).

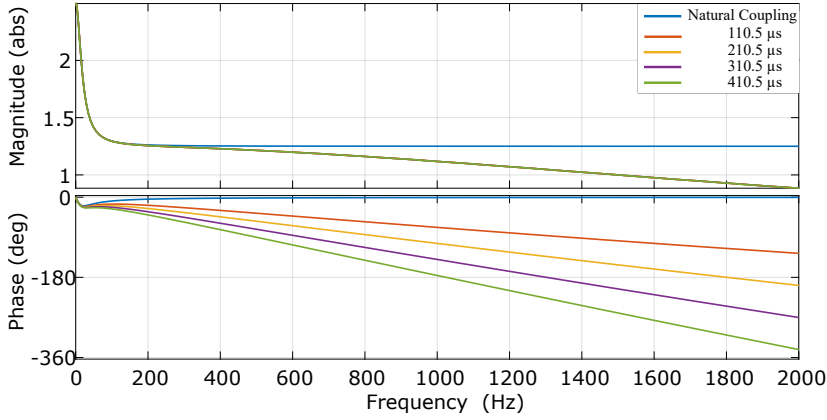


Figure 2.6: Bode plot results of real coupling and PHIL setup for various DRTS time steps

According to (2.12), the greater the delay in the loop, the greater the phase shift due to the term $e^{-T_{d_T}s}$. A comparison of the frequency responses of different time delays in the loop is shown in Fig. 2.6. Based on the figure, such delays do not occur in the real coupling; therefore, a greater delay, e.g., a larger time step for the DRTS, results in less accurate PHIL as it further deviates from real coupling.

In addition to accuracy, the stability impact of the interface is examined. In this thesis, Bode plots are primarily used for accuracy comparison, and Nyquist plots are used for stability analysis to improve intuition. A closed-loop setup is stable if the Nyquist plot from its open-loop does not encircle the critical point at $(-1, 0j)$. The total delay in the PHIL is $110.5\mu s$. The DRTS delay is then increased gradually, and the Nyquist plots are presented in Fig. 2.7. The figure illustrates that as the delay increases, the system becomes unstable. Therefore, the delay introduced by the interface components, especially DRTS, can, in addition to inaccuracy, lead to an unstable setup.

2.2.2 Low-Pass Filter Impact

The LPF filter is added to reject high-frequency noise in the sensor-measured values and can also be used to stabilize the system by limiting the loop bandwidth. To show the effect of the LPF, the Bode plots of the open-loop are shown at different filter cut-off frequencies in Fig. 2.8. The figure shows that as the cutoff frequency decreases, the gain decreases at higher frequencies.

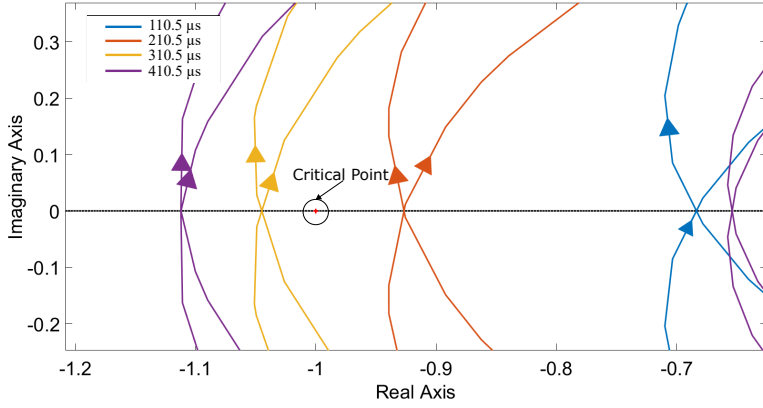


Figure 2.7: Nyquist plots at different delays

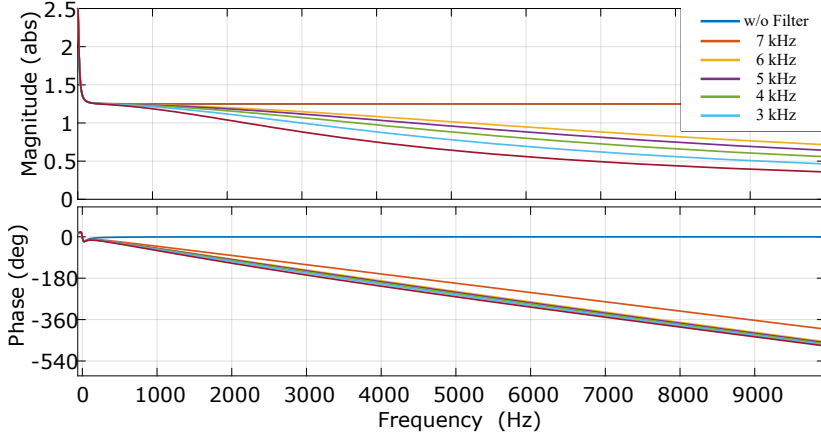


Figure 2.8: Bode plot results at different filter frequencies

To show the effect of the filter and the required cut-off frequency, the Nyquist plot is redrawn at different cut-off frequencies in Fig. 2.9. The figure shows that the setup can be stabilized if a filter with a cut-off frequency of at least 4 kHz is added in the feedback. However, according to Fig. 2.8, as the cut-off frequency decreases, the PHIL open-loop transfer function shifts further from the real coupling; therefore, it is necessary to make a trade-off between stability and accuracy when choosing the cut-off frequency.

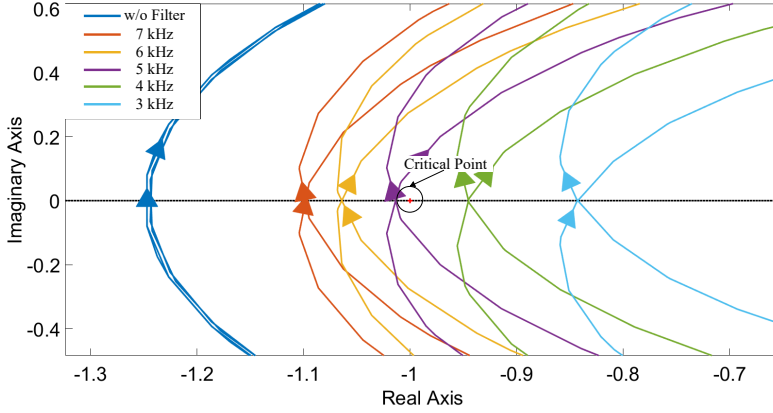


Figure 2.9: Nyquist plot at impedance ratio of 1.25 at different filter cut-off frequencies

2.2.3 Power Amplifier Impact

PAs impact the PHIL setup through time delays, as shown in its transfer function G_{PA} presented in (2.12), which may change depending on the type and the parameters of the PA, $e^{-T_{d,PA}s} \cdot T_{PA}$, where $T_{d,PA}$ is the delay of the amplifier and T_{PA} is a transfer function that is based on the amplifier's bandwidth. Therefore, the change in the amplifier will either result in the same effects as the change in delay shown before, or a change in bandwidth as shown in the change of the LPF.

2.3 Interface Algorithms

Interface algorithms enable communication between the EM and the HoI. In the previous subsection, the effect of each component was studied; however, the interface algorithm employed was the V-ITM. This section reviews and compares the five main interface algorithms as described in [26]. First, each interface algorithm is detailed; then, they are compared with respect to stability and accuracy.

2.3.1 Ideal Transformer Method (ITM)

The ITM, shown in Fig. 2.10, is widely used as it is straightforward to implement and it requires no additional hardware. The interface can be implemented using the Voltage-type Ideal Transformer Method (V-ITM, shown once more in Fig. 2.10a). Another option is the Current-type Ideal

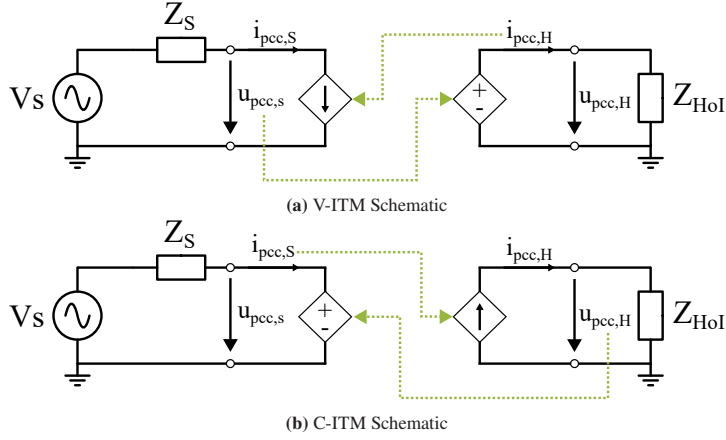


Figure 2.10: ITM Schematics

Transformer Method (C-ITM), given in Fig. 2.10b. The difference lies in the amplified signal and the feedback: in C-ITM, the current is amplified, and the voltage is the feedback, whereas in V-ITM, the voltage is amplified and the current is the feedback. For a passive impedance as in HoI, the V-ITM and C-ITM open-loop transfer functions as follows:

$$G_{ol,VITM} = e^{-T_{dT}s} \cdot G_{PA} \cdot G_{LPF} \cdot \frac{Z_s}{Z_{HoI}} \quad (2.16)$$

$$G_{ol,CITM} = e^{-T_{dT}s} \cdot G_{PA} \cdot G_{LPF} \cdot \frac{Z_{HoI}}{Z_s} \quad (2.17)$$

By comparing (2.16) and (2.17), the change is the ratio of the impedance in the transfer function. As a result, the stability can be reversed. For example, for resistive impedances, if $Z_{HoI}/Z_s > 1$, V-ITM is stable, C-ITM will be unstable, and vice versa.

2.3.2 Partial Circuit Duplication (PCD)

PCD is based on splitting the hardware and software into two sub-circuits and solving them iteratively. The schematic for PCD is shown in Fig. 2.11, where the linking impedance Z_{SH} is added on both sides to ensure the split. The open-loop transfer function can be written as follows:

$$G_{ol,PCD} = e^{-T_{dT}s} \cdot G_{PA} \cdot G_{LPF} \cdot \frac{Z_s \cdot Z_{HoI}}{(Z_s + Z_{SH})(Z_{HoI} + Z_{SH})} \quad (2.18)$$

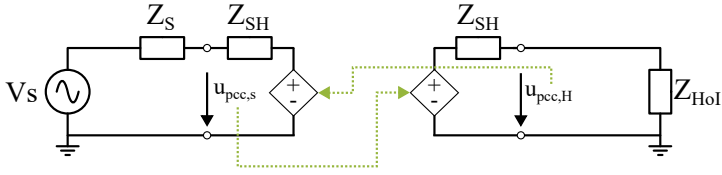


Figure 2.11: PCD schematic

By adding the impedance Z_{SH} , stability can, in theory, be more easily ensured than with ITM. However, to ensure stability, it is necessary that Z_{SH} exceed Z_s and Z_{HoI} , which affects accuracy as this linking impedance does not exist in the real coupling scheme. Furthermore, adding a high-power impedance increases the system's size, cost, and thermal stress.

2.3.3 Damping Impedance Method (DIM)

DIM is a combination of the ITM and PCD, which is achieved by adding the impedance Z^* as shown in the schematic in Fig. 2.12. The open-loop transfer function for this algorithm can be written as follows:

$$G_{ol,DIM} = e^{-T_{dT}s} \cdot G_{PA} \cdot G_{LPF} \cdot \frac{Z_s(Z_{HoI} - Z^*)}{(Z_s + Z_{SH} + Z^*)(Z_{HoI} + Z_{SH})} \quad (2.19)$$

By changing the value of Z^* , the interface algorithm shifts towards either PCD or ITM. If $Z^* = 0$, then the interface becomes PCD, and when $Z^* = \infty$, the interface shifts to ITM. Moreover, by inspection of (2.19), if $Z^* = Z_{HoI}$, then the open-loop gain is zero, and consequently the setup is stable. The issues of PCD are also present in DIM. Also, it is not always practically possible to set Z^* equal to Z_{HoI} , as the hardware impedance changes during the experiment due to the heat and noise.

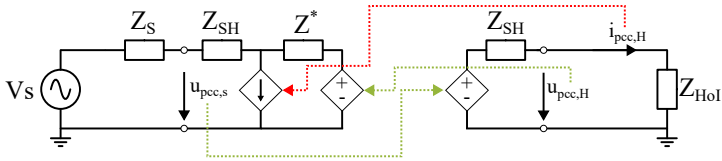


Figure 2.12: DIM Schematic

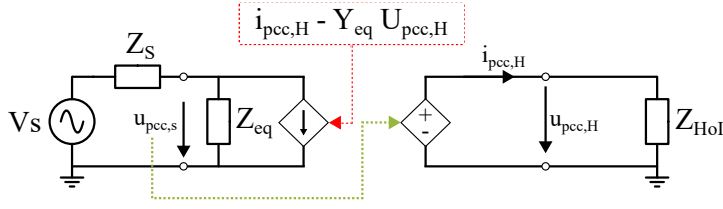


Figure 2.13: TFA Schematic

2.3.4 Time variant First order Approximation (TFA)

TFA simplifies the HoI as an RL or RC load. Using this assumption, the simplified model coefficients are updated at each simulation step based on the hardware's voltage and current from the previous timestep. The schematic is shown in Fig. 2.13, and the open-loop transfer function can be written as follows:

$$G_{ol,TFA} = G_{PA} \cdot G_{LPF} \left(1 - \frac{sT_{dT}}{2}\right) \frac{Z_s}{Z_{HoI}} \quad (2.20)$$

The TFA algorithm provides delay compensation; however, it has several drawbacks, including high noise sensitivity, high implementation complexity, and limitations with nonlinear HoIs.

2.3.5 Transmission Line Model (TLM)

TLM employs the Bergeron model, which is widely used in transmission-line modeling. The models decouple the circuit into two sides, with each side representing the other via resistive Norton or Thévenin equivalents, in which only the values from the previous time step are present. The same idea could be applied in PHIL, where the delay in the system is considered the same as the transmission line propagation time. Therefore, the linking impedance (R_{SH}) can be calculated based on the linking inductor or capacitor as follows:

$$R_{SH} = \frac{L}{T_{dT}} \quad R_{SH} = \frac{T_{dT}}{C} \quad (2.21)$$

where L is the value of the linking inductor, and C is the value of the linking capacitor in the transmission line. The schematic is shown in Fig. 2.14 and the open-loop transfer function can be written as follows:

$$G_{ol,TLM} = e^{-2 \cdot T_{dT} s} \cdot G_{PA} \cdot G_{LPF} \frac{Z_s - R_{SH}}{Z_s + R_{SH}} \frac{Z_{HoI} - R_{SH}}{Z_{HoI} + R_{SH}} \quad (2.22)$$

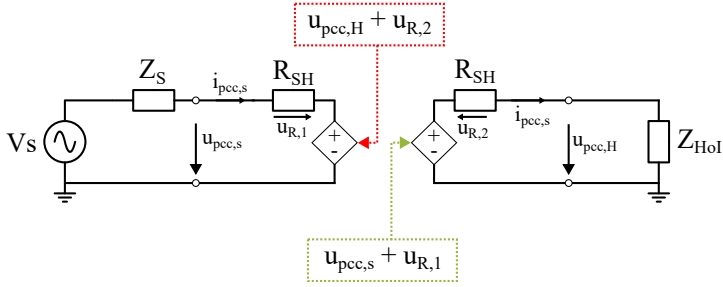


Figure 2.14: TLM Schematic

TLM provides high stability; however, there are some limitations that arise from replacing the linking components with resistors, as these resistors increase the loss of power, which might not be possible in all PHIL setups. Moreover, the value of R_{SH} must be adjusted when the simulated system changes, as it is calculated based on the linking components.

2.3.6 Comparison of Interface Algorithms

The frequency responses of all of the previously mentioned open-loop transfer functions for each interface algorithm are compared using the parameters in Table 2.1. G_{LPF} is set to 1 to see the intrinsic stability of the setup without a LPF. Moreover, the additional impedances required by some interface algorithms are shown in Table 2.2. From Fig. 2.15, it can be concluded that TFA is extremely unstable for the selected parameters, and that V-ITM is also unstable, but C-ITM, DIM, PCD, and TLM are stable.

The accuracy comparison is shown in Fig. 2.16, where the open loops of all IAs are plotted against real coupling. By considering both phase and magnitude, C-ITM provides the best accuracy, followed by TLM, PCD, and DIM.

Table 2.2: Extra impedances added for each IA

PCD/DIM	PCD/DIM	DIM	DIM	TLM
R_{SH}	L_{SH}	R^*	L^*	R_{SH}
$[\Omega]$	$[\text{mH}]$	$[\Omega]$	$[\text{mH}]$	$[\Omega]$
1.25	12.5	0.45	4.5	5

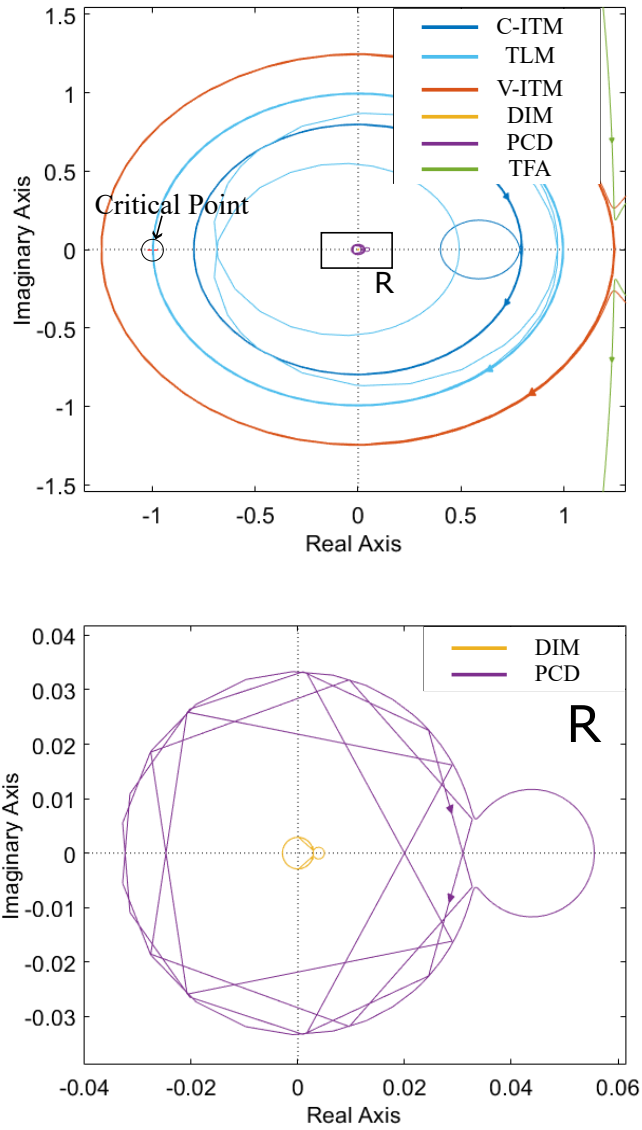


Figure 2.15: Nyquist Plot for Interface Algorithms

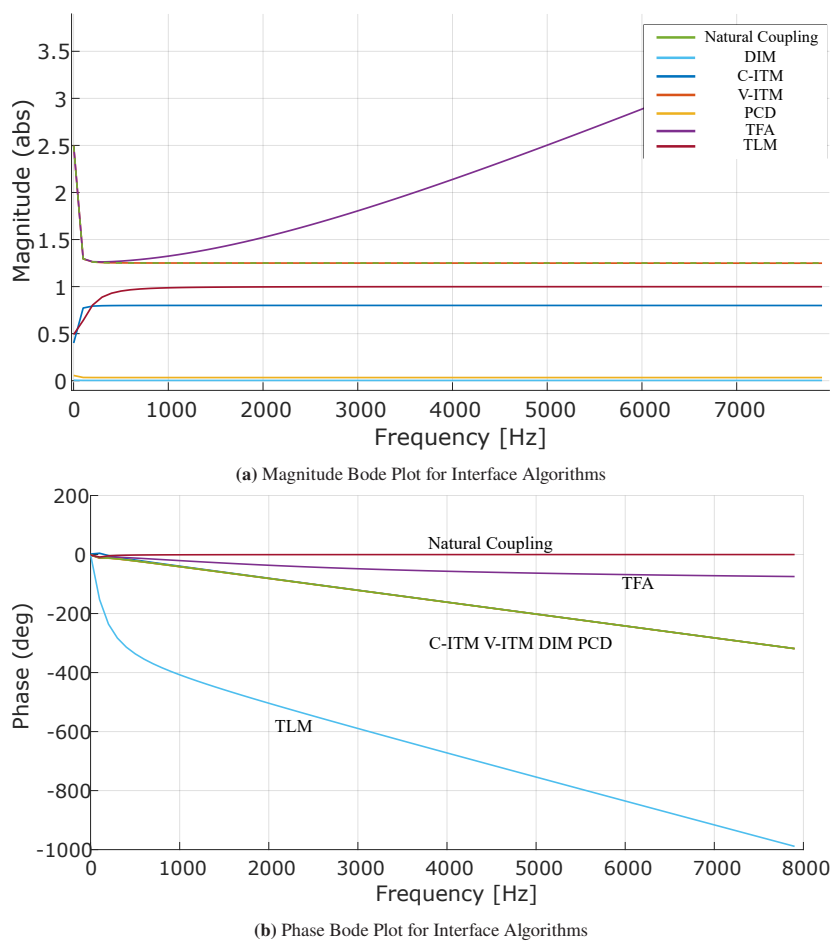


Figure 2.16: Interface algorithms accuracy comparison via Bode plot

2.4 PHIL State-of-the-Art

As shown in the previous section, for the real coupling scheme, which represents the ideal case in which the HoI is directly connected to a real grid, the PHIL test results may deviate from this ideal scheme due to the presence of interface components. In the literature, it has been shown that these interfaces can introduce inaccuracies, potentially compromising the validity of test results [38]. In addition to inaccuracy, the literature highlights that time delays introduced by the DRTS, PA, and the current/voltage sensors can eventually cause instability in the PHIL system [37]. Hence, the stability analysis for PHIL testing has been the subject of intensive investigation in recent years, as reviewed in the well-known literature [3, 4, 39]. The aforementioned interface algorithms, such as the ITM, PCD, DIM, and TLM, to connect the MoI to the HoI are evaluated in [26] to improve the stability and accuracy of a PHIL, among which the ITM is regarded as a straightforward and accurate algorithm. However, when the ITM is used, the stability of the PHIL setup is limited to the software/hardware impedance-ratio criterion. Another interface algorithm with a greater stability margin than ITM is DIM, which combines ITM with PCD. In [40, 41], the wideband system identification technique is employed to enhance the DIM interface algorithm, thereby ensuring simulation stability and accuracy. The modified DIM is proposed in [42], which updates the linking-impedance parameters based on the new HoI value.

Due to the added complexity and implementation costs of the DIM, the ITM and its variants have been further modified to maintain simplicity while enhancing the stability of PHIL. For example, the use of a feedback filter in ITM is one of the most common techniques for ensuring PHIL stability across a wide range of testing conditions. As shown in the previous section, the concept of this method is to add a LPF in the feedback loop in the DRTS software. This approach, first proposed in [27], allows damping the system dynamics and thus strengthening the stability of the PHIL loop. The main advantage of this method lies in its simplicity of implementation, as the LPF can be readily applied in the simulated part as a transfer function within the DRTS. A scheme in [43] relocates part of the delay outside the PHIL, and uses a phase-lead compensator and a digital linear-phase Frequency-Sampling Filter (FSF), thereby enhancing stability and accuracy. Although stability can be significantly improved, the use of LPFs, or compensators, affects the phase and magnitude of the PHIL transfer function, thereby degrading the accuracy of testing relative to the real coupling. A summary of the employed, or improved interface algorithms for PHIL testing is given in (2.3). As can be seen, a majority of PHIL users chose ITM for its simplicity and accuracy.

The accuracy of PHIL testing has been a subject of ongoing discussion for years. In [44], several indexes based on amplitude and phase difference have been introduced in order to validate mathematical models and the PHIL testing concerning the real coupling of the system. However, it focuses exclusively on passive loads (linear and nonlinear) and offers no practical

approach to assessing the accuracy of power electronics converter testing. The discrete-time impedance frequency responses are preferred for better evaluating PHIL stability over conventional continuous-time-based analysis [45], as PHIL is not a fully continuous system. To represent the discrete nature of DRTS and the analog HoIs in a PHIL, [C1,J1] propose a multi-rate discrete-time formulation of the PHIL closed-loop transfer function, which reproduces the phase more accurately than single-rate or continuous models.

Recent contributions have extended PHIL applications to power converters as HoI, focusing on improving both feasibility and stability. When high-power devices must be emulated with lower-rated hardware, [46] supplies a physics-informed scaling based on capability curves to preserve fundamental behavior across all four quadrants, and [47] contributes a harmonic-invariant scaling so that spectral characteristics are retained, together making scaled PHIL testing more representative of full-scale converters. Learning-based control also appears in [48], where an adaptive dynamic programming reinforcement-learning interface policy is proposed to test uncertain inverter-based resources dynamics without detailed plant models. The work in [49] proposes a multirate co-simulation framework for large-scale PHIL applications. Additionally, [50] presents a novel power interface using a golden section search algorithm to relax impedance ratio constraints. [51] implements a Smith predictor to mitigate delay-induced instability in a classic PV-inverter PHIL. Interface robustness is explicitly addressed in [52], which modifies the ITM interface using an MIMO optimal controller that preserves fidelity across a wide range of uncertainties. Authors in [53] study RHP poles in PHIL with a grid-tied converter using DQ impedance modeling and link their emergence to PLL dynamics. Lastly, for smart transformers, [54] enhances the C-ITM by incorporating a PR controller in the interface section, thereby improving stability and fidelity. Building on delay compensation, [55] shows a (damped) Smith predictor stabilizing positive- and negative-feedback PHIL interfaces; [56] presents an adaptive Smith predictor that uses online impedance identification to maintain robustness as the plant varies. Rather than a conventional LPF in the current feedback, [57] proposes a stabilizing digital filter directly derived from the frequency scan, providing guaranteed closed-loop stability under uncertainty. To improve stability, bandwidth, synchronization, and power-transfer fidelity, [58] also enhances phase-shift and gain-skew compensation at the interface. Authors in [37] demonstrate that PHIL loop delays are variable, and propose a methodology to characterize PHIL delays to improve stability precision. The idea of multi-rate partitioning of PHIL is also used in [59], which compares it with other methods, e.g., Hardware Inductance Addition (HIA), feedback current filtering (FCF), and partial shifting impedance (PSI), to improve bandwidth and enhance stability. A NelderMead auto-tuning approach is similarly examined in [60]. However, the impact of the controller on the HoI side for testing a grid-converter is not investigated. A different approach is taken in [61], which virtually shifts software impedance toward hardware through command shaping, improving stability and extending high-fidelity operation without additional components. In [62], an optimal PHIL interface design method is presented that synthesizes optimal controllers without iteration, explicitly

Table 2.3: Interface Algorithms Investigated in PHIL Literature

Reference(s)	Interface Algorithm				
	ITM	PCD	DIM	TFA	TLM
[26]	✓	✓	✓	✓	✓
[40–42]	✗	✗	✓	✗	✗
[55]	✓	✓	✗	✗	✗
[67]	✗	✗	✗	✗	✓
[27, 37, 43, 51–54, 56–59, 61, 62, 64, 66, 68, C1–C4, J1, J2]	✓	✗	✗	✗	✗

increases bandwidth, and defines metrics to measure absolute accuracy in real time. Adding an external inductor is proposed to interface the EM and GFM as HoI in [63], using C-ITM, while [64] examines both ITMs, extending the concept to GFM black-start testing with attention to timing and angle synchronization and delay compensation.

Authors in [J2] embed converter-controller dynamics in the PHIL loop and represent its impact on both stability and accuracy of PHIL with respect to the real coupling. Similar to converter versus grid output impedance-based stability analysis, the impedance models of GFL converter as HoI and EM are derived to analyze PHIL stability in [C2]. In addition to modeling the EM and converter output impedance, measurements at the PCC are performed to verify the accuracy of the impedance model. [C4] shows how the controller of a DC/AC converter alters the apparent source impedance, resulting in errors when using Nyquist with impedance-based criterion. A Kalman filter for online estimation of equivalent grid impedance interacting with a grid-tied inverter is addressed in [65]. For impedance measurement, [66] introduces a time-domain MIMO identification procedure that extracts dq -impedances in a single cycle and corrects errors due to nonzero grid impedance. [67] designs an optimal filter to emulate transmission-line impedance robustly under delay/uncertainty. [C3] studies the impact of sensor placement on PHIL stability with a GFL converter as HoI. An approach for PHIL stability analysis is formulated in [68] using Padé approximation to model delays.

2.5 Experimental Setups

In this thesis, several simulations are conducted to verify the introduced modeling approaches. For further verification, simulations are replaced with experimental results obtained primarily using two PHIL setups in the Energy Lab at Karlsruhe Institute of Technology (KIT). First,

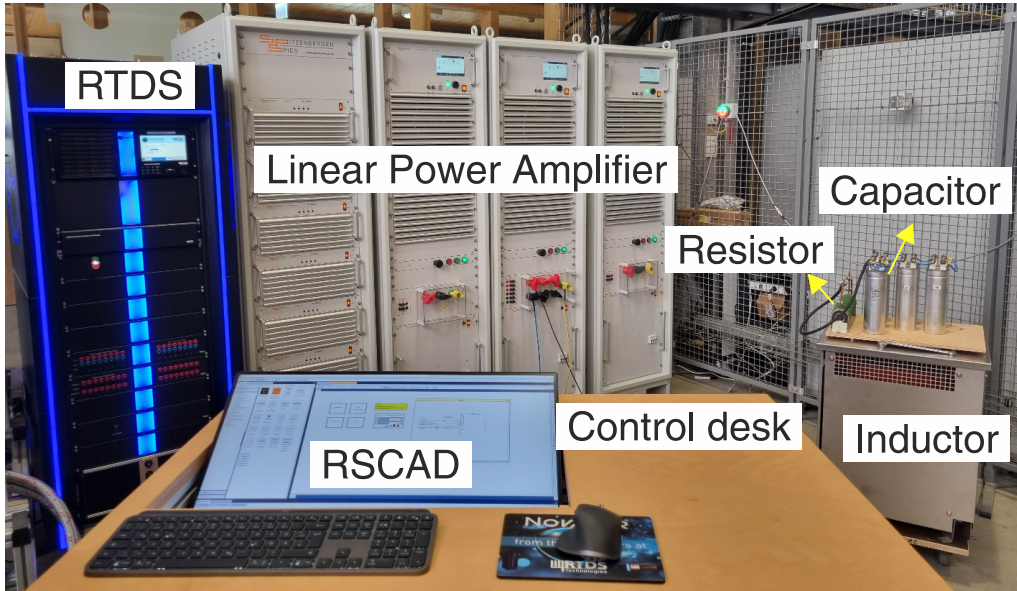


Figure 2.17: PHIL setup I for passive load testing at the Energy Lab, KIT

information about the used DRTS and PA is provided, as they are similar across both setups, and then the different HoIs used in each setup.

2.5.1 Digital Real-Time Simulator: NovaCor from RTDS

In this thesis, for the PHIL setups used, a DRTS manufactured by RTDS Technologies is employed. An overview of the key hardware-related characteristics of the simulator is provided in Table 2.4. The simulator provides multiple CPU cores, which determine the simulation's maximum computational performance based on the network model's size and complexity. The grid model and LPF are implemented in RSCAD for compilation on NovaCor. The bilinear (trapezoidal) method is used in RSCAD to discretize the first-order LPF [69]. The Small Form-factor Pluggable (SFP) connectors are replaced with D/A and A/D converters, enabling faster communication among NovaCor and PA.

Table 2.4: DRTS used for experimental setups

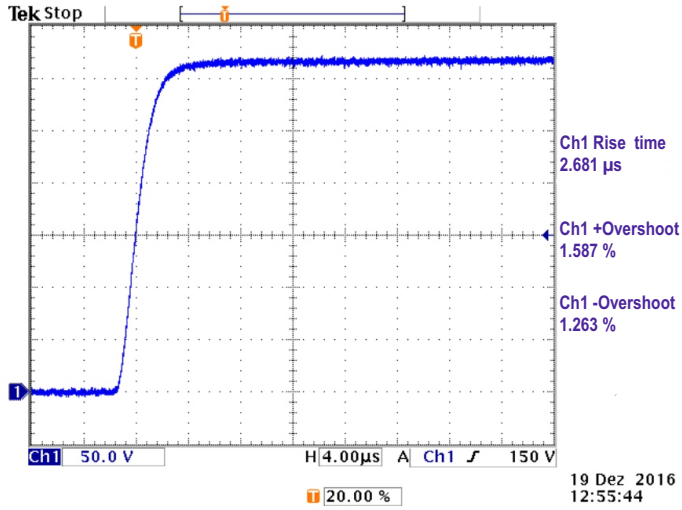
Simulator	NovaCor
Manufacturer	RTDS
Simulation Software	RSCAD FX1.2
CPU Cores ^{a)}	up to 10 cores
CPU Clock	3.5 GHz
CPU Type	IBM Power8
Analog Input Voltage	± 10 V
Analog Output Voltage	± 10 V
Input Voltage Resolution	$304 \mu\text{V}$
Output Voltage Resolution	$304 \mu\text{V}$
Isolation	Galvanically isolated
Data Acquisition ^{b)}	Continuous

a) Depending on the simulator configuration and licensed cores.

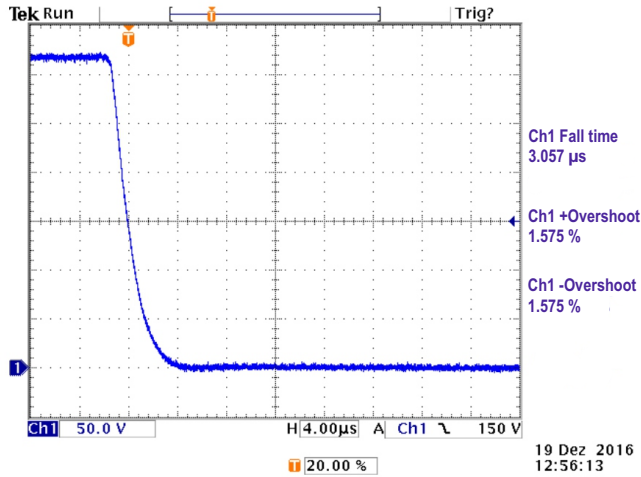
b) Up to 96 channels at $10 \mu\text{s}$.

2.5.2 Linear Power Amplifier: APS 15000 from Spitzenberger & Spies

The kVA APS 15000 4-quadrant amplifiers from Spitzenberger & Spies are used to provide the desired power to the supply HoI. 4-quadrant means that the amplifier supports bidirectional voltage and current, therefore, bidirectional power flow: source and sink operation. It provides a continuous output capability of 15 kVA in AC operation (single phase) and 15 kW in DC operation, with an increased continuous rating of 22.5 kVA/kW for approximately one hour, and a peak current capability of 616 A (p). With respect to dynamic performance, the amplifier offers a large-signal bandwidth from DC to 10 kHz (-3 dB) and a small-signal bandwidth (10%) up to 50 kHz (-3 dB). The specified slew rate exceeds $52 \text{ V}/\mu\text{s}$ (rise time $< 5 \mu\text{s}$ at 230 V (rms)), and the input-to-output delay is around $4.1 \mu\text{s}$ when fiber optic communication is used. These characteristics directly affect the achievable stability margins and the accuracy of fast transient reproduction in the PHIL loop. Therefore, the amplifier's dynamic characteristics are shown via step responses in Fig. 2.18a and Fig. 2.18b, taken from the manufacturer's data sheet. Also, except in Chapter 4, for the rest of the thesis, the transfer function and the delay of the amplifier are considered in the PHIL dynamics.



(a) Step up response from the amplifier



(b) Step down response from the amplifier

Figure 2.18: Step response of the linear amplifier taken from Spitzenberger & Spies user manual [36]

2.5.3 PHIL Setup I, Hol: Passive Loads

The DRTS and PA described above are used with a passive load to arrange a PHIL setup. The employed passive loads comprise an inductor, REO, 8 mH/111A, NPT-LD 100-111-8-150000;

a resistor, TE1000B1R0J; and 6 capacitors, KOMET C's 1,7kV / 47 uF, in series. For low-voltage/current operation, the resistor's temperature does not significantly affect its resistivity. However, as shown in Table 2.5, the inductance and internal resistance of the employed REO inductor vary with frequency, whereas the employed resistors and capacitors remain relatively constant over the 50-1000 Hz range. These values are measured with the R&S@HM8118 LCR-Messbrücken/-Messer LC meter. To verify the measurement accuracy of the data in Table 2.5, the impedance of the REO inductor at each frequency is calculated using a Meatest M-142 multi-function generator as a current source and measuring the inductor voltage, showing a good match between the datasheet data and the experimental results. Based on these measurements, $L(f)$ and $r(f)$ are defined in (2.23) as functions of frequency to estimate actual values in other frequencies than those given in the table.

$$L(f) = (5.9291e - 10) \cdot f^3 - (9.7235e - 07) \cdot f^2 - 0.00046659 \cdot f + 8.0371 \quad (2.23)$$

$$r(f) = (3.7209e - 12) \cdot f^4 - (1.2197e - 08) \cdot f^3 + (1.4196e - 05) \cdot f^2 - (0.00028625) \cdot f + 0.11441 \quad (2.24)$$

where f is the frequency, and the coefficients are the results of interpolation in a way that, for example, for the frequency of 750 Hz, the L and r are equal to the values given in Table 2.5, 7.3910 mH and 3.917 Ω , respectively.

2.5.4 PHIL Setup II, HoI: Grid Converter

In Fig. 2.19, another PHIL setup is arranged, with an active HoI, i.e., a three-phase grid-connected converter. The main hardware building blocks used to implement this HoI are given next.

2.5.4.1 Power Rack: Imperix PEB 8038 SiC Power Modules

The converter power stage was implemented using Imperix PEB 8038 half-bridge power modules. Each module integrates two 1200 V SiC MOSFETs, an embedded DC-bus capacitor bank (500 μ F @ 800 V), embedded protection functions (over-voltage/current/temperature), and galvanically-isolated onboard sensors for DC-bus voltage and AC-side current measurement. The module is specified for a nominal DC-bus voltage of 800 V (up to 850 V in the ratings table), with a maximum continuous leg current of 38 A_{RMS} at 20 kHz (and a switching frequency up to 50 kHz, indicated as a typical capability range). Direct access to the gating is provided via 650 nm optical

Table 2.5: Used REO inductor's frequency sensitivity

Frequency (Hz)	L (mH)	r (Ω)
50	8.0100	0.1288
60	8.0027	0.1436
75	7.9920	0.1686
100	7.9976	0.2195
120	7.9636	0.2687
150	7.9450	0.3559
180	7.9241	0.4598
200	7.9095	0.5368
250	7.8702	0.7355
300	7.8270	1.0080
360	7.7716	1.3455
400	7.7328	1.5870
450	7.6830	1.9020
500	7.6330	2.2300
600	7.5331	2.9020
720	7.4180	3.7160
750	7.3910	3.9170
800	7.3470	4.2500
900	7.2640	4.9030
1000	7.1890	5.5500

fiber inputs, enabling robust EMI performance in a laboratory environment. For safe switching operation, the manufacturer recommends a dead time of 400–500 ns [70].

2.5.4.2 Output Filtering: Passive Rack

To interface the converter with external loads/grids and to shape switching harmonics, an Imperix passive filter rack was used. The rack provides reconfigurable passive components accessible via 4 mm safety terminals and can be used in either three-phase AC or DC/DC configurations. It includes six power inductors (nominally 2.2 mH, rated 32 A) and two EMC filter sections with star-connected capacitors, with an effective output filter capacitance of approximately 10 μ F and a damping resistance of 1 Ω (per side). The main power circuits are specified for three-phase

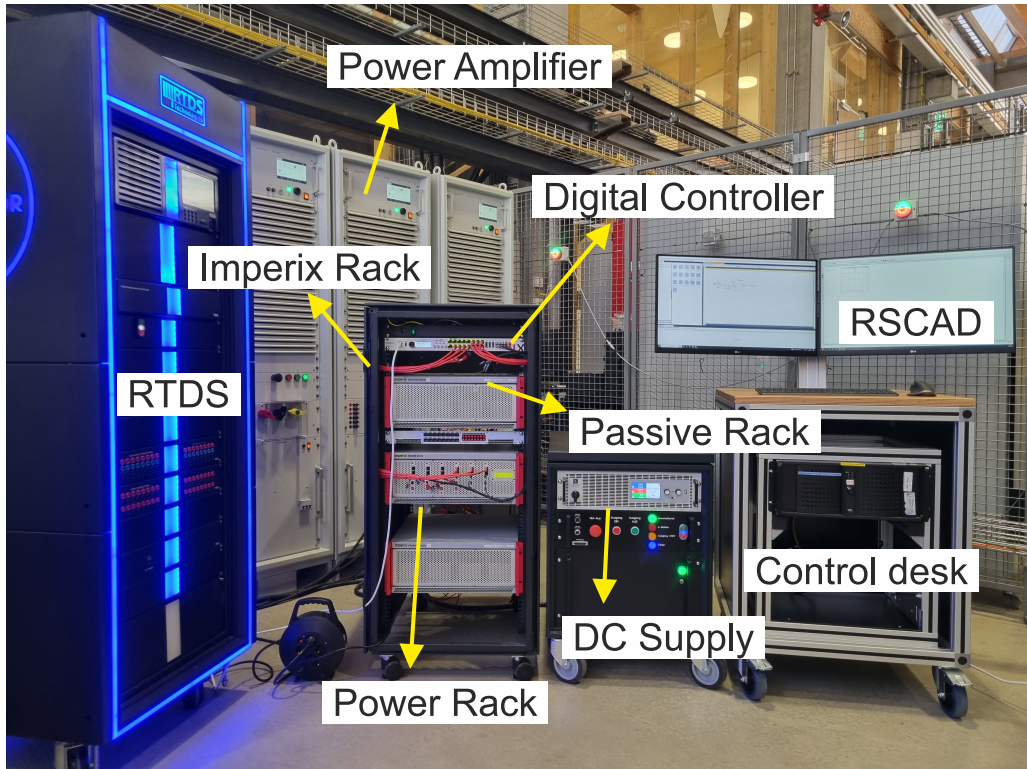


Figure 2.19: PHIL setup II with the Imperix grid converters at the Energy KIT

line-to-line voltages up to 520 V (RMS), currents up to 30 A (RMS) with EMC filtering, and 32 A (RMS) without EMC filtering [70].

2.5.4.3 Digital Controller: Imperix B-Box RCP

The converter control and modulation were executed on an Imperix B-Box RCP rapid control prototyping platform. The B-Box provides high-speed PWM generation (including optical PWM outputs) and a programmable analog front-end for measurement acquisition. The analog input stage offers 16 channels with a differential input range of ± 10 V and a large-signal bandwidth of approximately 410 kHz (without filtering). The ADC subsystem is 16-bit, supports simultaneous sampling, and operates at sampling rates up to 500 ksp/s. For timing-critical gating, the optical PWM outputs exhibit sub-20-ns-scale lane-to-lane delay asymmetry and low relative jitter (on the order of a few ns). The platform also provides programmable protection thresholds that can block PWM within about $1.6 \mu\text{s}$ after a threshold crossing [70].

2.5.4.4 Sensors

Accurate voltage and current measurements are essential for closed-loop control, stability investigations, and experimental validation within the PHIL setup. In this work, Imperix ModuLink sensors are employed for voltage and current acquisition. These sensors provide galvanic isolation, high measurement bandwidth, and balanced full-differential outputs compatible with the BoomBox control platform.

2.5.4.4.1 ModuLink ± 800 V Isolated Voltage Sensor

The ModuLink ± 800 V isolated voltage sensor is used for voltage measurements in the PHIL setup. It provides an optimized measurement range of ± 810 V and a full-scale input voltage range of ± 1.0 kV. The sensor has a nominal sensitivity of 2.46 mV/V and produces a balanced full-differential output signal. Its measurement bandwidth is between 60 kHz and 100 kHz, with a typical settling time of 5.3 μ s and a maximum settling time of 9.9 μ s. The typical uncalibrated sensitivity error is $\pm 0.15\%$, and the input-referred offset is typically ± 0.7 V. The sensor provides a permanent working isolation voltage of 1.2 kV_{peak} and an input impedance of approximately 8 M Ω . Therefore, it is suitable for DC-link and grid-voltage measurements in the PHIL test bench.

2.5.4.4.2 ModuLink ± 50 A Isolated Current Sensor

Current measurements are performed using the ModuLink ± 50 A isolated current sensor. The sensor provides a nominal peak current range of ± 50 A and a nominal rms current range of ± 35 A, while its linear input current range extends up to ± 110 A. It has a nominal sensitivity of 99.0 mV/A and provides a balanced full-differential output signal. The measurement bandwidth is at least 200 kHz, and the settling time is up to 2.0 μ s. The typical uncalibrated sensitivity error is $\pm 0.45\%$, and the typical input-referred offset is ± 0.05 A. The sensor provides a permanent galvanic isolation of 1.0 kV_{peak} and has an input impedance of approximately 2.1 m Ω . Therefore, it is suitable for current control, transient analysis, and impedance measurements in the PHIL setup.

2.5.4.4.3 Integration with the control platform

All sensors provide a differential analog output and are supplied with ± 15 V through an RJ45 connector. They include an embedded EEPROM accessible via a 1-wire link, which enables

auto-identification and the use of stored calibration parameters (offset and sensitivity) by the Imperix B-Box controller. This plug-and-play integration improves measurement accuracy and repeatability during experimental evaluation.

2.5.4.5 DC Supply: EA Elektro-Automatik PSI 91500-30

The DC link was supplied by a programmable EA Elektro-Automatik PSI 91500-30 DC power supply (PSI 9000 3U series). This unit provides a rated output voltage range of 0-1500 V and a rated current of 0-30 A, corresponding to a maximum output power of 15 kW. According to the manufacturer, the output voltage regulation time (10-100% load step) is below 2 ms. The specified output ripple for the PSI 91500-30 is below 2400 mV (PP) and 400 mV (RMS). The supply includes protective functions (OVP/OCP/OPP/OTP) and a discharge circuit for models with nominal voltage ≥ 200 V, discharging the output to below 60 V within 10 s after DC output shutdown under no/low-load conditions. A galvanically-isolated analog interface is available (selectable 0–10 V or 0–5 V ranges for programming/monitoring), and true master–slave operation is supported up to 36 units. The datasheet reports an efficiency of approximately 95% for the PSI 91500-30 [71].

2.6 Summary

In this chapter, first, the main PHIL interfaces used in this thesis are briefly introduced; then, via their transfer functions, their impact on the stability and accuracy of PHIL output, compared with the real coupling results, is examined. It has been shown that interface effects can be summarized in two: delays that affect the phase spectrum and bandwidth that affects both gain and phase. Classical interface algorithms are implemented in Simulink/MATLAB, and their frequency responses are compared under a single set of parameters. The State-of-the-Art of PHIL is presented, and lastly, the selected experimental setups for the verifications done later are introduced.

3 Power Hardware-in-the-Loop Modeling Domain

As mentioned in Chapter 2, PHIL systems comprising a digital simulator and physical hardware are a hybrid digital-analog setup. Due to its hybrid nature, accurately modeling the PHIL system and choosing an appropriate time domain, i.e., Continuous-Time (CT) or Discrete-Time (DT), can be challenging. CT-based modeling has been widely adopted in literature [26, 54, 59, 72] due to its simplicity and stability analysis tools, whereas other works [73, 74] demonstrated that the CT domain for stability assessment is not reliable since numerical discretization and holding effects of the real setup can be captured better in the discrete domain. Also, delays are less accurately represented (e.g., via Padé approximations) in continuous systems, potentially degrading model accuracy, especially at high frequencies. Several discretization techniques, i.e., step-invariant (also known as zero-order-hold), ramp-invariant (first-order-hold), adaptive discretization based on input in [75], and trapezoidal approximation (bilinear method) in [73] are used to discretize the CT transfer functions. However, the sampling time in the Single-rate Discrete (SDT), where the simulator time-step is used as the discretization time for the analysis, may fail to accurately represent the analog HoI. In other words, to address the dual nature of the PHIL, a possible solution is to treat the CT part in the discrete-time domain with a relatively small sampling time, building the model in a Multi-rate Discrete-Time domain (MDT). MDT is employed and developed to enhance stability by using a relatively small time step at the hardware-software intersection in [76]. The same concept can be applied to enhance the accuracy of PHIL systems modeling.

In this chapter, the proposed MDT modeling approach is developed and compared with conventional CT and SDT models, with the comparison conducted quantitatively using the introduced accuracy indices. The chapter also provides experimental validation of the MDT modeling approach using an RTDS-based PHIL with a linear amplifier across two test cases, an RL load and an RLC load, to evaluate its accuracy in practice. In addition, the measurement uncertainty is assessed, and the results are used to confirm the reliability of the experimental accuracy analysis. It is important to clarify that, throughout this chapter, the accuracy of the PHIL system does not refer to the accuracy of the PHIL with respect to the natural coupling shown in Fig. 3.1(a), but rather to the modeling of the PHIL system's configuration shown in Fig. 3.1(b). Next, the modeling approach for the selected PHIL section is presented using transfer functions. However,

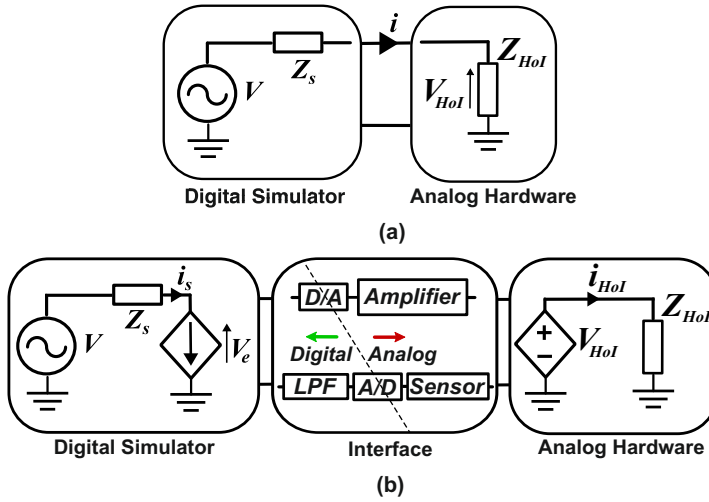


Figure 3.1: Generic scheme of PHIL: (a) Real coupling, (b) An existing PHIL scheme: a partly digital, partly analog system

as in this chapter, both continuous (s) and discrete (z) transfer functions are used, the arguments of the transfer functions are kept for better clarification.

3.1 PHIL Modeling Approach

The voltage-type ideal transformer method (V-ITM) shown in Fig. 3.1(b) is selected as the interface algorithm. In the V-ITM, the amplifier applies the voltage to the HoI (V_{HoI}), and the current (i_{HoI}) is fed back through the sensor. This section focuses on obtaining the closed-loop transfer function of each CT, SDT, and MDT model. The equivalent block diagrams for each are shown in Fig. 3.2, Fig. 3.3, and Fig. 3.4, respectively. Two different sampling times are chosen for the software and hardware sides of the PHIL system in the MDT method. The primary time step (T_{s1}) is assigned to the software side of the PHIL, and the secondary time step (T_{s2}), closer to the CT domain, represents the hardware side. The Thévenin model with an RL impedance is chosen as the simulated grid, and RL and RLC impedances are employed as HoI in two different case studies. Delays in the A/D and D/A conversions, sensors, and the DRTS are considered, in addition to the PA and LPF dynamics.

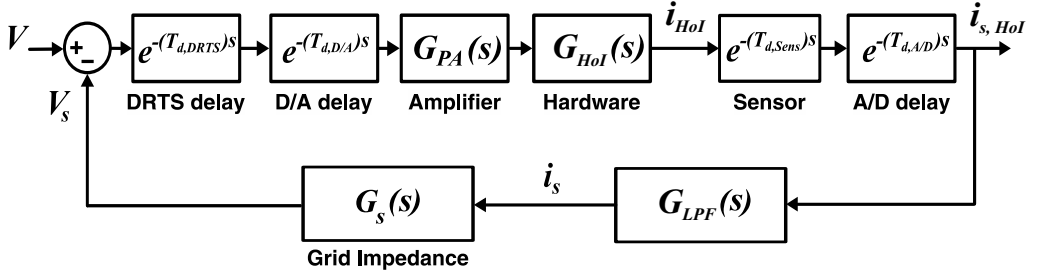


Figure 3.2: Continuous-time modeling block diagram

3.1.1 Continuous-Time Modeling

According to Fig. 3.2, the closed-loop transfer function of the system, $G_{cl}(s)$, implies the loop admittance driven by the measured current in DRTS, $i_{s, HoI}$, over the input voltage v . The transfer function of each unit to attain $G_{cl}(s)$ is defined in the following equations:

$$G_{cl}(s) = G_{fw}(s) / (1 + G_{fb}(s) \cdot G_{fw}(s)) \quad (3.1)$$

where $G_{fb}(s)$ is the feedback transfer function and $G_{fw}(s)$ is the transfer function of the forward path from input to $i_{s, HoI}$. $G_{fw}(s)$ is defined by the following relation:

$$G_{fw}(s) = G_{PA}(s) \cdot G_{HoI}(s) \cdot e^{-(T_{dT})s} \quad (3.2)$$

where:

$$G_{PA}(s) = e^{-(T_{d, Amp})s} / ((1/\omega_0)s^2 + (2D/\omega_0)s + 1) \quad (3.3)$$

$$G_{HoI}(s) = 1/Z_{HoI}(s) \quad (3.4)$$

$$T_{dT} = T_{d, DRTS} + T_{d, D/A} + T_{d, Sens} + T_{d, A/D} \quad (3.5)$$

The transfer function of the linear power amplifier, $G_{PA}(s)$, consists of a resonant frequency ω_0 and a damping factor D [36]. T_{dT} is the whole loop delay and $T_{d, DRTS}$, $T_{d, D/A}$, $T_{d, A/D}$, $T_{d, Sensor}$, and $T_{d, Amp}$ are delays introduced by the DRTS, A/D and D/A conversions, sensor measurements, and the power amplifier respectively. The impedance of the hardware, $Z_{HoI}(s)$, for the RL and RLC cases are respectively:

$$Z_{HoI, RL}(s) = R_{HoI} + L_{HoI}s \quad (3.6)$$

$$Z_{HoI, RLC}(s) = Z_{HoI, RL}(s) + 1/(C_{HoI}s) \quad (3.7)$$

Accordingly, $G_{fb}(s)$ in (3.8) contains the $G_s(s)$ as the simulated grid impedance, and $G_{LPF}(s)$ as LPF with ω_c as cut-off frequency:

$$G_{fb}(s) = G_{LPF}(s) \cdot G_s(s) \quad (3.8)$$

$$G_{LPF}(s) = \omega_c / (s + \omega_c) \quad (3.9)$$

$$G_s(s) = L_s \cdot s + R_s \quad (3.10)$$

3.1.2 Single-rate Discrete-Time Modeling

The step-invariant transformation, also known as the Zero-Order Hold (ZOH) discretization technique, has been chosen to model the holding effects originating from DRTS during the D/A conversion more accurately [74]. Fig. 3.3 represents the discretized model of the system. The ZOH transformation can be described analytically as follows:

$$G_{ZOH}(s) = (1 - e^{-(T_s)s})/s \quad (3.11)$$

Applying (3.11) to the derived $G_{fw}(s)$ from section 3.1.1 and performing the s to z mapping with the given sampling time, T_s , the $G_{fw,SDT}(z)$ becomes:

$$\begin{aligned} G_{fw,SDT}(z) &= Z\{G_{ZOH}(s) \cdot G_{fw}(s)\} \\ &= (1 - z^{-1})Z\{\mathcal{L}^{-1}\{G_{fw}(s)/s\}\}_{T_s} \end{aligned} \quad (3.12)$$

The term $(1 - e^{-sT_s})/s$ consists of two parts: the factor $1/s$ corresponds to the integration of a unit-step input, while the exponential term e^{-sT_s} represents a time delay of one sampling interval. The factor $(1 - z^{-1})$ appears due to the term $(1 - e^{-sT_s})$ in (3.11) after performing the s -to- z mapping, thereby accounting for the ZOH operation in discrete time. The division by s produces the Laplace-domain step response of $G_{fw}(s)$, and applying the inverse Laplace transform yields the corresponding time-domain step response. Sampling this response at T_s and applying the $Z\{\cdot\}$ transform gives its discrete representation.

It is to be noted that the DRTS delay is handled with ZOH transform, and the delay of the amplifier is considered with its transfer function in (3.3) and therefore the forward delay shown in (3.5) here is updated as:

$$T_{dT} = T_{d,D/A} + T_{d,Sens} + T_{d,A/D} \quad (3.13)$$

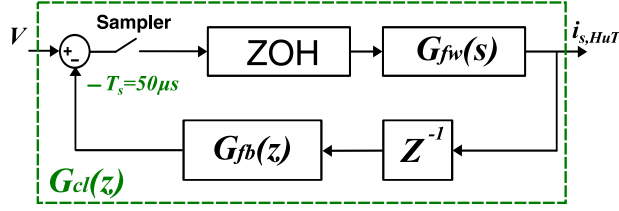


Figure 3.3: Single-rate discrete modeling block diagram

To avoid excessive modeling of the holding effect and to introduce unintentional additional unit delay, instead of the ZOH transform, the Bilinear Transform Method (BLT) is picked to transform the $G_{fb}(s)$ to its discrete counterpart. The approximate relation between s and z in the bilinear method is [77]:

$$s \approx 2(1 - z^{-1}) / (T_s(1 + z^{-1})) \quad (3.14)$$

Applying (3.14) to (3.8), the $G_{fb,SDT}(z)$ is obtained, but due to the complexity, the full representation is avoided here:

$$G_{fb,SDT}(z) = Z_{BLT}\{G_{fb}(s)\}_{T_s} \quad (3.15)$$

Therefore, the closed-loop SDT transfer function of the system, considering the sampling delay in the feedback, is achievable as:

$$G_{cl,SDT}(z) = \frac{G_{fw,SDT}(z)}{(1 + G_{fw,SDT}(z) \cdot G_{fb,SDT}(z)/z)} \quad (3.16)$$

3.1.3 Multi-rate Discrete-Time Modeling

In the MDT approach, the system is partitioned with two different sampling times. The sampling time of the section 3.1.2 is kept for the digital part of the setup but renamed as T_{s1} , and a smaller sampling time $T_{s2} \ll T_{s1}$ (blue line in Fig. 3.4) is assigned to the hardware section. The goal is to decouple the two system dynamics to represent the analog part of the circuit as an extremely fast-sampled DT model (e.g., up to 2-3 magnitude orders faster). Accurate modeling of delays minimizes transfer function phase errors and improves the overall model's accuracy. In the MDT modeling, it is possible to model delays that are smaller than T_{s1} , for example, with a sampling

time of $T_{s_2} \ll T_{s_1}$, and thus approximate the phase frequency dependency more accurately. Similarly, the closed-loop transfer function of the system in the z domain is attainable as follows:

$$G_{cl,MDT}(z) = G_{fw}(z)/(1 + G_{fw}(z) \cdot G_{fb}(z)) \quad (3.17)$$

where $G_{fb}(z)$ describes the feedback path and $G_{fw}(z)$ is the transfer function of the forward path from input to $i_{s,HoI}$. Due to the different sampling rates, two rate transition blocks, shown in yellow in Fig. 3.4 are added. According to the definition of the rate transition block, the slow-to-fast block acts as a unit delay (in this case, it represents the DRTS delay), and the fast-to-slow block acts as the ZOH of the A/D sampling. In the forward path, transfer functions with T_{s_2} sampling time are multiplied as follows:

$$G_{fw,T_{s_2}}(z) = G_{PA}(z) \cdot G_{HoI}(z) \cdot z^{-(T_{dT}/T_{s_2})} \quad (3.18)$$

The same approach as explained for $G_{fb}(z)$ in section 3.1.2, BLT is used here to obtain the discrete transfer functions of the power amplifier and HoI:

$$G_{PA}(z) = Z_{BLT}\{G_{PA}(s)\}_{T_{s_2}} \quad (3.19)$$

$$G_{HoI}(z) = Z_{BLT}\{G_{HoI}(s)\}_{T_{s_2}} \quad (3.20)$$

The sampling time of the transfer function $G_{fw,T_{s_2}}(z)$ is yet to be transitioned to T_{s_1} , so the forward path from input to $i_{s,HoI}$ is completed. As discussed above, the rate transition block, acting as a ZOH, handles fast-to-slow rate differences. However, instead of direct resampling of $G_{fw,T_{s_2}}(z)$ to $G_{fw,T_{s_1}}(z)$, which causes losing excessive information, $G_{fw,T_{s_1}}(z)$ is achieved in two stages:

1. $G_{fw,T_{s_2}}(z)$ is transformed back to continuous using bilinear transform using:

$$z = e^{sT_{s_2}} \approx (1 + sT_{s_2}/2)/(1 - sT_{s_2}/2) \quad (3.21)$$

and:

$$G_{FW}(s) = Z_{BLT}^{-1}\{G_{fw,T_{s_2}}(z)\} \quad (3.22)$$

Where Z_{BLT}^{-1} represents the discrete-to-continuous transformation.

2. Then $G_{FW}(s)$ is sampled with T_{s_1} using ZOH. Similar to 3.12:

$$G_{fw,T_{s_1}}(z) = (1 - z^{-1})Z\{\mathcal{L}^{-1}\{G_{FW}(s)/s\}\}_{T_{s_1}} \quad (3.23)$$

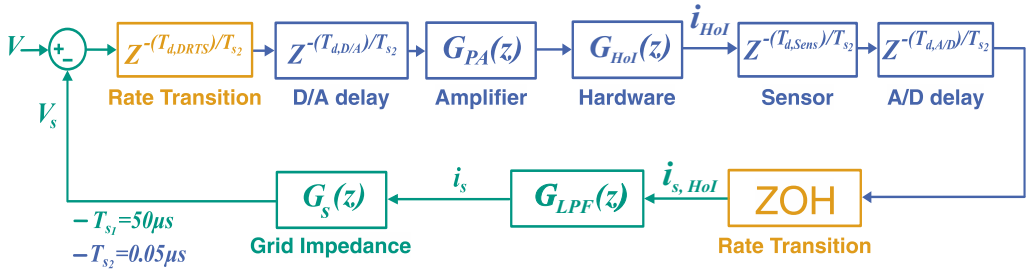


Figure 3.4: Multi-rate discrete modeling block diagram

Since the calculated $G_{fw,T_{s1}}(z)$ has the same sampling time as $G_{fb}(z)$, (3.17) is now resolvable. Following is the calculation of $G_{fb}(z)$ using the bilinear method to achieve the discrete transfer functions of the LPF and equivalent grid shown as $G_{LPF}(z)$ and $G_s(z)$, respectively:

$$G_{fb}(z) = G_{LPF}(z) \cdot G_s(z) \quad (3.24)$$

$$G_{LPF}(z) = \frac{\omega_c}{\left(\frac{2}{T_{s1}}\right) \left(\frac{1-z^{-1}}{1+z^{-1}}\right) + \omega_c} \quad (3.25)$$

$$G_s(z) = \frac{2 \cdot L_s}{T_{s1}} \frac{1-z^{-1}}{1+z^{-1}} + R_s \quad (3.26)$$

3.2 Definition of Accuracy

Based on the calculated closed-loop transfer functions in the previous section, the accuracy of a PHIL system model can be defined as the proximity of the models gain and phase values to a reference value (e.g., a benchmark model or experimental results) at each frequency [59]. The relative percentage error is measured at each frequency, and the mean of all measured errors has been employed for accuracy comparison purposes:

$$AVG_{gain} = \sum_{i=1}^N \frac{|G_{ref}(j\omega)| - |G_{model}(j\omega)|}{|G_{ref}(j\omega)|} \cdot 100 \quad (3.27)$$

$$AVG_{phase} = \sum_{i=1}^N \frac{\angle G_{ref}(j\omega) - \angle G_{model}(j\omega)}{\angle G_{ref}(j\omega)} \cdot 100 \quad (3.28)$$

where $|G_{ref}|$, and $\angle G_{ref}$ are the gain and phase of the closed-loop reference, which is the simulated MDT system in MATLAB/Simulink in the section 3.3 and experimental measurements

in section 3.4. G_{model} implies the closed-loop transfer function of the calculated CT, SDT, and proposed MDT model. Following the same procedure in [C1], the weighted average error is defined as:

$$WAVG_{gain} = \sqrt{\sum_{i=1}^N \frac{|\frac{1}{f_i} (|G_{ref}(j\omega)| - |G_{model}(j\omega)|)|^2}{|G_{ref}(j\omega)|^2}} \cdot 100 \quad (3.29)$$

$$WAVG_{phase} = \sqrt{\sum_{i=1}^N \frac{|\frac{1}{f_i} (\angle G_{ref}(j\omega) - \angle G_{model}(j\omega))|^2}{|\angle G_{ref}(j\omega)|^2}} \cdot 100 \quad (3.30)$$

In the following section, the G_{ref} is chosen to be the MDT closed-loop implemented in Simulink, and the validity of the linearized MDT model is verified using the accuracy error indexes.

3.3 Simulation Results

The goal of this section is to verify the analytical modeling given in the section 3.1, specifically the formulated rate transition blocks, with the Simulink model. Furthermore, it gives an overall insight into the CT and SDT behaviors compared to MDT.

To validate the MDT model's accuracy, a comparison between the analytical model in section 3.1.3 and the Simulink simulation has been carried out. The reference is set to the implemented MDT V-ITM PHIL model in Simulink for two different HoI cases: an RL load and an RLC load, respectively. The reference model is implemented in Simulink as follows:

- All the delays are modeled as shown in Fig. 3.4.
- Series RL branches for grid impedance and series RL/RLC branches are used as HoI.
- G_{LPF} shown in Fig. 3.4 is implemented in the feedback using (22).
- Two rate transition blocks shown in Fig. 3.4 are implemented for changing the sampling time.
- For the transfer function of the amplifier (16) is employed.

Results of all three MDT, CT, and SDT methods shown in this section are modeled based on the equations represented in section 3.1. The bode diagram is then calculated using the three linearized modeling approaches and compared with the frequency-sweep results of the Simulink

Table 3.1: PHIL simulation parameter

Setup	Value	Unit	Setup	Value	Unit
$T_{s_1}, T_{d,DRTS}$	50	$[\mu s]$	T_{s_2}	0.05	$[\mu s]$
$T_{d,Amp}$	3.1	$[\mu s]$	$T_{d,Sens}$	0.8	$[\mu s]$
$T_{d,D/A}$	3	$[\mu s]$	$T_{d,A/D}$	2	$[\mu s]$
$\omega_c/2\pi$	2	$[kHz]$	C_{HoI}	7.5	$[\mu F]$
L_s	0.8	$[mH]$	L_{HoI}	8	$[mH]$
R_s	1	$[\Omega]$	R_{HoI}	1	$[\Omega]$
$\omega_0/2\pi$	180	$[kHz]$	D	0.9	—

Table 3.2: RL accuracy calculation based on simulations

Model	Index	Error(%)	Index	Error(%)
CT		0.4451		0.0055
SDT	AVG_{gain}	0.0039	$WAVG_{gain}$	0.0001
MDT		0.0039		0.0001
CT		4.2291		0.0391
SDT	AVG_{phase}	9.1196	$WAVG_{phase}$	0.0872
MDT		0.0399		0.0004

model over a frequency range of 50-1000 Hz, with a step of 50 Hz. The PHIL setup parameters are given in Table 3.1.

3.3.1 RL Load as Hol

This section validates the modeling of the PHIL with an RL load via simulation. According to Fig. 3.5 and its zoomed plot at 650 Hz (Fig. 3.6), the linearized MDT model provides a more accurate approximation of the Simulink model across the entire range compared to the other models. As the frequency increases, phase deviations in the CT and SDT models increase as well, whereas the MDT modeling follows the reference throughout the frequency spectrum. It can be seen that the CT and SDT models underestimate the phase values concerning the Simulink model. In addition to the bode diagrams, the accuracy is also calculated using the indexes formulated from (3.27) to (3.30), and compared in Table 3.2. As can be seen for the phase indexes, the MDT achieves relatively negligible errors, at least 2 orders of magnitude smaller than those of the other two modeling approaches, confirming the accuracy of the proposed MDT modeling approach.

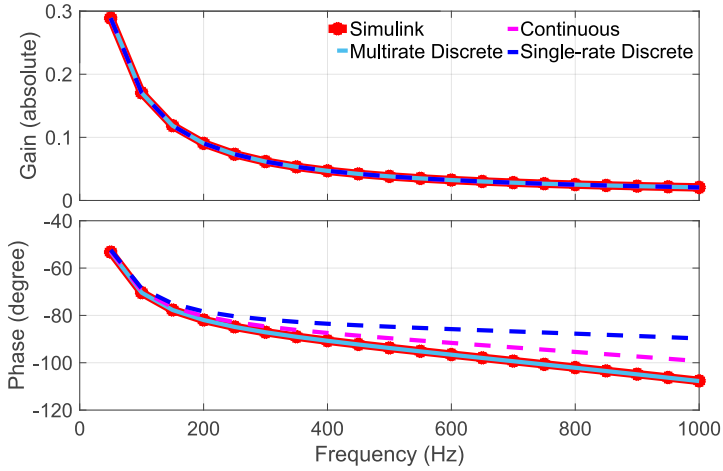


Figure 3.5: Frequency response comparison using RL as HoI

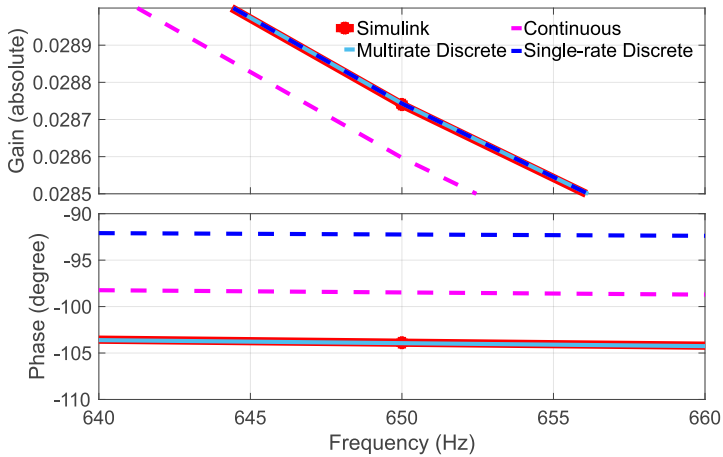


Figure 3.6: Zoomed frequency response using RL at 650 Hz

3.3.2 RLC Load as HoI

For further analysis of the accuracy of the MDT approach, the RLC load has also been examined as HoI. This testing is needed because the RLC load has a resonance frequency around 650 Hz, where modeling errors may be amplified. Diagrams in Fig. 3.7 demonstrate the frequency behavior of the PHIL system, where the spectrum range is divided into three main areas: smaller, around, and larger than the resonance frequency shown in 3.8, 3.9, and 3.10, respectively. In the analyzed frequency range, the MDT model overlaps with the simulator output. On the other

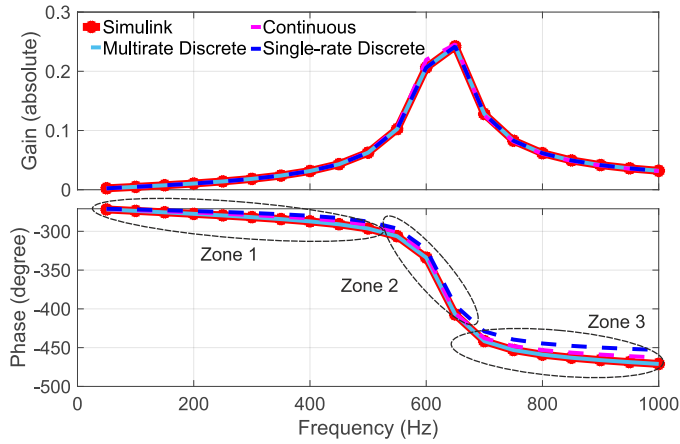


Figure 3.7: Frequency response comparison using RLC as HoI

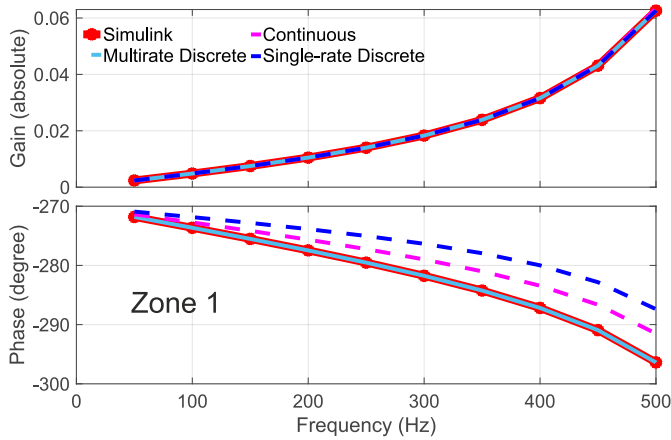


Figure 3.8: Frequency response using RLC as HoI, Zone 1

hand, the CT and SDT models diverge from the reference at frequencies both smaller and larger than the resonance frequency of the RLC testing system. Gain and phase graphs are shown at the resonance frequency in Fig. 3.11.

As with Bode diagrams, Table 3.3 assesses the accuracy of the described analytical MDT modeling. Both phase error indicators in the table demonstrate that the presented linear MDT is well formulated and reproduces behaviors similar to those of the MDT Simulink model.

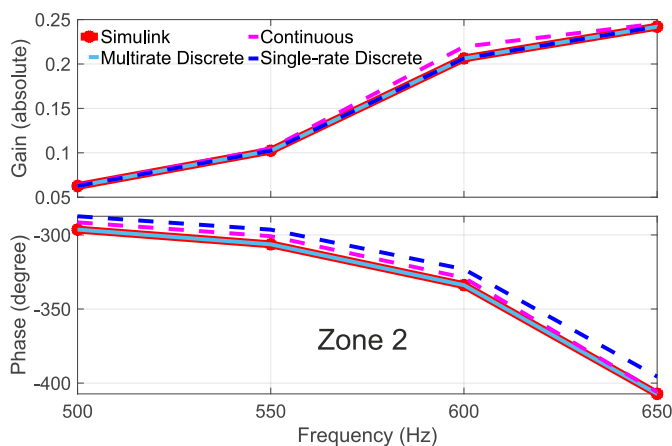


Figure 3.9: Frequency response using RLC as HoI, Zone 2

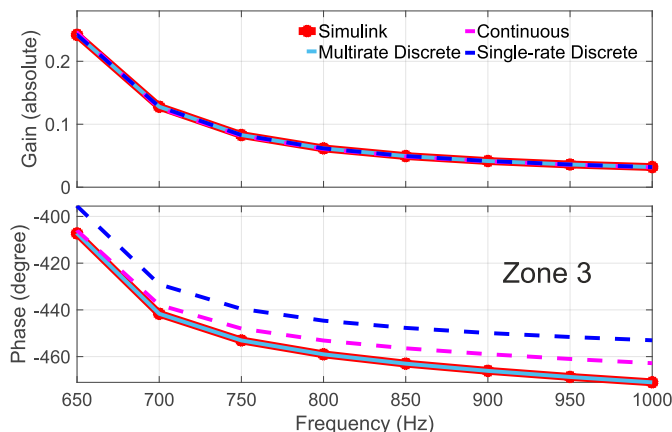


Figure 3.10: Frequency response using RLC as HoI, Zone 3

Table 3.3: RLC accuracy calculation based on simulations

Model	Index	Error(%)	Index	Error(%)
CT	AVG_{gain}	1.2297	$WAVG_{gain}$	0.0133
SDT		0.0033		3.28e-05
MDT		0.0045		4.02e-05
CT	AVG_{phase}	1.1097	$WAVG_{phase}$	0.0119
SDT		2.4933		0.0245
MDT		0.0013		1.31e-05

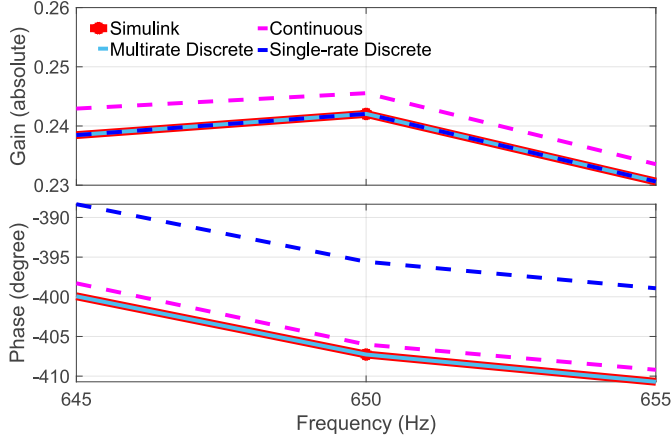


Figure 3.11: Zoomed frequency response using RLC as HoI

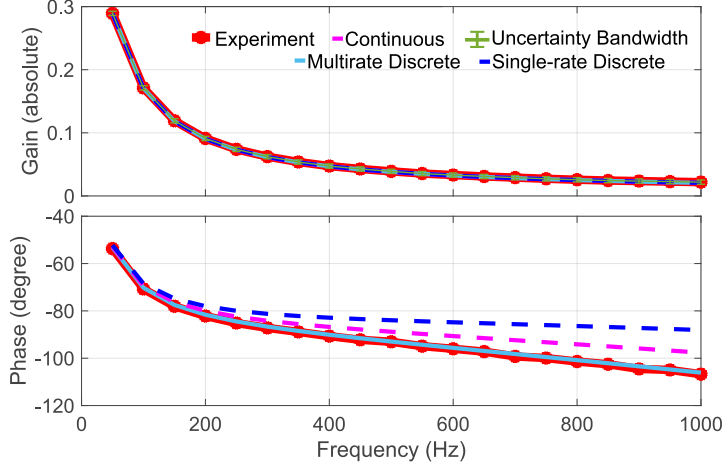


Figure 3.12: Frequency response comparison using RL as HoI

3.4 Experimental Results

The PHIL setup I described in section 2.5.3 is employed to verify the accuracy of the proposed modeling approach. Delays of A/D and D/A conversions can be considered negligible with respect to the DRTS time step (i.e., $50 \mu\text{s}$ due to the use of SFP connections). The remaining delays (e.g., amplifier, sensor) are treated as unitary, denoted by $T_{d,Conv}$. The parameter specifications for the experiment are provided in Table 3.5.

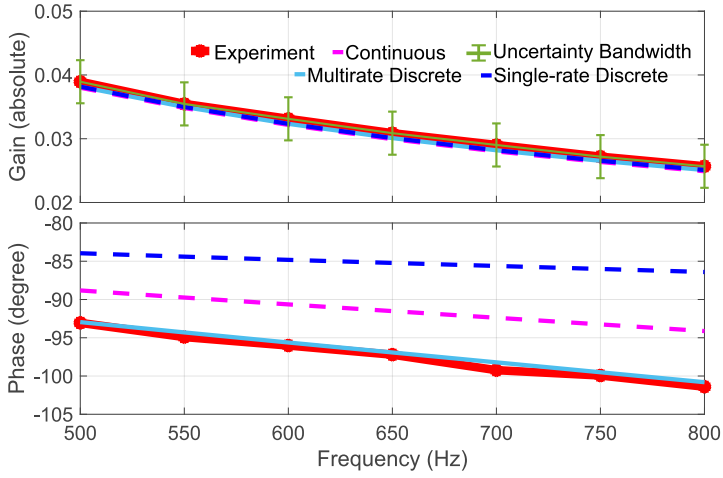


Figure 3.13: Zoomed frequency response using RL as HoI

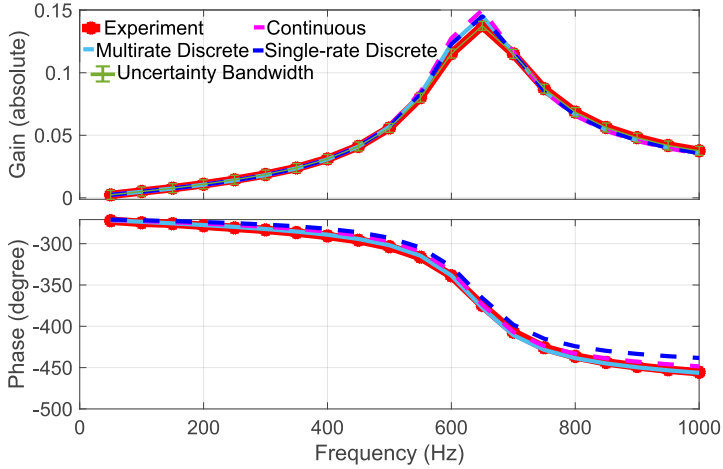


Figure 3.14: Frequency response comparison using RLC as HoI

3.4.1 Measurement Uncertainty

According to the uncertainty propagation of the used PA built-in current/voltage transducers, the uncertainty of magnitude measurements is given in Table 3.4.

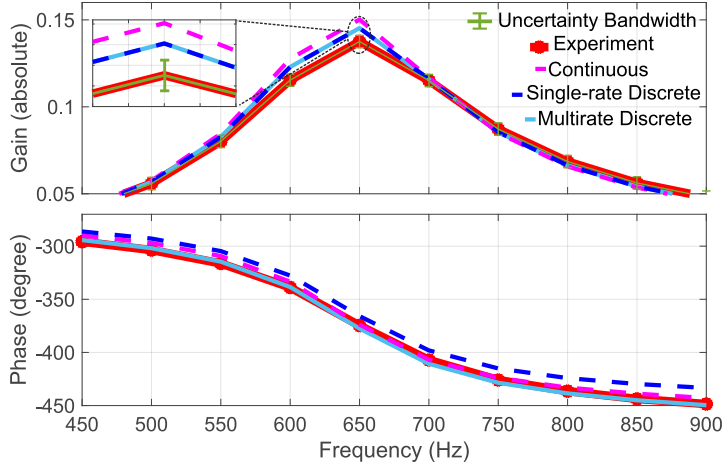


Figure 3.15: Zoomed frequency response using RLC as HoI

Table 3.4: Uncertainty of magnitude measurements [36]

Parameter	Range	Error	Unit
I (rms)	± 51	± 0.15	[A]
V (rms)	± 650	± 0.39	[V]

Then the uncertainty error of the gain measurements can be obtained as:

$$Y = I/V$$

$$dy = Y \cdot \sqrt{(di/I)^2 + (dv/V)^2} \quad (3.31)$$

where Y is the loop admittance gain and dy is the gain error propagated by current and voltage sensors' uncertainties, depicted as di and dv , respectively. As an example in the RL case, if a voltage equal to $V = 40$ V is applied at a frequency of 50 Hz, the current I results in 11.3 A, where the gain uncertainty, dy , is equal to ± 0.0034 S. Likewise, in the RLC case, I is approximately 0.01 A, and dy is calculated as ± 0.0035 S.

3.4.2 Accuracy Comparison

Similar to Section 3.3, the gain and phase of the loop admittance are obtained by measuring the amplitude and phase of the current at each frequency up to 1000 Hz with a 50 Hz step-size for the applied voltage. Results are shown in Fig. 3.12 - Fig. 3.15, where different models are compared

Table 3.5: PHIL experiment parameter

Setup	Value	Unit
V_s (rms)	40	[V]
$T_{s1}, T_{d,DRTS}$	50	[μ s]
$T_{d,Conv}$	4	[μ s]
f_c	2	[kHz]
C_{HoI}	7.5	[μ F]
L_s	0.8	[mH]
L_{HoI}	8	[mH]
R_s	1	[Ω]
R_{HoI}	1	[Ω]

with respect to the experimental reference. The experimental measurements shown in red color here are replaced with the simulated PHIL system response in the previous section. Uncertainty bandwidth is also added to the gain subplot. The phase subplots in Fig. 3.12 and Fig. 3.14 for both HoIs graphically reveal that the proposed MDT model is the most accurate relative to the reference among the studied models. More illustrative plots to judge gain measurements are shown in Fig. 3.13 and Fig. 3.15.

Analytical accuracy calculation results are given in Table 3.6 and Table 3.7. Beginning with Table 3.6, the smallest AVG_{gain} error among the considered approaches is equally achieved with SDT and MDT at 1.93%. However, all achieved AVG_{gain} errors can be considered acceptable since they are within the uncertainty error of $\pm 1.22\%$ ($dy = 0.0034$ S). Considering the phase accuracy with the $WAVG_{gain}$ index, MDT achieves the smallest weighted errors. The phase-related index reveals that MDT is around ten times more accurate in AVG_{phase} and at least 2.5 times better in $WAVG_{phase}$ than the other two methods, achieving the best phase match with the experimental response. This implies a better representation of the system delays, which is fundamental to estimating the stability of the PHIL system.

In Table 3.7, where the experiment has been repeated with the RLC load, the MDT shows errors lower than 1% in AVG_{phase} and 0.01% in that of $WAVG$. This proves a better phase accuracy of the MDT model with respect to the currently proposed models.

Therefore, considering the performed experimental accuracy investigations, the MDT approach shows higher accuracy for both examined HoIs.

Table 3.6: RL accuracy calculation based on experiments

Model	Index	Error (%)	Index	Error (%)
CT		2.4409		0.0215
SDT	AVG_{gain}	1.9349	$WAVG_{gain}$	0.0164
MDT		1.9349		0.0164
CT		5.0939		0.0576
SDT	AVG_{phase}	10.3394	$WAVG_{phase}$	0.1077
MDT		0.6033		0.0220

Table 3.7: RLC accuracy calculation based on experiments

Model	Index	Error (%)	Index	Error (%)
CT		3.7050		0.0612
SDT	AVG_{gain}	2.9292	$WAVG_{gain}$	0.0599
MDT		2.9295		0.0599
CT		1.2171		0.0177
SDT	AVG_{phase}	2.6379	$WAVG_{phase}$	0.0297
MDT		0.4030		0.0073

3.5 Summary

This chapter examines the accuracy of a V-ITM PHIL system modeling by testing RL and RLC loads as HoI. In addition to classical approaches, namely Continuous-Time (CT) and Single-rate Discrete-Time (SDT) modeling methods, a Multi-rate Discrete-Time (MDT) method is proposed. The MDT method uses a relatively short sampling time to model the analog hardware section of the setup and a larger time step for the real-time simulation. Accuracy is assessed using defined error indices based on the closed-loop transfer function, which describes the loop's admittance. The frequency response of the proposed linearized MDT model is verified with its MATLAB/Simulink model using Bode plots and error indices. To further validate the modeling approach, experimental results from a PHIL setup have been obtained, also accounting for the uncertainty bandwidth of the gain measurements. In both HoI cases, the proposed MDT model outperforms the primarily used CT and SDT models, achieving higher accuracy, particularly representing the system phase.

4 Grid Converter as an Hardware-of-Interest

As discussed in Chapter 2 in a typical PHIL setup, the DRTS imposes at least two time-step delays to emulate the grid, while interfaces such as sensors and power amplifiers (depending on their bandwidth) may introduce additional phase shifts. These phase shifts introduce inaccuracies relative to the real coupling and reduce stability margins. The primary objective of employing PHIL is to analyze the interaction between the HoI and the EM, which is often unknown before a PHIL experiment. The lack of prior knowledge of the HoI/EM interaction, along with delays introduced by system components and interfaces, threatens closed-loop stability and may lead to hardware damage. Therefore, ensuring setup stability during the preparatory phase of PHIL experiments is crucial to prevent hardware damage and ensure accurate results. It has been shown in Chapter 1, analyzing grid-connected inverters as HoI is increasingly common due to their wide-ranging applications [78] and [79]. However, several PHIL interface algorithms and stability enhancements described in Chapter 2 are either for passive load testing or consider only the converter's physical impedance, without accounting for the controller's impact. By varying the GFL's controller bandwidth, the power converter's equivalent transfer function changes, thereby shifting the stability boundaries of the PHIL setup. Such changes may also impact the PHIL's accuracy compared to the real coupling. However, in the literature, the HoI is not explicitly analyzed as a potential source of inaccuracy. Also, as noted in 2.4, most in-field studies focus on improving interface algorithms, with the ITM still widely used due to its simplicity. Those studies generally assess accuracy in the time domain or by comparing different interface algorithms rather than benchmarking against a real coupling. In this chapter, the stability and accuracy of the PHIL systems when a grid-converter is employed as HoI are analyzed using frequency responses and loop transfer functions. It analyzes the impact of the HoI's current controller bandwidth on both stability and accuracy, showing how HoI control dynamics influence PHIL performance beyond the interface sector.

The PHIL system chosen for the analysis is shown in Fig. 4.1. The MoI is represented by the Thévenin equivalent of the grid, while the HoI is a three-phase GFL converter with an LCL filter. A GFL converter synchronizes to the grid voltage (typically via a PLL) and regulates the injected

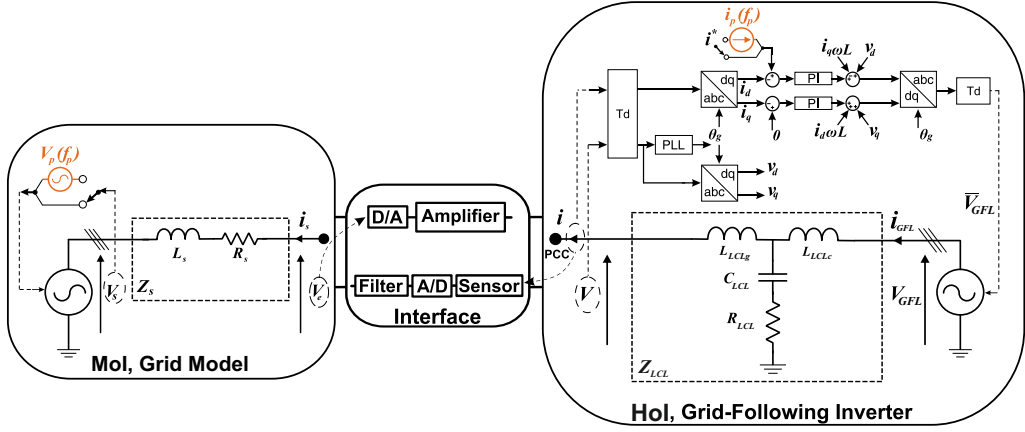


Figure 4.1: Power Hardware-in-the-Loop setup with 3 phase DC/AC converter as Hardware-of-Interest.

current. The accuracy is assessed by comparing the PHIL with the real coupling frequency responses, and stability is analyzed using pole-zero maps, first by modeling each component and then the entire PHIL via transfer functions in the discrete domain. Additionally, the obtained transfer functions are verified through simulation and experimental validation.

4.1 Mathematical Formulation of the Selected PHIL Setup

This section introduces a new approach to the mathematical modeling of the benchmark PHIL, namely the MoI interfaces and the GFL converter as HoI, and compares it with the real coupling case. The trapezoidal approximation (bilinear method) is used to discretize transfer functions. For simplicity, the argument (z) is removed from the transfer functions. In the following, the PHIL components are modeled.

4.1.1 Grid Model

The grid is represented as a Thévenin equivalent with a voltage source V_s and a line impedance Z_s :

$$Z_s = Z\{R_s + s \cdot L_s\} = R_s + \frac{2 \cdot L_s}{T_s} \cdot \frac{1 - z^{-1}}{1 + z^{-1}} \quad (4.1)$$

4.1.2 Converter Model

The transfer function of the system shown in Fig. 4.1 is illustrated in Fig. 4.2. The converter delay itself is shown as $T_{d_{PI}}$, and its transfer function is denoted T_d , which equals a one-time-step (50 μ s) delay in the discrete domain, denoted z^{-1} . The converter model is described mathematically as its ability to track the current setpoint, i/i^* :

$$\frac{i}{i^*} = \frac{G_{PI} \cdot Y \cdot z^{-1}}{1 + G_{PI} \cdot Y \cdot z^{-2}} \quad (4.2)$$

where G_{PI} and Y_{LCL} represent the proportional-integral controller and the combined admittance of the GFL converter and the grid, respectively:

$$G_{PI} = Z\{K_{P_i}(1 + \frac{K_{I_i}}{s})\} = K_{P_i}(1 + K_{I_i} \cdot \frac{T_s}{2} \cdot \frac{1 + z^{-1}}{1 - z^{-1}}) \quad (4.3)$$

$$\begin{aligned} Y &= Y_{LCL} + Y_s \\ Y_{LCL} &= Z\left\{\frac{s \cdot C_{LCL} \cdot R_{LCL} + 1}{a \cdot s^3 + b \cdot s^2 + c \cdot s + d}\right\} \\ Y_s &= Z\left\{\frac{1}{R_s + L_s \cdot s}\right\} = \frac{1 + z^{-1}}{R_s + 2 \cdot \frac{L_s}{T_s} + (R_s - 2 \cdot \frac{L_s}{T_s})z^{-1}} \end{aligned} \quad (4.4)$$

where the LCL formulation can be expanded as [80]:

$$\begin{aligned} a &= C_{LCL} \cdot L_{LCL_c} \cdot L_{LCL_g} \\ b &= C_{LCL} \cdot L_{LCL_c} \cdot R_{LCL} + C_{LCL} \cdot L_{LCL_g} \cdot R_{LCL} + C_{LCL} \cdot L_{LCL_c} \cdot r_{LCL_g} \\ &\quad + C_{LCL} \cdot L_{LCL_g} \cdot r_{LCL_c} \\ c &= L_{LCL_c} + L_{LCL_g} + C_{LCL} \cdot R_{LCL} \cdot r_{LCL_c} \\ &\quad + C_{LCL} \cdot R_{LCL} \cdot r_{LCL_g} + C_{LCL} \cdot r_{LCL_c} \cdot r_{LCL_g} \\ d &= r_{LCL_c} + r_{LCL_g} \end{aligned} \quad (4.5)$$

The following assumption has been made to perform the analysis in the discrete domain:

- The discretization of these variables has been performed using the Tustin method with a time sampling equal to $T_s = 50 \mu$ s.

- The PWM and measurement delays in the converter have been assumed to be equal to T_s to simplify the PHIL mathematical analysis. While different delays, converter types, or control strategies may yield varying numerical results, the proposed modeling framework remains valid and applicable.

4.1.3 Conventional PHIL Modeling

The classical approach to evaluate the PHIL system stability is to consider the HoI with its equivalent passive impedance (e.g., the AC filter of a converter), as shown in Fig. 4.2(a). The equivalent closed-loop transfer function can be expressed mathematically as:

$$\frac{i}{V_s} = \frac{G_{PA} \cdot Y_{LCL} \cdot z^{-1}}{1 + G_{LPF} \cdot G_{PA} \cdot \frac{Y_{LCL}}{Y_s} \cdot z^{-2}} \quad (4.6)$$

where the filter transfer function consists of a low-pass filter with time constant T_f :

$$G_{LPF} = Z\left\{\frac{1}{1 + T_f \cdot s}\right\} = \frac{1 + z^{-1}}{1 + \frac{2 \cdot T_f}{T_s} + \left(1 - \frac{2 \cdot T_f}{T_s}\right)z^{-1}} \quad (4.7)$$

It is assumed that the power amplifier has a unity gain $G_{PA} = 1$. This assumption is correct if the transient response of the amplifier is faster than the simulator time step $T_s = 50 \mu s$. In the case of linear power amplifiers, their fast voltage slew rate allows them to reach the new steady-state condition in about $4 \mu s$, which is more than ten times smaller than T_s .

Based on this modeling, stability is determined by the impedance ratio $\frac{Y_{LCL}}{Y_s}$. If this ratio satisfies the Nyquist criterion, the stability is guaranteed. If not, the system is unstable, and corrective actions must be taken to ensure stability. However, as shown in the mathematical formulation in (4.6), the converter controller is not accounted for in the analysis. As demonstrated in the next section, this leads to an incorrect characterization of the system's frequency behavior and, thus, of its stability.

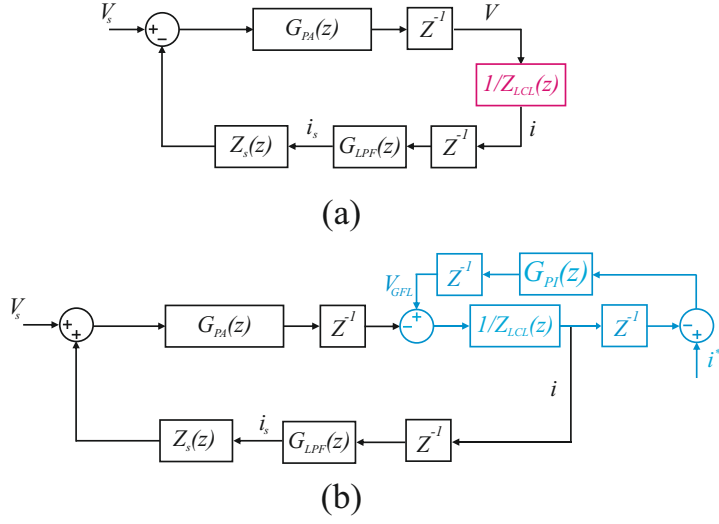


Figure 4.2: PHIL block diagram: a) without controller loop. b) with the controller loop.

4.1.4 Proposed PHIL Modeling

This section introduces the PHIL model, which includes a simplified converter model in the PHIL mathematical representation. The new model of the converter is shown in red in Fig. 4.2(a). It includes the AC filter impedance $1/Y_{GFL}$ and the converter controller G_{PI} .

The main difference between the two figures is that, although the AC filter remains in the forward path, the controller G_{PI} provides feedback action for the loop. The internal loop of the converter, CC_{loop} , can be described as:

$$CC_{loop} = \frac{Y_{LCL} \cdot z^{-1}}{1 + Y_{LCL} \cdot G_{PI} \cdot z^{-2}} \quad (4.8)$$

and obtaining the forward path transfer function of the system:

$$G_{fw} = -CC_{loop} \cdot z^{-1} \quad (4.9)$$

The closed-loop transfer function for the PHIL system $\frac{i}{V_s}$ is finally obtained:

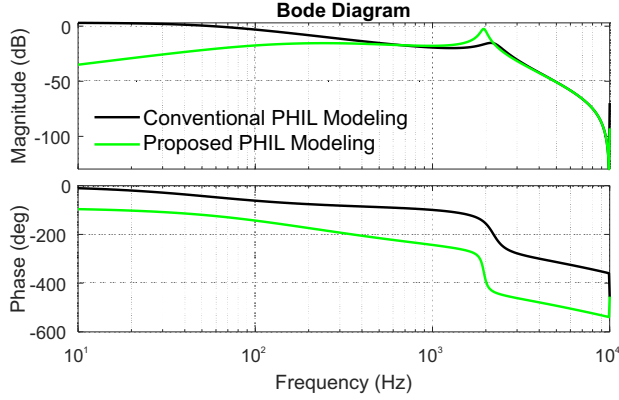


Figure 4.3: The impact of the controller loop on the PHIL analysis transfer function $\frac{i}{V_s}$.

$$\frac{i}{V_s} = \frac{G_{fw}}{1 - G_{fw} \cdot Z_s \cdot G_{LPF} \cdot z^{-1}} \quad (4.10)$$

As can be noted, the transfer function $\frac{i}{V_s}$ in the classical (4.6) and in the proposed analysis (4.10) approach differ substantially. To illustrate this difference, in Fig. 4.3, the Bode diagrams of the two transfer functions are shown when the current controller proportional gain is $K_{P_i} = 8$ and a filter with a time constant $T_f = 300 \mu s$ is used. As depicted in the figure, the frequency behavior between the classical model without modeling the converter control for PHIL stability analysis and the proposed model, which includes the converter controller model, has apparent differences. At lower frequencies, the classical approach overestimates the frequency amplitude, while at higher frequencies, it underestimates the resonance peak. Also, the frequency of resonance appears to be lower due to the current controller. Furthermore, the phase diagram shows an entirely different behavior in the frequency spectrum, which may lead to an incorrect assessment of the gain and phase margin during the loop stability analysis.

The transfer function $\frac{i}{i^*}$, which involves the capability of the converter to follow its reference, can be determined considering the open-loop and PHIL closed-loop transfer function:

$$H_{loop} = G_{LPF} \cdot Z_s \cdot z^{-1} \quad (4.11)$$

$$CH_{loop} = \frac{Y_{LCL} \cdot z^{-1}}{1 + Y_{LCL} \cdot H_{loop} \cdot z^{-1}} \quad (4.12)$$

From this point, the converter transfer function $\frac{i}{i^*}$ can be determined as in (4.13):

$$\frac{i}{i^*} = \frac{G_{PI} \cdot CH_{loop}}{1 + G_{PI} \cdot CH_{loop} \cdot z^{-1}} \quad (4.13)$$

This transfer function will be particularly important in the next section to compare the converter frequency behavior in the real coupling and the PHIL-coupled system.

4.2 Verification of the Transfer Functions

The calculated closed-loop transfer functions of the PHIL and the converter from the previous section are verified using MATLAB/Simulink. The PHIL described in Fig. 4.1 is implemented in Simulink using the parameters given in Table 4.1. Different sample frequencies via perturbation sources are applied to the system, namely V_p to verify the PHIL closed-loop transfer function and i_p to confirm the converter transfer function. Then, i is measured and fed into the Fourier Transform FTblock to obtain the gains and phases at each frequency. These measured values are compared to the frequency response of the obtained transfer functions in Table 4.2 and Table 4.3, respectively.

By comparing the transfer function frequency response and the measured values from the FT block in Simulink, it can be seen that the gain and phase values are nearly equal at each sample frequency. From the tables, the correctness of the calculated transfer functions in describing the benchmark's dynamic behavior can be concluded.

Table 4.1: PHIL simulation parameters.

T_s	$T_{d_{PI}}$	T_f	R_s	L_s	L_{LCL_g}	L_{LCL_c}	C_{LCL}	R_{LCL}	r_{LCL_g}	r_{LCL_c}	K_{P_i}	K_{I_i}
$[\mu s]$	$[\mu s]$	$[\mu s]$	$[\Omega]$	$[mH]$	$[mH]$	$[mH]$	$[\mu F]$	$[\Omega]$		$[\Omega]$	—	—
50	50	50	0.5	0.31	0.93	0.85	10	0.1		2	5.59	628.31

Table 4.2: Verification of the PHIL Transfer Function, $\frac{i}{V_s}$.

Frequency (Hz)	Transfer Function	Simulink	Parameter
100	1.33	1.33	Gain (absolute)
	-143	-142	Phase (Degree)
150	1.57	1.58	Gain (absolute)
	-160	-159	Phase (Degree)
200	1.67	1.67	Gain (absolute)
	-173	-173	Phase (Degree)
300	1.67	1.675	Gain (absolute)
	167	168	Phase (Degree)
500	1.49	1.41	Gain (absolute)
	144	145	Phase (Degree)
700	1.35	1.17	Gain (absolute)
	131	131	Phase (Degree)
850	1.01	1.29	Gain (absolute)
	123	123	Phase (Degree)
1000	1.28	0.86	Gain (absolute)
	116	116	Phase (Degree)

4.3 Impact of the Hardware on PHIL

This section demonstrates the effect of different current controller bandwidths on the stability and accuracy of the PHIL evaluation.

To assess the influence of different controller bandwidths, the current controller bandwidth is varied from 100 to 1100 Hz in both the real coupling and PHIL-coupled systems. The grid impedance is $Z_s = 1 + j0.2 \Omega$, and the LPF bandwidth is $150 \mu s$. The objective is to observe how the PHIL transfer function changes with bandwidth and how closely it matches the behavior of the real-coupling system. The pole-zero map of the converter loop, $\frac{i}{i^*}$, and PHIL $\frac{i}{V_s}$, is presented in Fig. 4.4 and Fig. 4.5, respectively.

Table 4.3: Verification of the Converter Transfer Function, $\frac{i}{i^*}$.

Frequency (Hz)	Transfer Function	Simulink	Parameter
100	1.04	1.04	Gain (absolute)
	-10	-10	Phase (Degree)
150	1.05	1.04	Gain (absolute)
	-17	-17	Phase (Degree)
200	1.03	1.03	Gain (absolute)
	-24	-24	Phase (Degree)
300	0.97	0.97	Gain (absolute)
	-36	-36	Phase (Degree)
500	0.85	0.83	Gain (absolute)
	-55	-55	Phase (Degree)
700	0.75	0.77	Gain (absolute)
	-69	-70	Phase (Degree)
850	0.71	0.74	Gain (absolute)
	-78	-80	Phase (Degree)
1000	0.70	0.74	Gain (absolute)
	-86	-90	Phase (Degree)

As can be noted, the real coupling system behaves differently from the PHIL system. While the real coupling system remains stable with a current controller bandwidth of 900 Hz, the PHIL system is already unstable at 500 Hz. To prove that, the time domain responses of the closed-loop system are depicted in Fig. 4.6 and Fig. 4.7 at a controller bandwidth of 700 Hz, confirming the pole-zero map outputs.

Also, by looking at the Bode plot in Fig. 4.8, it can be noted that the PHIL is able to represent the system up to 2 kHz at low bandwidths (e.g., 100 Hz) accurately. However, the accuracy deteriorates as the current controller bandwidth increases. For example, at a bandwidth of 500 Hz, the two frequency responses begin to differ above 1 kHz. The deviation is evident even before 1000 Hz, with a bandwidth of 1.1 kHz. This indicates that at higher frequencies, the HoI no longer behaves as in the real field, invalidating the accuracy of the PHIL evaluation.

If we look at the Bode plot of the transfer function $\frac{i}{V_s}$, shown in Fig. 4.9, it can be noted that there is a worse noise rejection capability from the PHIL system with the increase in the current controller bandwidth. This implies that any external noise will be amplified under high converter bandwidths.

4.4 Impact of the Feedback Filter

In this section, the interface feedback filter is designed to guarantee sufficient stability in large operation points.

As shown in section 2.2 for passive loads, the feedback filter typically has a stabilizing effect, allowing otherwise unstable systems to regain stability. In Fig. 4.10 and Fig. 4.11 the poles of the transfer function $\frac{i}{i^*}$, and $\frac{i}{V_s}$ are plotted, considering a current controller bandwidth of 700 Hz and a system impedance of $Z_s = 1 + j0.2 \Omega$. It can be seen that a feedback filter of only $550 \mu s$ (i.e., 1820 Hz) can let the system regain stability.

However, this comes at a cost in terms of accuracy across the frequency spectrum. As can be noted in Fig. 4.12, the slower the used filter, the larger the difference between the frequency response of the real coupling and PHIL systems. For a slow filter (e.g., $> 500 \mu s$), dynamics above 1 kHz are damped, and the LCL filter resonance peak shifts to higher frequencies.

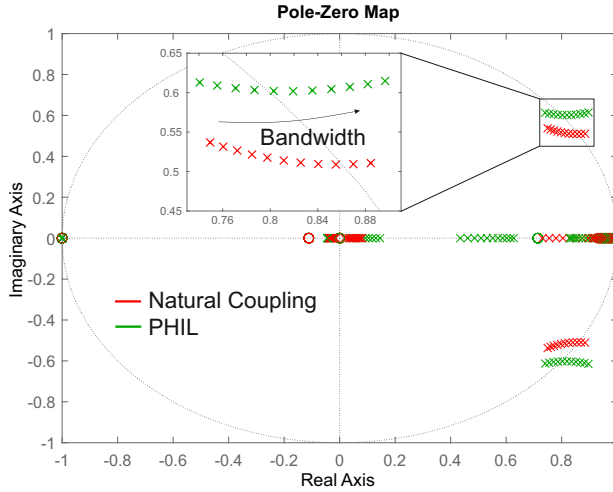


Figure 4.4: Poles of the transfer function $\frac{i}{i^*}$, considering variable current controller bandwidth (100 Hz to 1.1 kHz).

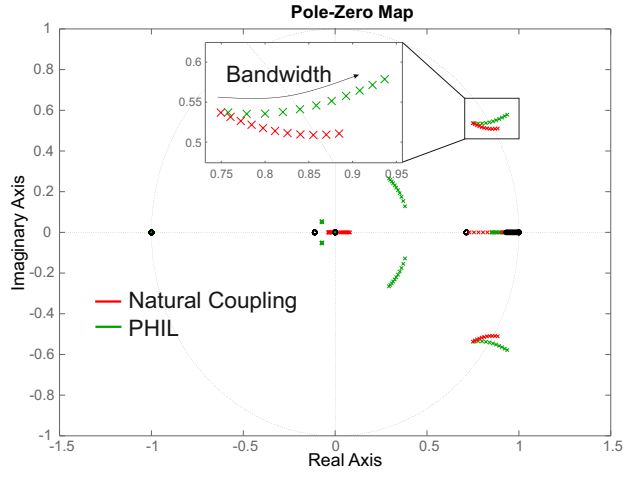


Figure 4.5: Poles of the transfer function $\frac{i}{V_s}$, considering variable current controller bandwidth (100 Hz to 1.1 kHz).

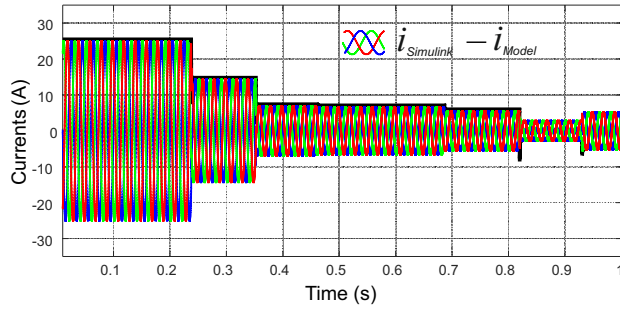


Figure 4.6: Time response of the real coupling at controller bandwidth 700 Hz.

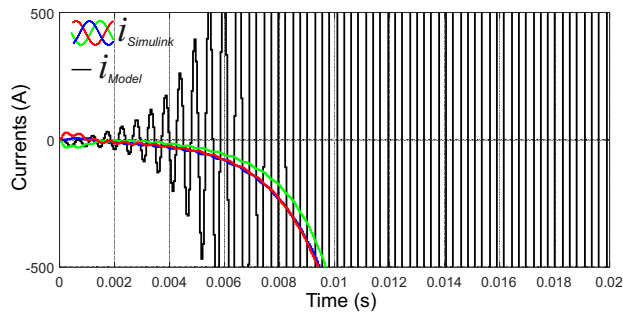


Figure 4.7: Time response of the PHIL at controller bandwidth 700 Hz.

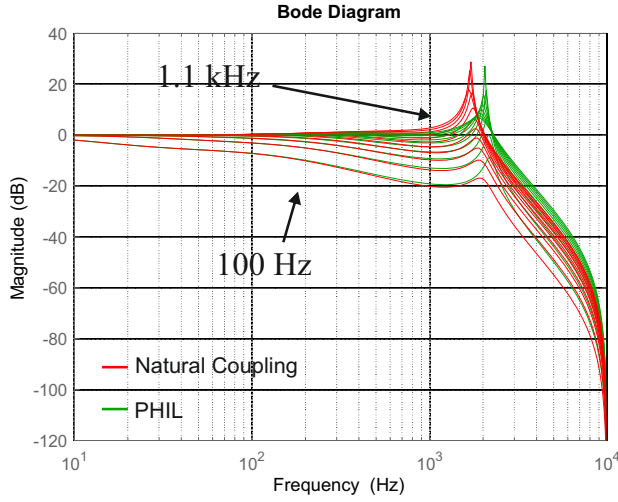


Figure 4.8: Bode plot of the transfer function $\frac{i}{i^*}$, considering variable current controller bandwidth (100 Hz to 1.1 kHz).

4.5 Impact of the Simulated Grid Impedance

One of the main uncertainties of the PHIL evaluation is the complex value of the grid impedance Z_s . The grid impedance changes depending on the connected loads and generators, namely the grid configuration, which leads to changes to the Thévenin equivalent. To achieve a stable PHIL

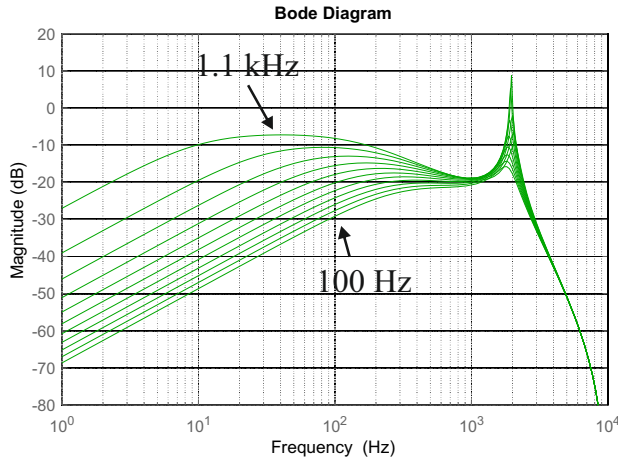


Figure 4.9: Bode plot of the transfer function $\frac{i}{V_s}$, considering variable current controller bandwidth (100 Hz to 1.1 kHz).

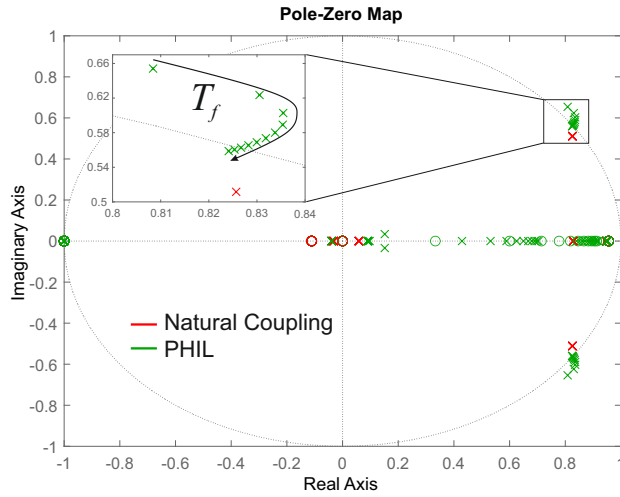


Figure 4.10: Poles of the transfer function $\frac{i}{i^*}$, considering different filter time constants [$50 \mu s - 550 \mu s$].

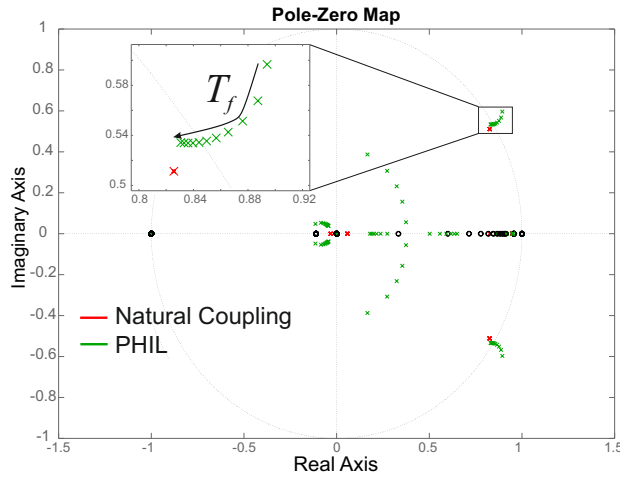


Figure 4.11: Poles of the transfer function $\frac{i}{V_s}$, considering different filter time constants [$50 \mu s - 550 \mu s$].

evaluation, the impact of impedance values under different feedback filter gains can be evaluated prior to conducting experiments.

For each of the five different values of Z_s , as demonstrated in Fig. 4.13, the time constant of the filter is varied from T_s to 11 times of it. It can be concluded that, to regain the stability of the PHIL system against changes in the grid impedance, the time constant of the filter can be accordingly changed; however, as discussed above, the high time constant of the filter deteriorates the accuracy of the PHIL system.

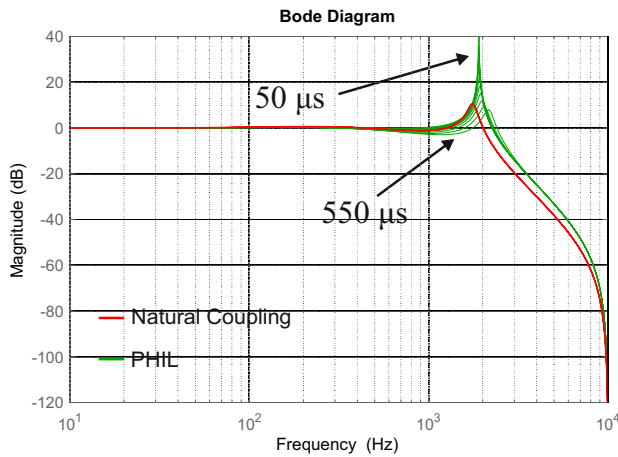
Table 4.4: PHIL experiment parameters.

T_s [μ s]	T_{DRTS} [μ s]	T_{conv} [μ s]	R_s [Ω]	L_s [mH]	L_{LCLc}, L_{LCLg} [mH]	C_{LCL} [μ F]	R_{LCL}, r_{LCLg} [Ω]	r_{LCLc} [Ω]	K_{P_i} —	K_{I_i} —
50	100	4.1	0.005	0.22	2.5	12	0.045	1.5	0.1	40

4.6 Experimental Results

To validate the PHIL and the converter models achieved in section 4.1, the PHIL setup II, described in 2.5.4, is employed. Parameter values for the experiment are given in Table 4.4. A frequency scan is performed on the described setup in two cases. In the first case, perturbation i_p , with the frequency range of 100-1000 Hz (f_p) and the magnitude of 55 A, is added to the reference current of the PI controller, i^* , and the corresponding harmonic is measured at the PCC, i , using DIN RAIL-MOUNTABLE current sensors of Imperix. The current signal, denoted as i^* , and the measured current signal, referred to as i , are fed into the FT block within the MATLAB/Simulink environment. This specific step is essential for computing the gain and phase of the ratio i/i^* at each harmonic frequency. The resulting outcomes, presented as red stars, are then compared with the results obtained through the model implemented in Simulink, as illustrated in Fig. 4.14.

The same procedure is used to verify i/V_s . This time, a 20 V perturbation is added to the voltage source in RTDS, V_p , and the current is measured with the IT 700-S ULTRASTAB current sensors. The measured gain and phase comparison is shown in Fig. 4.15. In both cases, the

**Figure 4.12:** Filter impact from T_s to $11 \cdot T_s$ with respect to the real coupling.

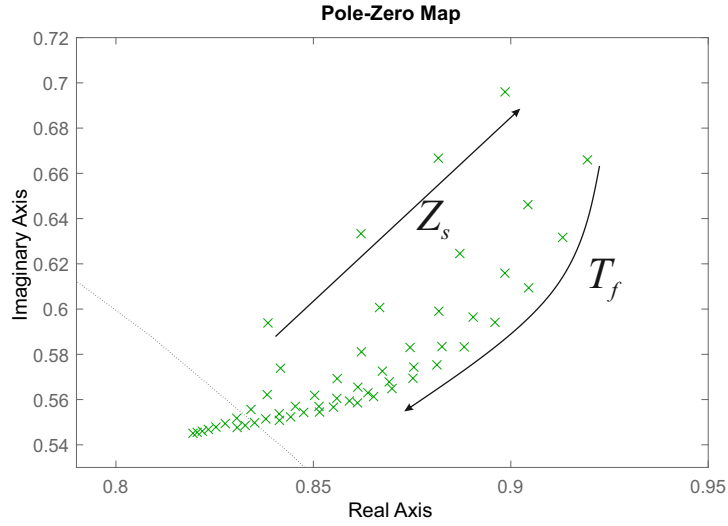


Figure 4.13: Filter impact from T_s to $11*T_s$ vs. grid impedance's resistance impact from 0.5 to $50\ \Omega$ for current controller bandwidth of 700 Hz .

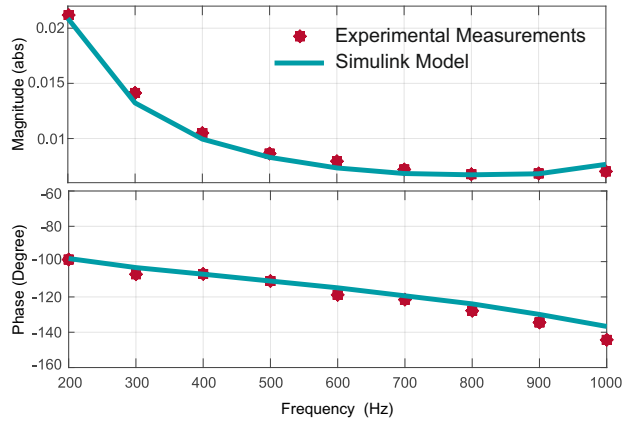


Figure 4.14: Frequency response comparison of $\frac{\hat{i}}{\hat{u}}$.

close agreement between the measured frequency response and the simulation results provides evidence of the validity of the obtained transfer functions.

In addition to Bode plots, a quantitative assessment is performed to evaluate the validity of the modeled transfer functions across measured gains and phases from experiments, using the

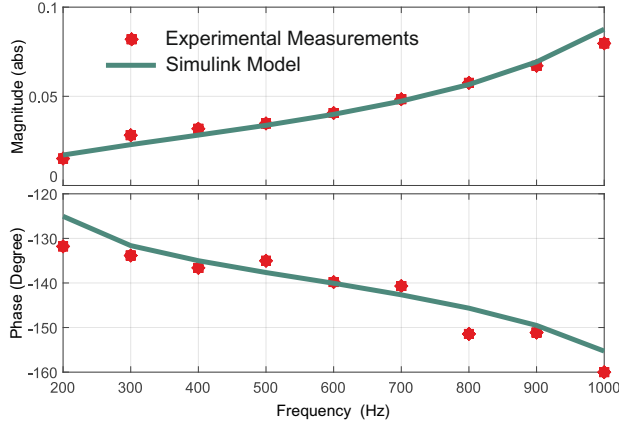


Figure 4.15: Frequency response comparison of $\frac{i}{V_s}$.

normalized root-mean-square error (nRMSE) and maximum deviation error (MaxDev). The following equations are used to achieve these error metrics:

$$\text{RMSE}_{\text{gain}} = \sqrt{\frac{1}{N} \sum_{i=1}^N (|G_{\text{model}}(j\omega_i)| - |G_{\text{ref}}(j\omega_i)|)^2} \quad (4.14)$$

$$\text{RMSE}_{\text{phase}} = \sqrt{\frac{1}{N} \sum_{i=1}^N (\angle G_{\text{model}}(j\omega_i) - \angle G_{\text{ref}}(j\omega_i))^2} \quad (4.15)$$

Where $|G_{\text{ref}}(j\omega)|$ and $|G_{\text{model}}(j\omega)|$ are the measured gain of the closed-loop transfer function (i/i^* or i/V_s) from experiments and modeling, respectively. The symbol $\angle$ represents the phase, i is the perturbation number, and N is the number of perturbation samples, i.e., 9 (from 200 to 1000 with a step of 100). The RMSE is then normalized by the range of experimentally measured values using the following equation:

$$\text{nRMSE} = \frac{\text{RMSE}}{\max_i \{G_{\text{ref}}(j\omega_i)\} - \min_i \{G_{\text{ref}}(j\omega_i)\}} \quad (4.16)$$

The equations used to evaluate MaxDev are:

$$\text{MaxDev}_{\text{gain}} = \max_i |G_{\text{ref}}(j\omega_i) - G_{\text{model}}(j\omega_i)| \quad (4.17)$$

$$\text{MaxDev}_{\text{phase}} = \max_i |\angle G_{\text{ref}}(j\omega_i) - \angle G_{\text{model}}(j\omega_i)| \quad (4.18)$$

Table 4.5: Accuracy of the modeling based on experiments.

Error Index \ Closed-Loop	i/i^*		i/V_s	
	Gain	Phase	Gain	Phase
nRMSE	0.055	0.036	0.080	0.025
MaxDev	0.001	8.942	0.007	6.747

Applying the measured values of gain and phase from each closed-loop transfer function to the equations described above will result in Table 4.5. From the Bode plots and the output results of the Table 4.5, the validity of the modeling of the benchmark PHIL, and the achieved transfer functions can be concluded.

4.7 Summary

PHIL has emerged as a key approach for realistically simulating grid behavior to test the system-level power electronic technologies. However, the stability and accuracy of PHIL setups are often constrained by trade-offs, previously believed to be due solely to the effects introduced by interface components. This section investigates the influence of not only the interface components but also an active HoI on the PHIL stability and accuracy. It is shown that the current controller bandwidth of a three-phase grid-following converter as a HoI affects the accuracy of PHIL results. The analysis is conducted by modeling the three main components of a PHIL system MoI, the interface, and the HoI using their respective transfer functions. These transfer functions are validated through perturbation-based simulations in Simulink. Subsequently, the sensitivity of PHIL stability and accuracy to both the current controller bandwidth and the interface feedback filter is evaluated. The results indicate that the choice of current controller parameters not only affects PHIL stability but also significantly influences accuracy, indicating the need for a more conservative controller tuning and a more refined feedback filter design. To further validate the findings, the derived transfer functions are experimentally verified.

5 Impedance-based Theory for Power Hardware-in-the-Loop Stability Analysis

In the previous chapter, the stability and accuracy of the PHIL system with a grid-connected converter acting as the HoI were analyzed using classical control-theoretic tools, including loop transfer functions and pole-zero maps. These methods provide valuable insight into the converter's internal control dynamics and the influence of each PHIL section on the system's closed-loop behavior. However, such methods generally require a detailed analytical model of the entire closed-loop system. In PHIL applications, this requirement is often difficult to fulfill because the HoI may not be fully known. In many practical testing scenarios, the HoI can only be represented as a gray- or black-box system, for which internal controller structures and parameters are not fully accessible. Under such conditions, deriving complete loop transfer functions becomes challenging, limiting the applicability of classical modeling approaches.

To overcome similar limitations in analyzing the stability of converter-grid interactions, impedance-based modeling has emerged as a powerful, widely adopted framework. In this approach, interconnected subsystems are characterized by their equivalent terminal impedance or admittance, allowing their interaction to be analyzed without requiring full knowledge of their internal structure. This makes the method particularly suitable for PHIL testing, where different physical and simulated components interact through the power interface. The impedance-based representation provides a modular, physically intuitive description of system dynamics and enables stability assessment using classical criteria, such as the Nyquist criterion. Moreover, it allows the dynamic influence of controllers, measurement systems, and interface components to be systematically incorporated into the analysis.

In this chapter, the impedance-based framework is first briefly introduced in section 5.1, and an example is made using the interaction between a GFL converter and a stiff grid. Subsequently, the same methodology is extended to the PHIL configuration in section 5.2, where the physical grid is replaced by an Emulated Grid (EG) implemented through the DRTS and power interface.

To obtain the impedance models, each component is represented by transfer functions, excluding the PLL model from the formulation. The influence of the PLL on the impedance model and the resulting stability analysis is neglected in this thesis, as incorporating the PLL would considerably increase the complexity of the HoI modeling. The resulting impedance models are verified through perturbation-based simulations and measurements. The system's stability is then assessed using the Nyquist criterion and benchmark time-domain responses. In one case, the impedances are experimentally measured to validate the analytically derived impedance models under realistic laboratory conditions. Based on this formulation, the influence of controller structures and sensor placement in section 5.3, and DC-side dynamics on the stability of the PHIL system, in section 5.4 are investigated. Section 5.5 concludes the chapter.

5.1 Impedance-based Theory for Grid Converters

The theory was first introduced in [81], where system stability was determined by applying the Nyquist criterion to the ratio between the load input impedance and the source output impedance to assess the stability of DC/DC converters interacting with their input filters. The concept was later generalized in [82], showing that both loads and sources can be characterized by their impedance and that the Nyquist criterion can be used to determine system stability. The approach was subsequently extended to grid-tied converters, as described in [83]. For grid-connected converters interacting with the power grid, system stability depends on the impedance ratio at the point of common coupling. The Nyquist criterion can therefore be applied to this ratio for stability assessment, since it represents the open-loop transfer function of the interconnected system. In [84], the method is further developed for impedance shaping and stability improvement using Bode plots of individual impedances rather than impedance ratios. Most grid-connected Voltage Source Converters (VSC) employ current control in a rotating (dq) reference frame synchronized with the grid voltage using a PLL [85]. However, both dq-domain current control and PLL-based grid synchronization introduce nonlinearities into power electronic systems. To address this issue, the harmonic linearization method is investigated in [86]. This method directly models the three-phase VSC impedance in the phase domain, thereby bypassing the limitations of the dq reference-frame approach. In [87], the impedance of an AC network and a Modular Multilevel Converter (MMC) is estimated.

Based on the literature reviewed, this section briefly introduces the fundamental principles of impedance-based modeling and stability analysis, and then illustrates the approach using a converter-grid interaction example. For simplicity, the argument (s) of the Laplace domain are removed from all the transfer functions.

5.1.1 Fundamentals of Impedance-based Stability Analysis

First, it is assumed that the system elements can be represented as Linear Time-Invariant (LTI) systems. In practice, this assumption is satisfied by deriving impedance models from the small-signal linearization of the devices around their operating point. Based on that assumption, the source is modeled as a Thévenin equivalent circuit, and the load is modeled as an impedance, as shown in Fig. 5.1. The current i could be described as follows:

$$i = \frac{V_s}{Z_s + Z_L} \quad (5.1)$$

$$i = \frac{V_s}{Z_L} \cdot \frac{1}{1 + \frac{Z_s}{Z_L}} \quad (5.2)$$

Following the assumption that both the voltage source and the load are intrinsically stable (V_s and Z_L), the stability of the interconnected system depends only on the term

$$H = \frac{1}{1 + \frac{Z_s}{Z_L}}.$$

The theory is based on the observation that H resembles the closed-loop transfer function of a negative feedback control system, where the forward gain is 1, and the feedback path is given by Z_s/Z_L . Therefore, the system will be stable if the open-loop transfer function, i.e., Z_s/Z_L , satisfies the Nyquist stability criterion. The same theoretical framework is extended to current-source representations. Fig. 5.2 shows the same setup in Fig. 5.1, but instead of representing the source using a Thévenin equivalent circuit, it is represented as a Norton equivalent circuit, and the load is represented using an admittance. The voltage V could then be described as follows:

$$V = \frac{I_s}{Y_s + Y_L} \quad (5.3)$$

$$V = \frac{I_s}{Y_L} \cdot \frac{1}{1 + \frac{Y_s}{Y_L}} \quad (5.4)$$

Under the same assumption done for the Thévenin equivalent circuit that the source and the load are intrinsically stable (I_s and Y_L), the setup will be stable if Y_s/Y_L satisfies the Nyquist criterion. It is also noted in [83] that (5.4) and (5.2) can be used interchangeably for stability analyses. This is important because many grid converters operate in the GFL mode, behaving as current sources rather than voltage sources.

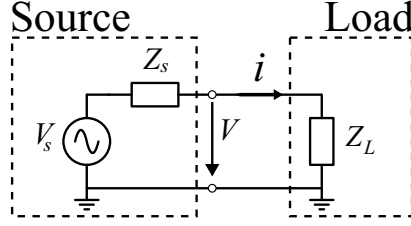


Figure 5.1: Voltage source impedance model

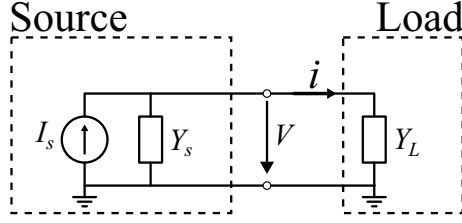


Figure 5.2: Current source impedance model

A grid can be represented with a voltage source and series impedance Z_s , and the converter could be described using a current source with a parallel admittance Z_c , as shown in Fig. 5.3. Following the basic theory in the previous subsection, the current i can be written as follows:

$$i = \left(I_c - \frac{V_s}{Z_c} \right) \cdot \left(\frac{1}{1 + \frac{Z_s}{Z_c}} \right) \quad (5.5)$$

Assumption: For active HoI, the impedance ratio alone is not sufficient for Nyquist-based stability assessment, and the complete relation $Z = N + P$ must be considered to correctly determine the stability condition, where Z denotes the number of right-half-plane (RHP) poles of the closed-loop system, N is the number of encirclements of the critical point $-1 + j0$ by the Nyquist plot of the open-loop transfer function, and P is the number of RHP poles of the open-loop transfer function.

For all considered configurations and parameter ranges, the standalone converter connected to an infinite bus is assumed to be internally stable. Since the standalone converter and its corresponding representation are governed by the same characteristic equation, the coupling condition does not alter the characteristic equation of the converter representation. Therefore, the converter introduces no additional RHP poles. Moreover, since the grid impedance is passive, the open-loop transfer function satisfies $P = 0$.

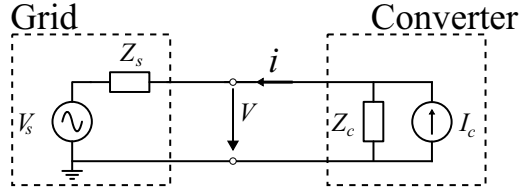


Figure 5.3: Impedance model of a converter-grid junction

Therefore, the Nyquist stability assessment reduces to the encirclement condition, and N directly determines stability, unless stated otherwise.

5.1.2 An example of Modeling a Grid and a Grid-Converter System

The selected benchmark for impedance modeling is shown in Fig. 5.4. To apply the theory, it is necessary to derive the transfer functions describing both loads and sources.

An equation describing the voltage at the point of common coupling from the grid side can be written as follows:

$$V = V_s + i \cdot Z_s \quad (5.6)$$

$$Z_s = L_s \cdot s + R_s \quad (5.7)$$

Since the grid is represented as a Thévenin equivalent circuit, it matches directly the model presented in Fig. 5.3. Therefore, the grid side impedance is Z_s itself.

To complete the impedance model, an equation describing the current at the PCC from the converter side is needed. To simplify the derivation, Z_{LCL} , i.e., the LCL filter impedance, transfer function can be split into two transfer functions, and the current can be written as follows:

$$L_{LCL_c} = L_{LCL_g}, \quad r_{LCL_c} = r_{LCL_g} \quad (5.8)$$

$$Z_L = L_{LCL_g} \cdot s + r_{LCL_g} = L_{LCL_c} \cdot s + r_{LCL_c} \quad (5.9)$$

$$Z_C = 1/(C_{LCL} \cdot s) + R_{LCL} \quad (5.10)$$

$$Y_{LCL,V} = \{i/V\}_{V_{GFL}=0} = \frac{Z_C + Z_L}{2 \cdot Z_C \cdot Z_L + Z_L^2} \quad (5.11)$$

$$Y_{LCL,V_{GFL}} = \{i/V_{GFL}\}_{V=0} = \frac{Z_C}{2 \cdot Z_C \cdot Z_L + Z_L^2} \quad (5.12)$$

$$i = Y_{LCL,V_{GFL}} \cdot V_{GFL} - Y_{LCL,V} \cdot V \quad (5.13)$$

(5.13) does not represent the converter's controller internal loop. Therefore, a relation between V_{GFL} and i can be derived as follows, under the assumption that the PLL is ideal:

$$V_{GFL} = (i^* - T_d \cdot i) G_{PI} \cdot T_d \quad (5.14)$$

$$G_{PI} = K_{P_i} + K_{I_i}/s \quad (5.15)$$

$$T_d = e^{-(T_{dPI})s} \quad (5.16)$$

Substituting (5.16) into (5.13) results in the final equation describing the current as shown in (5.17). By inspecting the equation, it can be matched to the converter model Fig. 5.3, where $Z_c = 1/Y_{GFL}$ and $I_s = H_{GFL} \cdot i^*$.

$$i = \underbrace{\frac{G_{PI} \cdot T_d \cdot Y_{LCL,V_{GFL}}}{1 + G_{PI} \cdot T_d^2 \cdot Y_{LCL,V_{GFL}}}}_{H_{GFL}} i^* - \underbrace{\frac{Y_{LCL,V}}{1 + G_{PI} \cdot T_d^2 \cdot Y_{LCL,V_{GFL}}}}_{Y_{GFL}} V \quad (5.17)$$

5.1.2.1 Impedance Model Verification

The model of a grid-connected converter, as shown in Fig. 5.4, is implemented in MATLAB/Simulink as a benchmark. Table 5.1 lists the parameters used in the simulation. Before

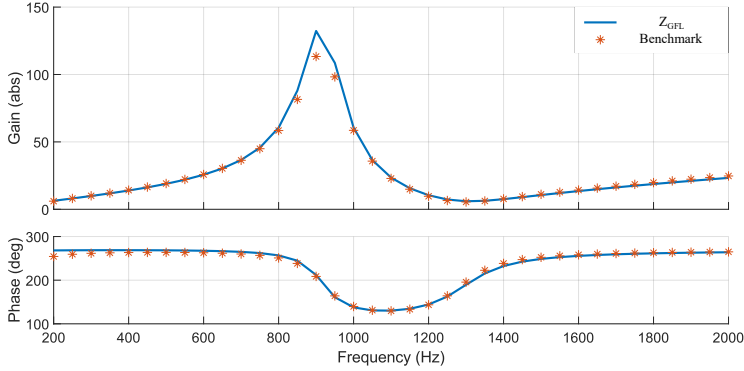


Figure 5.5: Impedance at different frequencies compared to Bode plot

response, i.e., i in the benchmark model. Fig. 5.6a shows the Nyquist criterion applied to the impedance ratio Z_s/Z_c , and the results of the benchmark current are shown in Fig. 5.6b. The benchmark results verify the Nyquist criterion's stability outcomes. The same diagrams in Fig. 7.11 are repeated with changing the values of R_s and L_s to $0.5\ \Omega$ and $25\ \text{mH}$, respectively. The results are then depicted in Fig. 5.7, where the Nyquist plot shows $-1 + 0j$ encirclements, i.e., unstable closed-loop, and the time-domain response, i in the benchmark model confirms it.

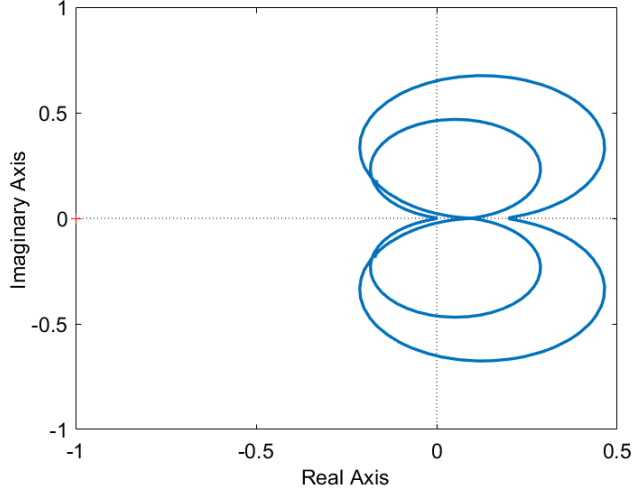
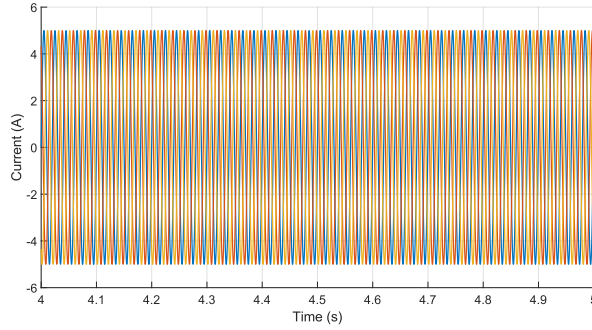
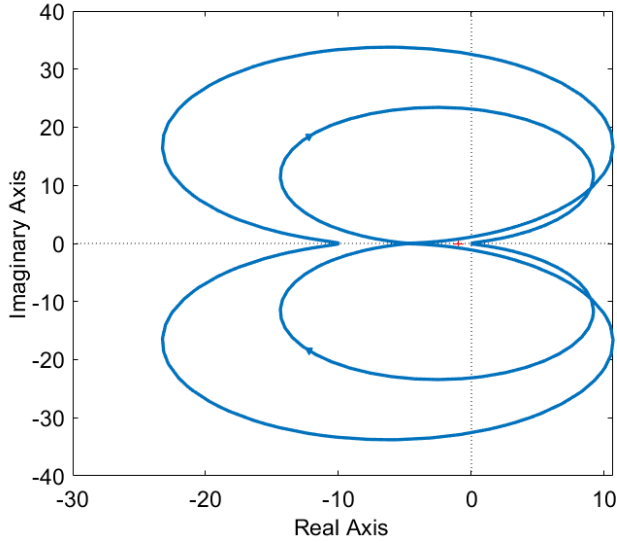
(a) Nyquist plot of Z_s/Z_{GFL} , showing a stable interaction(b) PCC current, i , from benchmark

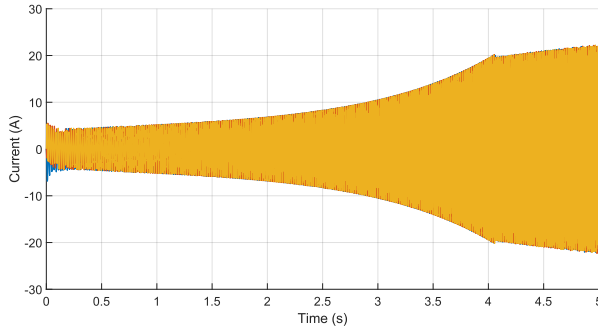
Figure 5.6: Frequency domain and time domain responses comparison for stability verification, at $R_s = 5 \text{ m}\Omega$, $L_s = 0.25 \text{ mH}$

5.2 Impedance-based Theory for PHIL Systems

In this section, the impedance-based approach shown in the previous section for a converter-grid junction stability analysis is expanded to a PHIL system where the GFL converter is employed as HoI. The difference is shown in Fig. 5.8, where Fig. 5.8a, shows the case of converter (HoI) and grid (MoI) which was discussed in previous section and Fig. 5.8b, shows that in a PHIL the



(a) Nyquist plot of Z_s/Z_{GFL} , showing an unstable interaction



(b) PCC current, i , from benchmark

Figure 5.7: Frequency domain and time domain responses comparison for stability verification, at $R_s = 0.5 \, \Omega$, $L_s = 25 \, \text{mH}$

Z_{MoI} is expanded to Z_{EG} due to the presence of interfaces when the same HoI is employed. As in the grid converter integration stability analysis discussed in the previous section, applying the impedance-based method for stability analysis in a PHIL setup eliminates the need for a detailed HoI or MoI model to analyze system stability [C2].

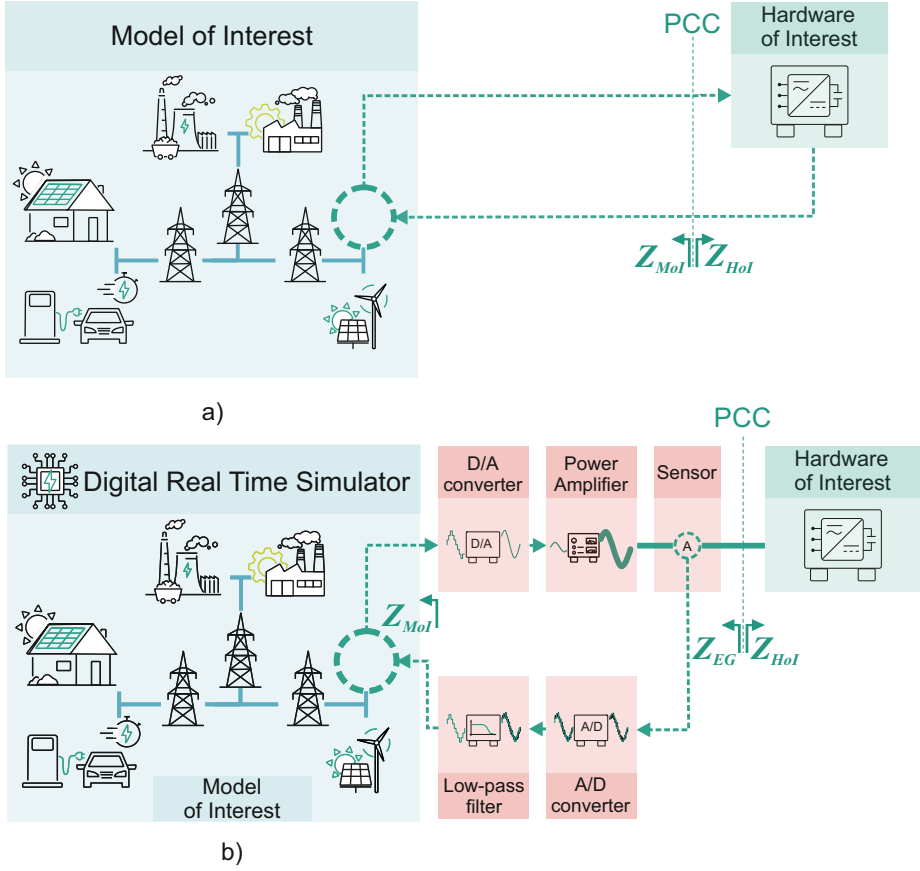


Figure 5.8: Impedance-based modeling in PHIL systems: a) Ideal natural coupling, b) PHIL actual scheme, which includes the interface impacts and changes the impedance from Z_{MoI} to Z_{EG}

5.2.1 Emulated Grid Impedance Model

As in the previous section, a Thévenin equivalent is used for the grid model in DRTS throughout the rest of this chapter. As shown in Fig. 5.9, it is a voltage source (V_s) with a series impedance (Z_s). This impedance consists of a resistance and an inductance in series, which is formulated in (5.19). The measured voltage after Z_s is applied to the HoI through a D/A converter and the

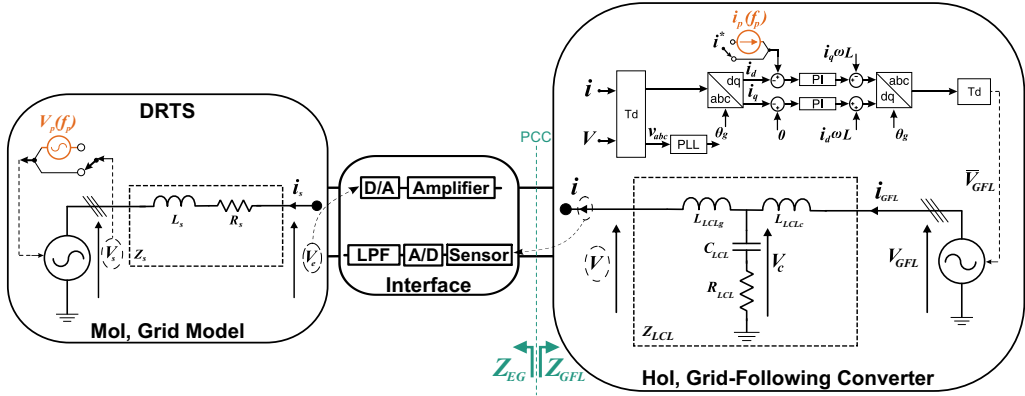


Figure 5.9: V-ITM PHIL scheme with a GFL converter as HoI

amplifier with their transfer functions. Although the transfer functions of the interface components are described in detail in section 2.1, they are briefly reviewed here for clarity:

$$Z_s = L_s \cdot s + R_s \quad (5.18)$$

$$G_{PA_v} = e^{-(T_{Amp})s} / ((1/\omega_0^2)s^2 + (2D/\omega_0)s + 1) \quad (5.19)$$

$$G_{D/A} = e^{-(T_{D/A})s} \quad (5.20)$$

$$G_{DRTS} = e^{-(T_{DRTS})s} \quad (5.21)$$

$$G_{fw} = G_{PA_v} \cdot G_{D/A} \cdot G_{DRTS} \quad (5.22)$$

where ω_0 and D are the resonant frequency and the damping factor of the amplifier, respectively. T_{Amp} , $T_{D/A}$, and T_{DRTS} are associated delays and G_{fw} is the forward path within the interface section (Fig. 5.9).

Similarly, the backward path, G_{fb} involves:

$$G_{fb} = G_{Sens} \cdot G_{A/D} \cdot G_{LPF} \quad (5.23)$$

$$G_{Sens} = e^{-(T_{Sens})s} \quad (5.24)$$

$$G_{A/D} = e^{-(T_{A/D})s} \quad (5.25)$$

$$G_{LPF} = \omega_c / (s + \omega_c) \quad (5.26)$$

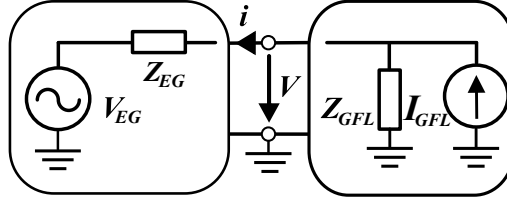


Figure 5.10: PHIL impedance model

where T_{Sens} and $T_{A/D}$ are the sensor and A/D converter delays, and ω_c is the cut-off frequency of the LPF. Through the KVL from V_s to PCC, V :

$$V = (V_s - G_{fb} \cdot Z_s \cdot i)G_{fw} \quad (5.27)$$

$$i = \underbrace{\frac{1}{G_{fb} \cdot Z_s}}_{H_{EG}} V_s + \underbrace{\frac{1}{G_{fb} \cdot Z_s \cdot G_{fw}}}_{Y_{EG}} V \quad (5.28)$$

According to (5.28), the current at the PCC point can be presented with chosen coefficients, H_{EG} , and $Y_{EG} = 1/Z_{EG}$. Therefore, Z_{EG} is not equal to Z_s anymore (in the previous section), and the interface components' impacts ($G_{fw} \cdot G_{fb}$) are included in it.

5.2.2 Hardware-of-Interest Impedance Model

As the GFL converter remained exactly the same as in the section 5.1.2, the impedance model of the converter does not change, and it will be the same as in (5.17). Therefore, considering (5.28) and (5.17), the whole setup can be represented with impedances, Z_{EG} and Z_{GFL} , and their associated sources, namely, V_{EG} and i_{GFL} , as:

$$V_{EG} = H_{EG} \cdot V_s \quad (5.29)$$

$$I_{GFL} = H_{GFL} \cdot i^* \quad (5.30)$$

$$i = [I_{GFL} - \frac{V_{EG}}{Z_{GFL}}] \underbrace{\left[\frac{1}{1 + \frac{Z_{EG}}{Z_{GFL}}} \right]}_{G_{ot}} \quad (5.31)$$

The proposed impedance model is represented in Fig. 5.10. As discussed in 5.1, assuming V_{EG} and i_{GFL} are stable sources (no right half-plane poles in H_{EG} , and H_{GFL}), the stability only depends on the Z_{EG}/Z_{GFL} .

5.2.3 Impedance Verification

The approach to impedance verification is similar to that in section 5.1.2.1 and will remain the same throughout the rest of the thesis. Parameters of PA are not repeated here as they are given in section 2.1, and Chapter 3, and they remain the same throughout the thesis. The PHIL setup with the parameters given in Table 5.2 is implemented in Simulink for perturbations and measurements, serving as a reference for verifying the calculated impedances in the previous section. To measure $Z_{EG_{ref}}$ (blue color in Fig. 5.11), the perturbation source $i_p(f_p)$ (in Fig. 5.9), is enabled to perform the frequency sweep. The sweep is performed with the current perturbation of 10 A and a frequency range of 200-1200 Hz. According to Fig. 5.10, the measured voltage over current (in d axis) at PCC equals the Z_{EG} . At each frequency, the gain and phase of the PCC voltage and current are measured using the Fourier transform block, which eventually delivers the gain and phase of the impedance $Z_{EG_{ref}}$, which is then compared with the Z_{EG} Bode plot. Similarly, for $Z_{GFL_{ref}}$, $V_p(f_p)$ in Fig. 5.9, makes the PCC measurements correspond to the converter side impedance measurement. The attained gain and phase are shown in red, in Fig. 5.11. The Bode plot of Z_{GFL} is then plotted in the same figure to illustrate the excellent match between the calculated impedance model, Z_{GFL} , and its Simulink reference, $Z_{GFL_{ref}}$.

The matching between impedances and their references in Fig. 5.11 confirms the validity of the modeled impedances.

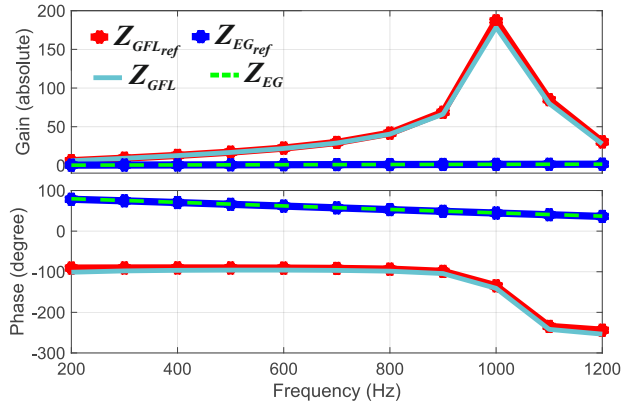


Figure 5.11: Impedance verification

Table 5.2: PHIL simulation parameter

T_{DRTS}	T_{Amp}	$T_{A/D}, T_{D/A}$	T_{Sens}	f_c	L_s	R_s	L_{LCLg}	C_{LCL}	$r_{LCLg,c}$	R_{LCL}	K_{P_i}	K_{I_i}	$T_{d_{PI}}$
[μs]	[μs]	[μs]	[μs]	[kHz]	[mH]	[m Ω]	[mH]	[μF]	[Ω]	[Ω]	—	—	[μs]
50	1.5	3	3	2	0.236	5	2.36	12	0.1	1.5	1	40	50

5.2.4 Stability Verification

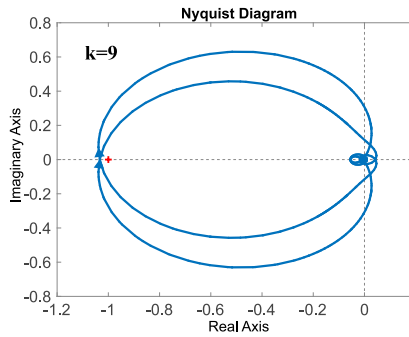
For stability verification, two different grid parameters are used with the same HoI. Therefore, Z_{L_g} is held constant, and its parameters are provided in Table 5.2. The grid-side impedance Z_s is adjusted according to variations in the parameter k , which is defined as follows:

$$k = Z_{L_g} / Z_s \quad (5.32)$$

$$Z_{L_g} = L_{LCLg} \cdot s + r_{LCLg} \quad (5.33)$$

Variations in k lead to changes in the grid-side impedance, which in turn affect the EG impedance and, ultimately, the ratio Z_{EG}/Z_{GFL} . Then, Z_{EG}/Z_{GFL} (i.e., stability criterion) is applied to the Nyquist plot, and the result is compared with Simulink. For example, if $k=9$, the graph encircles $(-1 + 0j)$ in the Nyquist plot (Fig. 5.12), showing an unstable system, confirmed by the benchmark's instability. Whereas, with $k=10$, the new Z_s eventually modifies the Z_{EG}/Z_{GFL} ratio and holds the system within the stable region (Fig. 5.14). As shown in Fig. 5.15, the current controller exhibits excellent tracking of reference changes.

Thus, the stability of the PHIL setup is examined through its impedance model. The following section presents experimental impedance verification results from an actual PHIL setup.

**Figure 5.12:** Nyquist plot of Z_{EG}/Z_{GFL}

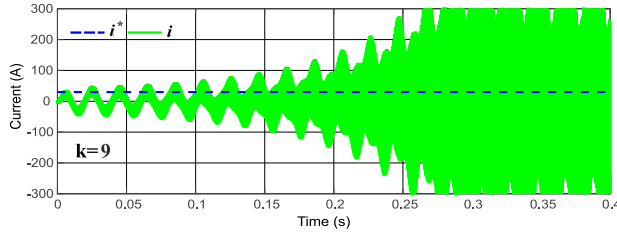


Figure 5.13: Time-domain response of the converter current

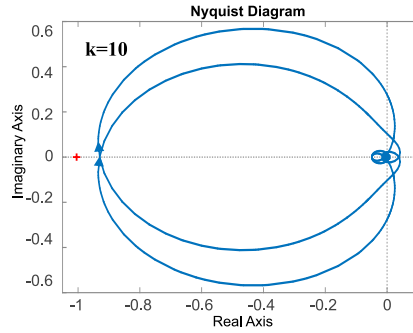


Figure 5.14: Nyquist plot of Z_{EG}/Z_{GFL}

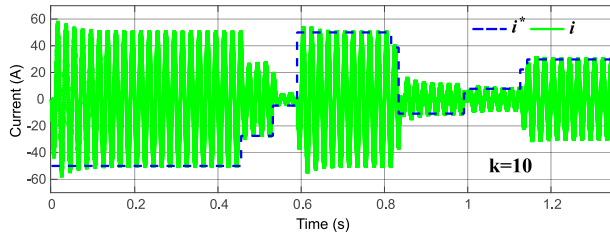


Figure 5.15: Time-domain response of the converter current

5.2.5 Experimental Verification

Similar to impedance verification in Simulink, the approach is the same, but the verification reference is experimental impedance measurements rather than Simulink. The setup used for this experiment is described in the section 2.5.4. The majority of the parameters used for the experiment are the same as in the simulation (Table 5.2), except that $K_{Pi} = 0.1$, which is reduced to avoid an overly fast controller response. To validate the accuracy of the calculated Z_{GFL} , the perturbation source, $V_p(f_p)$ shown in Fig. 5.9, is activated. Next, a three-phase disturbance with a magnitude of 2 V is added to V_s in RSCAD. Since the LCL filter capacitor exhibits inductive behavior at frequencies above 1200 Hz due to parasitic effects, and the resolution of measuring

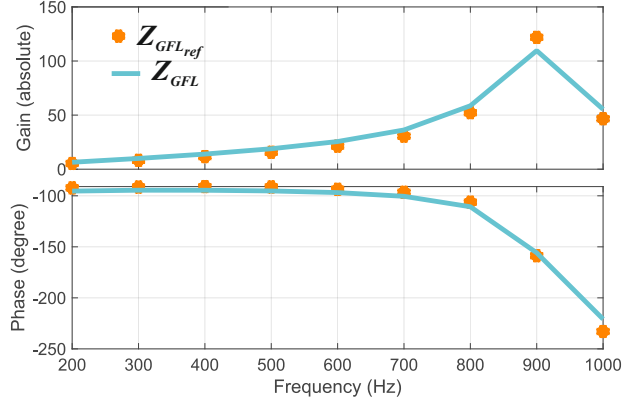


Figure 5.16: Experimental GFL converter impedance verification

high-frequency signals decreases with a $50 \mu s$ time step, the perturbation frequency is varied from 200 Hz to 1000 Hz in increments of 100 Hz. The resulting voltage and current at the PCC are measured with Imperix voltage and current sensors at each frequency to calculate the impedance, which equals Z_{GFL} . Using the Fourier transforms of the measured variables, the gain and phase of $Z_{GFL_{ref}}$ are obtained and compared with the Bode plot of the Z_{GFL} transfer function from the modeling section. This comparison is shown in Fig. 5.16, proving the correctness of the evaluated Z_{GFL} .

Similarly, for $Z_{EG_{ref}}$, the perturbation source $i_p(f_p)$ is added to i^* . For a 220 V (rms) voltage, T_{DRTS} is 2 times the chosen time-step T_s , one in the forward path and one in the feedback path.

The comparison results are presented in Fig. 5.17, demonstrating a close agreement between the model-predicted EG impedance and the reference values obtained from experimental data. The experimental impedance verification in this section confirms the correctness of the impedance model outlined in Fig. 5.10, and the functionality of the impedance-based approach to evaluate the stability of the PHIL setup ahead of running lab testing.

5.3 Sensor Placement Impact on the PHIL System Stability

The GFL converter used as the HoI in the previous section, the current controller, the physical LCL filter, and the digital control delays were modeled without voltage feedforward. However, in practical implementations of GFL converters, voltage feedforward is typically employed to

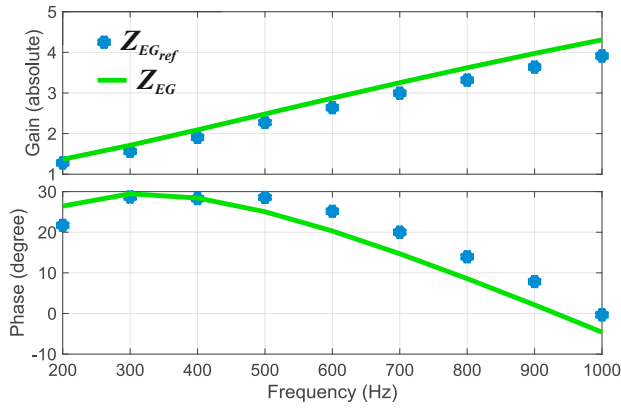


Figure 5.17: Experimental EG impedance verification

reduce the control effort required from the current controller. The presence of this feedforward alters the converter's dynamic behavior. In this section, while the grid model in DRTS is kept the same, the feedforward is added to the GFL converter impedance model. Also, the feedforward is implemented in the abc frame rather than in the d axis, since the PLL dynamics are not included in the impedance model. As a result, the voltage measurement used for feedforward depends directly on the sensor location; thus, the voltage sensor's placement influences the feedforward path and modifies the effective converter impedance. Consequently, sensor placement affects the interaction between the converter and the EG.

For the current sensor, it directly impacts the controlled variable, whether the grid-side current or the converter side current is controlled, which also changes the effective output impedance of the GFL converter.

Therefore, in this section, the impact of current- and voltage-sensor placement on PHIL stability across four scenarios: two for current-sensor placement and two for voltage-sensor placement within the LCL filter. The results are presented and validated in the time and frequency domains using Simulink/MATLAB.

As highlighted in [88], the placement of sensors for controlling a GFL converter can vary across LCL filters for different applications, making four combinations:

Case I: Current sensor location on the grid side inductor, and voltage sensor location across the PCC.

Case II: Current sensor location on the converter side inductor, and voltage sensor location across the PCC.

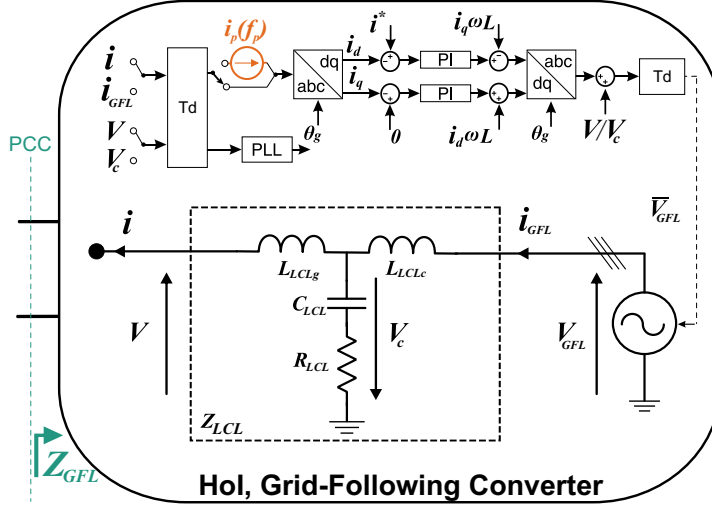


Figure 5.18: Possible combination of sensors: Cases I and II (i , i_{GFL}) for the current sensors and Cases III and IV (V , V_c) for the voltage sensors

Case III: Current sensor location on the grid side inductor, voltage sensor location across the capacitor of the LCL filter.

Case IV: Current sensor location on the converter side inductor, voltage sensor location across the capacitor of the LCL filter.

5.3.1 Hol Impedance Model Across Sensor Placement

As the same grid model as in section 5.2 is used, in the modeling section, the Z_{EG} is not repeated. For the converter side, all four different scenarios are depicted in Fig. 5.18. Altering the location of the current sensor means transitioning the controlled variable from i to i_{GFL} . Although the PLL's impact on the converter impedance is neglected, changing the voltage sensor affects the feedforward, thereby influencing the dynamics of the controlled variable. Establishing the stability criterion in this section involves deriving the open-loop transfer function for each scenario via impedance-based modeling.

5.3.1.1 Case I: i , V

In this case, the PCC variables are fed into the control unit; namely, i is controlled, and V is feed-forwarded. The EG side and GFL converter side LCL inductors are treated independently, namely, Z_{L_g} and Z_{L_c} . Therefore, the following equations are updated as given:

$$Y_{LCL,V_{GFL}} = Z_C / (Z_{L_g} \cdot Z_C + Z_C \cdot Z_{L_c} + Z_{L_c} \cdot Z_{L_g}) \quad (5.34)$$

$$Y_{LCL,V} = (Z_C + Z_{L_c}) / (Z_{L_g} \cdot Z_C + Z_C \cdot Z_{L_c} + Z_{L_c} \cdot Z_{L_g}) \quad (5.35)$$

$$Z_C = 1 / (C_{LCL} \cdot s) + R_{LCL} \quad (5.36)$$

$$Z_{L_g} = L_{LCL_g} \cdot s + r_{LCL_g} \quad (5.37)$$

$$Z_{L_c} = L_{LCL_c} \cdot s + r_{LCL_c} \quad (5.38)$$

and due to the added feedforward, the converter controller loop is now changed to:

$$V_{GFL} = (i^* - T_d \cdot i)G_{PI} \cdot T_d + V \cdot T_d^2 \quad (5.39)$$

$$i = \underbrace{\frac{G_{PI} \cdot T_d \cdot Y_{LCL,V_{GFL}}}{1 + G_{PI} \cdot T_d^2 \cdot Y_{LCL,V_{GFL}}}}_{H_{GFL,I}} i^* - \underbrace{\frac{Y_{LCL,V} - Y_{LCL,V_{GFL}} \cdot T_d^2}{1 + G_{PI} \cdot T_d^2 \cdot Y_{LCL,V_{GFL}}}}_{Y_{GFL,I}} V \quad (5.40)$$

which describes the current source I_{GFL} and the GFL converter impedance model. Compared to the converter impedance model without feedforward given in (5.17), the term $V \cdot T_d^2$ is added to (5.39) and therefore $-Y_{LCL,V_{GFL}} \cdot T_d^2$ is added to (5.40). The impedance model of the converter can be represented as:

$$I_{GFL,I} = H_{GFL,I} \cdot i^* \quad (5.41)$$

$$Z_{GFL,I} = -(1 + G_{PI} \cdot T_d^2 \cdot Y_{LCL,V_{GFL}}) / (Y_{LCL,V} - Y_{LCL,V_{GFL}} \cdot T_d^2) \quad (5.42)$$

5.3.1.2 Case II: i_{GFL} , V

The synchronization process occurs at the PCC; however, control is now transferred to the current on the converter side. Here, only the equations affected by these sensor placements are revised and provided here. Since the controlled variable is now the i_{GFL} , it is substituted to i in (5.39):

$$V_{GFL} = (i^* - T_d \cdot i_{GFL})G_{PI} \cdot T_d + V \cdot T_d^2 \quad (5.43)$$

Where the same as Case I, i_{GFL} can be achieved by applying superposition:

$$i_{GFL} = Y \cdot V_{GFL} - Y_{LCL,V_{GFL}} \cdot V \quad (5.44)$$

$$Y = (Z_C + Z_{L_g}) / (Z_{L_g} \cdot Z_C + Z_C \cdot Z_{L_c} + Z_{L_c} \cdot Z_{L_g}) \quad (5.45)$$

and i remains the same as in (5.13). Therefore, by replacing (5.44) to (5.43), and to (5.13), the converter model is achieved as follows:

$$i = \underbrace{\frac{G_{PI} \cdot T_d \cdot Y_{LCL,V_{GFL}}}{1 + G_{PI} \cdot T_d^2 \cdot Y}}_{H_{GFL,II}} i^* - \underbrace{\frac{Y_{LCL,V}(1 + Y \cdot G_{PI} \cdot T_d^2) - Y_{LCL,V_{GFL}} \cdot T_d^2(1 + Y_{LCL,V_{GFL}} \cdot G_{PI})}{1 + G_{PI} \cdot T_d^2 \cdot Y}}_{Y_{GFL,II}} V \quad (5.46)$$

5.3.1.3 Case III: V_c, i

Placing the voltage sensor at V_c means that synchronization and, consequently, feedforward is now over the capacitor of the LCL filter. This means the relation between V_{GFL} and the controlled variable holds:

$$V_{GFL} = (i^* - T_d \cdot i)G_{PI} \cdot T_d + V_c \cdot T_d^2 \quad (5.47)$$

$$V_c = V + i \cdot Z_{L_g} \quad (5.48)$$

and by returning (5.48) to (5.47) and (5.47) to (5.13) the impedance model is achieved as following:

$$i = \underbrace{\frac{G_{PI} \cdot T_d \cdot Y_{LCL,V_{GFL}}}{1 + (G_{PI} - Z_{L_g})T_d^2 \cdot Y_{LCL,V_{GFL}}}}_{H_{GFL,III}} i^* - \underbrace{\frac{Y_{LCL,V} - Y_{LCL,V_{GFL}} \cdot T_d^2}{1 + (G_{PI} - Z_{L_g})T_d^2 \cdot Y_{LCL,V_{GFL}}}}_{Y_{GFL,III}} V \quad (5.49)$$

5.3.1.4 Case IV: V_c, i_{GFL}

In the last scenario, the converter current is controlled, and the converter is synchronized with the grid at the filter capacitor leg. Therefore:

$$V_{GFL} = (i^* - T_d \cdot i_{GFL})G_{PI} \cdot T_d + V_c \cdot T_d^2 \quad (5.50)$$

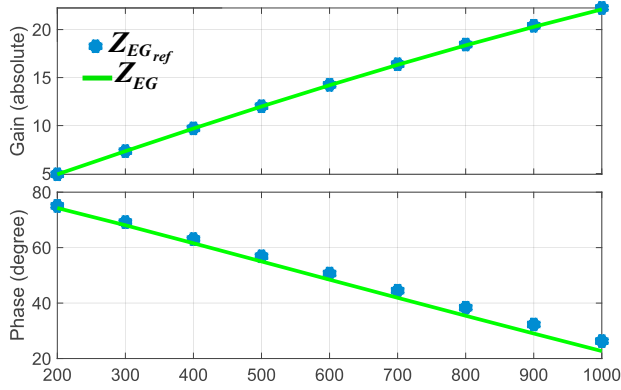


Figure 5.19: EG impedance verification

By returning (5.44) and (5.48) to (5.50), and (5.50) to (5.44) the impedance model is achieved and shown below:

$$i = \underbrace{\frac{G_{PI} \cdot T_d \cdot Y_{LCL,V_{GFL}}}{1 + (Y \cdot G_{PI} - Y_{LCL,V_{GFL}} \cdot Z_{L_g})T_d^2}}_{H_{GFL,IV}} i^* - \underbrace{\frac{Y_{LCL,V}(1 + Y \cdot G_{PI} \cdot T_d^2) - Y_{LCL,V_{GFL}} \cdot T_d^2(1 + G_{PI} \cdot Y_{LCL,V_{GFL}})}{1 + (Y \cdot G_{PI} - Y_{LCL,V_{GFL}} \cdot Z_{L_g})T_d^2}}_{Y_{GFL,IV}} V \quad (5.51)$$

with the setup now fully modeled across all scenarios, the models' veracity is validated in the next section.

5.3.2 Impedance Verification

To validate the impedance model, the HoI shown in Fig. 5.18 is replaced with HoI in Fig. 5.9 and implemented in Simulink using the parameters listed in Table 5.2. Only the value of Z_s is set as 0.7 times the value of Z_{L_g} . Perturbation sources, V_p and i_p in a range of 200-1000 Hz for f_p , are applied. Then, PCC current and voltage are measured and fed to the Fourier transform for gain and phase measurements of $Z_{GFL_{ref}}$ and $Z_{EG_{ref}}$, respectively. The achieved values are compared with the Bode plot of modeled impedances in section 5.3.1, and the comparison in each case is represented from Fig. 5.19 to 5.23.

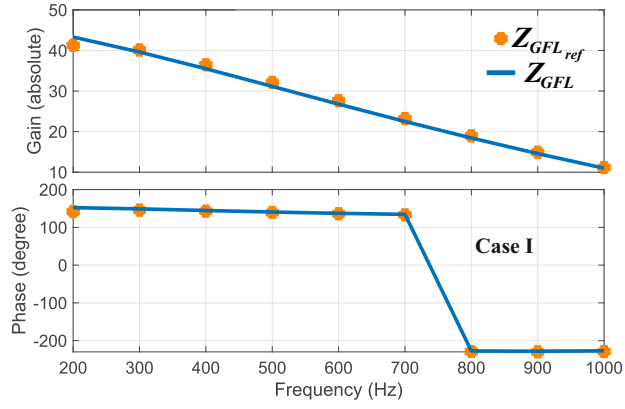


Figure 5.20: Case I, GFL converter impedance verification

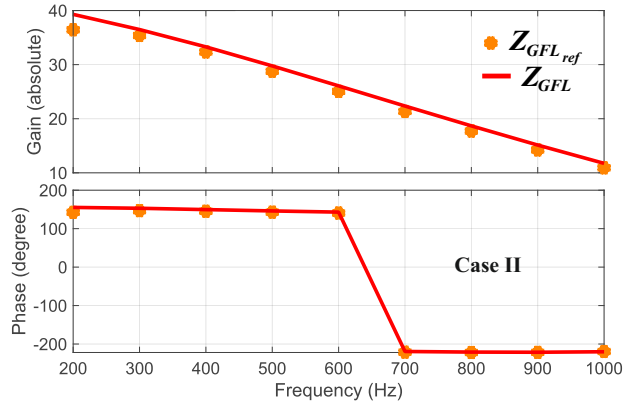


Figure 5.21: Case II, GFL converter impedance verification

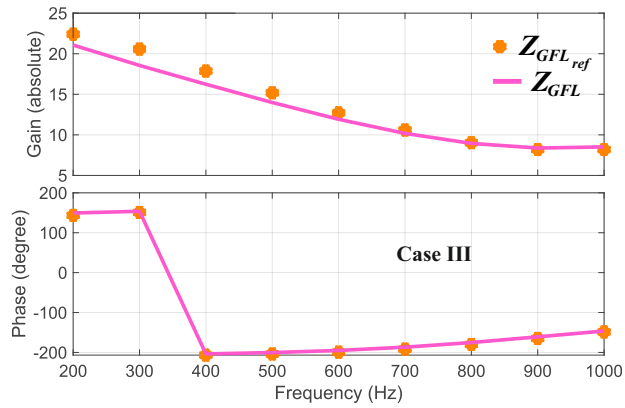


Figure 5.22: Case III, GFL converter impedance verification

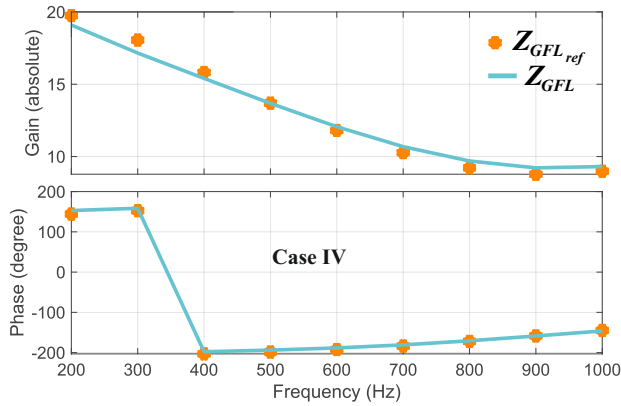


Figure 5.23: Case IV, GFL converter impedance verification

The proximity of the modeled frequency responses to the measured values, as referenced, validates the accuracy of the modeling approach.

A similar frequency response is observed in cases I and II, as well as in cases III and IV. In other words, the plots reveal minimal discrepancies in the converter impedance gain and phase when only the current-sensor location is altered. However, a notable reduction in gain is observed when the voltage sensor is repositioned across the capacitor rather than across the PCC. Additionally, beyond 400 Hz, a gradual divergence in the phase of cases III and IV is observed, resulting in a distinct alteration in the shape of the GFL converter impedance. With the model validated in the preceding section, the system's stability is assessed next using the impedance-based stability criterion.

5.3.3 Stability Verification

The stability analysis is performed using the Nyquist plot of the impedance-ratio stability criterion, Z_{EG}/Z_{GFL} , for each case of sensor arrangements using two different values for C_{LCL} , namely, 12 and 4 μF . The results are then compared with the time-domain response from Simulink. Similar to Bode plots, Fig. 5.24 indicates that the response and stability margin in cases I and II are close to each other, the same as with cases III and IV. All cases with this capacitor value are stable, and the margins appear close. However, with a 4 μF , as depicted in Fig. 5.25, there is a margin difference between group one, cases I and II, which are unstable, and group two, cases III and IV, which are within the stable zone. Based on Nyquist plots, placing the voltage sensor across the LCL filter capacitor enhances system stability, whereas the current sensor's location does not affect closed-loop stability. To prove this finding, the time domain response from the

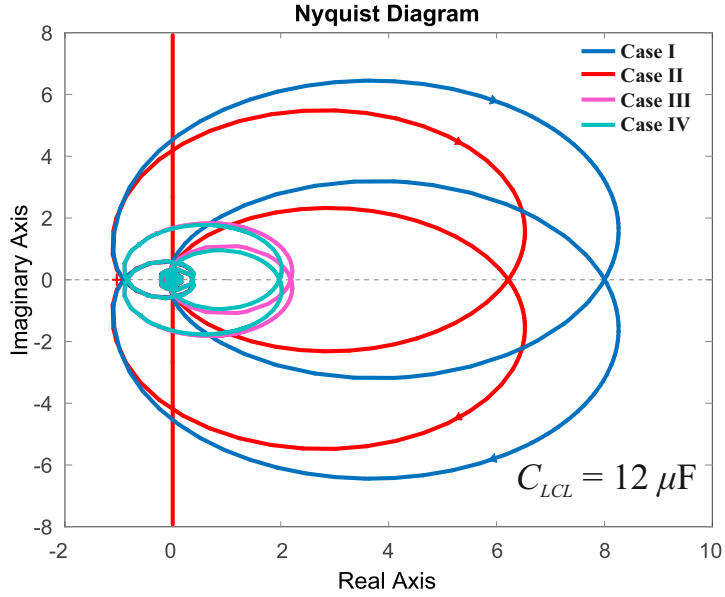


Figure 5.24: Nyquist plot of Z_{EG}/Z_{GFL} , all cases are stable

implemented Simulink model is shown in Fig. 5.26, where at 0.7 s, the voltage sensor is switched from the capacitor's location to the PCC (from V_c to V), and the system becomes unstable and at 0.8 s, it is switched back to case III and the system regains the stability, confirming the Nyquist plot's correctness.

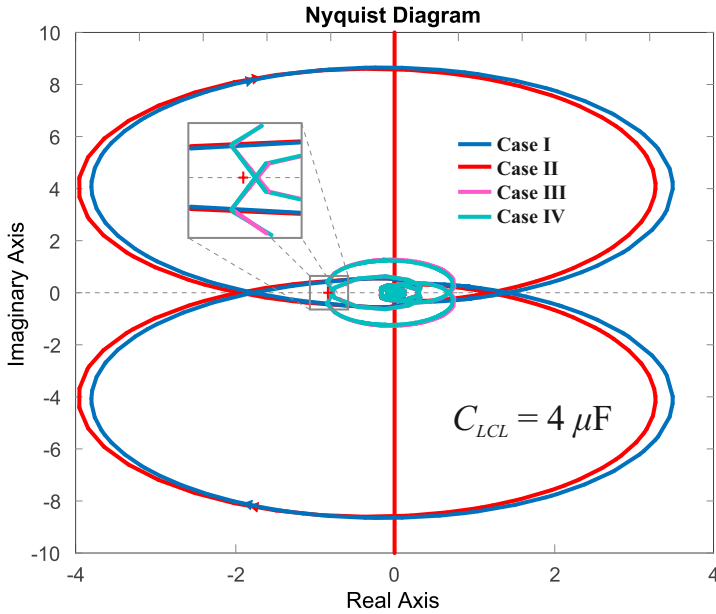


Figure 5.25: Nyquist plot of Z_{EG}/Z_{GFL} , cases I and II are unstable, cases III and IV are stable

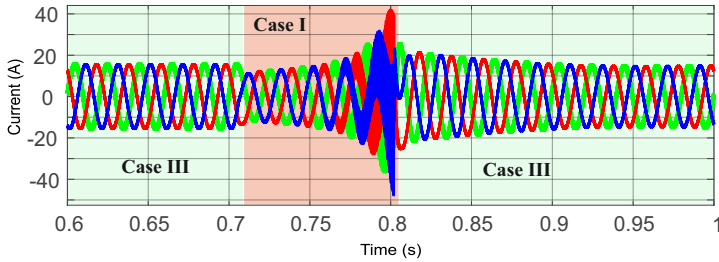


Figure 5.26: Time domain response of the controlled current when changing the position of the voltage sensor

5.4 Source Impact on the Impedance-based Stability Criterion

This section extends the GFL converter model by incorporating DC link dynamics and a cascaded DC voltage controller to assess the influence of the GFL converter control system on impedance-based stability analysis of a PHIL setup. The grid model and the interfaces are similar to the section 5.2 and 5.3, but for the GFL converter compared to the section 5.3.1.1, here, as shown in Fig. 5.27, the DC link of the GFL converter is not ideal, and there is a DC voltage controller over a capacitor creating the current reference for the current controller of the GFL converter. The



5.4.1 Impedance Model of the GFL Converter with a Dynamic DC Source

The structure of the converter can be seen in Fig. 5.27. The converter side of the PHIL includes the LCL filter, the cascaded controller, and the DC link. The cascaded controller consists of an inner current controller and an outer voltage controller. The current i at PCC can be described as a superposition of the LCL transfer functions seen from the grid side $Y_{LCL,V}$ and the converter side $Y_{LCL,GFL}$.

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According to this figure, the V_{GFL} depends on the DC link voltage V_{dc} , the reference of the DC link voltage V_{dc}^* , and the voltage and current at PCC:

$$V_{GFL} = [((V_{dc}^* - V_{dc} \cdot T_d) G_{PI,V_{dc}} - i \cdot T_d) G_{PI,i} + V \cdot T_d] T_d \quad (5.53)$$

The DC link voltage can be expressed as the difference between the power injected from the grid side into the DC link through the converter and the power consumed by the load. To achieve a stable DC link voltage, the injection and consumption of power in the DC link must be equal.

Assumption: The DC-link voltage is assumed to vary only slightly around its steady-state operating point ($V_{dc} = V_{dc_n} + \tilde{v}_{dc}$, with $\tilde{v}_{dc} \ll V_{dc_n}$), such that second-order terms can be neglected and $V_{dc}^2 \approx V_{dc_n} V_{dc}$ holds. By aligning the synchronous dq reference frame with the PCC voltage vector, the PCC voltage is entirely represented on the d-axis. Therefore, $v_q = 0$ and $v_d = V$, where V denotes the PCC voltage magnitude. Moreover, for the small-signal derivation, the PCC voltage magnitude is assumed to remain constant and equal to its operating-point value, i.e., $V = V_{rms}$.

$$V_{dc} = (V_n \cdot i \cdot \frac{3}{2} \cdot \frac{1}{V_{dc_n}} \cdot T_d^2 + I_L) Z_{dc} \quad (5.54)$$

The term T_d appears in the power-related equation, (5.54) of the present model, not as part of the physical power balance, but because the impedance model is derived from the corresponding Simulink implementation, where these terms are required to ensure a realizable and non-singular formulation. The DC link impedance Z_{dc} itself consists of the DC capacitor and a resistor in series:

$$Z_{dc} = R_{dc} + \frac{1}{s \cdot C_{dc}} \quad (5.55)$$

By replacing (5.55) in (5.54), then in (5.53) and the resulting equation in (5.52), the current at PCC is expressed depending on the voltage reference V_{dc}^* , the load current I_L and the voltage V at PCC with the coefficients $H_{GFL,1}$, $H_{GFL,2}$ and $Y_{GFL} = 1/Z_{GFL}$ shown in (5.56).

$$\begin{aligned}
i = & \underbrace{\frac{G_{PI,V_{dc}} \cdot G_{PI_i} \cdot T_d \cdot Y_{LCL,GFL}}{1 + G_{PI_i} \cdot T_d^2 \cdot Y_{LCL,GFL} + V_n \cdot \frac{3}{2} \cdot \frac{1}{V_{dcn}} \cdot T_d^4 \cdot Z_{dc} \cdot G_{PI,V_{dc}} \cdot G_{PI_i} \cdot Y_{LCL,GFL}}}_{H_{GFL,1}} V_{dc}^* \\
& - \underbrace{\frac{T_d^2 \cdot Z_{dc} \cdot G_{PI,V_{dc}} \cdot G_{PI_i} \cdot Y_{LCL,GFL}}{1 + G_{PI_i} \cdot T_d^2 \cdot Y_{LCL,GFL} + V_n \cdot \frac{3}{2} \cdot \frac{1}{V_{dcn}} \cdot T_d^4 \cdot Z_{dc} \cdot G_{PI,V_{dc}} \cdot G_{PI_i} \cdot Y_{LCL,GFL}}}_{H_{GFL,2}} I_L \\
& - \underbrace{\frac{Y_{LCL,V} - T_d^2 \cdot Y_{LCL,GFL}}{1 + G_{PI_i} \cdot T_d^2 \cdot Y_{LCL,GFL} + V_n \cdot \frac{3}{2} \cdot \frac{1}{V_{dcn}} \cdot T_d^4 \cdot Z_{dc} \cdot G_{PI,V_{dc}} \cdot G_{PI_i} \cdot Y_{LCL,GFL}}}_{Y_{GFL}} V
\end{aligned} \tag{5.56}$$

As mentioned, the grid impedance Z_{EG} equation remains the same as (5.28). As shown, the GFL converter equation is modified from (5.40) to (5.56) due to the cascaded controller and the addition of the DC link impedance to the converter. V_{dc}^* and I_L give the source/sink equations, and if internally stable, stability of the EG/GFL can be assessed by their output impedance ratio Z_{EG}/Z_{GFL} , which will be presented after verification of these impedances. Since the stability analysis without verification of the modeled impedances is not reliable, next the impedance verification is given.

5.4.2 Impedance Verification

To verify the modeled impedance, the PHIL setup is implemented in Simulink as a reference with the following parameters shown in Table 5.3, and the remaining parameters are the same as in Table 5.2. Even though the EG as in section 5.2 is adopted for this section, the Z_{EG} is verified with these new parameters once again. To find the grid impedance, perturbations via $i_p(f_p)$ (Fig. 5.27) at frequencies between 100 and 1600 Hz, each of the same magnitude, are added to the current i . For each perturbation frequency, the gain and phase of the impedance are determined using the Fourier transform on the measured current and voltage at PCC. The results are displayed in orange markers in a Bode plot in Fig. 5.28. For comparison, the modeled impedance is also plotted in blue in the same Bode plot. The figure shows a good match between the simulated and calculated grid impedance; therefore, the EG impedance is verified.

Similarly, for Z_{GFL} verification, perturbations are applied to the grid voltage V_s (Fig. 5.9) in the Simulink model; the current and voltage at the PCC are measured, and the gain and phase are determined via Fourier transform. These reference gain and phase values are plotted in a Bode

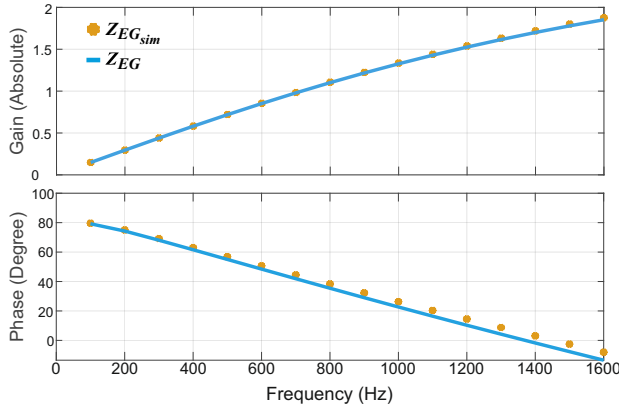


Figure 5.28: EG impedance verification

plot and compared with the calculated converter impedance Z_{GFL} shown in Fig. 5.29. Overall, the calculated converter impedance closely matches the reference impedance.

5.4.3 Stability Verification

Since the EG and GFL converter impedances have been successfully verified, as noted in 5.4.2, the stability of the setup can be assessed using the impedance ratio Z_{EG}/Z_{GFL} and the Nyquist criterion. This stability criterion applies only if the modeled sources are stable. Stability analysis is performed by varying the converter's AC-side parameters. Here, the EG impedance is changed by using the same k defined in (5.32). While Z_{L_g} is held constant, Z_s is varied via k to change the stability criterion Z_{EG}/Z_{GFL} . An increase in k reduces Z_s because Z_{L_g} is unchanged, resulting in a smaller grid resistance R_s and/or inductance L_s .

Table 5.3: PHIL simulation parameters

Parameter	Value	Unit	Parameter	Value	Unit
K_{P_i}	3	—	L_s	3.4	mH
K_{I_i}	50	—	C_{dc}	200	μ F
$K_{P_{dc}}$	0.1	—	R_s	0.143	Ω
$K_{I_{dc}}$	1	—	V_{dcn}	800	V
			V_s	310	V

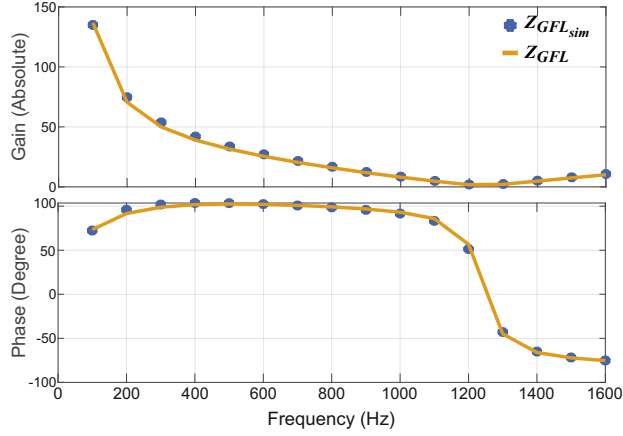


Figure 5.29: DC regulating GFL converter impedance verification

Below are two examples of different k -factors. In Fig. 5.30a, $k = 0.5$. As shown, the point $[-1, j0]$, marked with a red cross in the Nyquist diagram, is enclosed by the graph. This indicates that the system is unstable. For verification, the current i at the PCC is measured in the Simulink benchmark model. In Fig. 5.30b, the current is displayed and also shows the instability of the setup when k is 0.5. The current at the PCC is three-phase, but for clarity, only one phase is shown in this work.

When changing k to 0.7, the point $[-1, j0]$ in the Nyquist diagram is no longer encircled by the graph shown in Fig. 5.31a, indicating a stable setup. The current measured at the PCC in the benchmark is stable, as shown in Fig. 5.31b. Therefore, the Nyquist criterion-based analysis matches the benchmark measurements. Further analyses showed that the setup is unstable for k -factors below 0.5 and stable for k -factors above 0.7. There is a small error between 0.55 and 0.65: the Nyquist diagram indicates instability, but the setup remains stable. The reason for this mismatch is that the impedance model of the PHIL setup is formulated in the continuous domain. The benchmark, by contrast, is in the discrete domain. This difference for the k -factor of 0.6 can be seen in Fig. 5.32. The continuous Nyquist criterion in Fig. 5.32a predicts instability, whereas the discrete Nyquist criterion in Fig. 5.32b aligns with the Simulink. To address these mismatches, the multi-rate approach presented in Chapter 3 can be employed at the cost of increased complexity.

5.4.3.1 Source Model Impact on Impedance-based Stability Criterion

In this section, the sensitivity of the HoI parameters in the impedance-based stability analysis is examined. It is shown that when such a highly dynamic HoI is employed, the probability of unstable internal sources appearing in the impedance model of the PHIL system increases. Consequently, this may lead to errors in the validity assessment of the impedance ratio Z_{EG}/Z_{GFL} . For the sensitivity of the HoI parameters, some cases are shown graphically via Nyquist plots and time-domain responses, and for the rest, tables are used, where a checkmark indicates stability and a cross indicates instability.

Remark: In the tables, a checkmark indicates that the closed-loop system is stable according to the Nyquist criterion. For the considered cases, this corresponds to a condition where the Nyquist encirclement and the associated number of right-half-plane poles of the open-loop transfer function satisfy $N + P = 0$. Although the analysis is primarily based on Nyquist encirclements,

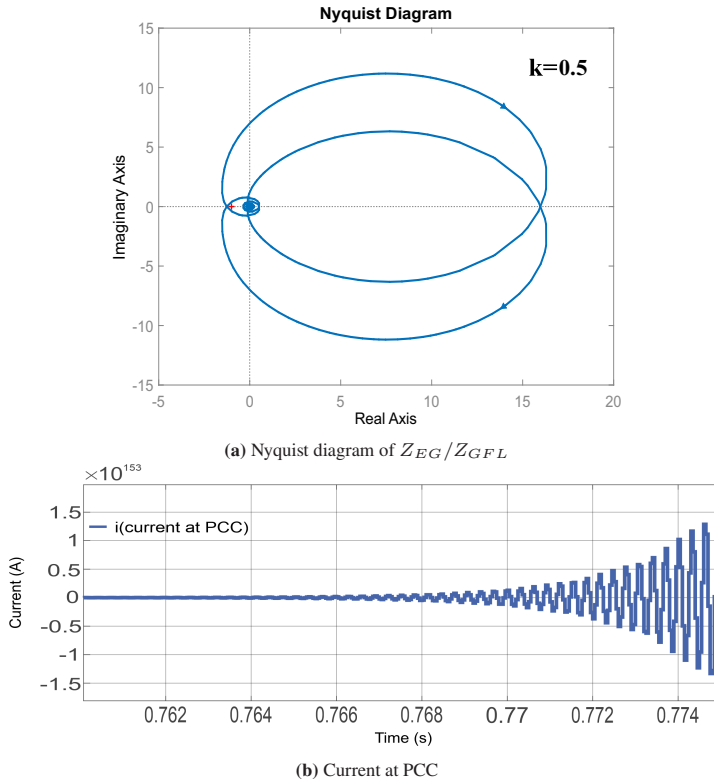
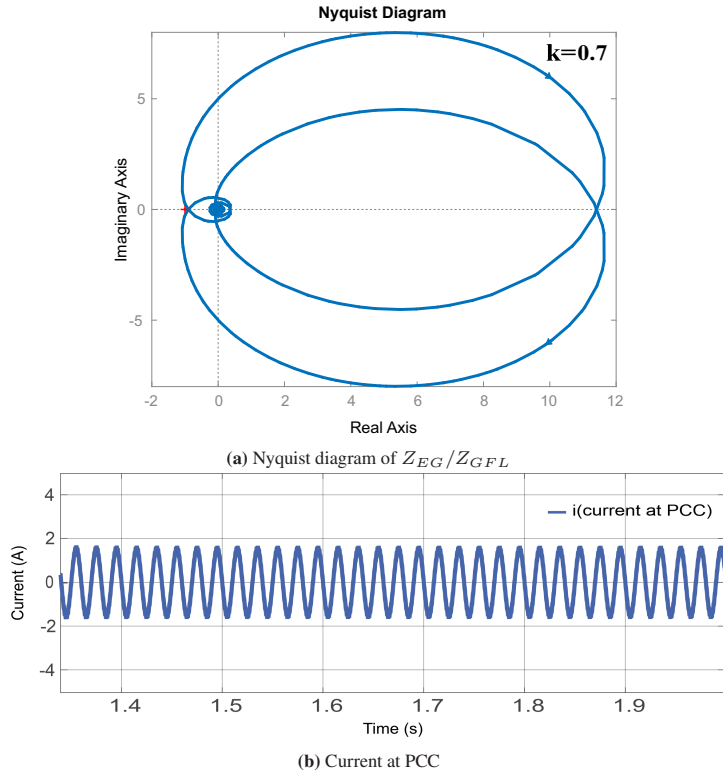
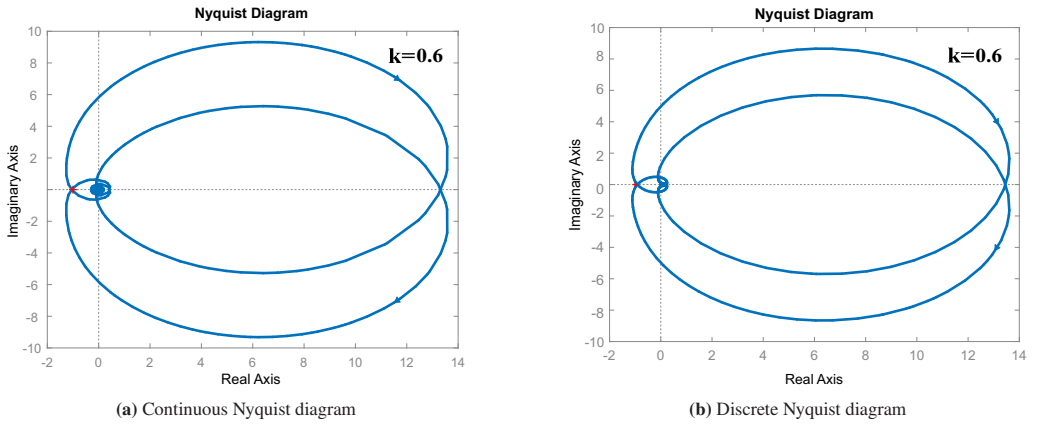


Figure 5.30: Stability analysis for $k=0.5$

Figure 5.31: Stability analysis for $k=0.7$ Figure 5.32: Nyquist criterion for $k=0.6$

additional verification, including the evaluation of P , confirms that the stability conclusions remain unchanged.

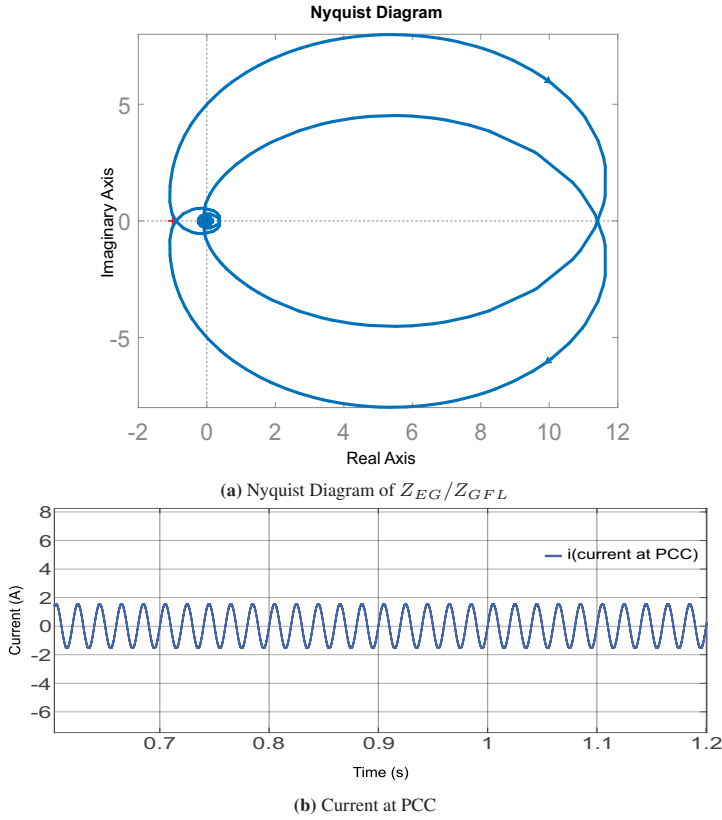


Figure 5.33: Stability analysis for $C_{dc} = 200 \mu\text{F}$

A. DC Capacitor

In this section, the size of the DC capacitor is varied. First, the setup is evaluated with a DC capacitor that has a capacitance of $200 \mu\text{F}$. In Fig. 5.33a, the Nyquist diagram of this setup is shown. It can be seen that the point $[-1, j0]$ is not encircled, and therefore, stability is predicted. This stability is confirmed by measuring the current at PCC. The result is displayed in Fig. 5.33b, which shows a stable current.

When changing the capacitance of the DC capacitor to $6 \mu\text{F}$, the Nyquist plot does not encircle the origin, indicating that the system is stable. In contrast, the time-domain result of the system is unstable, as evidenced by the benchmark current measurement in Fig. 5.34b.

In the literature, the stability criterion based on the impedance ratio was introduced under the assumption that the sources are stable. Therefore, when testing a dynamic HoI, it is necessary to

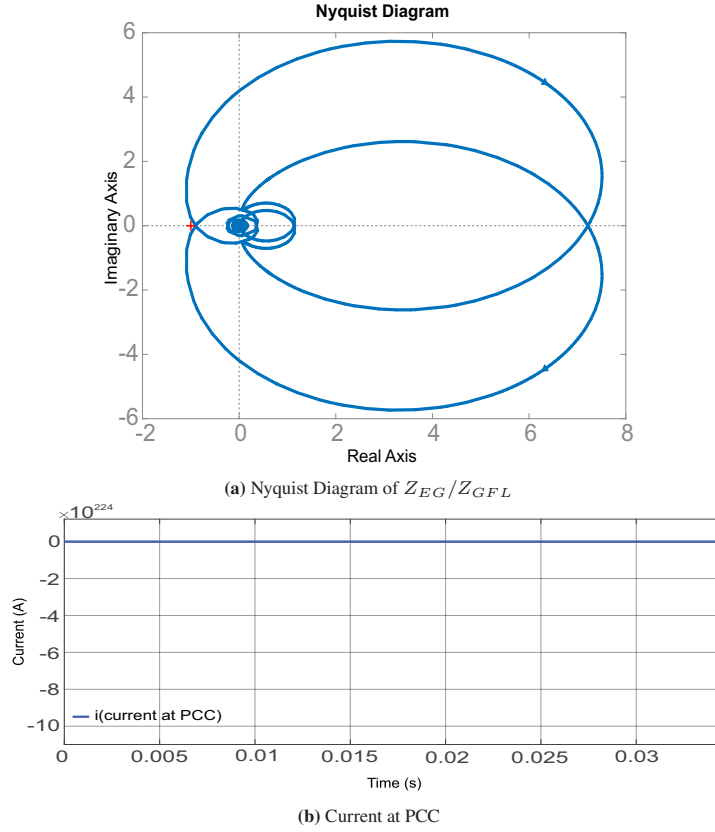


Figure 5.34: Stability Analysis for $C_{dc} = 6 \mu\text{F}$

verify whether the internal sources are stable. The impedance model of this setup consists of a single voltage source V_{EG} and a single current source i_{GFL} . Due to the presence of only passive elements in the modeled EG source, H_{EG} , it has no poles in the right half-plane in the pole-zero map, and therefore this source is internally stable. The modeled current source, on the other hand, can become unstable depending on the DC side's parameters. This instability can not be seen in the Nyquist diagram of the impedance ratio. Therefore, to determine the stability of a system, not only the impedance ratio but also the internal stability of the modeled sources must be checked.

The modeled current source of the converter side can be expressed by the following equation, as it was introduced in 5.4.1:

$$i = \frac{G_{PI,V_{dc}} \cdot G_{PI_i} \cdot T_d \cdot Y_{LCL,GFL}}{1 + G_{PI_i} \cdot T_d^2 \cdot Y_{LCL,GFL} + V_n \cdot \frac{3}{2} \cdot \frac{1}{V_{dcn}} \cdot T_d^4 \cdot Z_{dc} \cdot G_{PI,V_{dc}} \cdot G_{PI_i} \cdot Y_{LCL,GFL}} V_{dc}^* - \underbrace{\frac{T_d^2 \cdot Z_{dc} \cdot G_{PI,V_{dc}} \cdot G_{PI_i} \cdot Y_{LCL,GFL}}{1 + G_{PI_i} \cdot T_d^2 \cdot Y_{LCL,GFL} + V_n \cdot \frac{3}{2} \cdot \frac{1}{V_{dcn}} \cdot T_d^4 \cdot Z_{dc} \cdot G_{PI,V_{dc}} \cdot G_{PI_i} \cdot Y_{LCL,GFL}}}_{G_{ol}} i_L \quad (5.57)$$

To check the stability of the current source, the open-loop transfer function of the current source is used, which is defined as follows:

$$G_{ol} = G_{PI_i} \cdot T_d^2 \cdot Y_{LCL,GFL} - V_n \cdot \frac{3}{2} \cdot \frac{1}{V_{dcn}} \cdot T_d^4 \cdot Z_{dc} \cdot G_{PI,V_{dc}} \cdot G_{PI_i} \cdot Y_{LCL,GFL} \quad (5.58)$$

A DC capacitor with a capacitance of 6 μF is used to verify the second stability criterion. In Fig. 5.35a, the Nyquist diagram of the ratio Z_{EG}/Z_{GFL} is displayed. The point $[-1, j0]$ is not encircled, which indicates a stable system. However, when G_{ol} is checked with the Nyquist criterion, Fig. 5.35b shows that the internal source is unstable as the point $[-1, j0]$ is encircled.

The size of the DC capacitor has been varied for further investigation, and the behaviors of the stability criterion and the internal source are recorded in Table 5.4. In the first column, the DC capacitor size is displayed, followed by the source stability and the impedance-ratio stability. In the last column, the stability assessment of the modeled setup in Simulink is presented, which serves as the benchmark. As shown, the Nyquist plot of the impedance ratio alone does not reveal the benchmark's stability when the current source is internally unstable, i.e., for capacitor sizes below 14.3 μF .

This additional Nyquist analysis provides an indirect assessment of the right-half-plane poles of the overall system (P in section 5.1.1). Rather than explicitly evaluating P in the Nyquist criterion of the impedance ratio, the internal dynamics of the GFL converter are analyzed separately. This provides a more physically interpretable way to identify potential instabilities originating in the source subsystem that are not captured by impedance interactions alone.

B. Voltage Controller

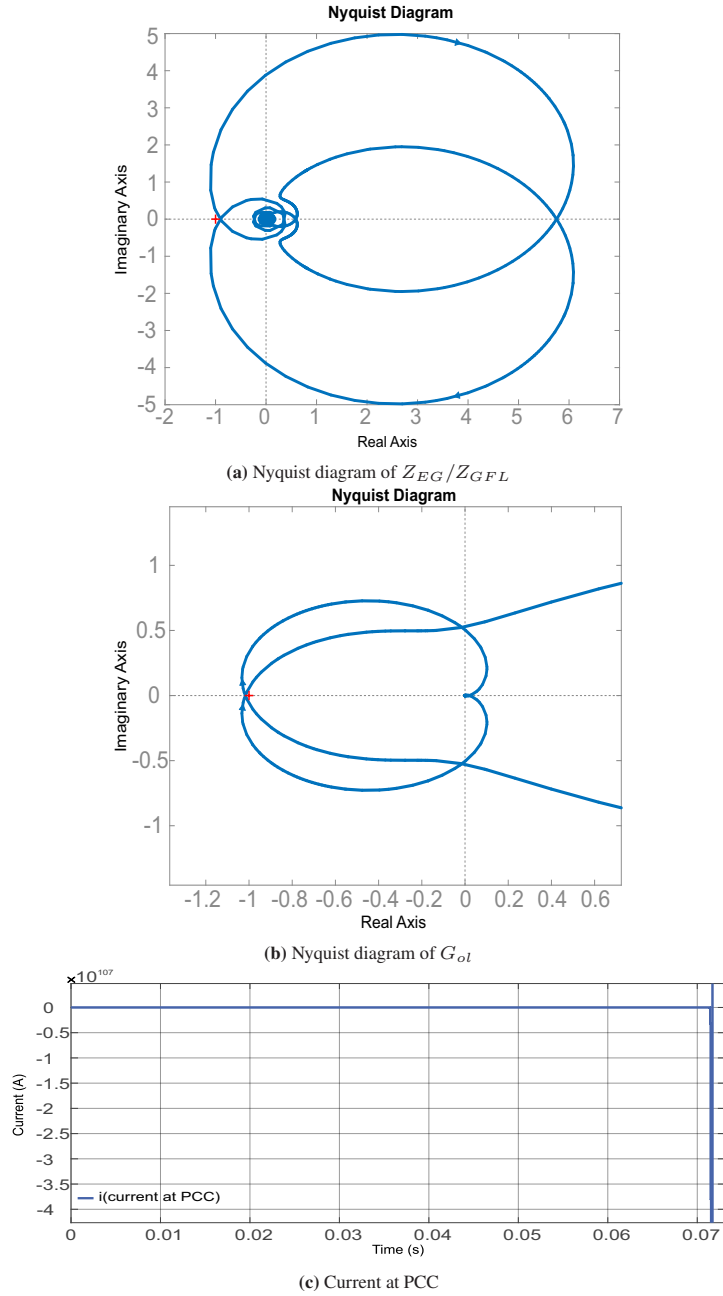
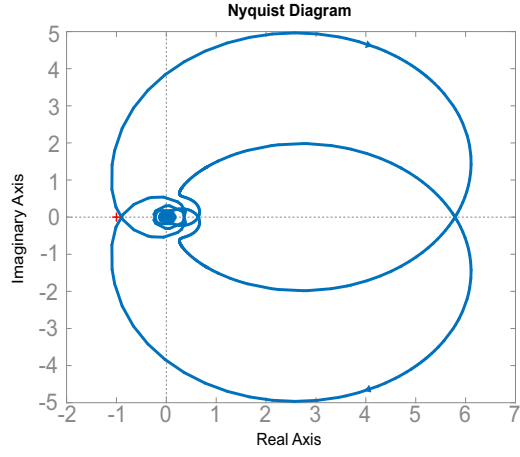
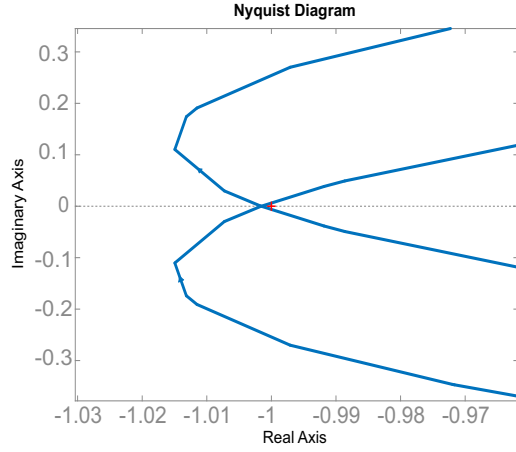
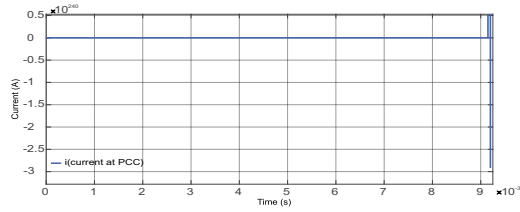
Figure 5.35: Stability analysis for $C_{dc} = 6 \mu\text{F}$

Table 5.4: Comparison of Stability for Different DC Capacitors

C_{dc}	G_{ol}	Z_{EG}/Z_{GFL}	Benchmark
400 μF	✓	✓	✓
200 μF	✓	✓	✓
50 μF	✓	✓	✓
20 μF	✓	✓	✓
14.3 μF	✓	×	×
6 μF	×	✓	×
3 μF	×	✓	×
1 μF	×	✓	×

For further verification, the voltage controller parameter is varied to examine the response of the impedance ratio Z_{EG}/Z_{GFL} and the open-loop transfer function G_{ol} in the Nyquist diagram. The proportional gain of the voltage controller is varied, and stability is assessed using the Nyquist criterion. The graph of the impedance ratio Z_{EG}/Z_{GFL} , on the other hand, does not encircle the point $[-1, j0]$ in the Nyquist diagram in Fig. 5.36a when $K_{P_{dc}}$ is 3.2. However, the graph of G_{ol} encircles the critical point shown in Fig. 5.36b. This indicates that the modeled current source in the converter's Norton equivalent is internally unstable. The measured current at the benchmark is shown in Fig. 5.36c, indicating that the current at the PCC is unstable.

Stability verification was performed for various proportional gains $K_{P_{dc}}$, and the results are presented in Table 5.5. The PHIL setup is stable when the Nyquist plot of the source and impedance ratio is stable. When the source is stable, and the impedance ratio is unstable, as in the case of a $K_{P_{dc}}$ of 1.4, the system is unstable. If the open-loop transfer function G_{ol} is unstable, the Simulink model is unstable. These cases are shown in the last three rows of the table, supporting the assumption that, when the modeled source is unstable, relying solely on the impedance ratio to assess stability is erroneous.

(a) Nyquist diagram of Z_{EG}/Z_{GFL} (b) Nyquist diagram of G_{ol} 

(c) Current at PCC

Figure 5.36: Stability analysis for $K_{Pdc}=3.2$

C. Current Controller

Table 5.5: Comparison of Stability for Different Voltage Controller Parameters

$K_{P_{dc}}$	G_{ol}	Z_{EG}/Z_{GFL}	Benchmark
0.01	✓	✓	✓
0.05	✓	✓	✓
0.1	✓	✓	✓
1	✓	✓	✓
1.4	✓	×	×
3.2	×	✓	×
5	×	✓	×
10	×	✓	×

The current controller parameter is the last HoI parameter, whose sensitivity is analyzed to assess the stability of the PHIL setup. In Table 5.6, the results of the stability analysis are shown when K_{P_i} , the proportional gain of the current controller, is changed. The first two rows show that if the modeled source and the impedance ratio are stable, the combined stability criterion predicts stability. This prediction is consistent with the Simulink model, which is also stable. However, when the open-loop transfer function G_{ol} is not internally stable, the assumption of a negligible number of right-half-plane (RHP) poles is no longer valid. As shown in Table 5.6 for $K_{P_i} = 9, 12, 15, 20$, although the modeled source is unstable, the benchmark system may remain stable or unstable depending on the interaction with the grid. In particular, while some cases exhibit stabilization due to the grid interaction, others do not, even when the impedance-ratio-based Nyquist evaluation yields $N + P = 0$. These observations indicate that, for internally unstable subsystems, the impedance ratio may no longer fully represent the closed-loop system dynamics. As a result, even when accounting for $P \neq 0$, the Nyquist-based stability assessment using the impedance ratio may not consistently predict the benchmark behavior. Therefore, classical impedance-based stability criteria, which implicitly assume $P = 0$ and the internal stability of the subsystems, may lead to misleading conclusions when these assumptions are violated.

5.5 Summary

In this chapter, impedance-based modeling and stability analysis, commonly applied to study converter integration with the grid, are employed to evaluate the stability of a PHIL setup using a GFL converter. The stability condition is determined using the Nyquist criterion, where the

Table 5.6: Comparison of stability for different current controller parameters

K_{P_i}	G_{ol}	Z_{EG}/Z_{GFL}	Benchmark
1	✓	✓	✓
3	✓	✓	✓
9	×	✓	✓
12	×	✓	✓
15	×	✓	✓
20	×	✓	✓
30	×	✓	×
45	×	×	×

open-loop transfer function corresponds to the impedance ratio at the PCC, Z_{EG}/Z_{GFL} . The analysis considers the effects of PHIL interface dynamics and delays, the converter controller, and the LCL filter. The modeled impedances are verified using Bode plots obtained from Simulink simulations and experimental measurements. Furthermore, time- and frequency-domain responses are compared to confirm the validity of the impedance model. The results demonstrate that this approach can ensure PHIL stability and prevent erroneous analyses and potential hardware damage. Moreover, based on the perturbation and measurement methods used for impedance verification, the stability can still be evaluated even if an accurate model of the HoI is not available.

Then, the influence of sensor placement on system stability is also investigated. Since the placement of voltage and current sensors in GFL converters varies by application, understanding their effects is particularly important for PHIL users. Therefore, a GFL converter with an LCL filter acting as the HoI is analyzed under four different sensor placement configurations. For each case, the converter impedance is analytically modeled and verified through Simulink simulations. The stability of each configuration is then assessed using Nyquist plots of the impedance ratio and confirmed through time-domain simulations. The results indicate that the location of the voltage sensor affects the stability margin, whereas the location of the current sensor has only a minor influence. Specifically, placing the voltage sensor across the filter capacitor improves system stability compared with placing it at the PCC. These findings provide practical guidance for PHIL users, enabling them to balance stability requirements with application-specific constraints without modifying HoI side parameters. However, since the sensitivity of HoI parameters is typically unknown to PHIL operators, awareness of their potential impact on overall system stability remains essential.

Finally, the impact of a GFL converter with a dynamic DC link as HoI is investigated. The GFL converter is modeled with a DC-link capacitor and a cascaded DC voltage controller. A new impedance model for this converter is derived and validated by comparison with a benchmark MATLAB/Simulink model. When DC-link dynamics are considered, both the source subsystem's internal dynamics and the Nyquist stability of the impedance ratio Z_{EG}/Z_{GFL} must be evaluated. If the internal sources are stable, the impedance-based Nyquist analysis provides a valid stability criterion: zero Nyquist encirclements of the impedance ratio indicate a stable PHIL setup, and nonzero encirclements indicate instability. However, if the internal source dynamics become unstable, the impedance-ratio-based assessment alone becomes invalid. In such cases, the overall system behavior may deviate from the impedance-based prediction, and even stable responses may be observed in simulation due to interactions within the complete system. Therefore, relying solely on the impedance ratio may lead to misleading conclusions, and particular care must be taken to avoid unstable internal dynamics during practical experiments. In general, the Nyquist criterion ($Z = N + P$) should be applied to the impedance ratio. In particular, when strong internal dynamics are present, the number of right-half-plane poles P may become non-zero, which can influence the overall stability assessment.

6 Ideal Transformer Algorithms for Grid-Converter Testing

Several IAs are proposed in the section 2.4 to address the trade-off between stability and accuracy. Among common IAs, the ITM is known for its accuracy, high bandwidth, and simplicity; however, the stability of ITM PHIL is limited to MoI/HoI impedances, shown only for passive-load testing as HoI. The ratio is inverted depending on the ITM mode, i.e., V-ITM or C-ITM, and therefore stability can be restored by changing the ITM mode. However, the transition from V-ITM to C-ITM for grid-converter testing remains absent from the literature. Traditionally, grid-following converters are modeled as current sources; therefore, the EG in the PHIL system is modeled as a voltage source. This implies that the amplifier should be operated in voltage mode; therefore, the proper ITM is V-ITM. Whether it is possible to test a GFL converter via C-ITM and a GFM converter via V-ITM has not yet been investigated. If so, the stability of PHIL for grid-converter testing can be restored by changing the ITM if one is unstable. For example, if the EG impedance is too high, then it can lead to V-ITM instability. In that case, stabilization solutions could involve changing the HoI parameters to increase its output impedance, but this is not possible if the HoI is a black box or if it is provided by a customer (i.e., PHIL operators are not allowed to change its parameters). Other solutions could be adding interface impedances or lowering the low-pass filter bandwidth, but they deteriorate accuracy as discussed in Chapter 2. Reducing the DRTS time step to decrease the loop delay and stabilize the system can lead to overrun when the MoI is complex. Therefore, similar to the approach proposed for testing passive loads, this chapter examines both ITM modes, V-ITM and C-ITM (and vice versa), to restore the PHIL system stability when the HoI is a grid converter. Each ITM is taken to test both GFL and GFM converters in four scenarios given in Table 6.1.

The impedance models of both the EG, comprising the DRTS, PA, interfaces, and the converter, including its controller, are derived and validated across four distinct test cases. The obtained impedance models are then used to determine the systems stability conditions based on the voltage-source and current-source output-impedance criteria commonly used in converter-integration stability analysis (section 5.1). All scenarios are implemented in MATLAB/Simulink to serve as a benchmark for the impedance-based stability verifications. The modeled impedances are

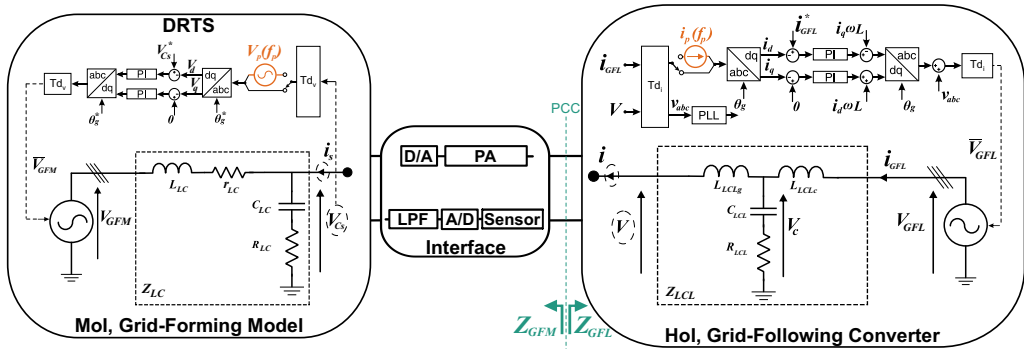
Table 6.1: Overview of considered PHIL configurations

Configuration Case	MoI	HoI	IA
Configuration I	GFM Converter	GFL Converter	V-ITM
Configuration II	GFM Converter	GFL Converter	C-ITM
Configuration III	GFL Converter	GFM Converter	V-ITM
Configuration IV	GFL Converter	GFM Converter	C-ITM

verified against measured impedances using perturbation signals and the Fourier transform in Simulink, and for the first scenario, experimentally. After verifying the impedances, the stability criterion is given via the Nyquist plot for each case. The Nyquist plot is then compared with the time-domain responses from the benchmark in Simulink to verify the stability analysis. The following section derives the impedance model for each case based on the transfer functions of the individual components.

6.1 Impedance Modeling

The impedance model of the PHIL system is derived using the relationship between the PCC voltage and current, along with the transfer functions of each component on both the EG and converter sides. When testing a GFL converter as the HoI, a GFM converter is modeled in the DRTS, and vice versa. All components are modeled using transfer functions and/or delays, while assuming an ideal PLL.

**Figure 6.1:** Case I and II, Selected PHIL Scheme

6.1.1 Configuration I

According to Fig. 6.1, an average model of a controlled-voltage source with an LC filter is implemented as MoI. Using the V-ITM, V_{Cs} is sent to the PA via a D/A converter and amplified in the PA output, resulting in V at the PCC. A GFL converter with an LCL filter is modeled in the HoI section, which is synchronized with V and its current, i_{GFL} , is controlled by PI controllers. Another pair of PI controllers with abc-dq transformations is tuned to control the LC filter output voltage, V_{Cs} , in the GFM converter. In this case, frequency is generated using a digital internal clock. For both sides, ADC and PWM impacts are modeled as a single sampling-time delay, T_d , at the input and at the output. The following equations describe the emulated-grid side of the PCC, where the goal is to find the Z_{GFM} , i.e., the relation between V and i . From Fig. 6.1, the following equations can be achieved. For simplicity, the (s) is not shown in the equations.

$$V_{Cs} = V_{GFM} \cdot H_v + i \cdot G_{LPF} \cdot G_{T_{fb}} \cdot H_i + V_{GFM} \quad (6.1)$$

$$H_v = Z_{rLLC} / Z_{LC} \quad (6.2)$$

$$H_i = \frac{Z_{RC_{LC}} \cdot Z_{rLLC}}{Z_{RC_{LC}} + Z_{rLLC}} \quad (6.3)$$

$$G_{LPF} = \frac{\omega_c}{1 + \omega_c \cdot s} \quad (6.4)$$

$$Z_{rLLC} = r_{LC} + L_{LC} \cdot s \quad (6.5)$$

$$Z_{RC_{LC}} = R_{LC} + \frac{1}{C_{LC} \cdot s} \quad (6.6)$$

$$Z_{LC} = Z_{rLLC} + Z_{RC_{LC}} \quad (6.7)$$

$$G_{T_{fb}} = e^{-s(T_{fb})}, \quad T_{fb} = T_{Sens} + T_{A/D} + T_{DRTS} \quad (6.8)$$

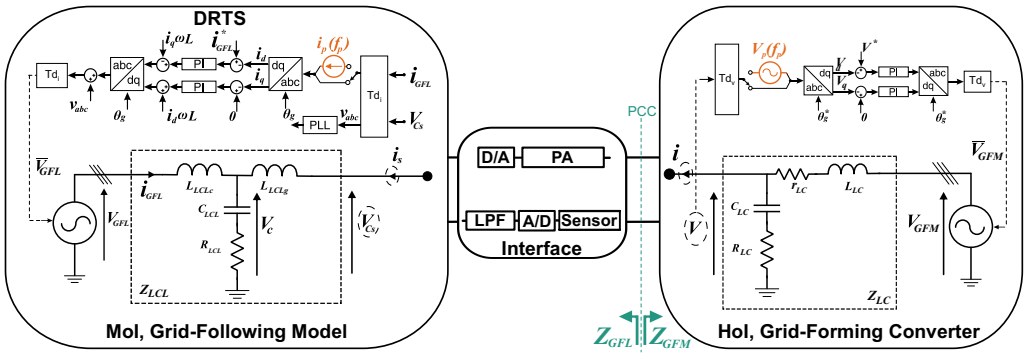


Figure 6.2: Case III and IV, Selected PHIL Scheme

Where H_v and H_i are the transfer functions, coefficients of GFM converter output voltage and PCC current, respectively. G_{LPF} is the low-pass filter used in the feedback, ω_c is the cut-off angular frequency, L_{LC} , r_{LC} , C_{LC} , R_{LC} , are the inductor, internal resistor, capacitor and its series resistor of the LC filter. The sensor delay T_{Sens} , A/D delay $T_{A/D}$, and DRTS delay T_{DRTS} in the feedback are summed in T_{fb} which the transfer function is given in $G_{T_{fb}}$. The relation between V and V_{Cs} can be found in the forward path in the interface section:

$$V = V_{Cs} \cdot G_{PA_v} \cdot G_{T_{fw}} \quad (6.9)$$

$$G_{T_{fw}} = e^{-s(T_{fw})}, \quad T_{fw} = T_{DRTS} + T_{D/A} + T_{PA} \quad (6.10)$$

$$G_{PA_v} = \frac{1}{(1/\omega_0^2)s^2 + (2 \cdot D/\omega_0)s + 1} \quad (6.11)$$

Similar to $G_{T_{fb}}$, $G_{T_{fw}}$ includes the DRTS, D/A and PA delays. The dynamics of the linear PA can be described as in (6.11), where ω_0 and D are the natural frequency and damping factor of the selected PA (Chapter 2). Expanding V_{GFM} , there is an internal voltage loop in the GFM converter control as shown in the figure, which can be described as follows:

$$V_{GFM} = (V_{Cs}^* - V_{Cs} \cdot T_{d_v}) G_{PI_v} \cdot T_{d_v} \quad (6.12)$$

$$G_{PI_v} = K_{P_v} + K_{I_v}/s \quad (6.13)$$

$$T_{d_v} = e^{-s(T_{d_{PI_v}})} \quad (6.14)$$

V_{Cs}^* is the voltage setpoint over the capacitor, G_{T_d} is the controller delay, and G_{PI_v} describes the dynamics of the PI controller. K_{P_v} and K_{I_v} are the proportional and integral coefficients of the voltage controller. From (6.9) and (6.14), V_{Cs} can be substituted to obtain:

$$V_{GFM} = \left(V_{Cs}^* - \frac{V}{G_{PA_v} \cdot G_{T_{fw}}} \cdot T_{d_v} \right) G_{PI_v} \cdot T_{d_v} \quad (6.15)$$

Using (6.1) and (6.9) gives:

$$i = \frac{1}{G_{LPF} \cdot G_{T_{fb}} \cdot H_i} \left[\frac{V}{G_{PA_v} \cdot G_{T_{fw}}} - (1 + H_v) V_{GFM} \right] \quad (6.16)$$

Finally, substituting (6.15) into (6.16) and collecting terms in V_{Cs}^* and V , the impedance model of the emulated GFM converter, including the interfaces of PHIL, can be described as:

$$i = \underbrace{-\frac{(1 + H_v) G_{PI_v} \cdot T_{d_v}}{G_{LPF} \cdot G_{T_{fb}} \cdot H_i}}_{H_{V_{Cs}, I}} V_{Cs}^* + \underbrace{\frac{1 + (1 + H_v) G_{PI_v} \cdot T_{d_v}^2}{G_{LPF} \cdot G_{T_{fb}} \cdot H_i \cdot G_{PA_v} \cdot G_{T_{fw}}}}_{Y_{GFM, I}} V \quad (6.17)$$

where the relation between i and V , describes the impedance model. To avoid confusion among Z_{GFM_s} in the other cases, the case index is added, $Z_{GFM,I}$:

$$Z_{GFM,I} = \frac{G_{T_{fb}} \cdot G_{LPF} \cdot H_i \cdot G_{T_{fw}} \cdot G_{PA_v}}{1 + T_{d_v}^2 \cdot G_{PI_v} (H_v + 1)} \quad (6.18)$$

It can be seen from (6.18) that not only the virtual impedance, Z_{LC} , created in DRTS, but also the PI controller dynamics and delay, the interface delays, and PA and low-pass filter dynamics are included in the impedance model. A similar approach is taken to obtain the Z_{GFL} , this time finding the relation between V and i from the converter side. From the internal current control loop of the GFL converter, the following equations can be achieved:

$$V_{GFL} = ((i_{GFL}^* - i_{GFL} \cdot T_{d_i}) G_{PI_i} + V \cdot T_{d_i}) T_{d_i} \quad (6.19)$$

$$G_{PI_i} = K_{P_i} + K_{I_i}/s \quad (6.20)$$

$$T_{d_i} = e^{-s(T_{d_{PI_i}})} \quad (6.21)$$

$$i_{GFL} = V_{GFL} \cdot Y_1 - V \cdot Y_2 \quad (6.22)$$

where G_{PI_i} is the transfer function of the current controller, and Y_1 and Y_2 are the transfer functions describing the influence of GFL and GFM converters on generating the i_{GFL} :

$$Y_1 = \frac{Z_{LCL_g} + Z_{C_{LCL}}}{Z_{LCL_g} \cdot Z_{C_{LCL}} + Z_{LCL_c} \cdot Z_{C_{LCL}} + Z_{LCL_g} \cdot Z_{LCL_c}} \quad (6.23)$$

$$Y_2 = \frac{Z_{C_{LCL}}}{Z_{LCL_g} \cdot Z_{C_{LCL}} + Z_{LCL_c} \cdot Z_{C_{LCL}} + Z_{LCL_g} \cdot Z_{LCL_c}} \quad (6.24)$$

where,

$$Z_{LCL_c} = r_{LCL_c} + L_{LCL_c} \cdot s \quad (6.25)$$

$$Z_{LCL_g} = r_{LCL_g} + L_{LCL_g} \cdot s \quad (6.26)$$

$$Z_{C_{LCL}} = R_{LCL} + 1/(C_{LCL} \cdot s) \quad (6.27)$$

r_{LCL_c} , L_{LCL_c} , r_{LCL_g} , L_{LCL_g} are the converter side and grid side inductors with its internal resistors, respectively, R_{LCL} and C_{LCL} , are the LCL capacitor and its series resistor. Similar equation as in (6.22), holds for the PCC current:

$$i = V \cdot Y_3 - V_{GFL} \cdot Y_2 \quad (6.28)$$

where Y_3 is:

$$Y_3 = \frac{Z_{LCL_c} + Z_{C_{LCL}}}{Z_{LCL_g} \cdot Z_{C_{LCL}} + Z_{LCL_c} \cdot Z_{C_{LCL}} + Z_{LCL_g} \cdot Z_{LCL_c}} \quad (6.29)$$

By eliminating V_{GFL} from substituting (6.22) into (6.19), and then inserting the result into (6.28). relation between i , V and i_{GFL}^* will be:

$$i = \underbrace{\left(Y_3 - \frac{Y_2 \cdot T_{d_i}^2 (1 + Y_2 \cdot G_{PI_i})}{1 + Y_1 \cdot G_{PI_i} \cdot T_{d_i}^2} \right)}_{Y_{GFL,I}} V - \underbrace{\frac{Y_2 \cdot G_{PI_i} \cdot T_{d_i}}{1 + Y_1 \cdot G_{PI_i} \cdot T_{d_i}^2}}_{H_{i_{GFL,I}}^*} i_{GFL}^* \quad (6.30)$$

Therefore, the impedance of the GFL converter is achieved:

$$Z_{GFL,I} = \frac{1}{-\frac{(1 + G_{PI_i} \cdot Y_2) T_{d_i}^2 \cdot Y_2}{1 + Y_1 \cdot T_{d_i}^2 \cdot G_{PI_i}} + Y_3} \quad (6.31)$$

From (6.31), it can be seen that, in addition to the LCL impedance, the current controller and digital controller delays appear in the impedance model.

6.1.2 Configuration II

In the second case, the GFM and GFL converters remain in the same places as in 6.1.1, but this time the interface is chosen to be C-ITM. Although GFM converters are modeled typically as voltage sources, one goal of this work is to show whether, due to the configuration of HoI, e.g., the output impedance of GFL converter is too low, or if GFL converter is connected to a weak grid, it is possible to emulate the GFM converter as a current source and invert the stability criteria or not. Therefore, in this case, the HoI impedance from 6.1.1 remains the same, and due to a change

of the amplifier mode, the impedance of the EG, GFM converter will be changed as follows. The output current, i_s , in Fig. 6.1, is given to the amplifier, which is now a current source:

$$i_s = V_{GFM} \cdot Y_{rLLC} - V_{Cs} \cdot Y_4 \quad (6.32)$$

$$Y_4 = Y_{rLLC} + Y_{rCLC} \quad (6.33)$$

$$Y_{rLLC} = 1/Z_{rLLC}, \quad Y_{rCLC} = 1/Z_{rCLC} \quad (6.34)$$

$$V_{GFM} = (V_{Cs}^* - V_{Cs} \cdot T_{dv}) G_{PI_v} \cdot T_{dv} \quad (6.35)$$

$$i = i_s \cdot G_{fw} \quad (6.36)$$

$$G_{fw} = G_{Tfw} \cdot G_{PA_i} \cdot G_{Tfw} \quad (6.37)$$

The transfer function of the amplifier in the current mode is (taken from the manufacturer, more details in the Chapter 2:

$$G_{PA_i} = \frac{1 + \frac{s}{\omega_Z}}{1 + \frac{2 \cdot \delta_P}{\omega_P} \cdot s + \frac{s^2}{\omega_P^2}} \quad (6.38)$$

which ω_P , and ω_Z are pole and zero angular frequency, and δ_P is the damping ratio. The following equations connect the voltage setpoint sent to the amplifier to the PCC voltage:

$$V_{Cs} = V \cdot G_{fb} \quad (6.39)$$

$$G_{fb} = G_{Tfb} \cdot G_{LPF} \quad (6.40)$$

From (6.32), (6.35), (6.36), (6.39), the impedance model of emulating a GFM converter with a current source is achieved as:

$$i = - \underbrace{G_{fw} \cdot G_{fb} (G_{PI_v} \cdot T_{dv}^2 \cdot Y_{rLLC} + Y_4)}_{Y_{GFM,II}} V + \underbrace{G_{fw} \cdot G_{PI_v} \cdot T_{dv} \cdot Y_{rLLC}}_{H_{V_{Cs,II}^*}} V_{Cs}^* \quad (6.41)$$

which $H_{V_{Cs,II}^*}$ is the coefficient of the source model, and $Y_{GFM,II}$ is the admittance model including the voltage controller, interfaces, and delays.

6.1.3 Configuration III

As shown in Fig. 6.2, in this section, the positions of GFM and GFL converters are reversed: GFL is now emulated using the V-ITM, and GFM converter is the HoI. The PCC variables are

denoted by the same letters, and the following equations are derived using the same approach as in the previous cases.

$$V_{Cs} = i_s \cdot Z_{LC_{LCL}} + i_{GFL} \cdot Z_{C_{LCL}} \quad (6.42)$$

$$Z_{LC_{LCL}} = Z_{LC_{LCL_c}} + Z_{C_{LCL}} \quad (6.43)$$

$$V_{GFL} = (i_{GFL}^* - i_{GFL} \cdot T_{d_i}) G_{PI_i} \cdot T_{d_i} + V_{Cs} \cdot T_{d_i}^2 \quad (6.44)$$

$$i_{GFL} = V_{GFL} \cdot Y_{LC_{LCL}} - i_s \cdot H_{i_s} \quad (6.45)$$

$$Y_{LC_{LCL}} = 1/Z_{LC_{LCL}} \quad (6.46)$$

$$H_{i_s} = Z_{C_{LCL}} / (Z_{C_{LCL}} + Z_{LC_{LCL_c}}) \quad (6.47)$$

$$V = V_{Cs} \cdot G_{fw} \quad (6.48)$$

$$i_s = i \cdot G_{fb} \quad (6.49)$$

Using (6.42), (6.44), (6.45), (6.48), (6.49), the impedance model of this case is calculated, and in packet form, it is shown as:

$$i = \frac{A_2}{A_0 \cdot A_1} V - \frac{A_3}{A_0 \cdot A_1} i_{GFL}^* \quad (6.50)$$

where,

$$A_0 = G_{fb} \cdot G_{fw} \quad (6.51)$$

$$A_1 = Z_{LC_{LCL}} (1 + G_{PI_i} \cdot G_{T_d}^2 \cdot Y_{LC_{LCL}}) - H_{i_s} \cdot Z_{C_{LCL}} \quad (6.52)$$

$$A_2 = 1 + Y_{LC_{LCL}} \cdot G_{T_d}^2 (G_{PI_i} - Z_{C_{LCL}}) \quad (6.53)$$

$$A_3 = G_{PI_i} \cdot G_{T_d} \cdot Y_{LC_{LCL}} \cdot Z_{C_{LCL}} \quad (6.54)$$

The impedance transfer function is then achieved:

$$Z_{GFL,III} = \frac{A_0 \cdot A_1}{A_2} \quad (6.55)$$

and for the GFM converter impedance the i and V relation yields as:

$$V_{GFM} = (V^* - V \cdot T_{dv}) G_{PIv} \cdot T_{dv} \quad (6.56)$$

$$i = V_{GFM} \cdot Y_{rLLC} - V \cdot Y_5 \quad (6.57)$$

$$Y_{rLLC} = 1/Z_{rLLC} \quad (6.58)$$

$$Y_5 = (Z_{rLLC} + Z_{CLC}) / (Z_{rLLC} \cdot Z_{CLC}) \quad (6.59)$$

$$i = \underbrace{-(G_{PIv} \cdot Y_{rLLC} \cdot T_{dv}^2 + Y_5)}_{Y_{GFM,III}} V + \underbrace{G_{PIv} \cdot T_{dv} \cdot Y_{rLLC}}_{H_{v^*,III}} \cdot V^* \quad (6.60)$$

$$Z_{GFM,III} = -\frac{1}{G_{PIv} \cdot Y_{rLLC} \cdot T_{dv}^2 + Y_5} \quad (6.61)$$

6.1.4 Configuration IV

And finally, the GFL converter in the DRTS is emulated via a current source mode, which makes the Z_{GFL} different while the Z_{GFM} remains the same as in case 6.1.3.

$$V_{GFL} = (i_{GFL}^* - i_{GFL} \cdot T_{di}) G_{PIi} \cdot T_{di} + V_{Cs} \cdot T_{di}^2 \quad (6.62)$$

$$i_s = V_{GFL} \cdot Y_1 \cdot H_{ig} - V_{Cs} \cdot Y_3 \quad (6.63)$$

$$H_{ig} = Z_{CLCL} / (Z_{CLCL} + Z_{LCLg}) \quad (6.64)$$

$$i_{GFL} = V_{GFL} \cdot Y_1 - V_{Cs} \cdot Y_3 \cdot H_{is} \quad (6.65)$$

$$i = i_s \cdot G_{fw} \quad (6.66)$$

$$V_{Cs} = V \cdot G_{fb} \quad (6.67)$$

In C-ITM, G_{PA_i} in (6.38) should be used in G_{fw} . Rearranging the equations given above will result in:

$$i = \frac{A_0 \cdot A_4}{A_6} V + \frac{A_5}{A_6} i_{GFL}^* \quad (6.68)$$

$$A_4 = H_{is} \cdot Y_1 \cdot T_{di}^2 [1 + Y_3 \cdot (H_{is} - 1) G_{PIi}] - Y_3 \quad (6.69)$$

$$A_5 = G_{fw} \cdot Y_1 \cdot H_{is} \cdot G_{PIi} \cdot T_{di} \quad (6.70)$$

$$A_6 = 1 + Y_1 \cdot H_{is} \cdot G_{PIi} \cdot T_{di}^2 \quad (6.71)$$

and therefore the impedance of the GFL converter in the final case is:

$$Z_{GFL,IV} = \frac{A_6}{A_0 \cdot A_4} \quad (6.72)$$

In the following section, the modeled impedances of this section are verified using perturbations and measurements in a wide frequency range.

6.2 Model Verification

In this section, the frequency responses of the modeled impedances of each case are compared with the measured impedances in MATLAB/Simulink. Setups shown in Fig. 6.1 and Fig. 6.2 are implemented in Simulink, and perturbations are applied using perturbation sources shown in orange, at the frequency range of 100-2000 Hz. The simulation parameters are given in the Table 6.2. Although some of the values may not reflect standard operating conditions, they demonstrate the capability and stability of one ITM (voltage- or current-type) in scenarios where the other becomes unstable. To measure the impedance of the HoI, the perturbation source implemented in the MoI is activated, i.e., the perturbation is applied from the opposite subsystem. The impedance measurement is performed while the simulation is running, i.e., the main source (50 Hz) is already exciting the system. The responses of each perturbation at PCC current and voltage are measured and given to the Fourier Transform. The achieved gain and phase of each perturbation signal are then plotted together with the frequency response of the impedances in each case in Bode plots given from Fig. 6.3 to Fig. 6.8. It should be noted that the impedance of the HoI is identical within each pair of cases. Therefore, it is shown only once for Cases I-II and Cases III-IV.

The proximity of the gains and phases at each frequency for all the impedances will prove that the modeled impedances in section 6.1 are correct for the desired frequencies. For example, in the modeling section, it is assumed that the θ_{grid} generated by GFM converter is fixed, and therefore the PLL impact is present in the benchmark (Simulink model) but is not considered in the impedance of GFL converter. However, from the impedance verifications in this section, it can be seen that ignoring the PLL impact does not affect the modeled impedance in the given frequency range, where the converter controllers, interface dynamics, and delays are contributing. In the following section, the impedance-based stability criterion is verified using the Nyquist criterion applied to the modeled impedance ratios.

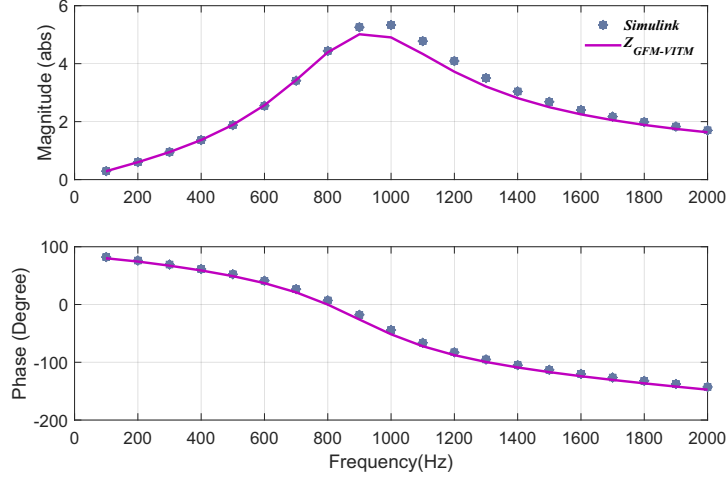
Table 6.2: PHIL simulation parameters

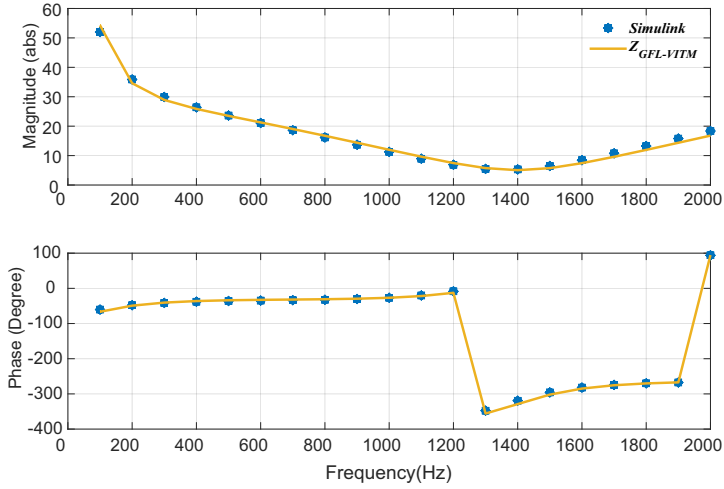
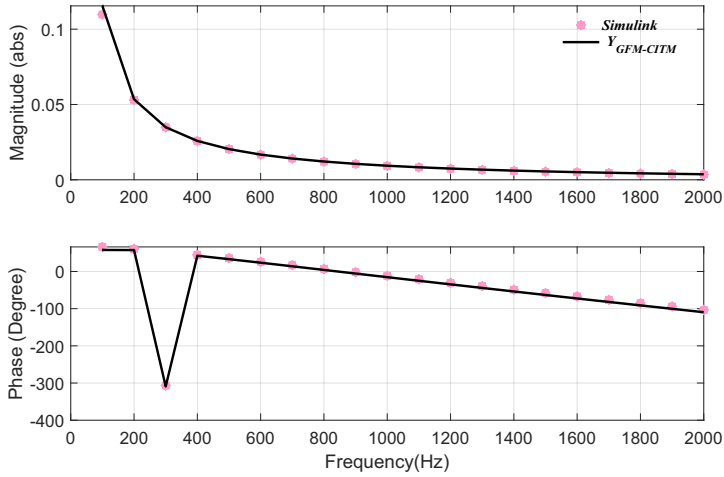
(a) Control and system parameters

Config	$T_s, T_{DRTS}, T_{d_i}, T_{d_v}$ [μ s]	$T_{A/D}$ [μ s]	$T_{D/A}$ [μ s]	T_{PA} [μ s]	T_{sens} [μ s]	$\omega_c/2\pi$ [rad/s]	$\omega_0/2\pi$ [rad/s]	$\omega_p/2\pi$ [rad/s]	$\omega_z/2\pi$ [rad/s]	δ	D
I	50	2	3	1.5	3	2000	18000	-	-	-	0.9
II	50	2	3	1.6	3	2000	-	55000	10000	0.77	-
III	50	2	3	1.5	3	2000	18000	-	-	-	0.9
IV	50	2	3	1.6	3	2000	-	55000	10000	0.77	-

(b) Controller, filter, and circuit parameters

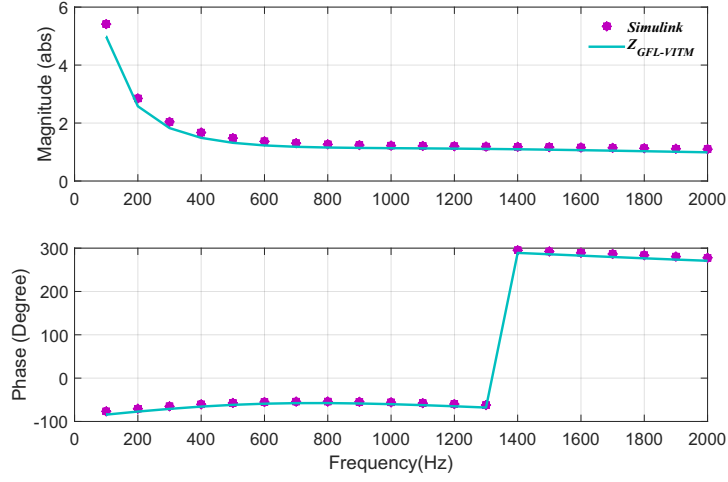
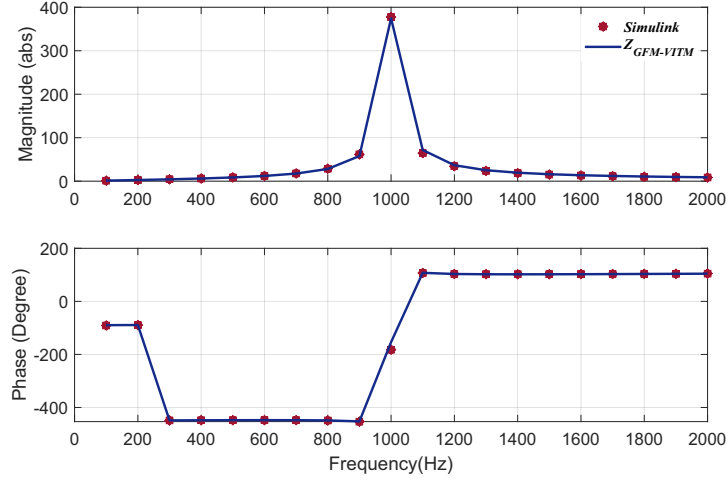
K_{P_v}	K_{I_v}	K_{P_i}	K_{I_i}	L_{LC} [mH]	r_{LC} [μ F]	C_{LC} [μ F]	R_{LC} [Ω]	$r_{LCLC,g}$ [Ω]	$L_{LCLC,g}$ [mH]	C_{LCL} [μ F]	R_{LCL} [Ω]
0.03	9.5	4.92	200	0.492	0.02	60	1.5	0.1	2.5	0.1	12
317.04	95113	4.92	200	4920	200	0.006	1.5	0.1	2.5	0.1	12
0.15	46.4	1.18	50	2.5	0.1	12	1.5	0.005	0.11	0.005	240
0.15	46.4	2950	125000	2.5	0.1	12	1.5	12.5	295	12.5	0.096

**Figure 6.3:** Case I, verification of the Z_{GFM}

Figure 6.4: Case I, verification of the Z_{GFL} Figure 6.5: Case II, verification of the Y_{GFM}

6.3 Stability Analysis

In this section, the stability of the PHIL system in each case is first analyzed using the impedance ratio and Nyquist plots, and then examples are provided to verify the Nyquist results against the benchmark in Simulink. Since it is risky to make a real-PHIL setup unstable for verification, this section performs stability verification via Simulink simulations, while impedance verification is conducted using real-PHIL lab experiments in the section 6.4.

Figure 6.6: Case III, verification of the Z_{GFL} Figure 6.7: Case III, verification of the Z_{GFM}

Now that the whole PHIL is modeled via new dynamic sources and their output impedances, the conventional stability criteria, i.e., Z_{GFM}/Z_{GFL} commonly used in grid integration of GFL converters, hold the same in case 6.1.1, and 6.1.4, but in 6.1.2, and 6.1.3 criterion will be inverse to Z_{GFL}/Z_{GFM} due to the C-ITM.

The parameters given in the first row of the Table 6.2 are examined for the first two cases where HoI is a GFL and MoI is a GFM converter, once operating in V-ITM and the other time operating as a C-ITM. Changes in ITM alter the EG output impedance, Z_{GFM} , and the stability criterion.

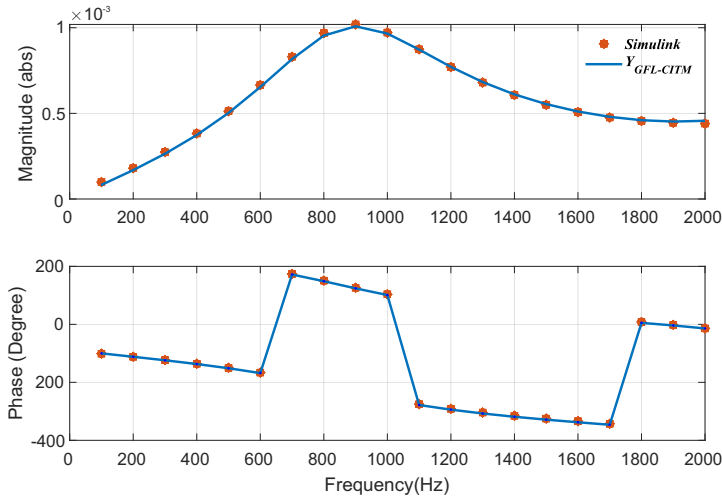


Figure 6.8: Case IV, verification of the Y_{GFL}

Therefore, for those parameters, Fig. 6.9 shows that only V-ITM is stable, and C-ITM encircles the critical point in the Nyquist plot. However, choosing a different set of parameters, the second row of the Table 6.2, the stability results are inverted, i.e., emulating the GFM converter as a voltage source gives an unstable PHIL setup, but as a current source, the PHIL is stable, as shown in Fig. 6.11. To verify the Nyquist results using the impedance ratio, the time-domain results in Simulink are given in Fig. 6.10, and Fig. 6.12, respectively. In Fig. 6.10, the PHIL system becomes unstable when the ITM configuration is switched from V-ITM to C-ITM at 1.056 s, confirming the Nyquist-based response shown in Fig. 6.9. Similarly, Fig. 6.11 shows that the system goes unstable when the configuration changes from C-ITM to V-ITM at 1.133 s, which is consistent with the corresponding Nyquist results. It means that, even when testing a GFL converter and emulating a GFM converter in a PHIL, depending on the parameters, both ITMs can be used to stabilize the PHIL.

As the results for the remaining two cases (Cases III and IV) follow similar trends, only the corresponding Nyquist plots are presented. When testing a GFM converter as the HoI and emulating a GFL converter in the PHIL setup, both V-ITM and C-ITM configurations can lead to stable operation. However, the achievable stability depends on the converter parameters. For instance, as illustrated in Fig. 6.13, when the GFL converter parameters correspond to those in the third row of Table 6.2, the system becomes unstable if the GFL converter is emulated as a current source, and therefore it should instead be emulated as a voltage source. Conversely, when the parameters in the last row of Table 6.2 are applied, the stability condition is reversed (Fig. 6.14).

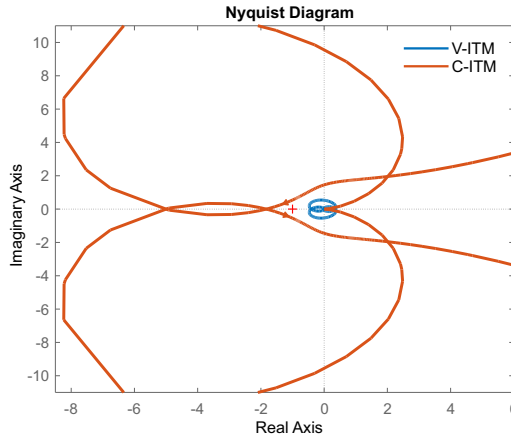


Figure 6.9: Case I, V-ITM is stable and C-ITM is unstable

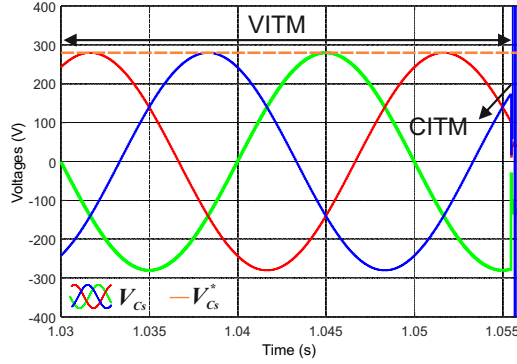


Figure 6.10: Case I, V-ITM is stable and C-ITM is unstable

Based on the results presented in this section, the impedance-ratio stability criterion is verified, demonstrating that the selection of voltage-source or current-source configuration in ITM-based PHIL setups should depend on the combined dynamics of the MoI/HoI and their associated interfaces, rather than on the conventional rule of assigning a current source to GFL converter and a voltage source to GFM converter. The findings indicate that, depending on the specific system parameters, both V-ITM and C-ITM can serve as stable and suitable interface configurations for either GFM or GFL converters.

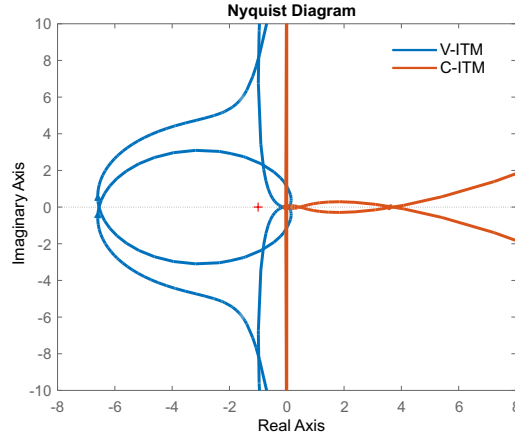


Figure 6.11: Case II, V-ITM is unstable and C-ITM is stable

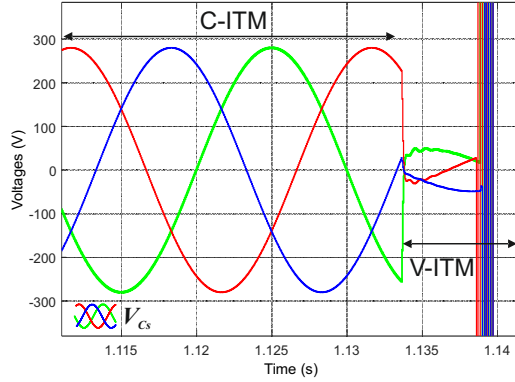


Figure 6.12: Case II, V-ITM is unstable and C-ITM is stable

6.4 Experimental Verification

To validate the impedances derived in Section 6.2, in this section, perturbation-based impedance measurements are performed using the experimental setup described in section 2.5.4. Since the modeled impedances incorporate all PHIL components, including interfaces, controllers, dynamics, physical impedances, and associated delays, the measured impedances obtained through perturbation signals should match the magnitudes and phases of the Bode plots presented in the modeling section. Although the stability verification is carried out only through simulation (for safety reasons), once the modeled impedances are experimentally verified, the stability analysis based on the impedance-ratio criterion is indirectly confirmed as well. The first case in the section 6.1 is chosen as an example for impedance verifications. To measure the impedance of the GFM

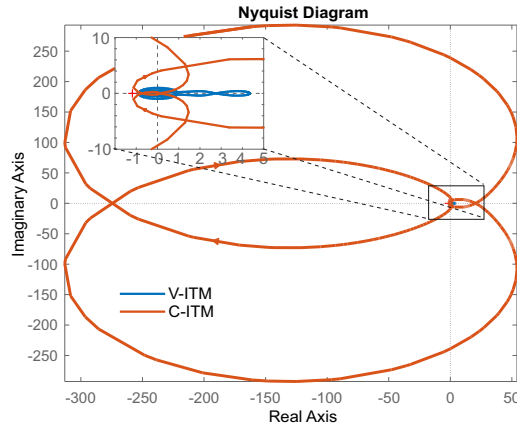


Figure 6.13: Case III, V-ITM is stable and C-ITM is unstable

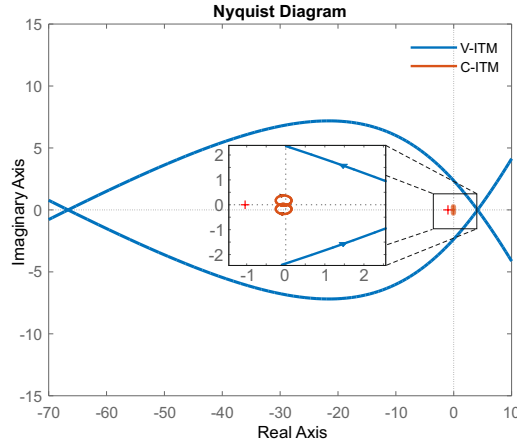


Figure 6.14: Case IV, V-ITM is unstable and C-ITM is stable

and GFL converters, a frequency-sweep methodology was implemented using a perturbation source within the RSCAD simulation environment. The parameters are similar to what is used in case I of the Table.6.2, with differences such as:

- Due to the use of the Aurora protocol, the open-loop delay is $4.2 \mu s$.
- The resistivity of the LCL inductors increases as the frequency increases and the heat from the experiment duration.

That is why the overall gain appears slightly higher than in the impedance-verification simulation. The perturbation signal frequency (f_p) was varied in 100 Hz steps from 100 Hz up to a maximum of 1200 Hz. This upper limit was selected based on practical hardware constraints: specifically, the Imperix passive LCL filter capacitor (C_{LCL}) loses its capacitance characteristics beyond approximately 1200 Hz, and the accuracy of generating high-frequency waveforms is limited by the HoI controller's 50 μs sampling time. PCC measurements of voltage and current (V , i) are captured using Imperix sensors, as illustrated in Figure 6.15. For the Z_{GFL} measurements, the voltage perturbation source (V_p) is activated. Conversely, for the Z_{GFM} measurements, the current perturbation source (i_p) is employed. The captured PCC variables are subsequently processed using Fourier transform to extract the precise gain and phase characteristics at each perturbation signal frequency. These experimental results are compared against the Bode plots of the impedances derived from the analytical modeling (as detailed in (6.4) and (6.3)). The frequency responses across the range from 200 Hz to 1200 Hz show good agreement between the experimental measurements and the analytical models, as depicted in Figures 6.16 and 6.17. This close alignment robustly confirms the correctness and validity of our impedance modeling approach within this frequency spectrum. The observed significant mismatch at 100 Hz, however, is attributed primarily to the limitations of the simplified Single-Input Single-Output (SISO) system impedance model. The low-frequency range (specifically 0-100 Hz) is heavily influenced by complex cross-coupling dynamics introduced by the PLL and the asymmetric design of the d-q axis control loops. Accurately capturing these specific effects requires a more comprehensive full 2x2 impedance matrix measurement and analysis that accounts for the critical off-diagonal elements (Z_{dq} and Z_{qd}).

6.5 Summary

The main goal of this section is to examine the ITM as a practical, straightforward, and accurate PHIL interface algorithm for grid converters and to evaluate its stability characteristics. Two widely used converter types, GFL and GFM converters, are examined under both V-ITM and C-ITM ITM configurations. The modeling incorporates the full PHIL, including the DRTS, signal conversions, numerical LPFs, sensors, amplifiers, and the dynamics of the converter controllers. The PHIL system is represented by the PCC impedances under four scenarios (GFM vs. GFL converters with V-ITM and C-ITM). These impedances are derived from the transfer functions of the individual components and verified across a detailed MATLAB/Simulink PHIL benchmark. The classical impedance-ratio stability criterion, traditionally defined for purely passive software/hardware systems, is extended to account for GFM/GFL output impedances, as well as the effects of PHIL interfaces and control loops. This criterion is validated through

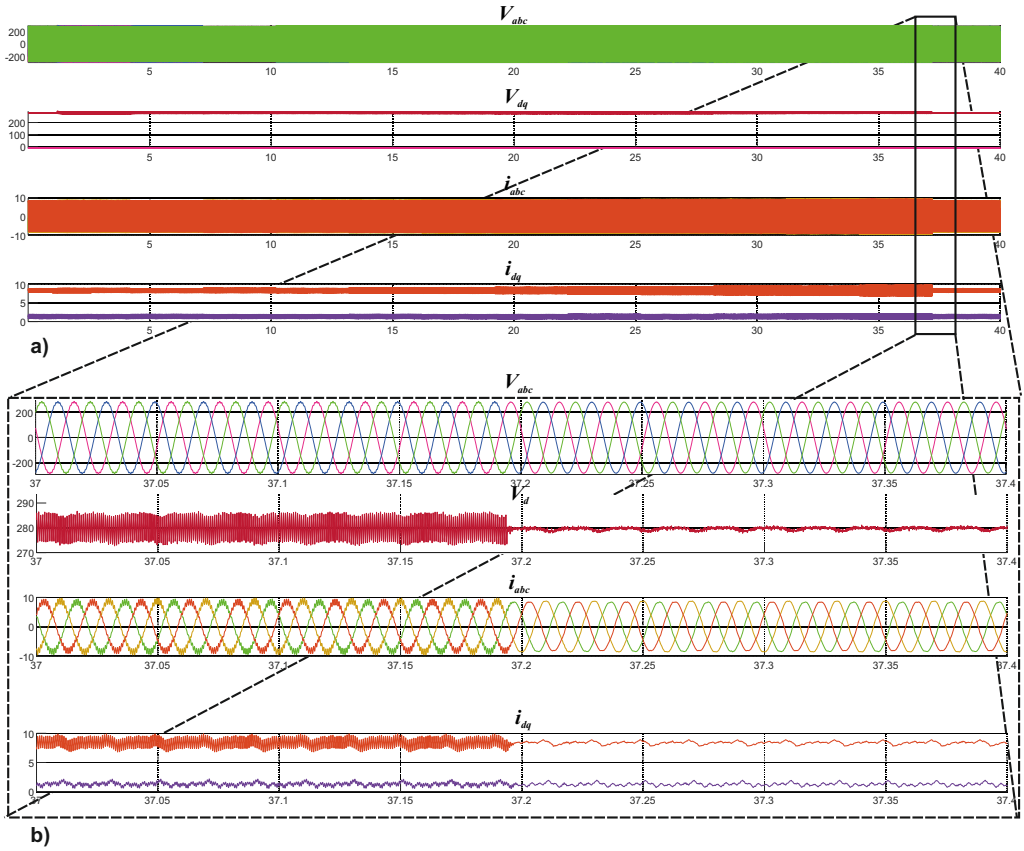


Figure 6.15: PCC measurements of perturbation signals from V_p : a) The full period of perturbation event, b) Magnified end of the event, 1200 Hz

both Nyquist analysis and time-domain simulations. The results demonstrate that, depending on the parameters of the MoI/HoI and their interfaces, either V-ITM or C-ITM can yield stable operation for both GFM and GFL converters, contrary to the conventional assumption that GFL converter should always use C-ITM and GFM converter should always use V-ITM. Finally, experimental impedance measurements using a 45-kVA RTDS-based PHIL setup further validate the impedance models and thereby indirectly confirm the stability analysis.

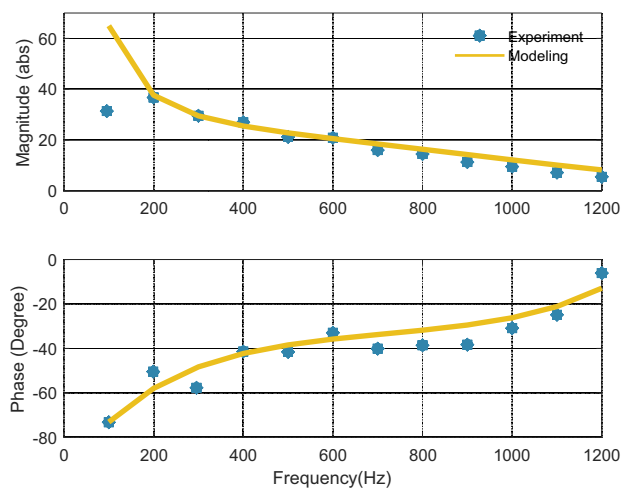


Figure 6.16: Impedance verification of Z_{GFL}

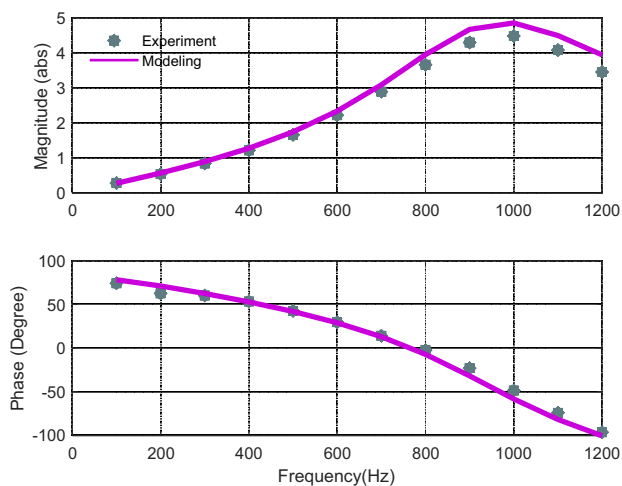


Figure 6.17: Impedance verification of Z_{GFM}

7 Impedance Model and Stability Analysis of a Back-to-Back Converter in a Multi-port Power Hardware-in-the-Loop

Back-to-Back (B2B) converters are increasingly used in power systems, including HVDC systems, wind turbine-to-grid connections, and motor drives [89,90]. This chapter analyzes the stability of a B2B converter in a PHIL setup. The goal is to realize that if a B2B converter is the HoI, with two EGs on each side of the converter, then how the stability of one side would affect the other, and what the stability criteria would be. A generic multi-port PHIL setup is shown in Figure 7.1. As can be seen, the setup contains two PHIL loops, which raises the question of whether the system can be analyzed using a single stability criterion or whether it should be analyzed using separate stability criteria for each grid.

7.1 Multi-port PHIL Benchmark Description

The benchmark consists of two identical EGs and the B2B HoI using V-ITM. The grid models (Fig. 7.2), IAs, and interface elements are the same as those used in Chapter 5.

The B2B converter can be divided into three main parts: an active front-end (AFE), a DC link, and a rectifier. Fig. 7.3 shows the B2B scheme. Both the AFE and the rectifier are modeled using the average model. In addition, both are GFL and are controlled in the dq-frame; therefore, a PLL is also required for synchronization with the grid [91]. It is assumed that the AC power equals the DC power, and the DC link is modeled as two controlled current sources connected in parallel to a capacitor and an equivalent series resistance. The DC current on each side is calculated using

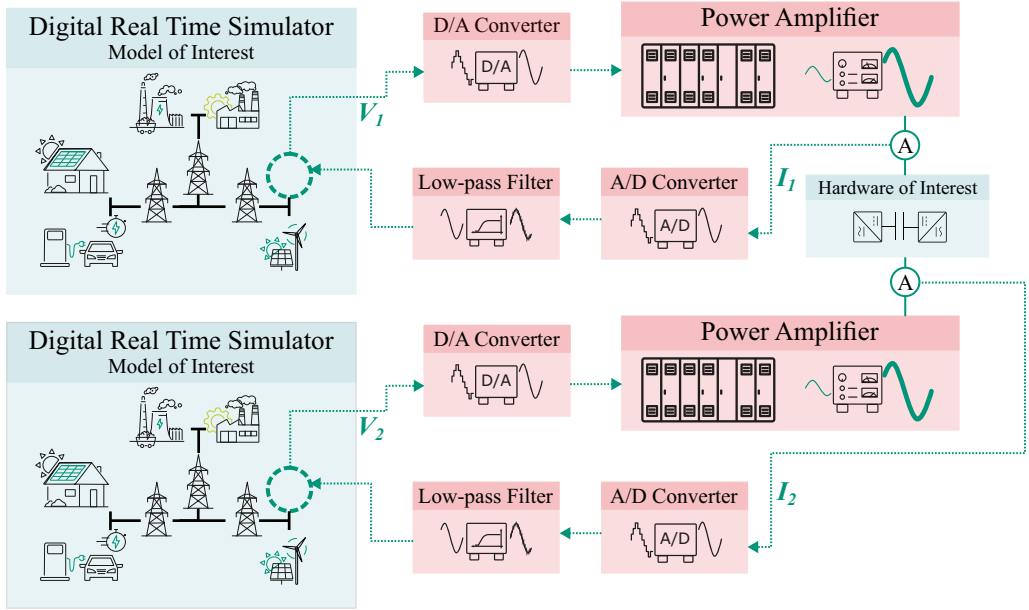


Figure 7.1: A generic multi-port V-ITM PHIL

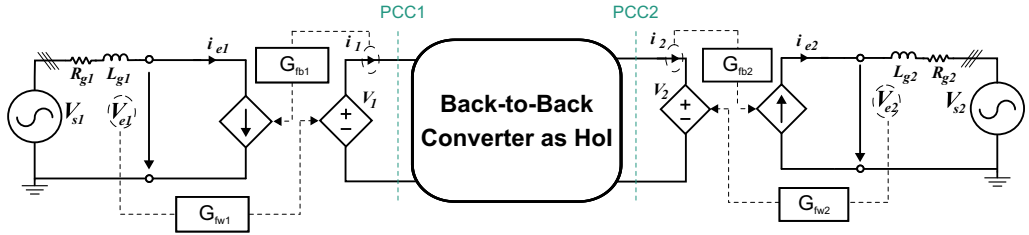


Figure 7.2: The multi-port V-ITM PHIL model

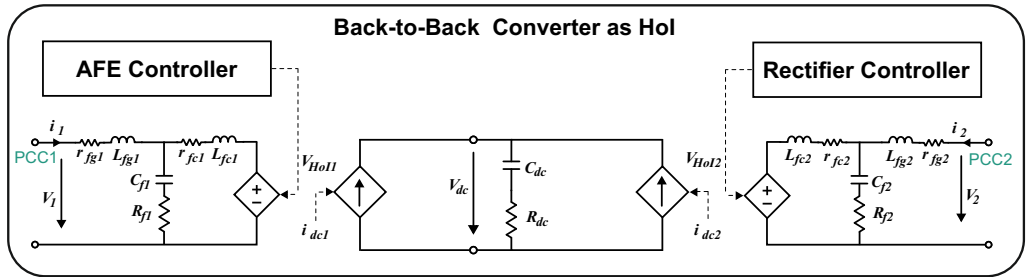


Figure 7.3: The B2B converter as Hol



$$i_{dc1,2} = \frac{3 \cdot V_{d1,2} \cdot i_{d1,2}}{2 \cdot V_{dc}} \quad (7.1)$$

7.2 Impedance Modeling

As similar EGs are used as in Chapter 5, the EG impedance modeling is not repeated here, and they are only renamed as Z_{EG1} and Z_{EG2} in this chapter. For the impedance modeling of the B2B converter, it is first necessary to derive the equations that describe the relationship between the PCC variables ($i_{1,2}$ and $V_{1,2}$) on the HoI side, as shown in Fig. 7.3. The corresponding EG impedances are derived based on Fig. 7.2. The saturation block is a nonlinear block that affects only under abnormal conditions and is not modeled in the impedance. For the AFE impedance modeling, an equation describing i_1 can be derived based on the model in Fig. 7.3, and Fig. 7.4. The result is shown in (7.2), where T_d represents the delay of the system. However, the impedance can not be directly extracted from the equation due to the presence of the V_{dc} term. Therefore, it was necessary to derive an equation for the DC voltage, as given in (7.3). Substituting (7.3) into (7.2) results in the non-linear equation 7.4, where the nonlinearities are highlighted in red.

$$i_1 = \frac{G_{PI,V_{dc}} \cdot G_{PI,i} \cdot Y_{LCL_{HoI1}} \cdot T_d}{1 + G_{PI,i} \cdot T_d^2 \cdot Y_{LCL_{HoI1}}} V_{dc}^* - \frac{G_{PI,V_{dc}} \cdot G_{PI,i} \cdot Y_{LCL_{HoI1}} \cdot T_d^2}{1 + G_{PI,i} \cdot T_d^2 \cdot Y_{LCL_{HoI1}}} V_{dc} + \frac{T_d^2 \cdot Y_{LCL_{HoI1}} - Y_{LCL_{V1}}}{1 + G_{PI,i} \cdot T_d^2 \cdot Y_{LCL_{HoI1}}} V_1 \quad (7.2)$$

$$V_{dc} = \frac{3(V_1 \cdot i_1 + V_2 \cdot i_2)Z_{dc}}{2 \cdot V_{dc}} \quad (7.3)$$

$$i_1 = \frac{T_d^2 \cdot Y_{LCL_{HoI1}} - Y_{LCL_{V1}}}{1 + G_{PI,i} \cdot T_d^2 \cdot Y_{LCL_{HoI1}}} V_1 + \frac{T_d \cdot G_{PI,V_{dc}} \cdot G_{PI,i} \cdot Y_{LCL_{HoI1}}}{1 + G_{PI,i} \cdot T_d^2 \cdot Y_{LCL_{HoI1}}} V_{dc}^* - \frac{1.5 \cdot T_d^2 \cdot Z_{dc} \cdot G_{PI,V_{dc}} \cdot G_{PI,i} \cdot Y_{LCL_{HoI1}}}{1 + G_{PI,i} \cdot T_d^2 \cdot Y_{LCL_{HoI1}}} \left(\frac{V_1 \cdot i_1}{V_{dc}} + \frac{V_2 \cdot i_2}{V_{dc}} \right) \quad (7.4)$$

where:

$$Z_{dc} = R_{dc} + \frac{1}{C_{dc} \cdot s} \quad (7.5)$$

$$G_{PI,V_{dc}} = K_{P_{dc}} + K_{I_{dc}}/s \quad (7.6)$$

$$G_{PI,i} = K_{P_i} + K_{I_i}/s \quad (7.7)$$

$$T_d = e^{-(T_{d_{PI}})s} \quad (7.8)$$

$$Y_{LCL_{HoI1}} = Z_{Cf1}/(Z_{L_{fg1}} \cdot Z_{Cf1} + Z_{Cf1} \cdot Z_{L_{fc1}} + Z_{L_{fc1}} \cdot Z_{L_{fg1}}) \quad (7.9)$$

$$Y_{LCL_{V1}} = (Z_{Cf1} + Z_{L_{fc1}})/(Z_{L_{fg1}} \cdot Z_{Cf1} + Z_{Cf1} \cdot Z_{L_{fc1}} + Z_{L_{fc1}} \cdot Z_{L_{fg1}}) \quad (7.10)$$

(7.4) is non-linear in five variables ($V_1, V_2, i_1, i_2, V_{dc}$). To linearize the equation, a multivariable first-order Taylor series expansion was applied. (7.11) represents the Taylor expansion applied, where $\hat{i}_1, \hat{V}_1, \hat{i}_2, \hat{V}_2, V_{dc_n}$ are the operating points, and f is (7.4).

$$\begin{aligned}
& (i_1 - \hat{i}_1) \frac{\partial f}{\partial i_1}(\hat{i}_1, \hat{i}_2, \hat{V}_1, \hat{V}_2, V_{dc_n}) \\
& + (i_2 - \hat{i}_2) \frac{\partial f}{\partial i_2}(\hat{i}_1, \hat{i}_2, \hat{V}_1, \hat{V}_2, V_{dc_n}) \\
& + (V_1 - \hat{V}_1) \frac{\partial f}{\partial V_1}(\hat{i}_1, \hat{i}_2, \hat{V}_1, \hat{V}_2, V_{dc_n}) \\
& + (V_2 - \hat{V}_2) \frac{\partial f}{\partial V_2}(\hat{i}_1, \hat{i}_2, \hat{V}_1, \hat{V}_2, V_{dc_n}) \\
& + (V_{dc} - V_{dc_n}) \frac{\partial f}{\partial V_{dc}}(\hat{i}_1, \hat{i}_2, \hat{V}_1, \hat{V}_2, V_{dc_n}) \\
& + f(\hat{i}_1, \hat{i}_2, \hat{V}_1, \hat{V}_2, V_{dc_n})
\end{aligned} \tag{7.11}$$

The result of the Taylor series expansion is then shown in (7.12).

$$i_1 = \underbrace{\frac{A}{F}}_{H_1} V_{dc}^* + \underbrace{\frac{E}{F}}_{H_2} V_2 - \underbrace{\frac{C}{F}}_{H_3} i_2 + \underbrace{\frac{B}{F}}_{Y_1} V_1 \tag{7.12}$$

where A, B, C, E , and F are defined as follows:

$$A = T_d \cdot G_{PI, V_{dc}} \cdot G_{PI, i} \cdot Y_{LCL_{HoI_1}} \tag{7.13}$$

$$B = T_d^2 \cdot Y_{LCL_{HoI_1}} - Y_{LCL_{V_1}} - \frac{1.5 \cdot \hat{i}_1}{V_{dc_n}} \cdot T_d^3 \cdot Z_{dc} \cdot G_{PI, V_{dc}} \cdot G_{PI, i} \cdot Y_{LCL_{HoI_1}} \tag{7.14}$$

$$C = \frac{1.5 \cdot \hat{V}_2}{V_{dc_n}} \cdot T_d^3 \cdot Z_{dc} \cdot G_{PI, V_{dc}} \cdot G_{PI, i} \cdot Y_{LCL_{HoI_1}} \tag{7.15}$$

$$E = \frac{1.5 \cdot \hat{i}_2}{V_{dc_n}} \cdot T_d^3 \cdot Z_{dc} \cdot G_{PI, V_{dc}} \cdot G_{PI, i} \cdot Y_{LCL_{HoI_1}} \tag{7.16}$$

$$F = 1 + G_{PI, i} \cdot Y_{LCL_{HoI_1}} \cdot T_d^2 + \frac{1.5 \cdot \hat{V}_1}{V_{dc_n}} \cdot T_d^3 \cdot Z_{dc} \cdot G_{PI, V_{dc}} \cdot G_{PI, i} \cdot Y_{LCL_{HoI_1}} \tag{7.17}$$

(7.12) shows that i_1 depends on V_{dc}^* , V_1 , V_2 , and i_2 . Therefore, the AFE is affected by the rectifier. The impedance model of the AFE is therefore:

$$Z_1 = F/B \tag{7.18}$$

For the impedance model of the rectifier, an equation describing i_2 is derived from Fig. 7.3 and Fig. 7.5, and is shown in (7.19). However, the impedance can not be extracted directly from the equation due to the presence of $\frac{V_{dc}^*}{V_{dc}}$. The value of this term can be determined based on the analysis of the AFE via the following assumption:

Assumption: If the AFE is stable and the DC-link capacitor is selected according to the standard ratings for a B2B converter, then it can be assumed that $\frac{V_{dc}^*}{V_{dc}} \approx 1$. If the AFE is unstable, then $V_{dc} \rightarrow \infty$; therefore, $\frac{V_{dc}^*}{V_{dc}} = 0$.

Based on the given assumption, (7.19) can be rewritten as a binary piecewise function, as shown in (7.20).

$$i_2 = \frac{G_{PI_{i2}} \cdot \frac{V_{dc}^*}{V_{dc}} \cdot T_d \cdot Y_{LCL_{HoI2}}}{1 + G_{PI_{i2}} \cdot T_d^2 \cdot \frac{V_{dc}^*}{V_{dc}} \cdot Y_{LCL_{HoI2}}} i^* + \frac{\frac{V_{dc}^*}{V_{dc}} \cdot T_d^2 \cdot Y_{LCL_{HoI2}} - Y_{LCL_{V2}}}{1 + G_{PI_{i2}} \cdot T_d^2 \cdot \frac{V_{dc}^*}{V_{dc}} \cdot Y_{LCL_{HoI2}}} V_2 \quad (7.19)$$

$$i_2 = \begin{cases} \underbrace{\frac{G_{PI_{i2}} \cdot T_d \cdot Y_{LCL_{HoI2}}}{1 + G_{PI_{i2}} \cdot T_d^2 \cdot Y_{LCL_{HoI2}}} i^* + \frac{T_d^2 \cdot Y_{LCL_{HoI2}} - Y_{LCL_{V2}}}{1 + G_{PI_{i2}} \cdot T_d^2 \cdot Y_{LCL_{HoI2}}} V_2}_{H_4} & \frac{V_{dc}^*}{V_{dc}} \approx 1 \\ -Y_{LCL_{V2}} \cdot V_2 & \frac{V_{dc}^*}{V_{dc}} = 0 \end{cases} \quad (7.20)$$

From (7.20), the impedance of the rectifier is shaped based on the state of the AFE side; therefore, the impedance of the rectifier Z_2 can also be written as a binary piecewise function as shown in (7.21).

$$Z_2 = \begin{cases} \frac{1 + G_{PI_{i2}} \cdot T_d^2 \cdot Y_{LCL_{HoI2}}}{T_d^2 \cdot Y_{LCL_{HoI2}} - Y_{LCL_{V2}}} & \text{AFE is stable} \\ \frac{-1}{Y_{LCL_{V2}}} & \text{AFE not stable} \end{cases} \quad (7.21)$$

Now that the output impedances of B2B's each side are modeled, the whole setup can be represented by Thévenin and Norton equivalent circuits, as shown in Fig. 7.6. The impact of the AFE on the rectifier side is shown in the variable impedance Z_2 , as described in (7.21). As mentioned at the beginning of the chapter, the EGs are similar to Chapter 5, therefore the same equation can be used for their Thévenin equivalent circuits. Only renamed here as V_{EG1} , Z_{EG1} and V_{EG2} , Z_{EG2} , two represent the impedance model of the two grid emulators at each side of B2B. The suggested impedance model is shown in Fig. 7.6, which splits the setup into two PHIL

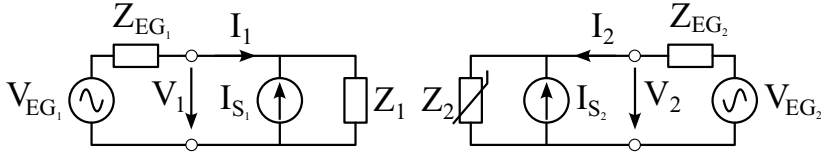


Figure 7.6: Impedance Model

setups. Based on the impedance model, the currents at points of coupling I_1 and I_2 can be written as follows:

$$I_1 = \left[I_{s1} + \frac{V_{EG1}}{Z_1} \right] \frac{1}{1 + \frac{Z_{EG1}}{Z_1}} \quad (7.22)$$

$$I_2 = \left[I_{s2} + \frac{V_{EG2}}{Z_2} \right] \frac{1}{1 + \frac{Z_{EG2}}{Z_2}} \quad (7.23)$$

where $I_{s1} = H_1 + H_2 + H_3$ and $I_{s2} = H_4$.

The ratio Z_{EG1}/Z_1 can be used to assess the stability of the AFE, and the ratio Z_{EG2}/Z_2 can be used to assess the stability of the rectifier. However, sides are not independent, as Z_2 depends on the stability of the AFE, and I_{s1} depends on V_2 and I_2 . Based on the shown dependencies, the source I_{s1} 's stability depends on the rectifier's stability. Therefore, it is necessary first to check the stability of the rectifier using Z_{EG2}/Z_2 , under the assumption that the AFE is stable. If the converter is stable, then I_{s1} is stable, and Z_{EG1}/Z_1 can be used to verify that the AFE is stable.

7.2.1 Impedance Verification

To verify the impedance model in the previous subsection, each grid voltage is perturbed by sinusoids of magnitude 10 V at frequencies ranging from 200 Hz to 2000 Hz. The voltage and current are measured at both points of common coupling. Then, the Fourier transform is applied to the measured values to obtain the impedances at the perturbation frequency. This verification is performed by modeling a benchmark in MATLAB/Simulink using the parameters in Table 5.1. In addition, the controllers' responses are verified using the same parameters. To verify the DC-voltage controller, a step of 50 V is applied to the reference, and the results are presented in Fig. 7.7. In addition, the rectifier controller was verified, a step of -1 A is applied, and the results are shown in Fig. 7.8.

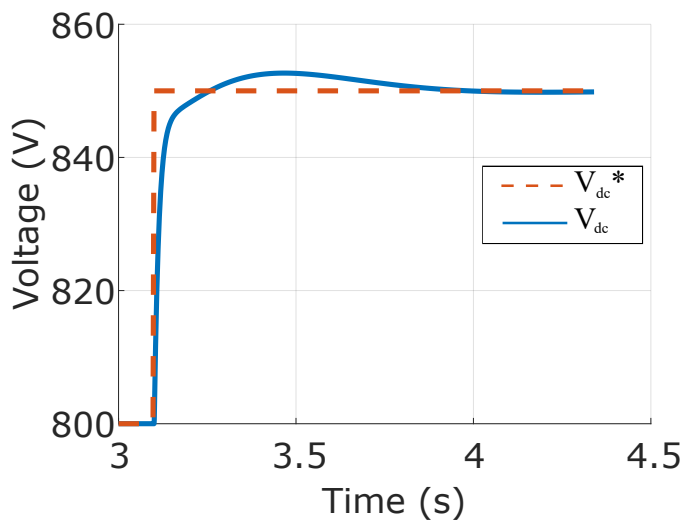


Figure 7.7: AFE controller response

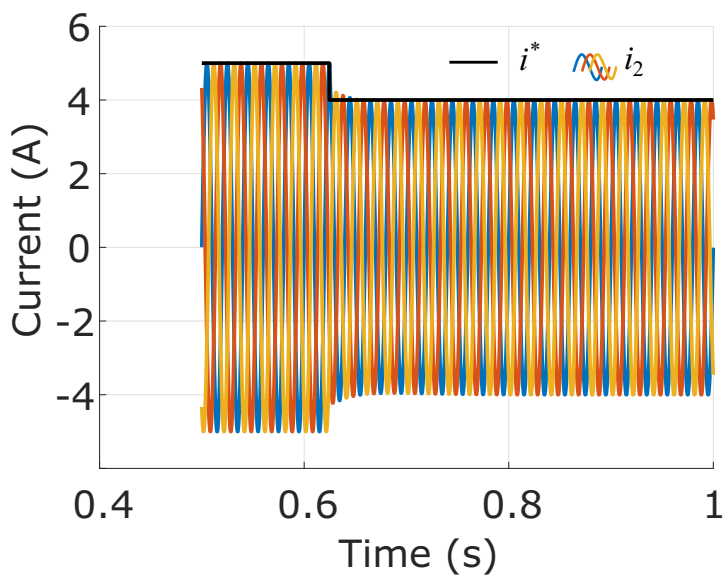


Figure 7.8: Rectifier controller response

7.2.2 Perturbation of Grid 1

The grid connected to the AFE (Grid 1) is perturbed, then V_1 and i_1 are measured and recorded in Fig. 7.9, representing Z_1 . The benchmark results are marked with yellow points, and the Bode plot of the modeled impedance, linearized using the parameters in Table 7.2, is shown in blue. The figure shows the measured and the modeled impedance match.

Under the same perturbation, V_2 and i_2 are then measured and recorded in Fig. 7.9, representing Z_{EG2} . The benchmark results are shown as light blue points, and the modeled impedance Bode plot is shown in green. The figure shows that the measured and modeled impedance match closely.

Table 7.1: PHIL Benchmark parameters

Parameter	Value	Unit	Parameter	Value	Unit
i^*	5	A	V_{dc}^*	800	V
V_{s1}, V_{s2}	310	V (peak)	T_{DRTS}	50	μs
ω_c	12.566×10^6	rad/s	C_{dc}	1600	μF
R_{dc}	30	m Ω	$C_{f1,2}$	12	μF
$R_{f1,2}$	1.5	Ω	L_{fc1}, L_{fg1}	2.36	mH
$r_{fg1}, r_{fc1},$	0.05	Ω	L_{fc2}, L_{fg2}	1.18	mH
$r_{fg2}, r_{fc2},$	0.025	Ω	R_{g1}	0.05	Ω
L_{g1}	2.36	mH	R_{g2}	0.025	Ω
L_{g2}	1.18	mH	$K_{P_{dc}}$	0.0759	–
$K_{I_{dc}}$	0.4	–	$K_{P_{i1}}$	4.72	–
$K_{I_{i1}}$	100	–	$K_{P_{i2}}$	2.36	–
$K_{I_{i2}}$	50	–			

Table 7.2: Z_1 linearization Parameters

$\hat{i}_1$	$\hat{i}_2$	$\hat{V}_1$	$\hat{V}_2$	V_{dcn}
[A]	[A]	[V]	[V]	[V]
-5	5	310	310	800

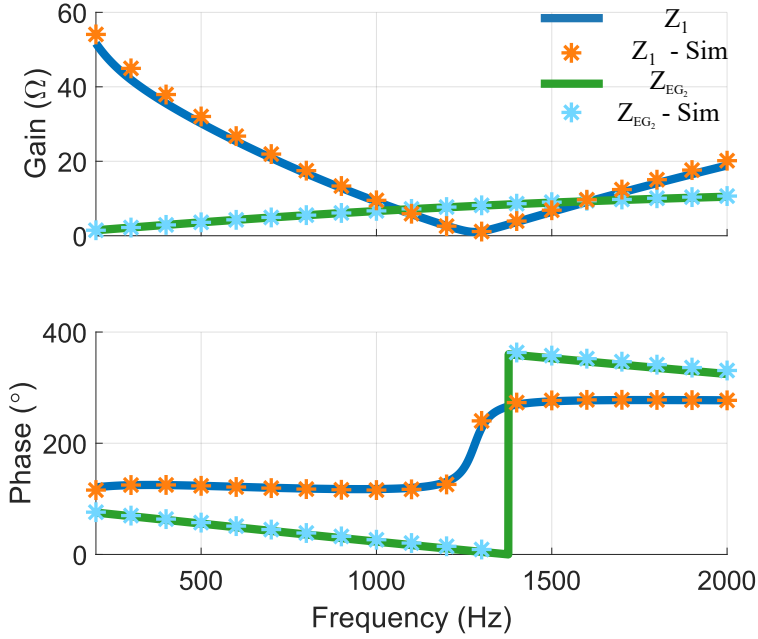


Figure 7.9: Grid 1 Perturbation Results

7.2.3 Perturbation of Grid 2

The grid connected to the rectifier (Grid 2) is perturbed, and V_2 and i_2 are measured. The same perturbations are applied, and then V_1 and i_2 are measured. The results are recorded in Fig. 7.10, representing Z_{G_1} . As shown in the figure, the measured impedance matched the modeled impedance.

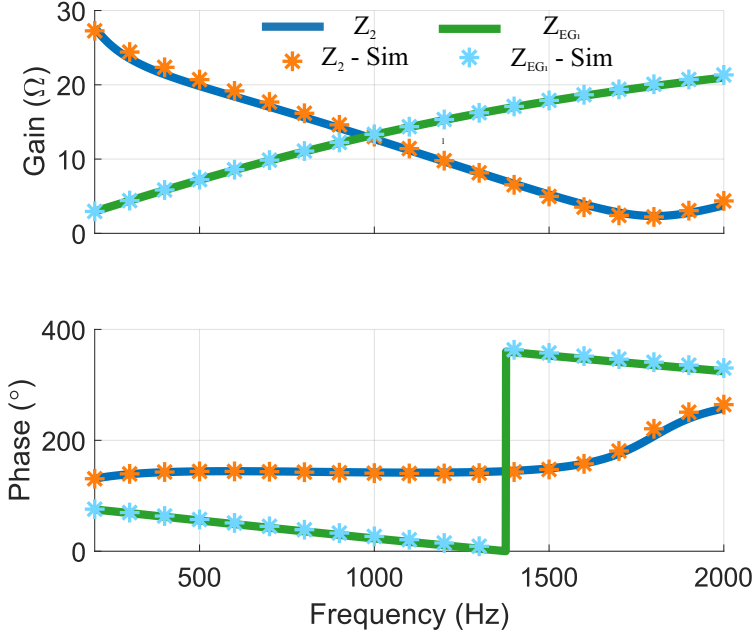


Figure 7.10: Grid 2 Perturbation Results

7.3 Stability Verification

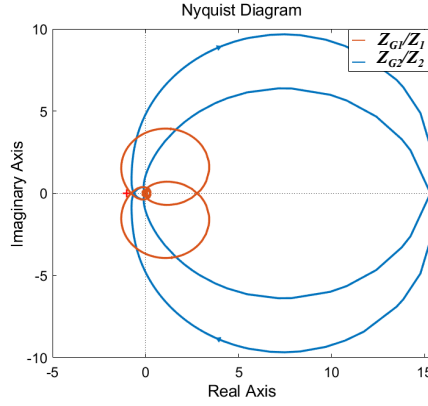
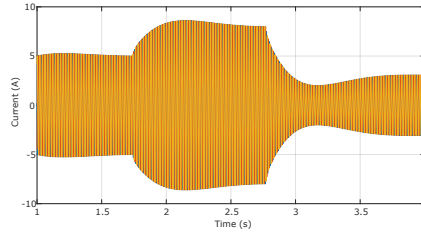
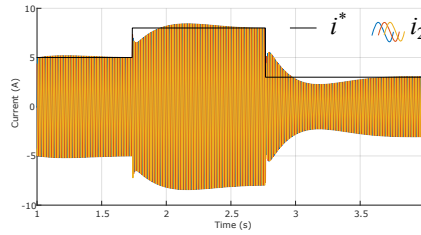
After verifying impedances, this section outlines the process for stability verification. To verify stability, the grid impedance is varied based on the grid-side inductor of the LCL filter, defined by the k factor:

$$k = \frac{Z_g}{Z_{L_g}} \quad (7.24)$$

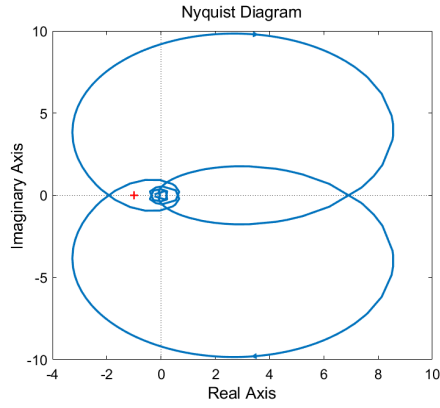
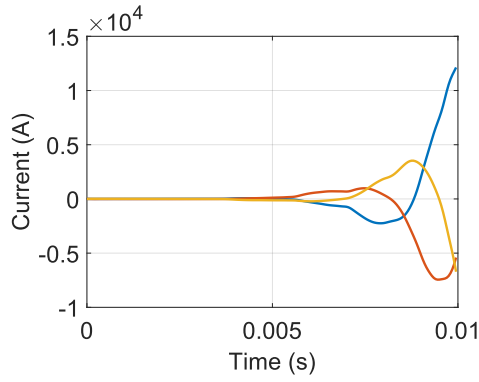
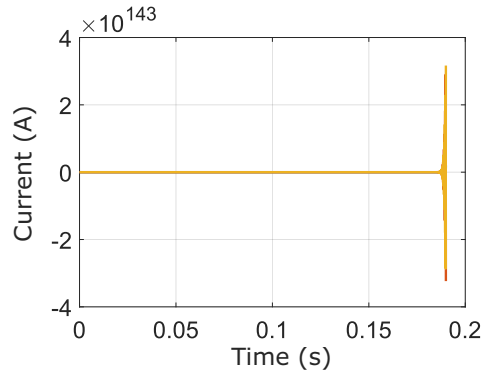
$$Z_g = R_g + L_g \cdot s \quad (7.25)$$

$$Z_{L_g} = r_{fg} + L_{fg} \cdot s \quad (7.26)$$

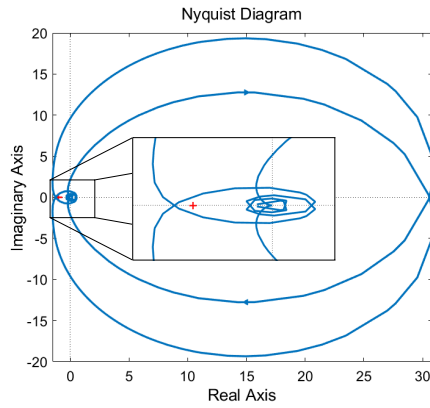
The value of $k_{1,2}$ is varied by varying the grid impedance. Therefore, generating cases for verification. Fig. 7.11a shows an example where the Nyquist plot shows stability for both sides. Figs. 7.11b and 7.11c verifies the Nyquist evaluation in the time-domain. As presented in Section 7.2, it is necessary to verify the stability of the rectifier first, assuming a stable AFE. This verification can be performed by plotting the Nyquist diagram of Z_{EG_2}/Z_2 at different k_2 values,


 (a) Nyquist plot of Z_{G1}/Z_1 at $k_1 = 1$ and Z_{G2}/Z_2 at $k_2 = 1$

 (b) Benchmark Simulation of i_1

 (c) Benchmark Simulation of i_2
Figure 7.11: Stability analysis at $k_2 = 1$ and $k_1 = 1$

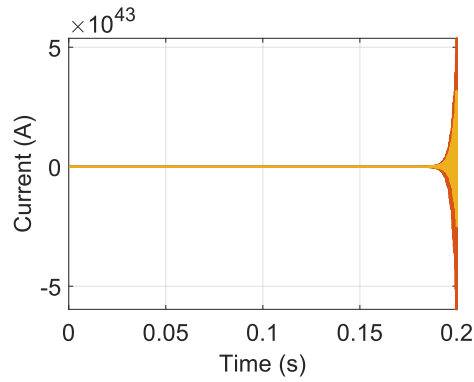
where an encirclement around $(-1, 0j)$ indicates instability. The Nyquist result is then compared to the time-domain results in the benchmark model. Fig. 7.12a shows that the rectifier will be unstable at $k_2 = 0.4$. This is also verified by the benchmark model in Figs. 7.12b and 7.12c. The figures show that both currents will be unstable, even though k_1 is chosen so that Z_{EG1}/Z_1 is stable. It is also necessary to examine the setup in a case where the rectifier is stable. A value of k_2 is chosen such that the rectifier is stable, and $k_1 = 0.4$. The Nyquist plot of Z_{G1}/Z_1 is shown in Fig. 7.13a, which predicts instability. This is also verified in the time-domain benchmark results in Fig. 7.13b. In addition, by inspecting Fig. 7.13c, the change of impedance based on the

(a) Nyquist plot of Z_{EG_2}/Z_2 at $k_2 = 0.4$ and $k_1 = 1$ (b) Benchmark Simulation of i_1 (c) Benchmark Simulation of i_2 **Figure 7.12:** Stability analysis at $k_2 = 0.4$

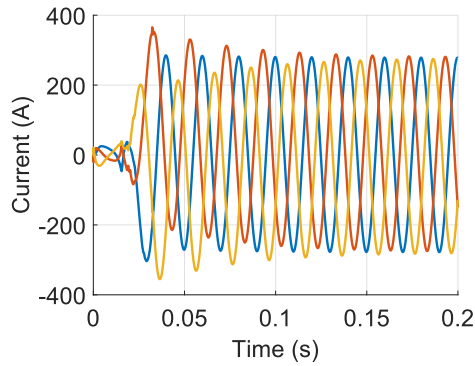
stability of the AFE can also be seen in the time-domain results, as the grid voltage is constant, and the current changes abruptly at 0.2 s.



(a) Nyquist plot of Z_{G_1}/Z_1 at $k_1 = 0.5$ and $k_2 = 1$



(b) Benchmark Simulation of i_1



(c) Benchmark Simulation of i_2

Figure 7.13: Stability analysis at $k_1 = 0.5$

7.4 Summary

This chapter examines the stability of a PHIL setup with a B2B converter as HoI. The model of the setup is introduced in 7.1. The setup consists of an AFE and a rectifier controlled in the dq-frame. The setup's impedance is first modeled, with the rectifier represented as a variable impedance that depends on the AFE stability. An impedance model is then proposed with two dependent sides and two stability criteria. A benchmark model is then modeled in MATLAB/Simulink. The impedance is verified via perturbation and measurement on the benchmark, and by comparison with the modeled impedance. The stability was then verified by varying the grids' impedance in both the impedance model and the benchmark. Then, Nyquist plots were used to evaluate the setup's stability, and the results were compared with time-domain results from the benchmark. The time-domain results also confirm that the rectifier impedance depends on the AFE stability. In addition to stability verification, the impedance model can be further expanded by linearizing the rectifier equation, thereby capturing the full system dynamics and reducing the rectifier equation to a single equation on the rectifier side.

8 Power Hardware-in-the-Loop Recommended Guidelines and Further Applications

The concept of PHIL has been significantly expanded and refined over the past decade, with several works providing fundamental guidelines for its application [3,4]. More recently, the IEEE P2004 working group introduced Recommended Guidelines for PHIL testing [5], establishing a common foundation for understanding and applying PHIL experiments. Nevertheless, a final step toward full standardization of PHIL systems remains.

Building on this context, this thesis has so far focused on developing the motivation and applications of the PHIL system, as well as methodologies for modeling and analyzing its stability and accuracy, particularly when using active HoI. In addition, an impedance-based stability approach has been proposed to address some of the most common challenges in PHIL setups.

This chapter addresses how a PHIL system should be designed, validated, and operated to maximize its benefits. Based on insights from previous chapters, existing research, and practical use cases, this chapter provides practical suggestions for PHIL modeling, design, laboratory implementation, and validation. Furthermore, it identifies several open challenges that must be addressed to enable broader industrial adoption of PHIL systems for testing and validation of electrical equipment.

8.1 Recommended Guidelines for Using PHIL Systems

This section collects experiences with PHIL experiments, both those discussed in the presented thesis and in the literature, to introduce design and implementation guidelines for safe, stable, and accurate PHIL testing.

8.1.1 Applicability of PHIL Based on Test Scenarios Dynamics

The PHIL concept has been developed to experimentally test hardware in realistic grid conditions. As a consequence, testing is strongly dependent on the scenario in which the HoI operates. For example, PHIL systems are particularly useful for dynamic transients, ranging from frequency support to fault ride-through applications.

The applicability and benefits of PHIL testing can be evaluated for systems, processes, and phenomena with the following transient dynamics: quasi steady-state transients, dynamic transients, fast electromagnetic transients:

- Quasi steady-state transients: in several cases, PHIL has been used to validate quasi steady-state phenomena, where transients evolve with slow dynamics. In these cases, PHIL offers only limited advantages for testing. The slow dynamics allow reducing the complexity of a simulation model (e.g., by employing average models), and thus the same scenario can be easily tested in a simulation environment without affecting testing accuracy.
- Dynamic transients: transients ranging from a few milliseconds to a few seconds (e.g., frequency and voltage transients, fault ride-through capabilities, harmonics) are among the reasons PHIL has been conceptualized. These transients cannot be easily reproduced in simulation without extensive simplifications, yet they are too complex for reduced laboratory test benches. PHIL offers optimal testing capabilities (more flexible and safer than the on-field testing), providing a realistic assessment of the hardware performance.
- Electromagnetic transients: PHIL has clear bandwidth limitations due to the time discretization of CPU-based DRTS (usually with a time-step of $50\ \mu s$), the limited bandwidth of the PAs (varying from a few kHz up to 10 kHz for larger units, up to 200 kHz for smaller ones), and the need for LPFs for loop stability purpose (typically, in the order of 200-500 μs time constants). As a result, transients that evolve within a few milliseconds (e.g., DC faults, switching dynamics) are currently challenging to reproduce in systems. Advanced interface algorithms integrated with FPGA units need to be designed to handle these transients.

8.1.2 Hardware Topology and Scalability

As mentioned above, the advantage of PHIL is its ability to create testing conditions that closely mimic the real operational environment, enabling system performance evaluation under realistic conditions. However, these conditions do not cover only the MoI, but also the HoI: the hardware that needs to be validated experimentally should have electrical and thermal performance close to the one that will be installed in the field (e.g., similar topology, architecture, switching technology, etc.).

Several papers addressed the problem of the scalability of results from a stability and accuracy perspective [47], targeting an up-scaling of the voltage and power in the DRTS and working with reduced-scale hardware in a laboratory. However, this brings several issues that affect the accuracy and fidelity of the results.

The following few guidelines can be followed when it comes to the hardware aspects of PHIL:

- **Modularity:** the HoI may consist of modular (e.g., high-voltage power converters) and non-modular (e.g., electrical machines) systems, where the properties of the high-power modular systems could be assessed using PHIL based on the assessed properties of the cascaded lower-power modules. For example, MMC may be studied from the behavior of the single cell, as proposed in the partial-PHIL in Section 8.3.1 and Section 8.3.1.3. Scaling up non-modular systems can lead to incorrect performance estimates because some of their properties, such as dynamic or thermal performance, cannot be easily scaled. On the other hand, energy storage systems, for example, exhibit a degree of modularity in their power and voltage ratings (e.g., battery stacks), which can be easily integrated into PHIL testing. It is strongly recommended to understand the modularity of the HoI before planning a PHIL validation. The PHIL testing provides realistic performance only if the reduced-scale hardware matches the full-scale system's electrical and thermal performance.
- **Device technology:** recent PHIL studies frequently employ low-voltage semiconductors to emulate high-voltage systems. Although passive components may follow per-unit scaling, low-voltage switches cannot accurately reproduce the switching dynamics of high-voltage hardware (e.g., 3.3 kV IGBTs, GTOs), potentially inflating transient performance estimates. When facility limitations mandate the use of lower-rated devices, these components must be modeled as ideal switches, disregarding their intrinsic switching characteristics and thermal losses.

8.1.3 PHIL System Accuracy, Stability, and Sensitivity

Stability and accuracy are strongly coupled in testing. The accuracy is related to the capacity of the testing to reproduce the real coupling case, i.e., like in field testing, without any added power interface between the HoI and the MoI. As mentioned in Chapter 2, the power interface introduces delays and non-linear dynamics. The following are general guidelines for stability, accuracy, and sensitivity.

- **Stability:** a stable PHIL is mandatory to avoid damage to the HoI. The PHIL stability depends on the loop transfer function, including the delays introduced by the power amplification and filter stages [C2]. Recent works have highlighted that multi-rate partitioning of the power interface can help increase PHIL system stability [76]. The PHIL system's stability can be estimated from offline simulations of its transfer function, provided knowledge of the HoI parameters. Typically, these parameters are only partially available and can vary during the experiment (e.g., temperature-dependent resistance). For obtaining a stable PHIL, testing the following is suggested:
 1. To perform an online estimation of the HoI impedance during PHIL operation by means of frequency-sweep approaches, and to represent in simulation the PHIL as an equivalent Thévenin (or Norton) generator. A more accurate understanding of the HoI equivalent impedance prevents neglecting important dynamics in PHIL stability.
 2. If the HoI impedance cannot be estimated during operation, it is vital to consider the influence of the control during operation. An offline frequency sweep for estimating the HoI impedance may overlook controller dynamics that are present during online operations.
 3. If no impedance estimation is possible, the controller dynamics that may create interaction with the power system under the considered conditions should be evaluated. This includes converters' power- and current-control systems, PLLs, communication, and automation dynamics (e.g., primary or secondary controllers).
- **Accuracy:** The inherent limitations of PHIL interfaces, such as limited measurement accuracy and limited bandwidth of PAs, can significantly affect the accuracy of PHIL tests [39]. As a consequence, PHIL testing results may differ from the field ones, and this is strongly undesired. For this reason, the PHIL accuracy definition needs to be introduced. If we consider the $|TF_{PHIL}|$, $|TF_{RC}|$, $\angle TF_{PHIL}$, and $\angle TF_{RC}$ the PHIL and real coupling

case (i.e., like in the field testing) amplitude and phase, respectively, we can define the amplitude $|A|$ and phase $\angle A$ accuracy indexes as:

$$|A(\omega)| = \frac{|TF_{PHIL}(\omega)| - |TF_{RC}(\omega)|}{|TF_{PHIL}(\omega)|} \quad (8.1)$$

$$\angle A^\circ(\omega) = \angle TF_{PHIL}(\omega) - \angle TF_{RC}(\omega) \quad (8.2)$$

These two error indices shall be performed across the whole frequency spectrum, and, as indicative guidelines, the following acceptance limits are suggested:

$$|A(\omega)| < 3dB \quad (8.3)$$

$$\angle A^\circ(\omega) < 5^\circ \quad (8.4)$$

The cutoff frequency, where the PHIL testing differs more than the above values from the real coupling, will be determined as the accuracy bandwidth of the PHIL testing.

8.1.4 Process Guidelines for PHIL Testing

This section provides a step-by-step guide on how to develop and perform a PHIL testing. The PHIL system design flowchart illustrated in Fig. 8.1 provides an overview of the steps needed to design a stable and accurate PHIL test system.

8.1.4.1 Scenario Case Development:

As a first step, the PHIL testing goal must be determined, and the power system scenario in the MoI must be developed for the HoI connection. First, the size and the required modeling depth of the scenario need to be analyzed [93], to understand if the power systems phenomena under study respect the PHIL system dynamic (including MoI, HoI, power amplification and filtering dynamic limitations). It is strongly suggested that the DRTS time step (T_s) of the MoI should

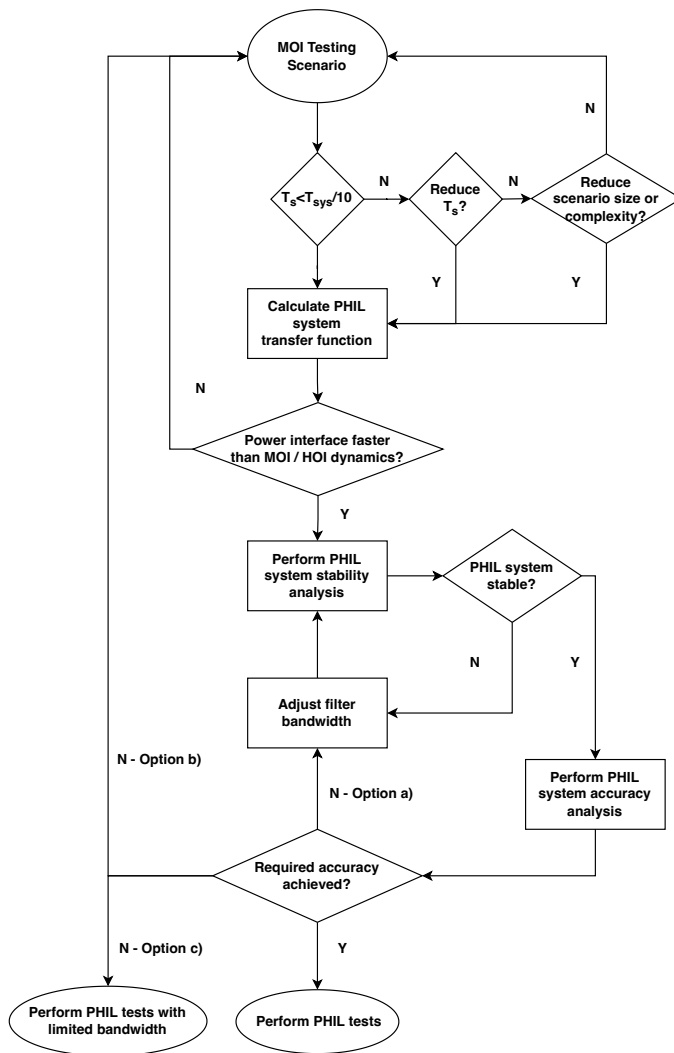


Figure 8.1: Decision Flowchart for developing and performing a stable and accurate PHIL testing

be at least 10 times smaller than the fastest scenario dynamic that is under investigation. If this requirement cannot be initially met, the following three options are available:

- a) Reduction of the time step size T_s considering the model size and the computational capacity of the DRTS.
- b) Reduction of the simulation model size in order to fit a smaller time step size T_s .
- c) If any of the above conditions cannot be met, the scenario under study should be rethought.

8.1.4.2 Hardware Requirements:

In the next step, the proper selection of hardware devices with respect to available DRTS, power rating, bandwidth, voltage, and current limits needs to be performed for the PHIL interface. For the hardware part, I/O ports, the respective signal connection terminals, the safe operating area (SOA) of the power amplifier stage, and the HoI must be considered. Once the hardware has been chosen, the transfer functions of the power interface (PA, sensors, analog/digital converters) should be determined, and stability analysis can be performed using the mathematical approach proposed in this thesis.

When defining the required PA bandwidth, it is important to first determine the MoI bandwidth $f_{ModelMax}$, which represents the highest frequency that will be controlled in the tested closed-loop system. The $f_{ModelMax}$ is typically not the fundamental frequency of the system. A few examples of properly determined $f_{ModelMax}$ are:

- AC applications: The frequency of the highest-order harmonic to be represented by the model.
- Impedance measurement applications: The highest perturbation frequency to be tested.
- Electric machine simulation: The highest frequency of the back electromagnetic force (EMF) to be modeled, the highest frequency of the machine torque ripple, or highest frequency of the current ripple generated by a converter driving the machine, whichever is higher.

Based on the empirical data, it is good engineering practice to select the PA bandwidth f_{Amp} to be 1.5 times higher than $f_{ModelMax}$. The properties of the PA at f_{Amp} should be:

- Amplifier gain > 3 dB

- Amplifier phase shift: $< -45^\circ$

8.1.4.3 PHIL System Stability:

For the evaluation of system properties such as system accuracy and stability, the complete PHIL setup, including filtering blocks and the PHIL interface, has to be modeled using transfer functions. Then, it is recommended to test the closed-loop PHIL system with a model representation of the HoI connected to the PHIL interface instead of the physical HoI. Stability analysis of the respective open-loop and closed-loop systems should be used to evaluate system stability properties, as per the literature [3, 5] and the suggestions in this work. In the initial testing stage, it is strongly recommended to use conservative settings (e.g., lower filter bandwidth) before starting. Then, in an iterative process, less conservative settings can be used until the desired stability limit is attained [17].

8.1.4.4 PHIL System Accuracy:

After verifying the stability of the PHIL system, the system's accuracy must be verified as well. Resulting open-loop and closed-loop transfer functions can be used for an error estimation of the PHIL setup as described in [5], and the indices in (8.3). If the accuracy is positively assessed, the PHIL can be performed. Otherwise, the following three options are available:

- a) Adjust the filter bandwidth, reducing the dynamic of the loop, increasing its stability. As a negative effect, testing accuracy decreases at higher frequencies.
- b) Redesign the scenario under study, reassessing stability and accuracy with the new scenario.
- c) Perform the PHIL testing assuming a limited bandwidth validity.

As a final step, the feedforward and feedback signal connections, I/O ports, measurement bus, software, and hardware-related safety monitoring devices, and protective emergency shut-off circuits must be verified and validated.

8.2 Test cases for PHIL Testing

A PHIL system is a powerful tool for testing hardware in realistic conditions. However, as mentioned in the previous sections, it is a relatively complex approach that requires several components and controllers. For this reason, it is vital to understand, in practice, which test case the PHIL adds value to the testing when simulations face modeling challenges or field tests are too complex to perform.

This section provides an overview of test cases conducted at large research centers worldwide, where the PHIL plays a vital role in more accurate testing of energy technologies. The test cases are arranged in a component-to-system approach.

8.2.1 Fast Frequency Support and Virtual Inertia

Background: One of the major challenges for future renewable-based energy systems is the decrease of rotating masses in the power system. To address this challenge, novel fast-frequency support and virtual-inertia strategies have been proposed in conjunction with energy storage systems.

Laboratory setup: The Power Hardware In the Loop lab in the Karlsruhe Institute of Technology (KIT), a 1 MVA PHIL system, composed of five 200 kVA COMPISO PAs, allows for various experiments on AC and DC energy storage systems providing frequency and inertia support. In recent works [16, 94], the KIT team has demonstrated the capability of flywheels to provide frequency and inertia support during disturbances, as well as acting as a virtual synchronous machine [22]. This multi PA setup also allows operation in the previously introduced MMSH configuration, with two MoI representing the primary and secondary sides of asynchronous grids, offering frequency support [21].

Testing of GFM converter and inertia support functionalities has also been conducted at the Norwegian Smartgrid Laboratory, featuring an OPAL-RT platform for real-time simulation and a 200 kVA COMPISO PA as PHIL interface [95]. However, the focus has primarily been on aspects related to the overall power system impact, including frequency nadir and ROCOF, and on the integration of intelligent electronic devices for wide-area monitoring.

PHIL Advantages: The following advantages in using PHIL testing for inertia and frequency regulation provisions have been found at the KIT and at SINTEF Energy Research :

- **State-of-the-art comparison:** The proposed frequency and inertia support approach has been validated in a realistic grid condition, comparing the performance with other papers proposing similar approaches [16]. As a consequence of the direct comparisons, the advantages and limitations of the proposed control approach have been easily highlighted.
- **Data-driven models:** As explained in recent works [93,96], the simulation models are valid only for specific scenarios. Simulations cannot represent all real hardware variables, such as auxiliary power consumption, temperature, and humidity dependencies. A data-driven model of the flywheel has been developed using PHIL testing with realistic frequency regulation scenarios, and then validated against a standard microgrid benchmark [97]. When tested under realistic conditions with other power systems, the model shows only minimal power and state-of-charge mismatches, allowing its use in any frequency-control-related approaches.
- **System limitations:** The commercial hardware has implemented several control safeguards (such as power ramp-rate characteristics) for avoiding instabilities. In [22], testing realistic flywheel settings with power ramp-rate shows the limitations of commercial flywheels in providing inertia support and the need to unlock ramp-rate settings for this service.
- **Real-time simulation of large power systems with phasor models:** The simulation in real time of large power systems to assess dynamics related to frequency oscillations or reaction to inertia support can be conveniently performed with phasor simulations. This reduces the computational complexity of the model, but the phasor model must be interfaced with a more conventional transient model to control the PA.

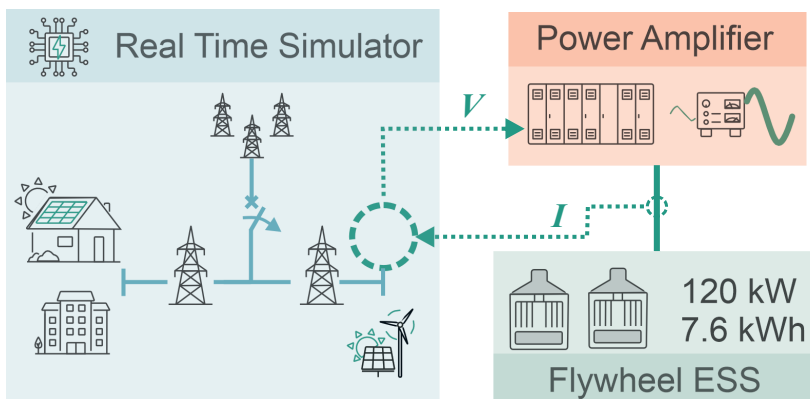


Figure 8.2: PHIL concept for flywheel applications testing

8.2.2 Microgrid Testing

Background: Modern microgrids exhibit high volatility caused by inverter-based, decentralized energy resources, flexible loads, and storage systems. In contrast to distribution grids, which can compensate for overproduction or increased load demand through the transmission system, islanded microgrids must autonomously manage generation and consumption. This results in stronger interactions between local and hierarchical control systems, the communication infrastructure, and protection devices. As highlighted in recent real-world and hardware-based studies below, microgrids must coordinate heterogeneous device behaviors, non-ideal load dynamics, and varying communication delays to maintain stability and power quality under both steady-state and transient conditions. These interactions can only be modeled to a limited extent, making hardware-based validation indispensable.

Laboratory setup: As described in IEEE Standard 2030.8 [98], pure simulations are often insufficient due to unavoidable model simplifications, which prevent reliable representation of proprietary algorithms and internal limitations of real components. Field tests, on the other hand, are costly, inflexible, and risky. Laboratory platforms such as the Electric Energy Systems Laboratory at NTUA [99] and the Smart Energy System Control Laboratory at KIT [100] bridge this gap by combining DRTS with microgrids via Single-Model, Multi-Hardware architecture (SMMH) PHIL, featuring reconfigurable AC/DC topologies that are galvanically isolated from the public grid. Observation and control of network elements occur through real communication and automation systems between components. These structures enable safe yet technically rigorous testing of both stable and critical operating conditions of microgrids.

PHIL Advantages: Several publications from NTUA and KIT demonstrate that the combination of real microgrids and new PHIL architectures, particularly SMMH, reveals dynamic interactions that simulations systematically underestimate:

- **Interoperable operation between microgrid and local controllers:** Modern microgrids are characterized by cross-layer coordination among Distributed Energy Resources (DER) primary control, secondary control, and demand-side management, and tertiary Energy Management System (EMS) control. New PHIL architectures enable simultaneous observation of interactions across all layers. According to Salcedo et al. [101], some interactions between the Supervisory Microgrid Controller and the local DER Controller can only be observed in PHIL, and these interactions are crucial for ensuring the microgrid remains stable and resilient. According to Wiegel et al. [102], microgrids must be validated as cyber-physical systems because real controller behavior, interactions among real controllers, and communication delays often dominate system dynamics.

- **Validation of microgrid dynamics:** Many DER manufacturers do not disclose internal algorithms, latencies, or limits. When modeling such components, the impact of the specific implementation is often underestimated or ignored entirely. However, proprietary synchronization algorithms, time-varying latencies, switching delays, and saturation effects are essential for stable microgrid operation, as the behavior of entire networks is often governed by the internal logic of individual DER units, given system size and coupling structure. PHIL makes it possible to systematically identify these modeling blind spots. Results from [103] show that interactions between GFM and GFL converters during transient events (islanding/grid transitions, faults) are fully observable and validly comparable only in CHIL/PHIL environments. This finding is supported by [104], which shows that the level of DER performance expected from simulations cannot be met in real-component tests because of nonlinear load behavior, resonance amplification in generators, and temporal delays.
- **Enabling standardization of validation procedures in real microgrids:** Using reference and benchmark systems together with defined PHIL test procedures, as described in [105], provides a consistent and reproducible basis for evaluating microgrids and components. This allows cross-manufacturer interoperability testing of microgrid and device controllers under identical boundary conditions. In [102], this approach is extended by integrating the SMMH architecture, real-time simulators, and a fully observable and controllable microgrid within the DRTS environment. This creates a comprehensive development and testing environment for rapid prototyping of central and hierarchical grid-control and EMS systems.

8.2.3 High Power Testing

Background: PHIL studies provide a versatile and powerful platform for testing and validating high-power system components and control strategies in a highly controlled yet realistic environment. This reduces the risk, cost, and time associated with deploying new technologies at high-power ratings and ensures robust performance under real-world conditions as an alternative to expensive field testing.

Several PHIL studies performed at Florida State University Center for Advanced Power Systems (CAPS) demonstrated applicability and flexibility of the PHIL concept in the kV/MVA range, validating a 3 MW, 13.8 kV, 60 Hz diesel generator for data center load applications, i.e., its capability in handling constant power load demands [106]. The successful PHIL testing enabled

revising the rating and consequently yielded a reduced number of generators required to carry data center loads, reducing costs significantly

Laboratory setup: Clemson University's eGRID (Electrical Grid Research, Innovation, and Development) Lab, located in North Charleston, South Carolina, is a state-of-the-art facility dedicated to advancing power systems and grid technologies [107]. It houses a 15 MW PHIL Grid Simulator that leverages the electrical infrastructure of the Dominion Energy Innovation Center and allows wind turbine generator (WTG) manufacturers to test both mechanical and electrical characteristics of their machines in a well-controlled and calibrated environment [108–110]. By moving many electrical testing scenarios previously available only through field demonstrations into a controlled environment, the HIL Grid Simulator gives WTG manufacturers a platform to ensure new innovations meet even more stringent global electrical standards. This increases reliability and lowers the cost of energy delivered. The 15 MW PHIL Grid Simulator provides electrical testing beyond fault ride-through testing for the Center to provide a complete suite of electrical testing solutions to the power conversion industry as a whole (not just the wind industry) at the multi-megawatt level. The PHIL setup at Clemson University is shown in Fig. 8.3.

CAPS is located in Tallahassee, Florida, USA, and the center has a state-of-the-art PHIL facility dedicated to advancing terrestrial and shipboard power systems. The available PHIL-interfaces are three 5 MW low- and medium-voltage AC and DC amplifiers and a 5 MW dynamometer with a speed range of up to 24 krpm. All PAs are interfaced to and controlled by real-time simulators. Overall, the amplifiers enable several nominal voltage setups, including 4.16 kV AC/700 A, 13.8 kV AC/200 A, 1 kV DC/2500 A, and combinations of four 6 kV/200 A DC setups.

PHIL Advantages: The CHIL and PHIL are being extensively used at the eGRID and CAPS facilities for robust evaluation of various use cases aimed at achieving the following objectives.

- **Grid Modernization:** Developing technologies and strategies to update the aging infrastructure of the electrical grid to meet contemporary demands.
- **Renewable Energy Integration:** Exploring methods to efficiently incorporate renewable energy sources into the grid, addressing challenges related to intermittency and variability.
- **Smart Grid Technologies:** Innovations in smart grid technologies, including advanced metering, demand response, and intelligent grid management systems.
- **Power Electronics:** Research on advanced power electronics for improved control and efficiency in power transmission and distribution.

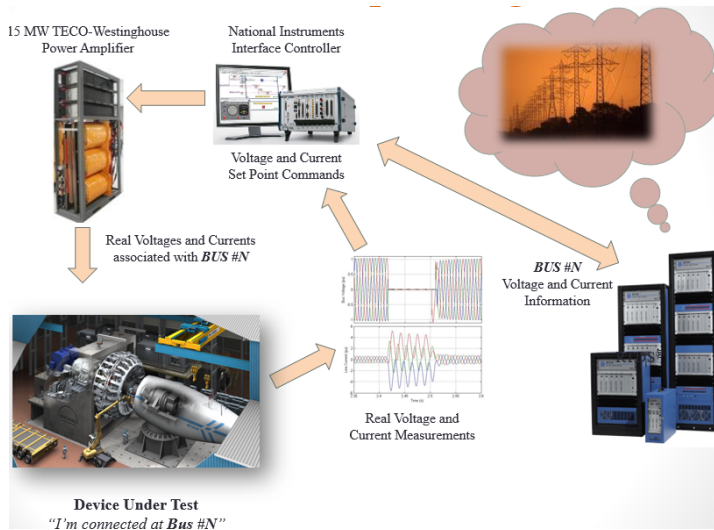


Figure 8.3: PHIL setup at Clemson University's eGRID.

- **Cybersecurity:** Enhancing the security of the electrical grid against cyber threats, ensuring resilient and secure operation.
- **Superconducting technologies:** Validation of superconducting technologies, such as motors and fault current limiters.
- **Motors:** research on high-power, high-speed generators and motors for naval applications.

8.2.4 Emulation of Electric Drives

Background: Another example of an application where PHIL can significantly simplify testing procedures and introduce additional flexibility is high-power inverter testing. The inverters for electric vehicle drive trains and industrial drives are traditionally tested using motor-generator groups, which, due to spinning masses, require specific safety measures in the test laboratory. Additionally, a single motor-generator group is suitable only for testing inverters with rated powers within a specific range. More flexible test benches are needed to accelerate inverter development.

Laboratory setup: High-power inverters can be tested using PHIL (to simulate the operation of an electrical machine) instead of motor-generator groups [33, 111, 112]. The model of an electrical machine is executed in a real-time simulator, and the setpoints are then sent to the PA to reproduce voltages and currents of the simulated machine. An example of the experimental

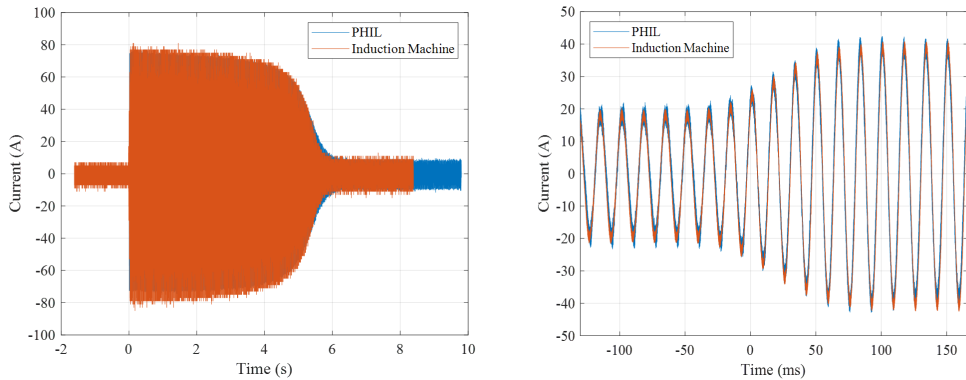


Figure 8.4: Transient response of a 22-kW induction machine vs. the same machine simulated with PHIL: (left) direct-online start transient, and (right) load step transient from 9 kW to 18 kW.

waveforms of the startup and load transients of a real 22 kW induction machine compared to the same machine simulated in PHIL is illustrated in Fig. 8.4 [112].

PHIL Advantages: Using PHIL for high-power machine emulation permits flexible validation of machine controllers and components:

- **Multi-machine emulation:** it can significantly simplify the test setup by replacing multiple motor-generator groups with a single PHIL system that simulates a wide range of electric machines (including different types). This is done by simply changing the simulation models to simulate different types of machines (or by loading different parameter sets to simulate the same type of machine with different properties), while using the same test setup hardware.
- **Sensor testing:** the PHIL emulation of machines enables the easy integration of various types of position/speed feedback devices (e.g., resolvers or encoders) into the simulated machine model.

All this makes the PHIL approach very practical and attractive because it significantly reduces the hardware requirements for the test equipment and the time required for reconfiguration, while enabling a much higher level of test system versatility.

8.3 Research Points to be Explored for PHIL

The PHIL is still a relatively novel topic when compared to electric drives and renewables. Recent advancements in PA technologies and real-time simulators have enabled wider adoption of this approach. However, a few remaining open topics need to be addressed to enable wider adoption of PHIL for testing and validation of electrical equipment in industrial environments. Some of those topics are summarized in this section.

Testing at medium voltage: the industry is currently focused on designing medium-voltage power converters for grid stability (e.g., MV DC grids) or for large electrochemical plants (e.g., electrolyzers, power-to-X). However, their testing in PHIL is challenging, due to the high power and voltage requirements. Two approaches are possible in this case: (i) employing a multi-MW low-voltage converter with a step-up transformer to the desired voltage. This solution has already been applied in several existing PHIL setups [107, 113, 114], and PA companies can offer off-the-shelf products. The main issue with this solution lies in the transformer dynamics and linearity, which require additional efforts to avoid inaccuracies during testing. To address this, dynamic compensation approaches have been incorporated into the PA controllers to account for transformer dynamics. (ii) employing a multi-MW medium-voltage converter (e.g., modular multi-level converters) that is connected directly to the System Of Interest (SOI). This approach can potentially increase test accuracy, but it is still in its early stages of adoption and needs further evaluation. Several facilities using this approach are currently under development, such as the High Power Grid Lab at the Karlsruhe Institute of Technology [115]. Major concerns regarding bandwidth and fault-current interruption (in half-bridge topologies) remain open points for future research.

Faults: PHIL testing is accurate only within a certain dynamic range. Due to delays and filters in the interface algorithm, and the limited transient capability of some switched-mode amplifiers, the faster dynamics generated by faults are difficult to emulate. In particular, DC fault phenomena, which are extremely important for the development of DC technologies, have time constants of a few milliseconds, making them difficult to reproduce accurately in hardware. In addition, testing laboratories take a conservative approach when performing fault studies due to the high risk of damaging equipment during testing. There is still no general consensus on how to emulate faults with PHIL.

Unbalanced grids: the majority of PHIL tests involve single-phase or balanced three-phase systems. No significant attention has been given to unbalanced systems mainly because of the nature and requirements of typical systems: electrical drives, power electronics for photovoltaic or energy storage systems. All these systems are usually controlled with a balanced current injection.

Recently, greater attention has been given to the single-phase fault-ride-through capability of converters. Initial studies on asymmetrical grid faults [116] provided an initial assessment of testing accuracy. However, the field still lacks a general approach to the study of unbalanced systems, particularly during transients.

Distributed PHIL: PHIL test laboratories are costly facilities that are typically tailored to specific testing needs, such as higher voltages or faster dynamics. In addition, larger laboratories may need to test specific bulk components that are not movable, such as transformers, long cables, or breakers.

Researchers in real-time simulation have recently been working on creating distributed real-time labs, where electrical variables are exchanged over the internet in real time between laboratories hundreds of kilometers apart, with reduced delays (tens to hundreds of milliseconds). This concept has already been proven in the field of digital real-time simulation [117–119], where simulated variables are exchanged among labs to investigate delay and stability. The concept of distributed-PHIL is relatively new [120, 121], with initial work on loop delay and stability analysis [122]. However, safety and accuracy aspects of this approach need to be further developed and standardized.

8.3.1 Advanced PHIL Systems Architectures

PHIL was initially conceived for testing a single hardware unit connected to a simulated system at a single point of connection [3, 4]. A first reason is that the PHIL was historically intended to replace laboratory testing, such as type-tests, and involved only one machine or converter interacting with the rest of the system; second, the DRTS and PA technologies were still rather immature and offered limited computational and testing capabilities.

The improvements in DRTS and PA technologies, together with reductions in costs per simulation core and kVA, enabled the realization of more complex PHIL system architectures, involving additional points of connection between the hardware and the simulation model. New PHIL system architectures are identified and classified in this section.

8.3.1.1 Multi-Model, Single-Hardware Architecture (MMSH)

Usually, shunt-connected devices (e.g., photovoltaics, batteries) can be tested with a single point of connection to the rest of the PHIL system. However, the same as Chapter 7, several series

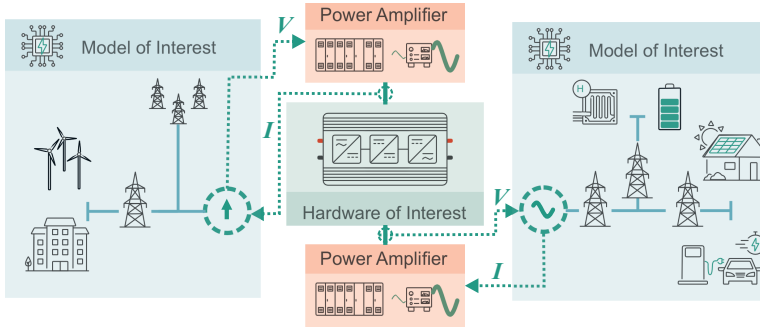


Figure 8.5: Multi-Model, Single-Hardware PHIL architecture (MMSH). A multi-port hardware is coupled to several simulation environments via separate PHIL systems.

devices (e.g., power lines, transformers, breakers, power electronic converters) require multi-port connections to correctly emulate the behavior of the environment (e.g., power grid, load, etc.) at all their connection ports (e.g., the primary and multiple secondaries of a transformer). To properly test these devices, a MMSH PHIL system architecture must be adopted. This architecture assumes connecting one HoI to two or more PA ports. Each of these ports is connected to the simulator using an independent power interface.

As an example of MMSH architecture, Fig. 8.5 shows a possible PHIL system architecture to test a power electronics converter connected between two independent distribution feeders. A three-stage power electronics converter, such as a Solid State Transformer (SST), is connected to the rest of the PHIL system at two points. In this case, a voltage-type PHIL interface algorithm is implemented on the primary side due to the GFL characteristics of the SST primary-side. A current-type PHIL interface algorithm connects the secondary side of the SST with the supplied distribution grid (right MoI). Any other voltage- and current-type interface algorithm can be used for this PHIL system architecture. If a disturbance occurs at the secondary side of the SST, its effect can be seen in the grid connected to its primary side, and vice versa.

Applications: series elements testing, such as power lines (e.g., superconductive), transformers, breakers, power electronics systems (uninterruptible power supplies, wind turbines, Type-4 converters, SSTs).

8.3.1.2 Single-Model, Multi-Hardware architecture (SMMH)

SMMH architecture assumes multiple individual HoIs being interfaced to a single MoI. As shown in Fig. 8.6, this architecture enables testing the interaction between different HoIs in realistic

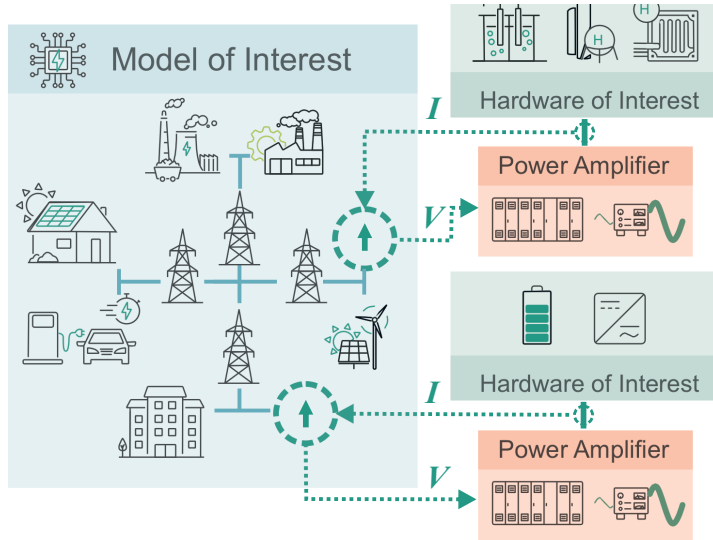


Figure 8.6: Single-Model, Multi-Hardware PHIL system architecture (SMMH). Several separated HoIs are connected to the same MoI by means of separated PHIL systems.

conditions [123]. This feature is particularly important during testing the control and plant interactions between power electronics converters (e.g., between wind turbine converters in wind farms). It is noted that the testing scenario and the interaction dynamic between these HoI systems are strictly dependent on the PHIL system dynamics. Faster dynamics, such as high-frequency resonances and harmonics, may be filtered out by slow power interfaces (e.g., limited-bandwidth PAs or low-bandwidth filtering).

Applications: microgrid high-level controller, harmonic oscillation and instability analysis, fast reconfigurable networks.

8.3.1.3 Partial-PHIL

High-voltage PHIL testing (e.g., for HVDC) is very challenging to perform in laboratories due to the need for (extra) high-voltage facilities and high-power supplies. The current state of the art primarily offers Simulation-in-the-Loop or CHIL solutions to test control strategies such as voltage balancing [124], protections [125, 126], and modulation schemes [127]. However, these approaches do not realistically assess losses and cooling performance, switching dynamics and dead times, the effect of energizing auxiliary power supplies, etc.

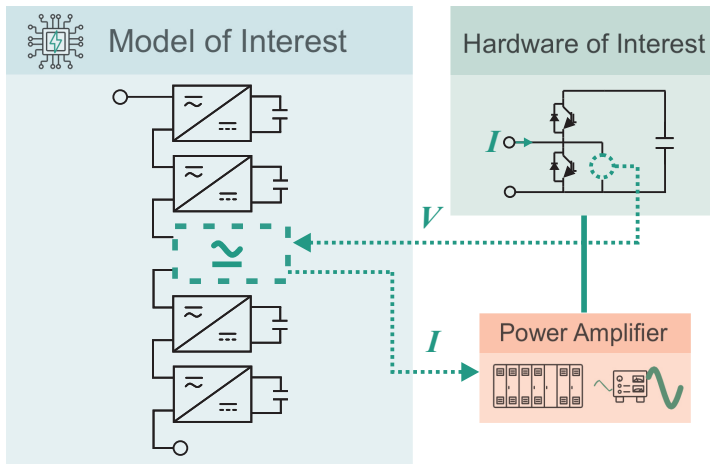


Figure 8.7: Partial PHIL System - validation of a full-scale low-voltage single submodule.

To partially address these problems and perform a more realistic assessment of high-voltage power electronics devices, the concept of a Partial-PHIL system is introduced, as shown in Fig. 8.7 [128]. The idea is to model the full converter in the DRTS, in conjunction with a replica controller in the loop, except for a single submodule implemented in low-voltage hardware and connected to a PA. The Partial-PHIL system enables the assessment of the real performance of a single submodule, for example, one of a modular multi-level converter (MMC), and then to improve the hardware design of the submodule before full assembly. With the DRTS and the replica controller in the loop, it is possible to replicate exactly identical voltage, current, and switching profiles of the submodule under test as in a real MMC. This approach offers clear advantages, enabling testing in low-voltage environments while retaining the accuracy of testing full-power rating modules.

Applications: high-voltage multi-level converters, such as MMC or Cascaded H-Bridge converters.

8.3.1.4 Testing More Energy Carriers: the Multi-Physics Hardware-In-the-Loop Concept

Novel energy technologies are designed to convert energy from multiple energy carriers to increase system-level energy efficiency. For example, waste heat from generators has been used for decades to feed local district heating networks, and now technologies such as fuel cells generate high-temperature heat as a by-product of chemical reactions. While industry attention has been heavily

focused on these multi-energy-carrier technologies, little has been done to test them under realistic laboratory conditions.

An innovative concept that is currently being introduced is the Multi-Physics Hardware-In-the-Loop. This concept involves parallel testing of the electrical, thermal, or gas layers of the system under test to validate the performance of each energy layer in a coordinated manner (i.e., not independently). To achieve comprehensive multi-physics testing, the thermal layer must be properly tested. For this reason, the concept of Thermal Hardware-In-the-Loop is introduced, where the MoI is any heating network, varying from a city-wide system to a single cooling loop, and the HoI is any technology tasked to absorb or generate heat, Fig. 8.8.

A first attempt at multi-physics Hardware-In-the-Loop was performed in [129], where the thermal and hydraulic layers were emulated together with the electrical one. The setup properly emulated the energy behavior of a small residential house and validated a heat pump concept as a system under test. Although the concept has been introduced, the following topics still need to be addressed: (i) for the hydraulic and thermal layers, the mathematical formulation of the power interface algorithm needs to be developed, as for the electrical layer (e.g., with the ITM). (ii) Novel hardware for the power interface needs to be designed and built. The dynamics of the thermal and hydraulic actuators are several orders of magnitude slower than those of the electrical actuators. Slower transients (e.g., daily thermal needs for a house) can be easily emulated with current actuator technologies. However, for faster thermal dynamics, such as the ones generated by different power electronic converter operations, this may be challenging.

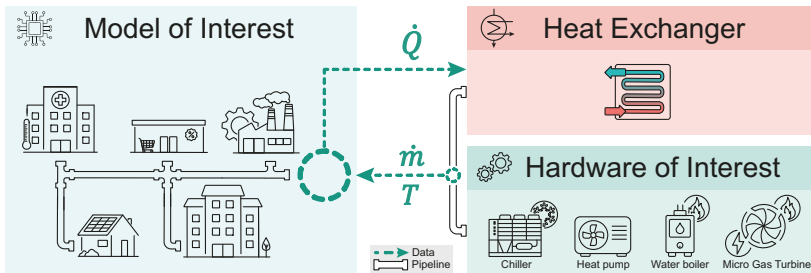


Figure 8.8: Thermal Hardware In the Loop concept, coupling a simulated heating network (MoI) with a thermal resource (HoI).

8.4 Summary

Reproducing realistic grid conditions in the lab in a safe, repeatable way allows manufacturers to reduce testing time and costs, and for utilities to alleviate integration concerns. The PHIL research field is relatively new, with the first publications published only twenty years ago and the first IEEE recommended practice published only in 2025. The chapter offers a recommended guideline for implementing PHIL systems in industrial facilities, considering different scenarios, hardware topologies, and scalability, testing accuracy, and stability. It introduces a first classification of PHIL testing architectures, including multi-port and multi-system configurations, to expand the classical single-device, single-system testing approach.

While the research field has been extensively explored, particularly regarding loop stability, significant work still needs to be done on scalability, dynamics, non-idealities, accuracy, and standardization. This offers fertile ground for new ideas for both academia and industry.

9 Summary, Conclusion and Outlook

9.1 Summary and Conclusion

This thesis investigates the modeling, stability, and accuracy of PHIL, with a particular focus on the influence of interface dynamics, converter control, and advanced modeling approaches. The work aims at providing both theoretical foundations and practical guidelines for reliable PHIL implementation in modern power electronic applications.

The thesis begins by establishing the fundamental role of PHIL interfaces and their impact on system behavior. It is shown that interface effects can be primarily categorized into time delays, which influence the phase response, and bandwidth limitations, which affect both gain and phase characteristics. Through transfer-function-based analysis and comparative studies of classical interface algorithms, the limitations of PHIL systems in reproducing simulation results are highlighted.

To improve modeling accuracy, a novel multi-rate discrete-time modeling approach is introduced. Unlike conventional continuous-time and single-rate discrete-time methods, the proposed method separates the fast dynamics of analog hardware from the slower real-time simulation domain. The approach is validated through frequency-domain analysis, error metrics, and experimental results, demonstrating superior accuracy, particularly in capturing phase behavior, compared to existing methods.

The thesis challenges the conventional assumption that PHIL limitations originate solely from interface components. It demonstrates that the dynamics of an active HoI, such as a grid converter, significantly influence both stability and accuracy. In particular, the current controller bandwidth is shown to play a critical role, affecting not only system stability margins but also the fidelity of PHIL results. This highlights the necessity of coordinated tuning between interface parameters and converter control.

To systematically analyze stability, the thesis adopts an impedance-based framework, leveraging the Nyquist stability criterion applied to the impedance ratio at the PCC. This approach incorporates the dynamics of the grid emulator, PHIL interfaces, and converter control systems. The developed impedance models are validated through simulations and experimental measurements, demonstrating that stability can be reliably assessed even in the absence of fully detailed hardware models. The analysis is further extended to include practical aspects, such as sensor placement, showing that, in that case, the voltage-sensing location significantly affects stability margins, while current sensing has a comparatively minor impact.

The work also advances converter modeling by incorporating dc-link dynamics, revealing additional internal stability conditions beyond the impedance-ratio criterion. It is shown that the presence of internal unstable dynamics can invalidate conventional stability assessments, emphasizing the importance of verifying both internal and external stability conditions in PHIL systems.

Furthermore, the thesis evaluates interface algorithm selection by comparing voltage-type and current-type interface methods for both grid-following and grid-forming converters. Contrary to common assumptions, the results demonstrate that stability is not strictly determined by converter type but depends on the interaction between system parameters and interface configurations.

The analysis is then extended to more complex systems by investigating a back-to-back converter as the HoI. A novel impedance modeling approach with coupled subsystems is developed, introducing dual stability criteria to capture the interdependence between converter stages. The results confirm that system stability depends on the interaction between subsystems, and a structured assessment procedure is proposed to guide stability evaluation in such configurations.

Finally, the thesis translates the developed theoretical insights into practical guidelines for industrial PHIL implementation. It proposes a classification of PHIL architectures, including multi-port and multi-system configurations, and outlines key considerations for scalability, accuracy, and stability. These contributions advance theoretical understanding of PHIL systems while providing practical tools for pre-experimental stability and accuracy assessment. The proposed methodologies reduce the risk of hardware damage, improve the reliability of results, and lay the groundwork for standardized PHIL testing procedures.

9.2 Outlook

- The proposed multi-rate modeling approach for PHIL systems has been examined using a set of passive loads. This concept can be further extended to include a grid converter as the HoI. In such a case, the impedance model of the grid emulator can be represented as $Z_{EG}(z)$, while the HoI impedance is described as $Z_{HoI}(s)$. If a digital controller is also included on the HoI side, Z_{HoI} becomes a multi-rate model as well.
- The mathematical approaches presented in this thesis rely on the knowledge of the MoI and HoI models. However, in industrial testing, such models are often unavailable or protected by intellectual property rights. Therefore, further research is needed on the automatic estimation of the MoI and HoI dynamics, for example, through impedance estimation methods, as well as on the automatic assessment of stability and accuracy margins.
- Due to the increased mathematical complexity, and because the PLL dynamics are typically separated from PHIL instability phenomena in the frequency range, i.e., they mainly affect the lower-frequency region rather than the delay, related range, the impact of the PLL has been neglected in the PHIL assessment of this thesis. Nevertheless, the PLL clearly affects the low-frequency behavior and can lead to inaccuracies. Therefore, especially when the HoI model is not fully known, the PLL dynamics should be included, which would require representing the converter-side impedance as a 2×2 matrix instead of a single element.
- This thesis has deliberately focused on a SISO-based stability analysis. However, when a multi-port PHIL setup is considered (a back-to-back converter), a more accurate impedance-based analysis requires a multi-input, multi-output representation, since the current on one side can be coupled to the voltage on the other side.
- The stability analyses presented in this thesis have considered either single-phase systems or perfectly balanced three-phase systems. Future work should place greater emphasis on unbalanced systems, as they better reflect practical power systems.

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List of Publications

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- [J1] F. Ashrafadehkordi, D. Kottonau, and G. D. Carne, “Multi-rate discrete domain modeling of power hardware-in-the-loop setups,” *IEEE Open Journal of Power Electronics*, vol. 4, pp. 539–548, 2023.
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