High-Frequency and Broadband Silicon Output-Stage Amplifiers for Wireless and Optical Transmitters

Zur Erlangung des akademischen Grades eines

DOKTORS DER INGENIEURWISSENSCHAFTEN (Dr.-Ing.)

von der KIT-Fakultät für
Elektrotechnik und Informationstechnik
des Karlsruher Instituts für Technologie (KIT)

angenommene

DISSERTATION

von

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Tag der mündlichen Prüfung: 16.07.2026

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Zusammenfassung

Diese Arbeit untersucht zentrale Entwurfsaspekte von hochfrequenten und breitbandigen Ausgangsstufen und demonstriert entsprechende Silizium-Implementierungen für drahtlose und optische Sendeanwendungen. Der Fokus liegt auf Bandbreite, Linearität, Effizienz und Stabilität, um den Herausforderungen von immer breitbandigeren und schnelleren Kommunikationssystemen zu begegnen.

Grundlegende Aspekte der digitalen Signalmodulation und des Verstärkerentwurfs werden behandelt, wobei die Einflüsse von Transistorkonfigurationen, differentiellen Architekturen und Anforderungen an die Ausgangstreiberleistung in verschiedenen Anwendungsszenarien hervorgehoben werden. Prinzipien von Silizium-Leistungsverstärkern (PAs) werden ebenfalls zusammengefasst, mit besonderem Schwerpunkt auf transformatorbasierter Leistungskombination und fortschrittlichen Power-Combining-Methoden für integrierte PA-Implementierungen.

Auf Grundlage dieser Überlegungen werden mehrere repräsentative transformatorbasierte lineare PAs vorgestellt, die in SiGe- und CMOS-Technologien realisiert sind und die *K*u-, *K*a- und V-Bänder abdecken. Diese Entwürfe untersuchen verschiedene architektonische Ansätze und Performance-Kompromisse. Zwei PAs nutzen eine strombasierte Leistungskombination, um die Ausgangsleistung (P_{out}) zu steigern und gleichzeitig eine mittlere bis hohe Power-Added Efficiency (PAE) beizubehalten. Ein 28-GHz PA zielt auf eine hohe Leistungsdichte bei gleichzeitig hoher Linearität und Effizienz ab und erreicht eine gesättigte P_{out} von 22.7 dBm sowie eine Spitzen-PAE von 38.1 %. Darüber hinaus werden Balanced- und Doherty-PAs entwickelt, um die Robustheit gegenüber Antennenvariationen bzw. die Back-off-PAE zu verbessern. Zudem werden Entwurfsstrategien angewendet, um die Fläche der Hybridkoppler zu minimieren.

Die Großsignalstabilität wird weiterhin als entscheidender Entwurfsaspekt bei breitbandigen SiGe-PAs untersucht. Die Auswirkungen nichtlinearer Kapazi-

täten auf die Stabilität werden analysiert, und die zugrunde liegenden Instabilitätsmechanismen werden mittels fortschrittlicher Großsignalanalyse identifiziert und durch Messungen an einem gefertigten PA verifiziert. Auf Grundlage dieser Erkenntnisse wird ein breitbandiges *K*u/*K*a-Band SiGe-PA mit Common-Collector–Common-Base (CC–CB)-Konfiguration vorgeschlagen und demonstriert. Dieses zeigt eine reduzierte Empfindlichkeit gegenüber Großsignalinstabilität und erreicht eine 17 – 28 GHz (49 %) P_{1dB} 3-dB-Bandbreite.

Schließlich wird ein linearer 100-GBd SiGe-Optikmodulator-Treiber für optische Kurzstreckenverbindungen demonstriert, wobei Aspekte des Hochgeschwindigkeitsbetriebs hervorgehoben werden. Solche Verbindungen sind kritische Komponenten sowohl in drahtlosen Backhaul-Infrastrukturen als auch in KI-basierten Datenübertragungssystemen. Der Treiber liefert einen differentiellen Spannungshub von 2.6 V_{pp} bei einer Ratio of Level Mismatch (RLM) von 91 % für ein 75-GBd PAM4-Signal.

Abstract

This work investigates critical design aspects of high-frequency and broadband output-stage amplifiers and demonstrates corresponding silicon implementations for wireless and optical transmitter applications. The study focuses on bandwidth, linearity, efficiency, and stability, addressing the challenges arising from increasingly broadband and high-speed communication systems.

Fundamental aspects of digital signal modulation and amplifier design are addressed, emphasizing the effects of transistor configurations, differential architectures, and output-driving requirements across diverse application scenarios. Silicon power amplifier (PA) principles are also summarized, with a particular focus on transformer-based power combining and advanced combining techniques for integrated PA implementations.

Based on these considerations, several representative transformer-based linear PAs implemented in SiGe and CMOS technologies are presented, covering the *K*u-, *K*a-, and V-bands. These designs explore different architectural choices and performance tradeoffs. Two PAs employ current power combining to enhance output power (P_{out}) while maintaining moderate to high power-added efficiency (PAE). One 28-GHz PA targets high power density with both high linearity and efficiency, achieving a saturated P_{out} of 22.7 dBm and a peak PAE of 38.1 %. Additionally, balanced and Doherty power-combining PAs are developed to improve robustness against antenna variations and back-off PAE, respectively. Design strategies are also applied to limit the area of the hybrid couplers.

Large-signal stability is further investigated as a critical design aspect in broadband SiGe PAs. The effects of nonlinear capacitances on stability are analyzed, and the underlying instability mechanisms are identified using advanced large-signal analysis and verified through measurements of a fabricated PA. Guided by these insights, a *K*u/*K*a-band broadband SiGe PA employing a common-collector–common-base (CC–CB) configuration is proposed and demonstra-

ted, exhibiting reduced sensitivity to large-signal instability and achieving a 17 – 28 GHz (49 %) P_{1dB} 3-dB bandwidth.

Finally, a 100-GBd linear SiGe optical modulator driver is demonstrated for short-reach optical links, highlighting high-speed operation considerations. These links are critical components in both wireless backhaul and AI-related data transmission systems. The driver delivers a differential swing of 2.6 V_{pp} with a ratio of level mismatch (RLM) of 91 % for a 75-GBd PAM4 signal.

Acknowledgment

First, I would like to express my sincere gratitude to Prof. Dr.-Ing. Ahmet Çağrı Ulusoy for his full support during my work at IHE and for granting me a great deal of research freedom. I would also like to thank Prof. Dr.-Ing. Hermann Schumacher for generously taking the time to serve as the second examiner of this thesis.

Furthermore, I am grateful to the technical staff at IHE—Andreas Lipp, Thorsten Fux, Mirko Nonnenmacher, and Andreas Gallego—for their invaluable assistance with packaging. My thanks also go to Simone Gorre, Marion Jentzsch, and Angela Ziemba for patiently guiding me through the complexities of university bureaucracy and paperwork. I extend my special thanks to Florian, Lucas, Basim, Christian, Kateryna, Selina, Matthias, Joachim, Tai-Yu, Daniel, Alex Q., Luca, Ibrahim, Kaan, and Ahmed. I deeply value the immense support and fruitful discussions I received, and my regards also go to those among you who were my office mates. Finally, I offer my warmest regards to all my other former colleagues at IHE for the wonderful time we spent working together.

Last but not least, I owe my deepest gratitude to my family for supporting me throughout my life, as well as my parents, my brother Prof. Tsai, and Leo. My sincere appreciation also goes to the faculty at NTUEE, particularly Prof. Huei Wang and Jeng-Han, for their mentorship during my earlier years.

Berlin, July 2026

Tsung-Ching Tsai

Contents

Acronyms and Symbols

List of Abbreviations

NR	New Radio
FR	frequency range
mm-wave	millimeter-wave
MIMO	multiple-input multiple-output
eMBB	enhanced mobile broadband
UE	user equipment
BS	base station
B5G	beyond-5G
EIRP	effective isotropic radiated power
PA	power amplifier
Tx	transmitter
BV	breakdown voltage
HBT	heterojunction bipolar transistor
CPE	customer premises equipment
Satcom	satellite communication
LEO	low-Earth orbit

GEO	geostationary orbit
DRA	direct-radiating array
TID	total ionizing dose
FWA	fixed wireless access
AI	artificial intelligence
IM/DD	intensity modulation and direct detection
DSP	digital signal processing
NRZ	non-return-to-zero
PRBS	pseudo-random binary sequence
PAM	pulse-amplitude modulation
SNR	signal-to-noise ratio
ISI	intersymbol interference
PAPR	peak-to-average power ratio
QAM	quadrature amplitude modulation
BW	bandwidth
CC–CB	common-collector–common-base
IMD	intermodulation
CW	continuous wave
THD	total harmonic distortion
AM–PM	amplitude–to–phase
ACPR	adjacent-channel power ratio
CCPR	co-channel power ratio

NPR	noise power ratio
SNDR	signal–to–noise–and–distortion ratio
EVM	error-vector magnitude
RLM	ratio of level mismatch
AM–AM	amplitude–to–amplitude
FET	field-effect transistor
CE	common-emitter
CS	common-source
CB	common-base
IHP	Leibniz Institute for High Performance Microelectronics
CC	common-collector
CD	common-drain
CMRR	common-mode rejection ratio
RHP	right-half-plane
NDF	normalized determinant function
LO	local oscillator
Si-based	silicon-based
PAE	power-added-efficiency
TF	transformer
BEOL	back-end-of-line
OMN	output matching network
MIM	metal-insulator-metal

SRF	self-resonance frequency
VSWR	voltage standing wave ratio
LMBA	load-modulated balanced PA
MAG	maximum available gain
IL	insertion loss
CTAT	complementary-to-absolute-temperature
AWG	arbitrary waveform generator
GF	GlobalFoundries
EM	electromagnetic
IMN	input matching network
RL	return loss
QB	quasi-balanced
OBO	output power back-off
ISMN	interstage matching network
DPD	digital predistortion
MZM	Mach–Zehnder modulator
EAM	Electro-absorption modulator
EF	emitter-follower
DLN	distributed load network
VNA	vector signal analyzer
GD	group delay

1 Introduction

As modern society increasingly relies on networked communication infrastructures for information exchange—including mobile voice and data services—the demand for advanced communication techniques continues to grow. The resulting surge in data-rate requirements drives the development of circuits operating at increasingly higher frequencies and wider bandwidths, enabled by advanced, high-performance, and cost-effective silicon semiconductor technologies. Within this context, transmitter frontend circuits—particularly output-stage amplifiers—play a critical role, as they account for the dominant portion of the total power dissipation. This work focuses on the design of modern silicon transmitter output-stage amplifiers, considering different application scenarios and a range of design objectives.

1.1 5G, Satellite, and Optical Backhaul Communications Using Silicon Technologies

Parts of the following section were previously published in [1, 6, 7, 9] and [10].

The ever-growing demand for high-data-rate mobile data transmission has driven the standardization and deployment of 5G New Radio (NR). Defined as frequency range 2 (FR2), spanning the *K*a-band to the V-band, millimeter-wave (mm-wave) operation together with massive multiple-input multiple-output (MIMO) techniques is employed to enhance data rates and spectral efficiency for enhanced mobile broadband (eMBB). Consequently, interest in mm-wave front-end integrated modules for both user equipment (UE) and base stations (BSs) has increased significantly. More recently, frequency range 3 (FR3), extending from the X-band to the *K*a-band, has been actively discussed for

beyond-5G (B5G) systems and is regarded as a promising candidate to bridge and extend the conventional frequency range 1 (FR1).

To address the high path loss at mm-wave frequencies, phased-array systems are employed to achieve the required effective isotropic radiated power (EIRP). In multi-Gb/s systems, silicon technologies are favored for their ability to enable high levels of integration with digital and mixed-signal circuitry. However, the scaling of supply voltage in modern high-performance silicon technologies poses significant challenges for the design of medium- and high-power output-stage amplifiers, i.e., power amplifiers (PAs), in phased-array transmitters (Tx). For example, the collector–emitter breakdown voltage (BV_{CEO}) of state-of-the-art SiGe heterojunction bipolar transistors (HBTs) typically lies in the range of $1.4 - 1.7\,\mathrm{V}$. Nevertheless, owing to the use of antenna arrays in phased-array architectures, the required element output power can still be achieved using silicon technologies, depending on the application scenario. In UE with limited form factor and, consequently, a restricted number of antenna elements [SPD+16], a higher per-element output power (P_{out}) is required [DDT+19]. For BS applications, certain scenarios—such as local-area customer premises equipment (CPE) and medium-range coverage—demand a medium per-element P_{out} exceeding 20 dBm [Cam18].

Beyond terrestrial cellular systems, satellite communication (Satcom) applications have also expanded rapidly in recent years, driven by the demand for global broadband coverage. Large-scale *K*a-band Satcom phased arrays now deployed for low-Earth orbit (LEO) constellations, where uplink and downlink are separated into $27 - 30\,\mathrm{GHz}$ and $17.7 - 20.1\,\mathrm{GHz}$ bands, respectively [ACC+23]. Given the successful commercial development of phased arrays with thousands of elements in LEO, next-generation large-scale direct-radiating arrays (DRAs) in geostationary orbit (GEO) are foreseeable. For a target EIRP of 74 dBW, the required PA per-element P_{out} is in the range of $15 - 25\,\mathrm{dBm}$ [ACC+23]. In this context, SiGe BiCMOS technology becomes particularly attractive for emerging *K*a-band DRA applications due to the PA's high efficiency [6] and the availability of integrated CMOS circuitry for enhanced system functionality. Moreover, SiGe technology has been demonstrated to exhibit tolerance to total ionizing dose (TID) and heavy-ion effects, making it well suited for space applications [Cre13, TIT+21]. At even higher frequencies, the V-band such as 60 GHz is extensively explored to support high-throughput communication [NC17]. In addition, fixed wireless access (FWA) has emerged as a prominent solution in

urban environments, offering a cost-effective alternative to traditional cable or fiber deployments. While much of the current focus remains on the *K*a-band, the V-band is increasingly regarded as a key candidate for achieving even higher data rates [AWZ+20].

In parallel with wireless communication systems, the backhaul infrastructure, core networks, and data centers are driving the development of 800-GbE and 1.6-TbE systems. The rapid advancement of artificial intelligence (AI) infrastructure further intensifies the demand for high-speed data transmission, making optical communication a focal point due to its inherently broadband nature. Conventional short-reach optical links employing intensity modulation and direct detection (IM/DD) are undergoing significant upgrades to accommodate the rapidly increasing network throughput [Cha19]. As a result, single-lane data rates are moving beyond 200 Gb/s [All25]. Furthermore, driven by the massive demand for pluggable optical modules, direct-drive transceiver architectures [All25, MKQ+25] have emerged as a promising solution to significantly reduce power consumption compared with conventional modules equipped with digital signal processing (DSP) chips. In this context, the design of linear output-stage amplifiers for linear-drive transmitters plays a crucial role, particularly when implemented in advanced silicon technologies.

1.2 Modulation Formats and Transmitter Amplifier Design Considerations

In the aforementioned communication systems, digital modulation schemes are employed to enable reliable and spectrally efficient data transmission. For the design of transmitter front-end amplifiers, a clear understanding of the requirements and characteristics of commonly used modulation techniques is essential.

A random binary sequence with a bit period of T_b, representing realistic bit streams with randomly distributed 0s and 1s, exhibits a sinc-shaped spectrum in the frequency domain, with nulls occurring at the symbol (baud) rate ($R_s = 1/T_b$) and its harmonics. Such a signal is also referred to as a non-return-to-zero (NRZ) signal. In practice, a pseudo-random binary sequence (PRBS) is typically used, since its length is finite. In this case, the spectrum consists of multiple

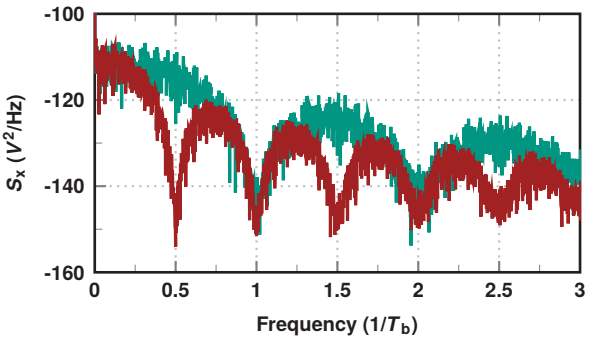


Figure 1.1: Power spectral density of an NRZ signal with symbol rate of $1/(T_b)$ (green) and a PAM-4 signal with symbol rate of $1/(2T_b)$ (red), both achieving the same bit rate.

closely spaced impulses whose envelope still follows the sinc function described above, as shown in Figure 1.1. Despite the two-level nature of NRZ signals, more efficient data transmission can be achieved by employing multi-level modulation schemes such as M-ary pulse-amplitude modulation (M-PAM or PAM-M). For the same bit rate, these schemes reduce the occupied bandwidth. For instance, in a PAM-4 signal, as shown in Figure 1.1, we take symbol rate of $1/(2T_b)$ to achieve the same bit rate as the NRZ signal, which shifts the null positions of the sinc spectrum by $1/(2T_b)$. This effectively halves the required bandwidth, though at the cost of a reduced signal-to-noise ratio (SNR), as four amplitude levels are used to encode the bits, which are squeezed into the same voltage range.

For prevention of intersymbol interference (ISI) in the time domain, the Nyquist criterion [Nyq28] was derived for band-limited signals. It states that the channel's or matched filter's single-sided bandwidth (W) must be at least half the signal's symbol rate $1/T_b$, i.e., $W \geq 1/(2T_b)$, where $1/(2T_b)$ is referred to as the Nyquist frequency. Hence, the Nyquist frequency dictates the bandwidth requirement for high-speed wireline and optical transmissions, where raw data sequences are directly conveyed.

In parallel, properly designed and shaped pulses can be employed to synthesize PAM signals. For example, a (root-)raised cosine pulse shaper satisfies the Nyquist criterion, with its shape and bandwidth adjustable via the roll-off factor

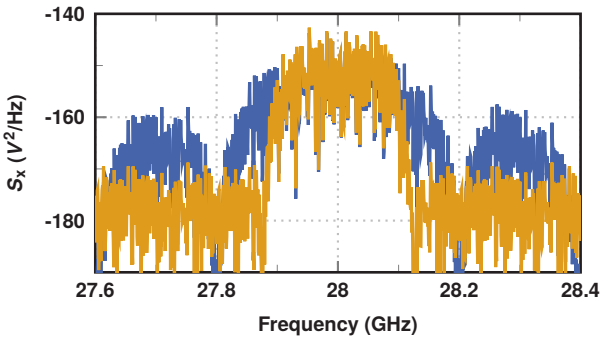


Figure 1.2: Power spectral density of 16-QAM signals at 28 GHz with/without raised-cosine filter (orange/blue). Symbol rate is 200 MHz.

(α) [Joh07, Beh11]. Particularly in wireless applications, this type of pulse shaping is widely adopted, since RF bandwidth is very limited and signal leakage into adjacent channels is strictly prohibited. However, incorporating a pulse shaper also increases the peak-to-average power ratio (PAPR) of the signal [VMR17], which poses additional design challenges for wireless transmitters, particularly for the PAs.

Moreover, to further enhance spectral efficiency in wireless/RF passband transmissions, two independent baseband PAM data streams, $x_\mathrm{I}(t)$ and $x_\mathrm{Q}(t)$, can be orthogonally combined to form a quadrature amplitude modulation (QAM) signal. This is achieved by mixing $x_\mathrm{I}(t)$ and $x_\mathrm{Q}(t)$ with cosine and sine carriers at center frequency f_c, respectively, thereby up-converting the baseband signals to the passband centered at f_c. The resulting passband waveform $x(t)$ can be expressed as $x(t) = x_\mathrm{I}(t)\cos(2\pi f_\mathrm{c}t) - x_\mathrm{Q}(t)\sin(2\pi f_\mathrm{c}t)$. With raised-cosine pulse shaping characterized by α, the occupied RF bandwidth (RFBW) relative to the symbol rate is given by $(1+\alpha)R_\mathrm{s}$. This bandwidth is a critical design parameter for wireless transmitters and PAs. For visualization of this concept, Figure 1.2 shows the spectrum of an example 16-QAM signal at 28 GHz. With raised-cosine filter ($\alpha = 0.35$), the signal occupies only an RFBW of 270 MHz while achieving a data rate of 800 Gb/s. Compared to the case without pulse shaping at the same data rate, the RFBW is much smaller.

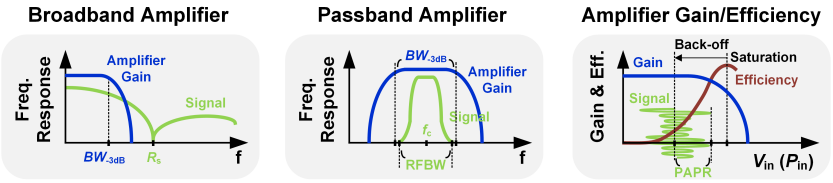


Figure 1.3: Illustration of the requirements for broadband and passband transmitter amplifiers based on signal characteristics.

A key characteristic of a high-order M-QAM signal ($M > 4$) is its non-constant envelope. This is due to the random superposition of multiple pulses, and when these pulses constructively interfere, they generate instantaneous peaks that are much higher than the signal's average power. This behavior is quantified by the PAPR or Crest factor. A high PAPR requires RF PAs to operate with a larger back-off from its saturation point to prevent non-linear distortion. This, however, compromises the PA's efficiency, as a regular PA achieves its maximal efficiency at the saturaton point. Therefore, managing PAPR is a critical design consideration for both the transmitter and the PA in modern wireless communication systems.

Figure 1.3 summarizes the requirements for transmitter amplifiers for both broadband and passband applications. Regarding bandwidth, the 3-dB bandwidths ($BW_{\text{-3dB}}$) of the amplifiers should generally encompass the corresponding signal bandwidths. Furthermore, when the signal amplitude is large enough to drive the amplifiers into the nonlinear region and efficiency becomes a concern, the PAPR of the signal must also be taken into account.

1.3 Goals and Outlines of This Work

This work investigates important design aspects of high-frequency, broadband output-stage amplifiers and demonstrates corresponding silicon implementations for wireless and optical transmitter applications. The discussion focuses on bandwidth, linearity, efficiency, and stability.

Chapter 2 begins with various approaches for assessing amplifier linearity. It then discusses amplifier topologies, including transistor configurations and dif-

ferential architectures, as both strongly influence linearity performance. Subsequently, the linear driving capability is examined, highlighting the fundamental differences in output-stage amplifier requirements across different application scenarios. The chapter concludes with a discussion on stability, with particular emphasis on the underlying theory and new insights into large-signal stability analysis methods.

Chapter 3 reviews the fundamentals of PA design, with an emphasis on transformer-based power combining in silicon technologies and their modeling. It further introduces advanced power-combining techniques relevant to modern integrated PA implementations.

Chapter 4 presents a set of representative transformer-based linear PA implementations in silicon technologies, covering the *K*u-, *K*a-, and V-bands. These implementations explore different performance tradeoffs and architectural choices, including output-power enhancement, power-density optimization, high efficiency, and advanced power-combining strategies. Through these examples, the chapter highlights how transformer-based techniques can be leveraged to address diverse design requirements in modern SiGe and CMOS PAs.

Chapter 5 presents an in-depth investigation of large-signal stability, treating stability as a top design priority in broadband SiGe PA design. The chapter begins with an examination of nonlinear capacitance effects and the identification of instability mechanisms using the stability analysis methods detailed in Section 2.5. A stabilization case study is then presented. Subsequently, a broadband SiGe PA based on a common-collector–common-base (CC–CB) transistor configuration, which exhibits reduced sensitivity to large-signal instability, is proposed and demonstrated.

Finally, Chapter 6 is a concise chapter presenting design considerations for interfacing with optical modulators, along with an illustrative example of a 100-GBd, linear SiGe optical modulator driver for short-reach optical links, a critical component for both wireless backhaul infrastructure and AI-related data transmission systems.

2 Transistor Amplifier Design

This chapter discusses key design aspects of transistor amplifier design, including linearity, transistor topologies, and stability. It is not intended to replace standard textbook treatments of the subject. Instead, it highlights several essential considerations and introduces new insights and selected details that form the foundation for well-engineered output-stage amplifiers.

2.1 Linearity Assessment

Linearity of an amplifier is crucial, as complex signals with amplitude modulation are widely adopted in modern applications. The nonlinearity of amplifiers originates from several factors. First, the input voltage–to–ouput current characteristic of a physical transistor device is inherently nonlinear. Second, distortion occurs in the output voltage swing once it extends into the region below the knee voltage [Cri06]. Third, nonlinear parasitic and intrinsic capacitors of the transistor introduce memory effects and phase distortion [Beh11]. Fourth, additional memory effects arise from thermal dynamics and bias-envelope modulation [FPdC+04]. Since amplifiers in output stages are typically required to deliver large voltage swings or high output power, their linearity characterization is of particular importance. In the following, the key linearity metrics are introduced.

If the nonlinear input–output characteristic of an amplifier is approximated by a third-order polynomial function, $y = \alpha_1 x + \alpha_2 x^2 + \alpha_3 x^3$, the input 1-dB gain compression point (A_{IP1dB}) and the input third-order intercept point (A_{IIP3}) related to third-order intermodulation (IMD_3) can be calculated as [Beh11]:

$$A_{\mathrm{IP1dB}} = \sqrt{0.145\left|\frac{\alpha_1}{\alpha_3}\right|} \quad and \quad A_{\mathrm{IIP3}} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|}, \tag{2.1}$$

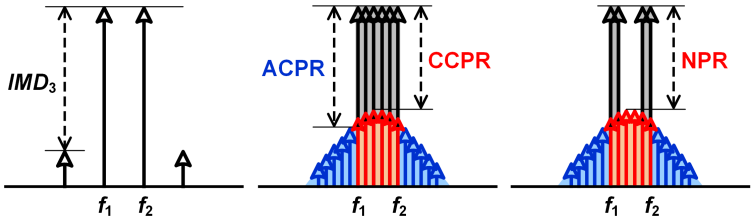


Figure 2.1: Illustrations of the linearity metrics – IMD_3, ACPR, CCPR and NPR.

under one-tone continuous-wave (CW) and two-tone excitations, respectively. Equation (2.1) only considers third-order nonlinear effects. If higher-order effects are pronounced, the calculated values would deviate considerably. Nevertheless, in most devices, the coefficients of higher-order terms (e.g., α_5 for the fifth-order term) are much small than α_3, so (2.1) usually provides a valid preliminary evaluation of amplifier linearity. In some applications, under one-tone excitation, total harmonic distortion (THD) is used to quantify total amount of harmonic distortion associated with gain compression behavior [SSCG20]. Moreover, as elaborated in [FPdC+04], the polynomial coefficients $\alpha_1, \alpha_2, \alpha_3$ depend on the device bias conditions, and therefore vary with the input voltage swing. In some cases, nulling effects occur for IMD_3 [vdHdGdV02, FPdC+04], making a straightforward calculation of A_{IIP3} more challenging. Finally, the coefficients can also be modeled as complex numbers to account for amplitude–to–phase (AM–PM) distortion. The polynomial model can be further extended into a memory polynomial to capture memory effects in amplifier design [DZM+04].

Besides the aforementioned basic metrics, co-channel distortion ratios are also of interest [CS13]. The reason is that IMD_3 only accounts for adjacent-channel distortion, characterized by its corresponding index, the adjacent-channel power ratio (ACPR), whereas the co-channel distortion directly affects the in-band signal quality, as illustrated in Figure 2.1. Several figures of merit can be used to assess the in-band signal quality, such as co-channel power ratio (CCPR), noise power ratio (NPR), signal–to–noise–and–distortion ratio (SNDR), and error-vector magnitude (EVM). Among them, NPR is straightforward and widely adopted in Satcom applications. As can be seen in Figure 2.1, the direct measurement of CCPR is usually challenging, since the co-channel distortion is buried in the in-band signal. By introducing a notch in the middle of the

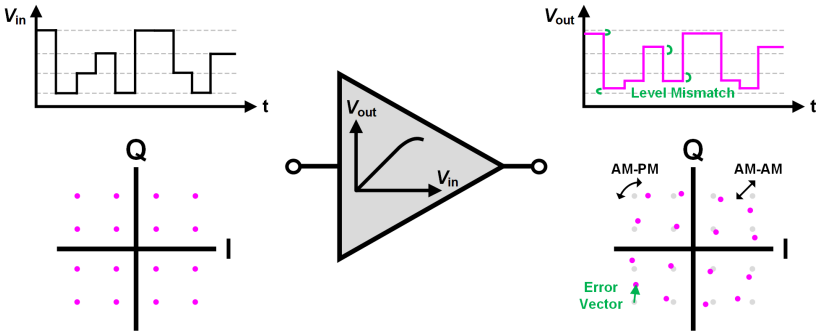


Figure 2.2: Illustrations of the linearity metrics – ratio of level mismatch (RLM) and error-vector magnitude (EVM). The level mismatch and error vector are caused by the nonlinearity of an amplifier.

band during a multi-tone test, the co-channel distortion can be exposed and measured. The relative power of the distortion with respect to the signal power is then defined as NPR.

For modulation schemes such as PAM-M and M-QAM, advanced metrics are used for linearity assessment: the ratio of level mismatch (RLM), derived from the eye diagram for time-domain signals, and the EVM, derived from the constellation diagram. As illustrated in Figure 2.2, level mismatches in a PAM-M signal arise as a consequence of gain compression, i.e., the amplitude–to–amplitude (AM–AM) effect of the device. For PAM-4 signals, the RLM can be defined in two ways depending on the evaluation scenario. In [IEE18b], it is expressed as

$$RLM_1 = 3\frac{min(V_{n+1} - V_n)}{V_3 - V_1}, \quad n, n+1 \in [0, 3], \tag{2.2}$$

where the four levels are denoted as V_0 to V_3, from low to high. Alternatively, [IEE18a] defines RLM in a stricter form as

$$RLM_2 = min[(3ES_1), (3ES_2), (2 - 3ES_1), (2 - 3ES_2)], \tag{2.3}$$

with $ES_1 = \frac{V_1 - V_{mid}}{V_0 - V_{mid}}$, $ES_2 = \frac{V_2 - V_{mid}}{V_3 - V_{mid}}$ and $V_{mid} = \frac{V_0 + V_3}{2}$. For a perfectly linear PAM-4 signal, the RLM equals unity.

For M-QAM signal, exemplified by 16-QAM in Figure 2.2, both AM–AM and AM–PM effects contribute to increased number of error vectors. The EVM is defined with respect to the rms magnitude [VMR17] as

$$EVM_{\mathrm{rms}} = \frac{\sqrt{\frac{1}{N}\sum_{i=1}^{N} |S_{\mathrm{ideal,i}} - S_{\mathrm{measured,i}}|^2}}{\sqrt{\frac{1}{M}\sum_{i=1}^{M} |S_{\mathrm{ideal,i}}|^2}}. \tag{2.4}$$

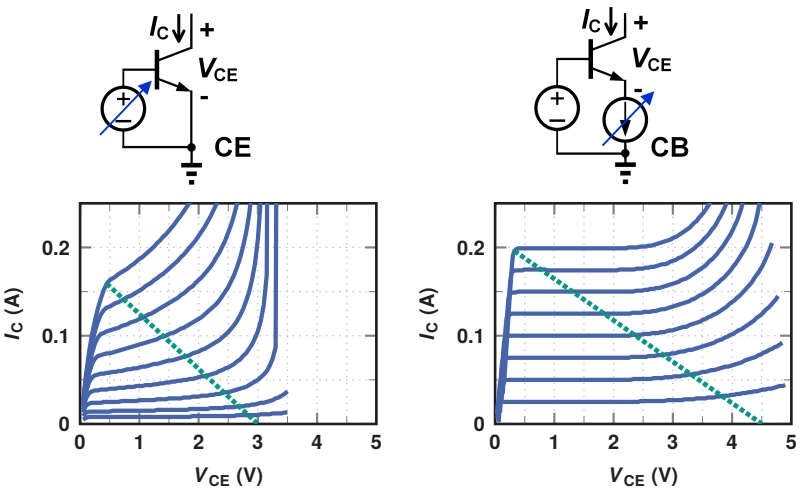
It is worth mentioning that the EVM of a transmitter also depends on other factors such as phase noise of the local oscillator (LO), I/Q mismatch, LO leakage and channel-response flatness [WMT+17]. However, if the focus is solely on evaluating the linearity impact of the output-stage amplifier, the other factors can initially be assumed to be ideally conditioned.

2.2 Transistor Configurations

Various configurations of transistor amplifiers are briefly discussed in this section. The focus is placed more on heterojunction bipolar transistors (HBTs), as they exhibit more complex effects compared to field-effect transistors (FETs). For instance, breakdown effects and the nonlinear behavior of the diffusion capacitance exert particular influences on amplifier design.

2.2.1 CE/CS, CB/CG and Cascode

A common-emitter (CE) or common-source (CS) amplifier is the most widely used configuration due to its high power gain and high input resistance. In low-frequency small-signal analysis, a CE amplifier provides power gain up to $\beta g_{\mathrm{m}} R_{\mathrm{L}}$, where β is the current gain, g_{m} the transconductance, and R_{L} the load resistance. However, at high frequencies, the capacitance between the base and collector introduces a feedback path that reduces the power gain and increases the effective input capacitance through the Miller theorem, thereby limiting the bandwidth. To mitigate this, neutralization techniques for the Miller capacitance can be applied [GHL09]. Such techniques are readily implemented in differential amplifiers, and inductors can also be used when available [Hey17].



(a) CE (b) CB

Figure 2.3: Output I–V curves of (a) CE configuration with the sweep of V_{BE} and (b) CB configuration with the sweep of I_E.

An alternative approach is to place a common-base (CB) or common-gate (CG) stage on top of the CE/CS amplifier, forming a cascode configuration. The CB/CG stage functions as a current buffer, with a current gain close to unity while providing a non-inverting voltage gain of $g_m R_L$. The effective input capacitance of the cascode is much smaller than that of a standalone CE/CS stage, since the input resistance of the CB/CG stage is as low as $\approx 1/g_m$. This significantly improves the bandwidth. In addition, the CB/CG stage typically contributes marginal feedback capacitance, which greatly enhances reverse isolation at high frequencies. For low-frequency small-signal analysis, the power gain of a cascode amplifier is still $\approx \beta g_m R_L$ for a low-frequency small-signal analysis. While this appears no greater than that of a CE/CS amplifier, a standalone CE/CS loses the gain as frequency increases due to the strong capacitive feedback.

2.2.2 Current-Clamping CB

If the load resistance can be freely chosen and the output linear power is of primary concern, a CB amplifier performs better than a CE amplifier. This advantage originates from the distinct breakdown and self-heating behavior at the collector-base junction, which results in an extended breakdown voltage range as observed in the output voltage-to-current characteristic [SSCG20,RZSM19]. Figure 2.3 compares the output I–V characteristics of the CE and CB configurations, based on Leibniz Institute for High Performance Microelectronics (IHP) SiGe SG13G2 technology. As can be seen, the CE configuration exhibits pronounced breakdown and self-heating effects as V_{CE} or I_C increases (Figure 2.3(a)). In contrast, the CB configuration allows V_{CE} to be extended to about 4.5 V, with notably flatter I_C responses (Figure 2.3(b)).

In practice, the CB stage is typically employed in a cascode configuration, where the input current source is provided by a CE stage. For RF PAs, this current source can be replaced by an inductor, introducing a current-clamping effect [RZSM19]. With current clamping, the bias current of the CB device dynamically follows the input power level, thereby mitigating gain compression and AM–AM distortion. Consequently, both the linearity and back-off efficiency of the PA are further improved.

2.2.3 CC/CD and Combinations

A common-collector (CC) or common-drain (CD) amplifier is typically used as a buffer, providing high input resistance for the preceding stage and low output resistance for the following stage. In low-frequency small-signal analysis, the voltage gain of a CC amplifier ≤ 1 while current gain equals $(\beta + 1)$; this implies the power gain also equals $\approx (\beta + 1)$. In addition to these small-signal impedance characteristics, CC/CD amplifiers are often employed as the output stage in audio amplifier chains operating in class-A mode [GHL09], and they can also be found in RF applications reported in the literature [BSTSN15,CWW19].

Considering the amplifier's frequency response, the CC/CD configuration introduces a zero in the output impedance [GHL09], which can be used to cancel the pole generated by the input capacitance of a subsequent CE/CS stage. This effect is analogous to an inductive peaking technique, effectively boosting the

amplifier's bandwidth. Therefore, the CC/CD configuration can also serve effectively as a preceding stage when bandwidth enhancement is required. For example, [TKA+07] demonstrated a broadband amplifier utilizing this topology, where four cascaded CC stages precede a cascode amplifier. In addition, a CC–CB configuration can also be employed for broadband purpose [SSCG20]. A CC–CB RF amplifier also exhibits improved large-signal stability [10], as will be elaborated in Section 5.2.

2.3 Differential Pair and Pseudo-Differential Pair

Differential signaling is preferred in circuit systems because it offers higher immunity to crosstalk and environmental noise. Two amplifier topologies are commonly used to amplify differential signals: the differential pair and the pseudo-differential pair. The choice between them involves a tradeoff among performance characteristics such as power consumption and linearity.

A differential pair incorporates a tail current source at the source or emitter, which minimizes the variation of bias current and the resulting transconductance g_{m} caused by the preceding DC biasing level. However, headroom must be reserved for the tail current source, necessitating a higher supply voltage and thus increasing DC power consumption. In contrast, a pseudo-differential pair saves DC power but suffers from sensitivity to the DC bias level. For wireless applications with a defined passband, the amplifier is typically AC-coupled, where the DC bias level is provided separately and can be well controlled. Under such conditions, with power consumption prioritized, a pseudo-differential pair is usually adopted.

In terms of linearity, the two topologies exhibit distinct behaviors due to their different output–input current–voltage (I/V) characteristics. For MOSFETs, it has been shown that a pseudo-differential pair achieves a higher A_{IIP3} level than a differential pair [Beh11]. For bipolar transistors, the linearity in terms of IIP_3 is derived in Appendix A.1, where an A_{IIP3} level of $\approx 5.7V_{\mathrm{T}}$ is obtained for a bipolar pseudo-differential pair, which exceeds that of a bipolar differential pair ($\approx 4V_{\mathrm{T}}$). This indicates that for linearity considerations, a pseudo-differential pair is generally more favorable for both MOSFET and bipolar implementations.

Another important parameter for differential circuits is the common-mode rejection ratio (CMRR), defined as A_{dm}/A_{cm}, where A_{dm} and A_{cm} denote differential-mode and common-mode gain, respectively. The CMRR of a differential pair is $1 + 2g_m R_{tail}$, which is typically large due to the high R_{tail} of a current source. However, when the real current source exhibits a parasitic capacitance C_{tail}, $|Z_{tail}|$ decreases with frequency, leading to a reduction in CMRR. In a pseudo-differential pair, the situation is more severe: since $R_{tail} = 0$, the CMRR is only 1. Nevertheless, the required CMRR depends on system specifications [AKGR22, HLKR24]. For instance, in band-limited RF/mm-wave differential amplifiers, baluns are typically employed and provide sufficient common-mode rejection. Therefore, when power consumption and linearity are prioritized, a pseudo-differential pair remains the preferred choice [KHL+23].

2.4 Linear Output Driving Capability

Output-stage amplifiers in transmitters are responsible for delivering sufficient voltage swing or power to the subsequenct load components, which present specific impedance values. These impedances must be considered first, as they dictate the required output voltage swing (V_{out}) or P_{out}, i.e., the driving capacity. Given a specific transistor configuration, the amplifier must satisfy these requirements to ensure adequate linearity of V_{out} or P_{out}.

For wireless RF and mm-wave transmitters, the amplifier operates over a defined passband and typically employs matching networks consisting of inductors, capacitors, and distributed elements. Owing to the presence of the output matching network, the load impedance of the output-stage transistors can be more freely selected. In this context, P_{out} can be maximized by simultaneously maximizing both V_{out} and the output current I_{out}. A transistor inherently supports a maximum voltage V_{max} and a maximum current I_{max}, as limited by its breakdown and saturation characteristics, respectively. Considering its output I–V characteristics with a knee voltage V_{knee} [Cri06], the achievable maximum output power is then expressed as

$$P_{max} = \frac{1}{8} (V_{max} - V_{knee}) I_{max}, \tag{2.5}$$

and the corresponding optimum resistance R_{opt} is

$$R_{\text{opt}} = \frac{(V_{\text{max}} - V_{\text{knee}})}{I_{\text{max}}}. \tag{2.6}$$

Figure 2.3 illustrates this concept, where the green load lines define the maximal allowable peak-to-peak voltage swing (i.e., $V_{\text{max}} - V_{\text{knee}}$) and peak-to-peak current swing (i.e., I_{max}). Following this design methodology, the output-stage amplifier is also referred to as a power amplifier, since it aims to maximize P_{out}. If a higher P_{out} is targeted, either V_{max} or I_{max} must be increased. Enhancement of V_{max} can be achieved by choosing semiconductor technologies with higher breakdown voltage, or by adopting different transistor configurations, as shown in Figure 2.3 for SiGe technologies. Enhancement of I_{max} relies on increasing the device size; however, the size cannot be increased indefinitely, as R_{opt} given in (2.6) decreases significantly, making the lossy output matching network less efficient. In this context, power-combining techniques become essential.

By contrast, in applications such as optical transmitter frontends, the output-stage amplifier is designed for broadband driving, where narrowband matching networks are generally not employed and the load resistance is directly defined by the subsequent optical modulator. In such cases, a target output voltage $V_{\text{out,TGT}}$ is first specified according to the modulator type, and the required I_{out} is then determined accordingly. For a fixed load resistance, higher driving capability can be achieved by increasing the transistor size and, consequently, I_{out}; however, this comes at the expense of reduced bandwidth due to increased parasitic capacitance, as well as higher DC power consumption.

2.5 Stability

Parts of the following section were previously published in [1].

Stability is a key aspect of a functional amplifier design. Numerous methods exist for stability verification; in this section, the commonly adopted approaches for RF and mm-wave applications are outlined, and the rationale behind the most effective ones is discussed. The analysis is organized into small-signal and

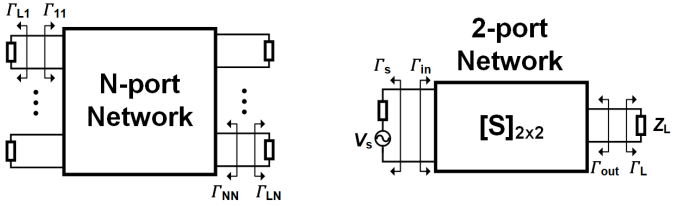


Figure 2.4: An N-port network and the reduced two-port network representations.

large-signal categories to provide a comprehensive understanding of amplifier stability.

2.5.1 Small-Signal Analysis

In general, for RF and mm-wave circuits with N ports, as represented in Figure 2.4, possible instability can be checked by observing all the reflection coefficients seen into the network and into the load sides (Γ_{nn} and Γ_{Ln}) at each port. If $|\Gamma_{\mathrm{nn}}| < 1$ and $|\Gamma_{\mathrm{Ln}}| < 1$ for all $n = 1, 2, ..., N$, the N-port network is unconditionally stable [Gui97]. This port-based approach is simple and intuitive, as it essentially checks whether negative resistance appears at the ports.

For amplifier design, an N-port network reduces to a two-port network. As shown in Figure 2.4, the conditions for unconditional stability can be expressed as $|\Gamma_{\mathrm{s}}| < 1$, $|\Gamma_{\mathrm{L}}| < 1$, $|\Gamma_{\mathrm{in}}| < 1$ and $|\Gamma_{\mathrm{out}}| < 1$. To fulfill these four Γ conditions, graphical analysis can be used, where stability circles for Γ_{s} and Γ_{L} are calculated, which are the boundaries for $|\Gamma_{\mathrm{in}}| = 1$ and $|\Gamma_{\mathrm{out}}| = 1$ [Gui97]. As an alternative, a simple stability factor–K-factor (Kf)–was developed in [Rol62, Kur65] to summarize the conditions for unconditional two-port stability:

$$Kf = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \quad and \quad \Delta = S_{11}S_{22} - S_{12}S_{21}. \tag{2.7}$$

The unconditional stability conditions are then given by $Kf > 1$ and $|\Delta| < 1$. Furthermore, based on this definition of Kf, the maximum gain (G_{max}) of a two-port network can be expressed as $G_{\mathrm{max}} = \frac{|S_{21}|}{|S_{12}|}(Kf - \sqrt{Kf^2 - 1})$, obtained under simultaneous conjugate matching at both ports. For $Kf < 1$, this expression

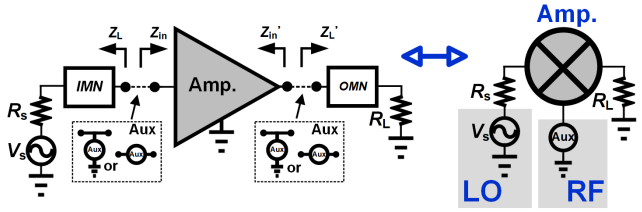
becomes undefined; instead, the boundary condition $Kf = 1$ is used, and $G_{\max}$ reduces to the maximum stable gain (MSG).

Despite its simplicity, the proviso of using Kf, described in [Rol62], must be satisfied: the unloaded two-port network must itself be stable, meaning the unloaded system characteristic function does not contain right-half-plane (RHP) roots [PSH93]. In this context, the normalized determinant function (NDF) was proposed as a more rigorous stability check method [PSH93, SP93]. The papers also presented amplifier examples where $Kf > 1$ but oscillations still occurred—instabilities that NDF was able to detect. Nevertheless, practical NDF simulations may suffer from accuracy limitations when commercial device models include excessive parasitic components, thereby preventing access to the intrinsic device terminals [SR21].

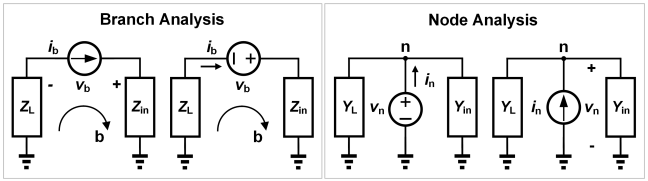
In parallel, small-signal loop gain analysis based on Nyquist criterion is also useful. [TVHK01] proposed a double-injection technique to calculate the true return ratio and the corresponding bilateral loop gain. However, using the Nyquist plot for the loop gain provides only the difference between the number of RHP zeros and poles, without revealing the exact number of RHP zeros. Consequently, any RHP pole-zero cancellations can lead to hidden instabilities [Gui06].

2.5.2 Large-Signal Analysis

In the large-signal operation of an amplifier, parasitic capacitance modulation introduces additional feedback loops, which can lead to the fulfillment of oscillation conditions [Loh66, SJR06, PRC+21, 1]. Since the aforementioned small-signal stability analysis does not include the effects of capacitance modulation, advanced simulation methods are required for reliable stability checks. One of the reliable methods for stability checking involves using auxiliary small-signal voltage or current sources [ACP+02, SJR06, PLSF16]. By inserting these auxiliary sources at sensitive nodes or branches of the circuit, impedance or admittance responses can be obtained, providing insight into the system behavior at these critical locations. In addition, the approach can be applied to the large-signal region of an amplifier design. With a one-tone large-signal excitation, based on the harmonic balance (HB), the amplifier is linearized and treated as a mixer with the auxiliary source [PLSF16]. As shown in Figu-



(a)



(b)

Figure 2.5: (a) Auxiliary sources (Aux) can be applied for mixer-like stability simulations in RF amplifier designs [ACP+02, PLSF16]. Z_L indicates the loading impedance seen into the side of source or load; Z_{in} is the impedance seen into the active device. (b) Branch and node analyses and different configurations using auxiliary voltage or current sources. $Z_L = 1/Y_L$ and $Z_{in} = 1/Y_{in}$ [1]. © IEEE.

re 2.5(a), the two input sources — the large-signal excitation and the auxiliary source — can be considered analogous to a local oscillator (LO) signal and an RF signal in a mixer simulation. The resulting frequency responses from the auxiliary sources are then approximated as rational functions in the s-domain using the vector-fitting technique [GS99], facilitating complete pole-zero identifications [CMA+19, ACA+11]. Alternatively, direct evaluation of oscillation conditions in the frequency domain [Sua15] offers a quicker in-situ method for identifying potential oscillations in the circuit. This approach eliminates the need to export data for offline analysis, streamlining the evaluation process. However, a few aspects require clarification, including the use of auxiliary voltage or current source, the oscillation conditions and the examination of poles or zeros. In this section, we review and clarify these aspects.

Branch/Node Analyses and Oscillation Conditions

As illustrated in Figure 2.5(a), in the simulation of an amplifier, the auxiliary small-signal sources can be inserted either in parallel or in series. The series configuration facilitates branch analysis, while the parallel configuration is used for node analysis, as shown in Figure 2.5(b). Take branch analysis for example, applying an auxiliary current source i_b in a branch yields an impedance response Z_b. Equivalently, using an auxiliary voltage source v_b produces an admittance response Y_b, which is the reciprocal of Z_b. In simulations, since the source $i_b(s)$ is ideally open for all RF signals except at the center frequency, using v_b as the auxiliary source is more convenient[1]. The similar principle applies to node analysis, which gives us the reciprocal responses Y_n and Z_n at the node.

In an analysis, the circuit can be modeled as two components: the loading impedance Z_L and the input impedance Z_{in}. By convention, as shown in Figure 2.5(a), Z_L represents the impedance seen into the source or load, while Z_{in} represents the impedance seen into the side with active components. Consequently, the responses of Z_b and Y_n can be expressed as $Z_b = Z_L + Z_{in}$ and $Y_n = Y_L + Y_{in}$, where Y_L and Y_{in} are reciprocals of Z_L and Z_{in}, respectively. To determine instability from the frequency responses of Z_b and Y_n, one-port oscillation conditions [Gui06] can be applied:

$$\mathfrak{Re}[Z_b(\omega)] \leq 0 \quad \textit{and} \quad \mathfrak{Im}[Z_b(\omega)] = 0, \tag{2.8}$$

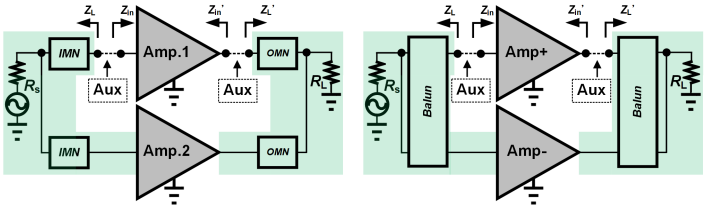
and

$$\mathfrak{Re}[Y_n(\omega)] \leq 0 \quad \textit{and} \quad \mathfrak{Im}[Y_n(\omega)] = 0, \tag{2.9}$$

respectively.

In addition, considering the amplitude dependence of Z_{in} and Y_{in}, Kurokawa conditions are derived to ensure a stable oscillation [Kur69, Gui06], where assumptions are made that Z_L and Y_L remain constant despite amplitude variations (i.e., $\frac{\partial Z_L}{\partial A} = 0$ and $\frac{\partial Y_L}{\partial A} = 0$), implying the exclusive presence of passive components in the source or load. In parallel, Z_{in} and Y_{in} are assumed to be constant over a small frequency range (i.e., $\frac{\partial Z_{in}}{\partial \omega} = 0$ and $\frac{\partial Y_{in}}{\partial \omega} = 0$). However, these assumptions do not hold in complicated circuitry, particularly in multi-way combined amplifiers, where the source or load contains active components.

[1] Otherwise, bandstop or bandpass filters need to be added [Alm09].



(a) (b)

Figure 2.6: In power-combined amplifiers, the loading impedances Z_L and Z_L' also include the impedance from active devices, highlighted in green. This inclusion leads to a deviation in the original derivation of the Kurokawa conditions. Examples include (a) a differential-combined amplifier and (b) a binary-combined amplifier [1]. © IEEE.

Example scenarios are shown in Figure 2.6. To address such cases, we consider both amplitude and frequency dependencies of Z_L, Y_L, Z_{in} and Y_{in} and generalize the Kurokawa conditions. For branch analysis, the condition is derived in the Appendix A.3 as

$$\frac{\left(\frac{\partial R_T}{\partial A}\frac{\partial X_L}{\partial \omega} - \frac{\partial X_T}{\partial A}\frac{\partial R_L}{\partial \omega}\right)|_{\omega_0,A_0}}{\left(\frac{\partial X_T}{\partial \omega}\frac{\partial X_L}{\partial \omega} + \frac{\partial R_T}{\partial \omega}\frac{\partial R_L}{\partial \omega}\right)|_{\omega_0,A_0}} > 0, \tag{2.10}$$

where $R_L = \mathfrak{Re}(Z_L)$, $X_L = \mathfrak{Im}(Z_L)$, $R_T = \mathfrak{Re}(Z_L + Z_{in}) = \mathfrak{Re}(Z_b)$ and $X_T = \mathfrak{Im}(Z_L + Z_{in}) = \mathfrak{Im}(Z_b)$. Likewise, in the node analysis, its counterpart condition of (2.10) is

$$\frac{\left(\frac{\partial G_T}{\partial A}\frac{\partial B_L}{\partial \omega} - \frac{\partial B_T}{\partial A}\frac{\partial G_L}{\partial \omega}\right)|_{\omega_0,A_0}}{\left(\frac{\partial B_T}{\partial \omega}\frac{\partial B_L}{\partial \omega} + \frac{\partial G_T}{\partial \omega}\frac{\partial G_L}{\partial \omega}\right)|_{\omega_0,A_0}} > 0, \tag{2.11}$$

where $G_L = \mathfrak{Re}(Y_L)$, $B_L = \mathfrak{Im}(Y_L)$, $G_T = \mathfrak{Re}(Y_L + Y_{in}) = \mathfrak{Re}(Y_n)$ and $B_T = \mathfrak{Im}(Y_L + Y_{in}) = \mathfrak{Im}(Y_n)$.

Notably, with the conditions $\frac{\partial Z_L}{\partial A} = 0$ and $\frac{\partial Z_{in}}{\partial \omega} = 0$, equation (2.10) reduces to

$$\left(\frac{\partial R_{in}}{\partial A}\frac{\partial X_L}{\partial \omega} - \frac{\partial X_{in}}{\partial A}\frac{\partial R_L}{\partial \omega}\right)|_{\omega_0 A_0} > 0, \tag{2.12}$$

which is consistent with the original expression in [Kur69]. Moreover, under certain conditions, such as $\frac{\partial R_{\mathrm{L}}}{\partial \omega} = 0$ and $\frac{\partial R_{\mathrm{in}}}{\partial A} > 0$ as assumed in [Gui06], (2.12) can be further simplified to

$$\frac{\partial X_{\mathrm{L}}}{\partial \omega}|_{\omega_0, A_0} > 0. \tag{2.13}$$

The counterpart simplifications in node analysis are similar to (2.12) and (2.13), but in forms of admittance. Despite the simplicity of (2.13), it is important to reiterate that its applicability relies on numerous assumptions that do not hold in practical scenarios. Furthermore, while simulations of Z_{b} and Y_{n} provide information of R_{T}, X_{T}, G_{T} and B_{T}, parameters from the loading side such as R_{L}, X_{L}, G_{L} and B_{L} cannot be extracted. As a result, confirming the generalized Kurokawa conditions (2.10) and (2.11) based solely on the simulations of Z_{b} and Y_{n} is challenging. Specifically, simplifying them by observing the existence of positive slope of X_{T} or B_{T} in the frequency domain, as shown in [Sua15], is not feasible. Consequently, it is recommended to rely solely on (2.8) and (2.9) for identifying potential oscillation frequencies in circuit simulations. The validity of this approach will be demonstrated through measurements of an unstable PA example in Section 5.1.4.

Driving Point Impedance/Admittance and Sensitivity

To understand the simulations of Z_{b} and Y_{n} from a systematic perspective, we can relate them to the driving point impedance and admittance (Z_{dp} and Y_{dp}), as originally defined in [H.W45]. In branch analysis, the Z_{b} is equal to Z_{dp}, which can be further expressed by the impedance matrix $[Z]$ of the entire circuit system. Hence, the relationship in s-domain at branch b is expressed as[2]

$$Z_{\mathrm{b}}(s) = Z_{\mathrm{dp}}(s) = \frac{\Delta(s)}{\Delta_{\mathrm{bb}}(s)} \tag{2.14}$$

[2] The impedance matrix $[Z]$ has size of $B \times B$, where B is the number of branches. Branch b belongs to one of them and is under examination.

where $\Delta(s)$ is the determinant of $[Z]$ and $\Delta_{bb}(s)$ is the element in b-th row b-th column of $adj([Z])$, the adjugate of $[Z]$. Similarly, in node analysis at node n, we can express the relationship in terms of admittance as[3]

$$Y_n(s) = Y_{dp}(s) = \frac{\Delta'(s)}{\Delta'_{nn}(s)} \tag{2.15}$$

where $\Delta'(s)$ is the determinant of system admittance matrix $[Y]$ and $\Delta'_{nn}(s)$ is the element in n-th row n-th column of $adj([Y])$.

For stability of the entire system, it is crucial that $\Delta'(s) = 0$ and $\Delta(s) = 0$ do not exhibit RHP roots. Specifically, in branch analysis, according to (2.14), examination of RHP zeros of Z_{dp}(s) is essential; similarly, in node analysis, according to (2.15), careful scrutiny should be applied to RHP zeros of Y_{dp}(s). This is consistent with the oscillation condition (2.8) or (2.9), where the equality holds when Z_{dp} or Y_{dp} becomes zero, aligning with the zero examinations discussed here. It is worth mentioning that while some studies examine RHP poles, their focus lies on the Y_b and Z_n [CMA+19, ACA+11], which corresponds to the reciprocal relationship with Z_{dp} and Y_{dp}, respectively. In contrast, we emphasize here the examination of zeros for Z_{dp} and Y_{dp}. Despite this difference in focus, both approaches are equivalent and serve to address the same underlying system characteristic. Moreover, since the system characteristic is unique, $\Delta(s) = 0$ is equivalent to $\Delta'(s) = 0$. However, $\Delta_{bb}(s)$ differs from $\Delta'_{nn}(s)$ since Z_{dp}(s) and Y_{dp}(s) from equations (2.14) and (2.15) are not identical. Reduced sensitivity arises if either $\Delta_{bb}(s) = 0$ or $\Delta'_{nn}(s) = 0$ yields identical RHP roots as in the corresponding $\Delta(s) = 0$ or $\Delta'(s) = 0$. This pole-zero cancellation renders instability undetectable in simulation, causing a lower sensitivity. Given the distinct properties of $\Delta_{bb}(s)$ and $\Delta'_{nn}(s)$, different sensitivities emerge in stability assessment from Z_{dp} and Y_{dp}. Therefore, both node and branch analyses are essential for a comprehensive evaluation of stability [AAC+08, CMA+19]. In the following stability simulations of the amplifier designs, we will do both analyses and check both (2.8) and (2.9).

[3] The admittance matrix $[Y]$ has size of $N \times N$, where N is the number of nodes. Node n belongs to one of them and is under examination.

3 Power Amplifier Basics and Topologies

This chapter reviews the fundamentals of PA design and introduces key design considerations as well as modern PA topologies and techniques for silicon-based (Si-based) integrated implementations, which serve as the basis for the following chapters.

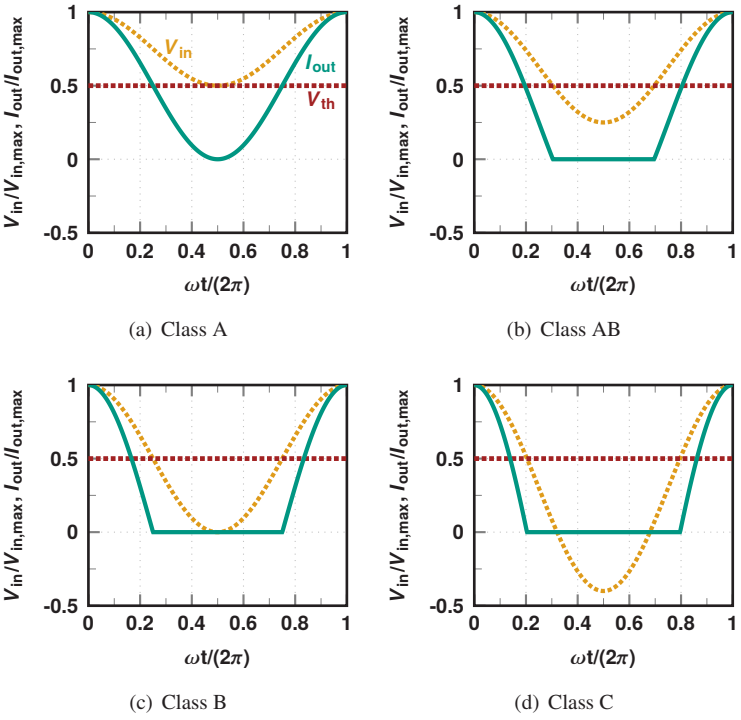
3.1 PA Classes and Efficiency

Linearity and efficiency are two primary performance metrics in PA design. Both are governed by the device bias, which defines the operation classes such as Class A, AB, B, and C [Cri06]. In defining these classes, the device is modeled as a linear transconductance current source. The conduction angle θ represents the portion of one period during which the device conducts output current. The value of θ is determined by by the extent to which the quiescent bias voltage exceeds the device threshold voltage (V_{th}).

Considering an ideal device that exhibits the following relationship between the input voltage V_{in} and output current I_{out}:

$$I_{\text{out}} = \begin{cases} 0, & V_{\text{in}} < 0.5V_{\text{in,max}} \\ 2V_{\text{in}} - 1, & V_{\text{in}} \geq 0.5V_{\text{in,max}}, \end{cases} \tag{3.1}$$

where $V_{\text{in,max}}$ denotes the maximum attainable input voltage, and the threshold voltage V_{th} is assumed to be $0.5V_{\text{in,max}}$. The maximum output current $I_{\text{out,max}}$ occurs when $V_{\text{in}} = V_{\text{in,max}}$. Under the conditions, Figure 3.1 illustrates the waveforms of operations of class A/AB/B/C, where different V_{in} with different quiescent bias voltage levels are applied. The required V_{in} amplitude increases from class A to class C to achieve the same I_{max}, which results from the



(a) Class A (b) Class AB

(c) Class B (d) Class C

Figure 3.1: Input voltage and output current waveforms of an amplifier operating in classes A, AB, B, and C. The time axis is normalized to one signal period.

reduction of the overall transconductance. According to (3.1), the I_{out} curves exhibit distinct conduction behaviors. In class A operation, the bias level lies midway between V_{th} and $V_{in,max}$; hence, the conduction angle θ equals 2π. In class B operation, the bias level is set exactly at V_{th}, making only half the signal period conduct, i.e., $\theta = \pi$.

Subsequenctly, by Fourier series analysis [Cri06], Figure 3.2(a) shows the I_{out} components at different harmonic orders vesus the conduction angle θ. Class A operation offers the most linear behavior, as higher-order harmonics are zero, while the DC current is the largest, indicating the highest power consumption. In Class-B operation, the fundamental current remains the same as in Class-A,

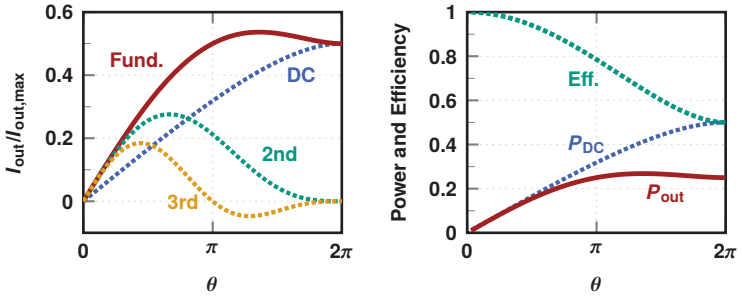


Figure 3.2: Effects of the conduction angle θ: (a) Amplitudes of current components at different harmonic orders. (b) DC power, fundamental power, and efficiency.

but the second harmonic component increases. Between Class-A and Class-B, the Class-AB operation yields the highest fundamental current with a lower DC current compared to Class-A. Class-C operation is typically the least desirable, as it is highly nonlinear and provides a low fundamental current. Assuming that the load impedance provided by the output matching network presents zero impedance for all higher harmonics, the fundamental output power (P_{out}), DC power (P_{DC}), and the resulting efficiency, calculated as

$$Efficiency = \frac{P_{\text{out}}}{P_{\text{DC}}}, \tag{3.2}$$

are illustrated in Figure 3.2(b). From class A to class B operation, the efficiency improves from 50 % to 78.5 %, while maintaining the same P_{out}. Despite the efficiency advantage of class B, the device exhibits lower gain, requiring a higher V_{in}, which often imposes constraints on the overall system link budget. Therefore, class AB operation represents a good compromise, offering the highest P_{out}, moderate gain, and improved efficiency compared to class A. Moreover, in practical RF and mm-wave PA designs, preceding driver stages are typically employed to boost the gain. These driver stages reduce the required V_{in} level but consume additional DC power. For balancing these two factors, power-added-efficiency (PAE) is commonly used to evaluate overall efficiency,

rather than the drain or collector efficiency defined in (3.2). The PAE can be expressed as

$$PAE = \frac{P_{\text{out}} - P_{\text{in}}}{P_{\text{DC,Driver}} + P_{\text{DC,PA}}}, \tag{3.3}$$

where P_{in} is the input power, and $P_{\text{DC,Driver}}$ and $P_{\text{DC,PA}}$ denote the DC power consumption of the driver and output stages, respectively.

Furthermore, based on class AB or class B operation, the output matching network can be engineered to provide specific harmonic terminations, thereby shaping the output voltage waveform to reduce its overlap with the current waveform. This approach enhances efficiency, as the resulting behavior resembles that of a switching-type amplifier. Representative examples of such techniques include the class F and class J amplifiers [Cri06].

3.2 Bandwidth

The bandwidth requirement of an amplifier, discussed in Section 1.2, is dictated by the transmitted signal, and the amplifier gain must span the instantaneous bandwidth of the chosen modulation. However, a broadband gain response does not necessarily imply broadband output power. This is because the overall gain can be distributed across multiple stages, whereas the output power is determined primarily by the final stage of the amplifier chain. Consequently, a broadband PA must not only support a single carrier frequency with wide instantaneous modulation bandwidth, but also maintain sufficient output power across multiple carrier frequencies.

A broadband output power profile is ensured when R_{opt}, as depicted in (2.6), maintains in the desired range across multiple carrier frequencies. However, for RF and mm-wave PAs, the device output capacitance introduces an imaginary component that must be resonated out by the output matching network. The design procedure is typically guided by load-pull simulations [Cri06] to determine the optimum impedance Z_{opt}. For broadband operation, load-pull must be performed at multiple carrier frequencies, and the output matching network must then provide the required Z_{opt} at each frequency. The broadband matching strategy can be simplified by extracting the equivalent output capacitive net-

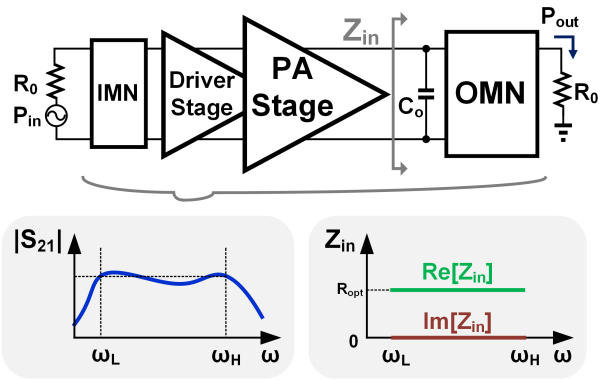


Figure 3.3: A broadband PA must provide not only wideband gain but also wideband output power. This requires the output matching network to deliver a broadband optimum impedance.

work of the device. The matching network that absorbs this output capacitance should provide the impedance relationship [WSH10]:

$$\Re\mathrm{e}[Z_{\mathrm{in}}(\omega)] = R_{\mathrm{opt}} \quad \textit{and} \quad \Im\mathrm{m}[Z_{\mathrm{in}}(\omega)] = 0. \tag{3.4}$$

Figure 3.3 illustrates the design consideration.

Broadband PA design becomes increasingly challenging as larger device sizes are used. A larger device introduces higher output capacitance and additional inductance from interconnects, making the device output network more complex and harder to model with simple equivalents. Consequently, designing an output matching network that resonates out the varying reactive components across all desired frequencies becomes difficult. For Si-based integrated PA implementations, the broadband behavior of the matching network is further influenced by the resistivity of the silicon substrate, particularly when a compact transformer network is used [10].

3.3 Transformer-Based Power Combining

For PA designs, differential operation can also be regarded as a form of power combining, as the effective device size is doubled compared to a single-ended

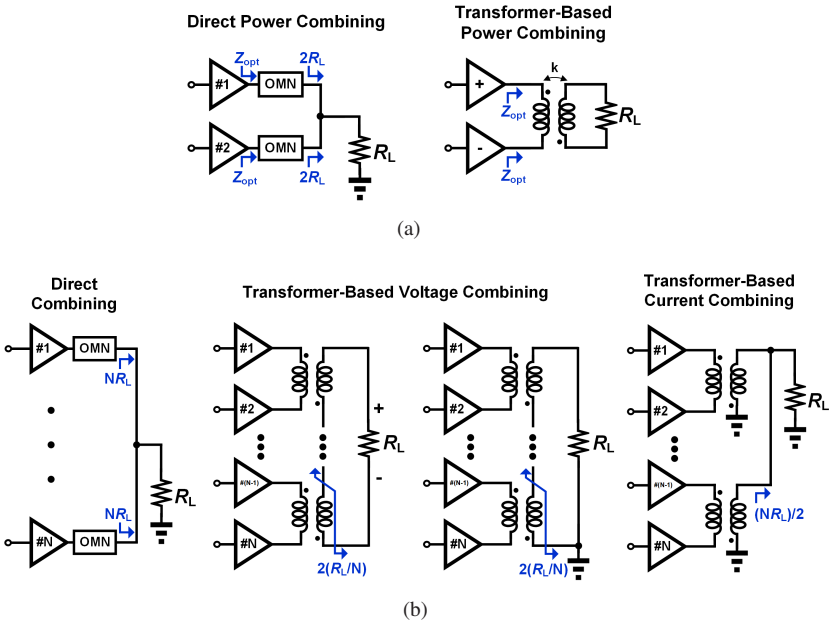


Figure 3.4: (a) Power combining topologies: direct and transformer-based combinings. Transformer-based combining offers the advantage of simultaneously providing impedance matching. Z_{opt} represents the single-ended optimum impedance. (b) N-way power combining topologies and the corresponding load impedance conditions (N: even number).

amplifier. Because transmitters typically employ single-ended antennas, a balun is needed to interface the differential terminals with single-ended ports. In addition, the PA's optimum load impedance generally differs from the system impedance, necessitating an additional matching network. In RF and mm-wave differential PA implementations, transformers (TFs) are particularly attractive—they can simultaneously provide impedance transformation, balun functionality, and power combining, as illustrated in Figure 3.4(a). In Si-based technologies, the availability of multiple metal layers in the back-end-of-line (BEOL) facilitates the integration of compact on-chip transformers, which in turn has driven the development of various transformer-based power combining techniques [SWWH99, AKRH02, CRN09, GXC12].

In general, when targeting higher output power, N-way power combining techniques can be employed, as illustrated in Figure 3.4(b). For output impedance matching, the transformation ratio $m = \frac{R_L}{R_{opt}}$ ($R_{opt} = \mathfrak{Re}[Z_{opt}]$) of the output matching network (OMN) should be kept low, since a higher m leads to higher loss in a basic L-matching network [Ali11]. In N-way direct-combining, the effective m becomes $\frac{NR_L}{R_{opt}}$, whereas for transformer-based voltage and current combining, the effect m values reduce to $\frac{R_L}{NR_{opt}}$ and $\frac{NR_L}{4R_{opt}}$, respectively. The reduction in m highlights the superior matching capability of transformers. Moreover, [AKRH02] demonstrates that the efficiency of transformer matching networks is independent of m, therefore eliminating the design constraints typically imposed by LC-based matching networks. In addition, on-chip transformers provide a unique advantage: they inherently isolate the DC potentials between the two windings, thus removing the need for DC-blocking capacitors [SWWH99].

As shown in Figure 3.4(b), transformer-based voltage combining collects the output power in series with respect to voltage, whereas current combining collects the output power in parallel with respect to current. Owing to its symmetrical physical structure, a voltage combiner is inherently well-suited for PAs with differential outputs. However, when applied to PAs with single-ended outputs, the voltage combiner degenerates into an asymmetrical structure, which suffers from severe common-mode issues and performance degradation caused by phase and amplitude mismatches. These mismatches are caused by parasitics in the physical coupled-inductor transformer as both the number of combined units (N) and the operating frequency increase [GXC12]. A current combiner, on the other hand, is more suitable for single-ended output, since before N-way combining, a transformer can be designed as a balun for a single PA unit. This property naturally enables scalable extension to N-way combining in a more straightforward manner [CHW+16, LR21].

3.3.1 Si-Based On-Chip Transformer Models

In practical designs, an on-chip transformer is realized by a pair of coupled inductors L_1 and L_2, with mutual inductance $M = k\sqrt{L_1 L_2}$, where k denotes the coupling factor. This structure can be modeled as an ideal transformer accompanied by leakage inductances [Ali11, Lon00]. Figure 3.5 illustrates such

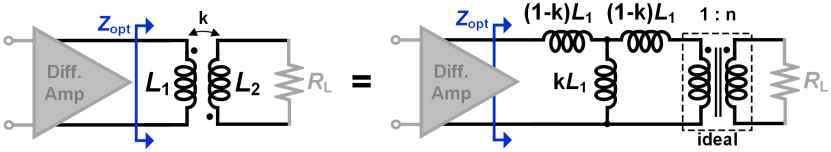


Figure 3.5: A coupled-inductor transformer model, incorporating an ideal transformer and leakage inductances. Z_{opt} represents the differential optimum impedance.

a model with an effective turn ratio of $n = \sqrt{\frac{L_2}{L_1}}$ and leakage inductances kL_1 and $(1-k)L_1$. This representation provides clear insight into how impedance matching between R_{L} and differential Z_{opt} is performed, with the kL_1 branch primarily responsible for absorbing the output capacitance of the devices. Two matching examples using the coupled-inductor model are shown in Figure 3.6 on Smith charts. Since the transformation ratio m is usually > 1 in Si-based PAs—indicating scaling down from the load side to the device side—the n of the transformer is also > 1, meaning L_2 has more turns than L_1. By properly adjusting k, L_1 and L_2, the impedance matching can be achieved. The matching trajectory from the load side (R_{L}) to the device side (Z_{opt}) follows this sequence: an ideal transformer, followed by a series inductance $(1-k)L_1$, then a shunt inductance kL_1, and finally another series inductance $(1-k)L_1$.

Despite the simplicity of the coupled-inductor model (Figure 3.5), a Si-based on-chip transformer is subject to several parasitic effects, including series resistances, inter-winding capacitances, and capacitances from the metal layers to the lossy silicon substrate [Lon00]. To account for these effects, [Lon00] proposed a compact model by adding the parasitics directly to the coupled-inductor representation. However, this approach fails to capture common-mode behavior, rendering it unsuitable for complete circuit analysis, where the common-mode information is important as well [ZZ19]. To overcome this limitation, [ZZ19] introduced two-section distributed models that better represent both differential- and common-mode characteristics. These two-section models can be realized either with lumped elements or coupled lines: the latter offers better modeling for broadband modeling [WW21a], while the former provides clearer insight into how individual parasitic components influence transformer performance.

For further investigation, a transformer is simulated using electromagnetic (EM) tools and subsequently modeled using the two-section lumped approach, as

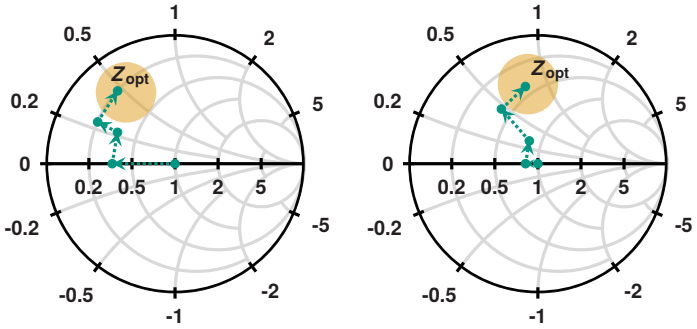
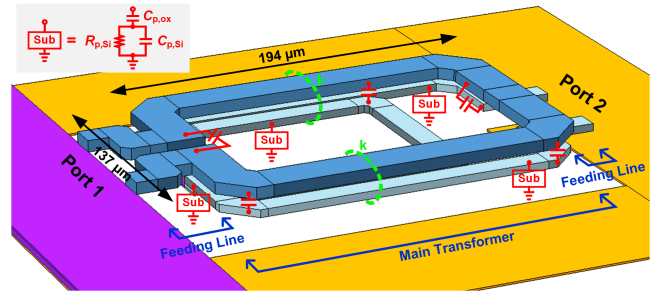


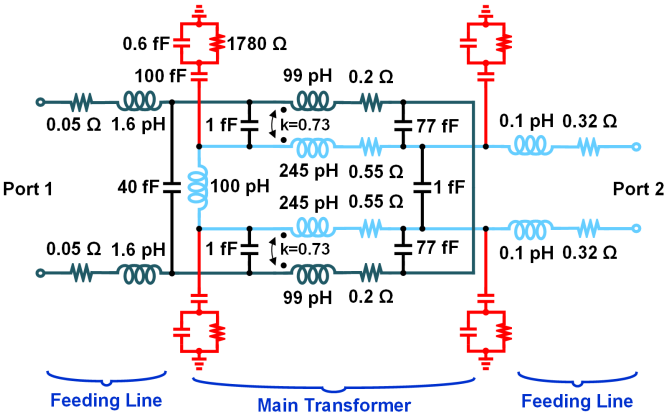
Figure 3.6: Transformer matching trajectories under conditions: (a) $N = 1.7$, $k = 0.8$, $L_1 = 300\,\text{pH}$ and (b) $N = 1.1$, $k = 0.8$, $L_1 = 400\,\text{pH}$, both at 30 GHz. Orange circles indicate the common Z_{opt} regions on Smith chart for Si-based PAs.

shown in Figure 3.7(a) and (b), respectively. The implementation is based on IHP SiGe SG13 technology, which offers one poly layer, seven aluminum metal layers (M1-M5, TopM1 and TopM2) and metal-insulator-metal (MIM) capacitor layers. The transformer consists of the main body and two feeding lines for port 1 and port 2, where the main transformer is represented by two coupled inductors with parameters defined in Figure 3.5. The two-section separation allows the parasitic capacitances between the windings to be modeled more accurately. All parasitic parameters in the two-section model are extracted by fitting the EM-simulated S-parameters in both differential and common modes. With both ports terminated by 50 Ω, the EM simulated and fitted curves from $0.1 - 35$ GHz are shown in Figure 3.8.

During model fitting, the inductance and coupling factor k of the main transformer dominate the overall curve shapes, and their initial values are extracted from Z-parameters using the simple coupled-inductor model (Figure 3.5). Several refinement iterations are then carried out to account for resistances and capacitances. The parasitic networks to silicon substrate, represented by $C_{\text{p,ox}}$, $C_{\text{p,Si}}$ and $R_{\text{p,Si}}$ in Figure 3.7(b), play a crucial role in shaping the S-parameter curves at higher frequencies and, more importantly, dominate the common-mode responses. As shown in Figure 3.8, the model achieves decent accuracy for the differential-mode response, but not for the common-mode response. This



(a)



(b)

Figure 3.7: (a) An example transformer EM view with illustration of the magnetic as well as parasitic effects and (b) the corresponding two-section lumped model with extracted component values.

limitation arises because only four substrate parasitic networks are included in the model, all associated with the winding connected to port 2, which is physically exposed to the substrate (see Figure 3.7(a)). The common-mode accuracy could be improved by incorporating additional substrate parasitic networks. In addition, the substrate parasitic networks influence the self-resonance frequency (SRF) of the extracted L_1 and L_2 values from the EM simulation when the transformer is simplified as a pair of coupled inductor, as shown in Figure 3.5.

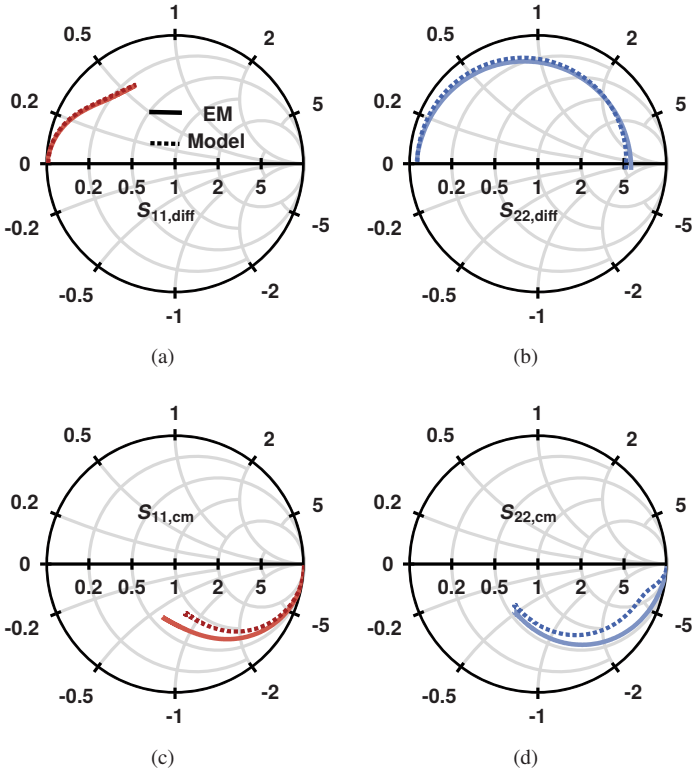


Figure 3.8: Comparison between EM simulation results (solid lines) and the fitted two-section transformer model (dotted lines) across 0.1 – 35 GHz: differential-mode responses of (a) S_{11} and (b) S_{22}, and common-mode response of (c) S_{11} and (d) S_{22}. Port-1 and -2 are both terminated with 50 Ω.

By properly modeling the $C_{p,ox}$, $C_{p,Si}$ and $R_{p,Si}$ values, the SRF of the EM and two-section models can be made consistent.

In parallel, as mentioned in Section 2.3, the CMRR of balun networks is critical for RF differential amplifiers. Therefore, the CMRR values are also simulated for the aforementioned models. The common way of calculating a balun's CMRR is normally through S-parameters, as presented in [BE95]. However,

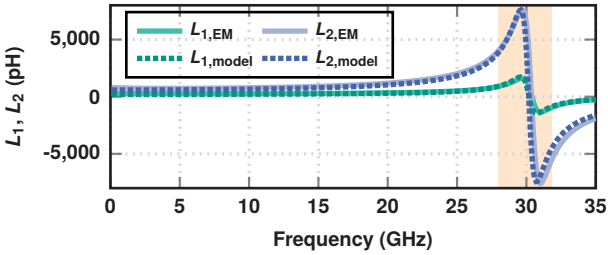


Figure 3.9: Extracted self-inductance of the transformer from EM simulation and the two-section model. The self-resonance frequency (SRF) is accurately modeled by adjusting the parameters of the substrate parasitic networks. The area of SRF is highlighted in orange.

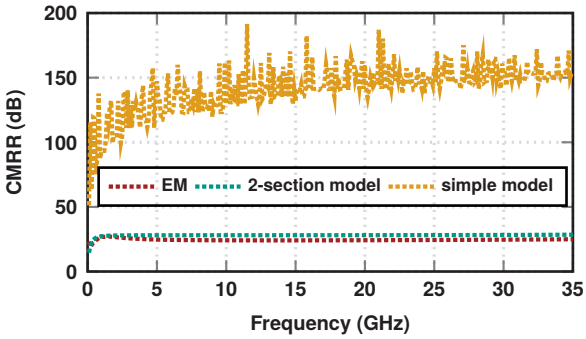


Figure 3.10: CMRR simulations of the transformer with EM model, simple coupled-inductor model and the two-section lumped model.

this calculation is susceptible to the load impedance. In Appendix A.2, a new way of expressing a balun's intrinsic CMRR is proposed and derived using Z-parameters or Y-parameters. The results are independent of load impedance and provide a more precise definition of the intrinsic CMRR of any balun network. Figure 3.10 demonstrates the CMRR simulations for the same transformer (Figure 3.7(a)). Using the simple coupled-inductor model (Figure 3.5) yields a large CMRR of more than 100 dB above 1.4 GHz, which significantly deviates from the EM model due to the missing capacitive components. In contrast, using the two-section lumped model (Figure 3.7(a)) produces results that are

relatively closer to the EM model, showing that the transformer achieves a CMRR of more than 24 dB across 0.4 – 35 GHz.

3.4 Advanced Power Combining

This section presents advanced power-combining techniques, including the balanced amplifier, the Doherty amplifier, and their variants.

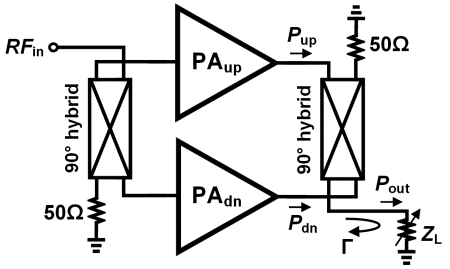
3.4.1 Balanced Amplifiers

Balanced amplifiers, employing two 90° hybrid couplers at the input and output, offer broadband S-parameter performance in both gain and return loss [Gui97]. This topology has been further explored for PA applications, where it combines power from two identical PA elements and, importantly, exhibits insensitivity to variations in load/antenna impedance [BCS06]. Such a property is particularly valuable in modern large-scale phased-array systems, where resilience to variations in antenna impedance is a critical design requirement [MHHW20, PdVA21].

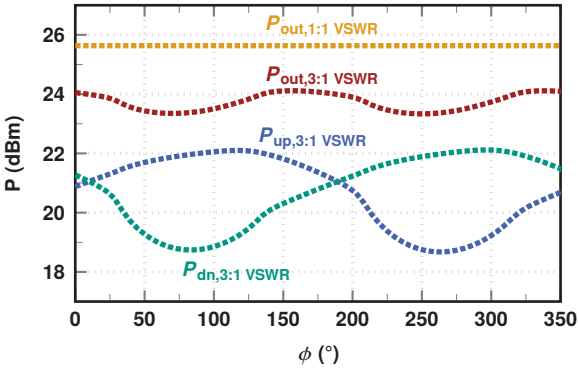
Figure 3.11(a) shows the schematic of a balanced amplifier, while Figure 3.11(b) presents simulated power profiles using real IHP SG13S HBT devices and ideal, lossless couplers under 50 Ω. At a voltage standing wave ratio (VSWR) of 3:1—corresponding to a reflection coefficient magnitude $|\Gamma| = 0.5$—the compensation of the two PA elements (PA_{up} and PA_{dn}) reduces output power variation over the phase (ϕ) range of Γ ($\Gamma = |\Gamma|e^{j\phi}$). As shown, P_{out} varies by less than 0.8 dB, whereas P_{up} and P_{dn} show variations of up to 3.4 dB. Nevertheless, compared with the matched condition (VSWR=1:1), P_{out} still drops approximately 1.25 dB due to mismatch loss between the coupler and the load, which cannot be readily compensated.

For reference, the relationships between VSWR and load impedance Z_L in a 50-Ω system are:

$$|\Gamma| = \frac{VSWR - 1}{VSWR + 1} \quad and \quad Z_L = 50\left[\frac{1+\Gamma}{1-\Gamma}\right]. \tag{3.5}$$



(a)



(b)

Figure 3.11: (a) A balanced amplifier and its (b) P_{out} insensitivity to load variations.

3.4.2 Doherty Amplifiers

A Doherty amplifier combines two power amplifier elements—a main and a peaking amplifier—such that the load resistance of the main amplifier is modulated by the peaking amplifier and an impedance inverter. In this load-modulation process, the voltage swing of the main amplifier is boosted in the power backoff region, thereby enhancing both output power and efficiency. Such efficiency enhancement is particularly important for modern communication signals, which typically exhibit a high peak-to-average power ratio (PAPR) of 6 – 10 dB.

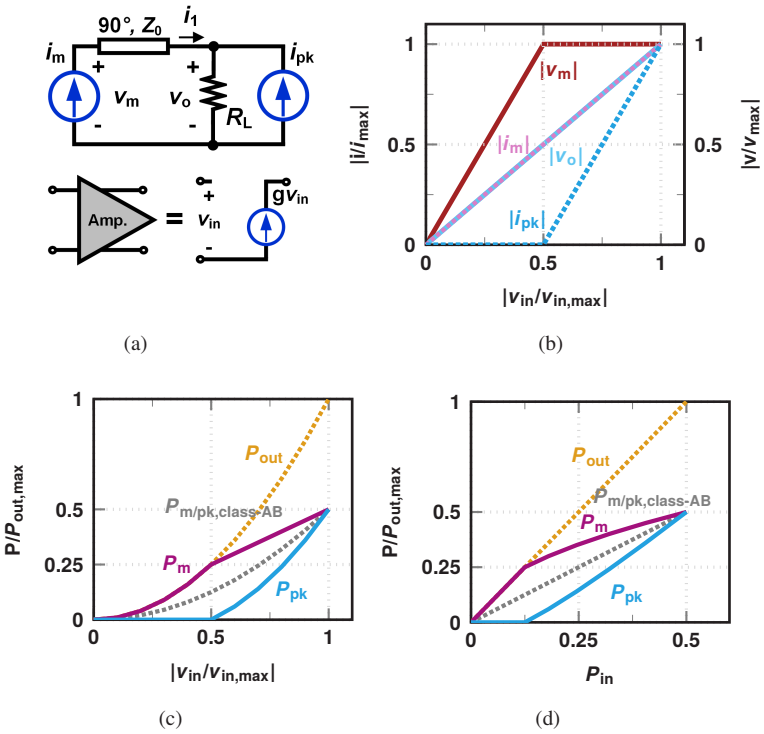


Figure 3.12: (a) A simplified model of a classic Doherty amplifier and its (b) normalized current and voltage profiles. (c) The corresponding output power profiles of the main and peaking amplifiers. (d) A linear P_{out} profile with respect to input power.

Figure 3.12(a) shows a typical model of a current-combined Doherty amplifier [Cri06], where the current sources i_{m} and i_{pk} represent the main and peaking amplifiers, respectively, and R_{L} denotes the load resistance. The quarter-wavelength transmission line with a characteristic impedance of Z_0 serves as an impedance inverter, relating the voltages and currents at both sides as

$$\begin{bmatrix} v_{\text{m}} \\ i_{\text{m}} \end{bmatrix} = \begin{bmatrix} 0 & jZ_0 \\ j/Z_0 & 0 \end{bmatrix} \begin{bmatrix} v_{\text{o}} \\ i_1 \end{bmatrix}, \tag{3.6}$$

which expands to

$$v_{\mathrm{m}} = \jmath Z_0 i_1 \quad \textit{and} \quad v_{\mathrm{o}} = -\jmath Z_0 i_{\mathrm{m}}. \tag{3.7}$$

Replacing the i_1 with $(\frac{V_0}{R_{\mathrm{L}}} - i_{\mathrm{pk}})$ gives $v_{\mathrm{m}} = Z_0 \left[\frac{Z_0}{R_{\mathrm{L}}} i_{\mathrm{m}} - \jmath\, i_{\mathrm{pk}}\right]$. If the peaking amplifier current i_{pk} is delayed by 90°, meaning $i_{\mathrm{pk}} = -\jmath\, i_{\mathrm{p}}$, the main amplifier voltage v_{m} gets modulated in a subtractive manner by i_{p} as

$$v_{\mathrm{m}} = Z_0 \left[\frac{Z_0}{R_{\mathrm{L}}} i_{\mathrm{m}} - i_{\mathrm{p}}\right]. \tag{3.8}$$

To ensure this modulation, the peaking amplifier must therefore be delayed by 90° at the input. Further, if the i_{m} and i_{pk} satisfy the following relations with respect to the scalar input drive voltage level v_{in}:

$$|i_{\mathrm{m}}| = g\, v_{\mathrm{in}} \quad \textit{and} \quad |i_{\mathrm{pk}}| = i_{\mathrm{p}} = \begin{cases} 0, & v_{\mathrm{in}} < \frac{v_{\mathrm{in,max}}}{2} \\ 2g(v_{\mathrm{in}} - \frac{1}{2} v_{\mathrm{in,max}}), & v_{\mathrm{in}} > \frac{v_{\mathrm{in,max}}}{2}, \end{cases} \tag{3.9}$$

where $v_{\mathrm{in}} \in [0,\, v_{\mathrm{in,max}}]$, $|i_{\mathrm{m}}|, |i_{\mathrm{p}}| \in [0,\, i_{\mathrm{max}}]$ and the transconductance $g = i_{\mathrm{max}}/v_{\mathrm{in,max}}$, then substituting (3.9) into (3.7) and (3.8) yields the voltage responses:

$$|v_{\mathrm{o}}| = g Z_0 v_{\mathrm{in}} \quad \textit{and}$$
$$|v_{\mathrm{m}}| = \begin{cases} g \frac{Z_0^2}{R_{\mathrm{L}}} v_{\mathrm{in}}, & v_{\mathrm{in}} < \frac{v_{\mathrm{in,max}}}{2} \\ g \left(\frac{Z_0^2}{R_{\mathrm{L}}} - 2Z_0\right) v_{\mathrm{in}} + Z_0 i_{\mathrm{max}}, & v_{\mathrm{in}} > \frac{v_{\mathrm{in,max}}}{2}. \end{cases} \tag{3.10}$$

Since the main and peaking amplifier are typically designed with identical device sizes, they deliver the same i_{max} at the saturated $v_{\mathrm{in,max}}$ level. Therefore, the optimum loading resistances are both equal to R_{opt}, resulting in $Z_0 = R_{\mathrm{opt}}$ and $R_{\mathrm{L}} = \frac{1}{2} R_{\mathrm{opt}}$. Consequently, the voltage responses become

$$|v_{\mathrm{o}}| = g Z_{\mathrm{opt}} v_{\mathrm{in}} \quad \textit{and} \quad |v_{\mathrm{m}}| = \begin{cases} 2g R_{\mathrm{opt}} v_{\mathrm{in}}, & v_{\mathrm{in}} < \frac{v_{\mathrm{in,max}}}{2} \\ R_{\mathrm{opt}} i_{\mathrm{max}}, & v_{\mathrm{in}} > \frac{v_{\mathrm{in,max}}}{2}, \end{cases} \tag{3.11}$$

where it can be seen that $|v_{\mathrm{m}}|$ increases with a slope twice that of $|v_{\mathrm{o}}|$ when $v_{\mathrm{in}} < \frac{v_{\mathrm{in,max}}}{2}$, and it saturates earlier, reaching $R_{\mathrm{opt}} i_{\mathrm{max}}$ once $v_{\mathrm{in}} > \frac{v_{\mathrm{in,max}}}{2}$.

The mathematical relationships described above are illustrated in Figure 3.12(b). For brevity, the quantities $|v_{\text{in}}|$, $|i_{\text{pk}}|$, $|i_{\text{m}}|$, $|v_{\text{o}}|$ and $|v_{\text{m}}|$ are normalized, and R_{opt} is set to unity. From the voltage and current characteristics, the output powers of the main and peaking amplifiers (P_{m} and P_{pk}) are calculated by

$$P_{\text{m}} = \frac{1}{2}|v_{\text{m}}||i_{\text{m}}| \quad \textit{and} \quad P_{\text{pk}} = \frac{1}{2}|v_{\text{o}}||i_{\text{pk}}|, \tag{3.12}$$

and the total output power P_{out} delivered to the R_{L} after power combining is simply the sum: $P_{\text{m}} + P_{\text{pk}}$. The corresponding power characteristics are shown in Figure 3.12(c). For comparison, the two amplifiers are biased identically in class-AB, resulting in an $|i_{\text{pk}}|$ profile that matches the $|i_{\text{m}}|$ curve in Figure 3.12(b). In this case, $|v_{\text{m}}|$ also follows the $|v_{\text{o}}|$ curve, indicating that no early saturation occurs at the main amplifier. Then, both amplifiers deliver the same output power, denoted as $P_{\text{m/pk,class-AB}}$, as shown in Figure 3.12(c). The total output power remains:

$$P_{\text{out}} = P_{\text{m}} + P_{\text{pk}} = 2P_{\text{m/pk,class-AB}}. \tag{3.13}$$

As can been seen, at a normalized input $|v_{\text{in}}| = 0.5$, the main amplifier operating with the Doherty mechanism delivers more power ($|P_{\text{m}}|$) than the class-AB baseline $P_{\text{m/pk,class-AB}}$, while $|P_{\text{pk}}|$ remains zero since the peaking amplifier just begins turning on. According to (3.13), the Doherty load modulation does not increase the total output power, but since only one amplifier is active, the overall DC power consumption is lower—resulting in improved efficiency at this backoff point. Furthermore, as illustrated in Figure 3.12(d), when the x-axis is re-scaled to input power, the resulting P_{out}–P_{in} curve is linear. This indicates that a Doherty amplifier can simultaneously achieve high linearity and high efficiency. However, in practical implementations, the device transconductance g used in (3.9) is usually not constant, and AM-PM distortion introduces phase errors that impair the intended quadrature relationship between the main and peaking amplifiers. As a result, a design tradeoff between linearity and efficiency remains unavoidable.

Doherty and Doherty-Like Load-Modulated PAs Based on 90° Hybrid Couplers

The load-modulation effect can also be achieved using a 90° hybrid coupler. As illustrated in Figure 3.13(a), leaving one coupled port (referenced to the amplifier terminals, the port 3) either open-circuited or short-circuited enables the realization of current-combined or voltage-combined Doherty amplifiers, respectively [LC20, MHHW20]. The use of a 90° coupler can facilitate reconfigurability for load adaptation or for switching between (quasi-)balanced and Doherty modes of operation.

For example, in the amplifier with an open-circuited coupler, the voltages of the main and peaking amplifiers is expressed as

$$v_{\mathrm{m}} = Z_0 \left[2\frac{Z_0}{R_{\mathrm{L}}} i_{\mathrm{m}} - \jmath\, i_{\mathrm{pk}} \right] \quad \textit{and} \quad v_{\mathrm{pk}} = -\jmath\, Z_0 i_{\mathrm{m}} = \frac{1}{\sqrt{2}} v_{\mathrm{o}}, \tag{3.14}$$

as detailed in Appendix A.4. If i_{pk} is delayed by 90°, meaning $i_{\mathrm{pk}} = -\jmath\, i_{\mathrm{p}}$, then v_{m} can also be modulated subtractively by i_{p} as $v_{\mathrm{m}} = Z_0 \left[2\frac{Z_0}{R_{\mathrm{L}}} i_{\mathrm{m}} - i_{\mathrm{p}} \right]$, resembling (3.8). This enables the realization of a Doherty amplifier.

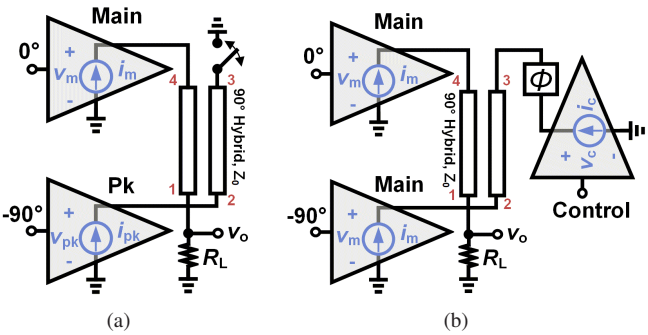


Figure 3.13: (a) An implementation of Doherty PA by using a 90° hybrid coupler. (b) A load-modulated balanced PA (LMBA), which can also functions as a Doherty-like PA.

In addition, the driving point impedance values seen by the main and peaking amplifier, Z_{m} and Z_{pk}, are of particular interest. Considering the typical case shown in Figure 3.12(b), the impedances can be expressed as

$$Z_{\mathrm{m}} = \begin{cases} 2R_{\mathrm{opt}}, & v_{\mathrm{in}} < \frac{v_{\mathrm{in,max}}}{2} \\ R_{\mathrm{opt}}, & v_{\mathrm{in}} = v_{\mathrm{in,max}} \end{cases} \quad \textit{and} \quad Z_{\mathrm{pk}} = \begin{cases} \infty, & v_{\mathrm{in}} < \frac{v_{\mathrm{in,max}}}{2} \\ R_{\mathrm{opt}}, & v_{\mathrm{in}} = v_{\mathrm{in,max}}, \end{cases} \tag{3.15}$$

where the load modulation effect is clearly evident. As derived in Appendix A.4, using the open-circuited coupler for current combining yields a similar load modulation effect:

$$Z_{\mathrm{m}} = \begin{cases} 2Z_0, & v_{\mathrm{in}} < \frac{v_{\mathrm{in,max}}}{2} \\ Z_0, & v_{\mathrm{in}} = v_{\mathrm{in,max}} \end{cases} \quad \textit{and} \quad Z_{\mathrm{pk}} = \begin{cases} \infty, & v_{\mathrm{in}} < \frac{v_{\mathrm{in,max}}}{2} \\ Z_0, & v_{\mathrm{in}} = v_{\mathrm{in,max}}, \end{cases} \tag{3.16}$$

assuming $R_{\mathrm{L}} = Z_0$.

In parallel, the load-modulated balanced PA (LMBA) was proposed [SPC16], in which an additional control signal is applied to port 3 (Figure 3.13(a)). As shown in Figure 3.13(b), depending on the control signal current $\jmath\, i_{\mathrm{c}} e^{j\phi}$, the driving point impedances at port 2 and port 4 are

$$Z_2 = Z_4 = Z_0 \left[1 + \sqrt{2} \frac{i_{\mathrm{c}} e^{j\phi}}{i_{\mathrm{b}}} \right], \tag{3.17}$$

where the current sources at port 2 and port 4 are $i_2 = i_{\mathrm{b}}$ and $i_4 = \jmath\, i_{\mathrm{b}}$, respectively. The phase term $e^{j\phi}$ is introduced by an additional phase shifter implemented at port 3. The LMBA architecture offers reconfigurability, allowing fine-tuning the optimum load impedance of the PA devices to improve efficiency. Moreover, a Doherty-like variant of the LMBA has been proposed to further enhance backoff efficiency [PHFB18, QR21]. In this approach, the DC bias of the amplifier at the control port (port 3 in Figure 3.13(b)) is reduced so that the load modulation described in (3.17) is triggered only within a specific backoff region. With proper phase adjustment via $e^{j\phi}$, both Z_2 and Z_4 decrease as i_{c} increases, and the efficiency is improved in the backoff region.

4 SiGe and CMOS Transformer-Based Power Amplifiers

As detailed in Section 3.3, the adoption of transformers in silicon PA designs has become mainstream. This chapter presents multiple transformer-based linear PA examples implemented in both SiGe and CMOS technologies, spanning the *K*u-, *K*a-, and V-bands. Each PA targets a specific design goal: two employ current power combining to enhance P_{out}, one focuses on achieving high power density, and two others demonstrate advanced power-combining architectures—balanced and Doherty amplifiers. Together, these examples illustrate the design flexibility and performance advantages enabled by transformer-based approaches in silicon technologies.

4.1 Two-Way Current-Combined Linear PAs

Parts of the following section were previously published in [1] and [9].

In this section, two linear two-way current-combined PAs are presented. They target the *K*u-/*K*a-band and V-band, and are implemented in SiGe and CMOS SOI technologies, respectively. The designs are suitable for low-voltage applications.

4.1.1 Design of a *K*u-/*K*a-Band SiGe PA in IHP SG13S

This subsection presents a *K*u-/*K*a-band transformer-based two-way current-combined PA, implemented in IHP SiGe SG13S technology, aiming for 17.3 –

21.2 GHz Satcom applications. The following discusses detailed design considerations and presents comprehensive simulation and experimental results of the fabricated PA.

Design of Common-Emitter PA Cores and Transformer-Based Matching Networks

Cascode configuration is widely adopted in *K*u-/*K*a-band SiGe power amplifiers [JLC22, 6]. However, in this technology and the target frequency, large parasitic collector-emitter capacitance of the common-base device can cause negative resistance within a certain frequency range at the output port. Due to the negative resistance, S_{22} values become greater than unity or sensitive to an antenna load variation. This concern has been reported in the deep-scaled CMOS technology [TNH13] and can be solved by neutralization for common-base (gate) device at the cost of degradation of power-added-efficiency (PAE). To avoid this, capacitive-neutralized common-emitter configuration is used.

As shown in Figure 4.1(a), for a sufficient output power (P_{out}), the single-ended common-emitter amplifier is composed of 6 unit cells, each containing 8 multipliers, i.e., $Q_{1,\,2}$ consists of 48 multipliers. For reducing interconnection loss, particularly from the collector side, the devices are arranged interdigitally, meaning the unit cells are placed long-side-to-long-side, which is more area-efficient than a short-side-to-short-side arrangement. The core adopts a pseudo-differential pair, as illustrated in Figure 4.1(b). The capacitive neutralization technique is applied for uncontional small-signal stability. With V_{bias} of 0.88 V, the simulated maximum gain (G_{max}) is shown in Figure 4.1(c). Accordingly, the neutralization capacitance (C_{n}) of 100 fF is selected to maintain the K-factor greater than unity and a high G_{max}, which is equal to maximum available gain (MAG). Subsequencly, two identical PA cores are current-combined with transformers for the target P_{out} and the entire PA is shown in Figure 4.1(d).

To enhance large-signal stability, an empirical compact RC network is proposed for MMIC design [TPB99], functioning as a high-pass filter for eliminating the low-frequency subharmonic spurs. In [TPB99], the RC network design appears to be based purely on rule of thumb, with no clear design method provided. However, the selection of the RC values is not trivial. Excessive resistance leads to unnecessary considerable degradation of gain. Meanwhile, the sizing of the

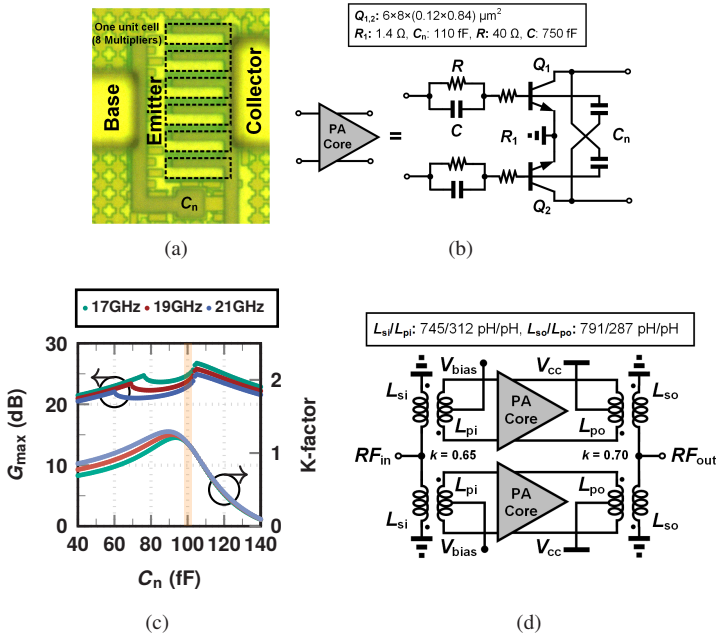
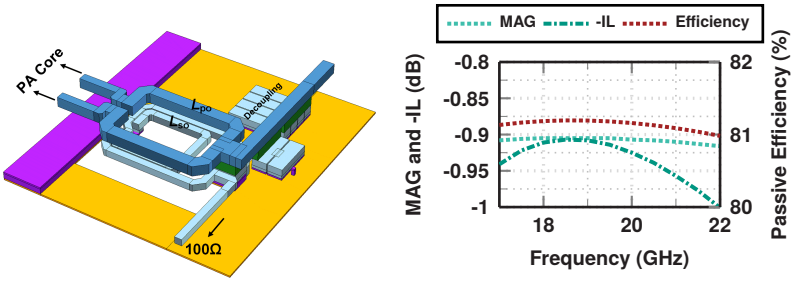


Figure 4.1: (a) Top view of the single-ended common-emitter devices (6×8 multipliers). (b) Core of the PA, and its (c) G_{max}/Kf simmulations. (d) The entire two-way transformer-combined circuit. This PA is also named PA_wRC, for further discussion in Section 5.1.3 and 5.1.4 [1]. © IEEE. The supply voltage V_{cc} is 1.5 V.

capacitor impacts the filtering of lower frequencies and thus the effectiveness of oscillation suppression. With the aid of node and branch analyses (see Section 2.5.2), the guidelines for sizing the RC network have become clearer, though the process remains largely trial-and-error. The selection of the RC values, as well as a comparison with another PA version without the RC network, will be detailed in Section 5.1, where more advanced discussions on large-signal stability, its cause and stabilization will be provided.

Load-pull simulation is conducted for the pseudo-differential pair, as shown in Figure 4.1(b). With V_{bias} of 0.87 − 0.88 V, the unit PA core demonstrates an optimum PAE and an optimum P_{out} of 55.8 % and 21.3 dBm at 18.8 GHz, respectively. An optimum impedance 17.5 + j16.6 is chosen, where PAE of



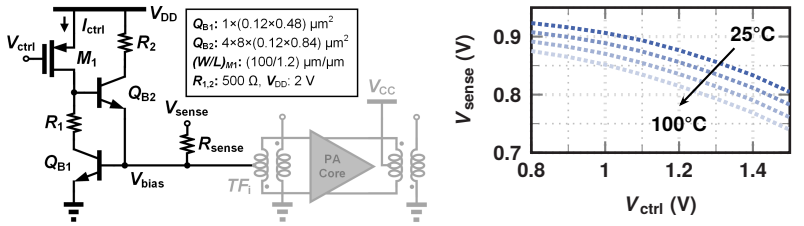
(a) (b)

Figure 4.2: (a) Layout/EM view of the stacked transformer-based output matching network (OMN). (b) Simulation of MAG, passive efficiency and insertion loss (IL) of the OMN [1]. © IEEE.

53.7 % and P_{out} of 20.9 dBm are presented. Accordingly, an output transformer (TF_o) network is designed to match this impedance to 100 Ω, as modeled and analyzed in Section 3.3.1 and Figure 3.7. Demonstrated in Figure 4.2(a), the TF_o possesses primary-turn inductance L_{po} of 287 pH, secondary-turn inductance L_{so} of 791 pH and a coupling factor (k) of 0.7. The resulting effective turn ratio is roughly 1.7. Figure 4.2(b) shows the simulated MAG and efficiency of the TF_o network are roughly −0.9 dB and >81 % over the target band 17.3 – 21.2 GHz. Considering the targeted load-pull impedance of $17.5 + \jmath 16.6$, the insertion loss (IL) is also shown. The load-pull impedance remains approximately unchanged for all frequencies in the target narrow band. Therefore, the variation of IL is within 0.1 dB.

Biasing Network Design

Since the performance of an HBT is highly dependent on temperature, to prevent thermal runaway, a complementary-to-absolute-temperature (CTAT) voltage reference is desirable for a PA [SSCG20]. To sense the junction temperature variation correctly, such biasing network has to be placed as close as possible to the PA core [SSCG20, JGC20]. In this PA, a BiCMOS CTAT biasing network is designed as illustrated in Figure 4.3(a), including a main CTAT sensor Q_{B1}, a β-helper Q_{B2} and a tunable PMOS current source M_1. Additional $R_{1,2}$ are



(a) (b)

Figure 4.3: (a) Proposed BiCMOS CTAT biasing network. (b) Simulated adjustable bias voltages of the CTAT biasing network and its temperature effect from 25 to 100°C [1]. © IEEE.

for the prevention of any instability loop formed with the PA. Furthermore, R_{sense} is used to detect the real-time V_{bias} and can also act as a resistive biasing network, if needed. Regarding the design of thermal coupling, the proximity of the biasing network to the PA core is important but poses challenges due to their comparable footprints. Particularly at higher frequencies, it results in increased interconnections between devices within the PA core, leading to additional losses. To mitigate this, one strategy is to position only the CTAT sensor (i.e., Q_{B1}) alongside with the PA core, while other components such as Q_{B2} are situated farther away [JGC20]. However, the Q_{B2} supplements DC current in large-signal operation of the PA core and is also sensitive to temperature variation, which suggests the effectiveness of the separation strategy might still be compromised. With the primary objective of reducing the additional impact of the biasing network on the PA core, this design proposes relocating the entire biasing network further away, while also integrating a tunable M_1 to regulate the temperature gradient. Figure 4.3(b) shows V_{sense} (i.e., V_{bias})-over-V_{ctrl} results in a DC simulation, and the ambient temperature is also swept from 25 to 100 °C. It indicates V_{bias} drops with the increase of temperature, which proves the CTAT characteristic. In addition, the adjustable M_1 also provides a wide tuning range of V_{bias}.

Experimental Results – Continuous Wave (CW)

The chip micrograph is shown in Figure 4.4. The core area measures 0.52 mm^2, excluding the pads but including the on-chip decoupling networks. Regarding

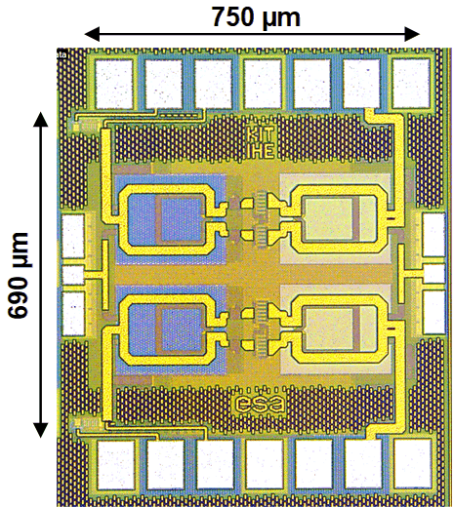


Figure 4.4: Chip micrograph of the *K*u-/*K*a-band PA [1]. © IEEE.

DC bias, the tunable PMOS current source allows for adjustment of V_{bias} in the range of 0.87 – 0.88 V to fit the collector current (see Figure 4.3), which is then maintained for the following measurements. No thermal runaway is observed.

In the measurement of S-parameters at 17.3 – 21.2 GHz as shown in Figure 4.5, this PA achieves a gain of 16.1 – 18.3 dB and a greater-than-unity K-factor over the entire frequency range. Figure 4.6 shows the CW large-signal results of 18.8 GHz, 19.25 GHz and the target band 17.3 – 21.2 GHz. Over the frequency range, the PA provides saturated output power (P_{sat}) of 22.5 – 23.0 dBm and saturated PAE (PAE_{sat}) of 33.5 – 39.3 %. Considering 4-dB output power back-off (OBO), it achieves $PAE_{4\text{dB}}$ of 19.7 – 22.6 %. As for 6-dB OBO, it delivers $PAE_{6\text{dB}}$ of 13.7 – 15.1 %. Note that the back-off refers to the P_{sat} where PAE peaks.

Experimental Results – Noise Power Ratio (NPR) and Modulated Signals

For NPR characterization, multi-tone signals are generated by Keysight IQtools on MATLAB with M8190A arbitrary waveform generator (AWG), and then up-

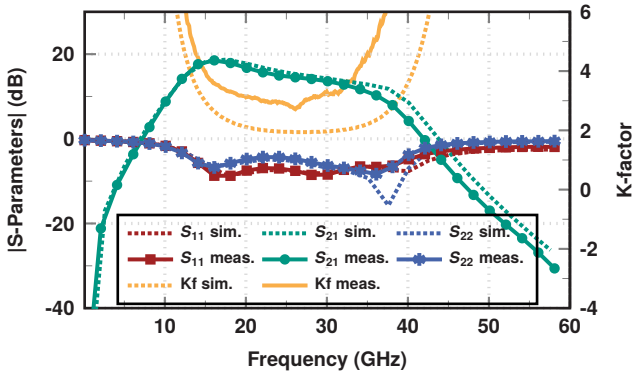


Figure 4.5: Simulated and measured S-parameters and K-factor of the PA [1]. © IEEE.

converted by E8267D PSG vector signal generator. The relative phase between tones is chosen as random to produce a Guassian-noise signal. The width of the notch is defined as 5 % of a single 50-MHz channel. The peak-to-average power ratio (PAPR) is measured separately as roughly 10.4 dB by a DSA93204A oscilloscope. With the PA, the output signal is characterized directly by the oscilloscope and analyzed with Keysight Vector Signal Analysis (VSA) software. As shown in Figure 4.7, at 15-dB NPR, the PA achieves output power (P_{out}) of 18.6 dBm with greater than 20 % PAE at both 18.8 GHz and 19.25 GHz. At 13-dB NPR, the PA achieves output power (P_{out}) of 20.4 dBm with greater than 26 % PAE at 18.8 GHz. Note that some systems can tolerate lower NPR [HBD+20]; hence, NPR of 13 dB is also pointed out. In addition, Figure 4.8 illustrates the large-signal sweep of the NPR measurements. At low-power region, the NPR is limited by the LO feed-through from the adopted E8267D PSG, since the LO leakage signal is also seen as noise in the middle of the notch.

In addition to NPR tests, DVB-S2 or DVB-S2X modulated signals are often adopted to evaluate *K*a-band transceivers for satellite applications [WYF+22]. Therefore, 16-APSK signals with 100 MBd and 1 GBd are also adopted here for further evaluation of the proposed PA. The constellation radius ratio of the 16-APSK is chosen as 2.57 and roll-off factor of the pulse-shaping raised-cosine filter is 0.35. The measured PAPR of the adopted signal waveform is roughly 7 dB. As illustrated in Figure 4.9, when tested with 16-APSK 100-MBd signal

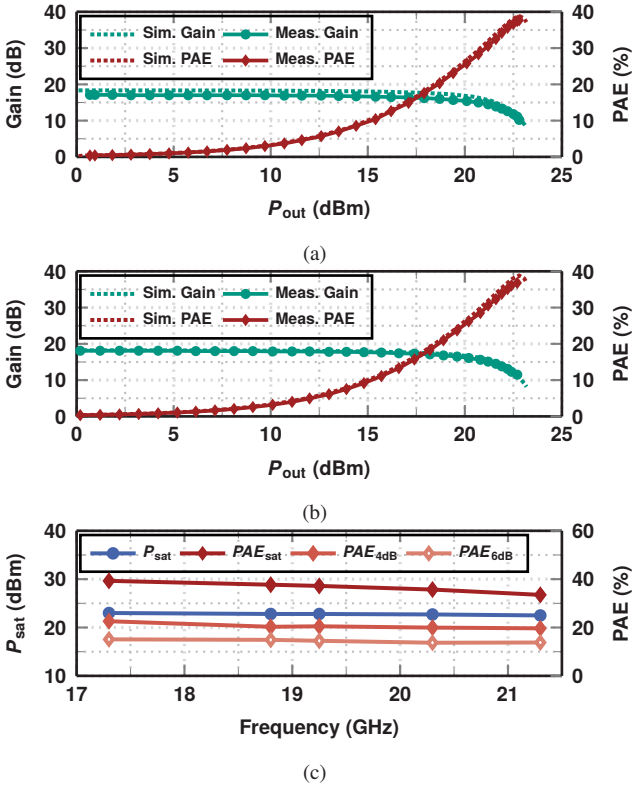


Figure 4.6: Simulated and measured (a) 18.8 GHz and (b) 19.25 GHz CW large-signal sweep of the PA. (b) Summary of 17.3 – 21.2 GHz measured large-signal results [1,12]. © IEEE.

at 18.8 GHz, the PA achieves average power (P_{avg}) of 22.0 dBm with 32.5 % PAE at −16.6 dB EVM; as for 1-GBd signal, the PA has 21.2 dBm P_{avg} with 28.1 % PAE at −16.1 dB EVM. At 19.25 GHz with 100 MBd, the PA achieves P_{avg} of 21.8 dBm with 32.0 % PAE at −16.4 dB EVM; as for 1-GBd signal, the PA provides 21.0 dBm P_{avg} with 27.1 % PAE at −16.1 dB EVM.

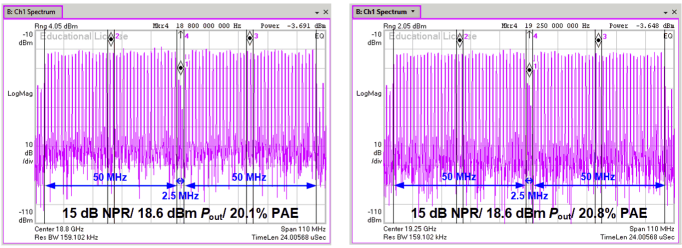


Figure 4.7: NPR measurements of the PA: spectra of 18.8 GHz (left) and 19.25 GHz (right) with overall signal of 100 MHz and notch of 2.5 MHz at NPR of 15 dB [1]. © IEEE.

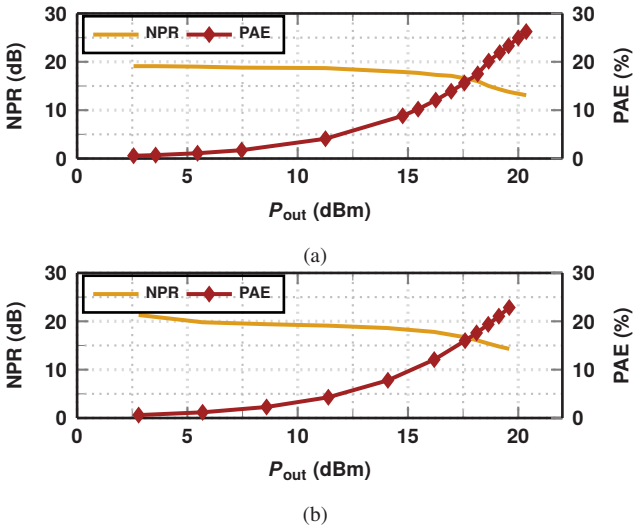
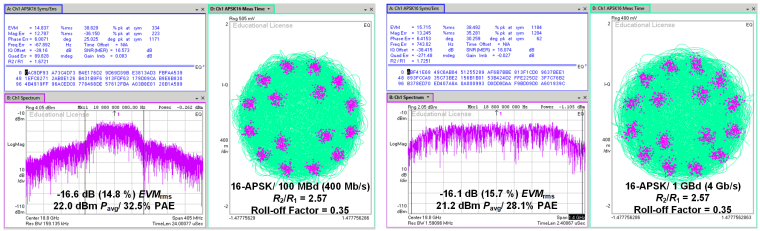


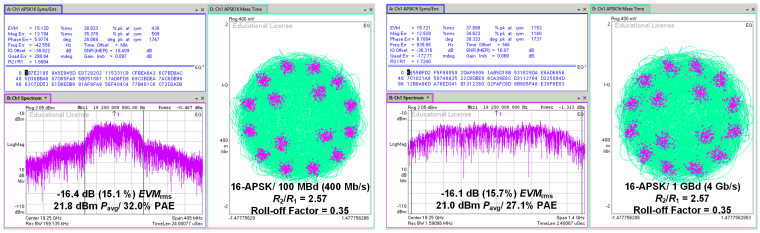
Figure 4.8: NPR measurements of the PA: large-signal sweep at (a) 18.8 GHz and (b) 19.25 GHz [1]. © IEEE.

4.1.2 Design of a V-Band CMOS PA in GF 22FDX

This subsection presents a V-band transformer-based two-way current-combined PA, implemented in GlobalFoundries (GF) 22-nm FD-SOI technology (22FDX-EXT®V1.0_2.0). As mentioned in Section 1.1, the



(a)



(b)

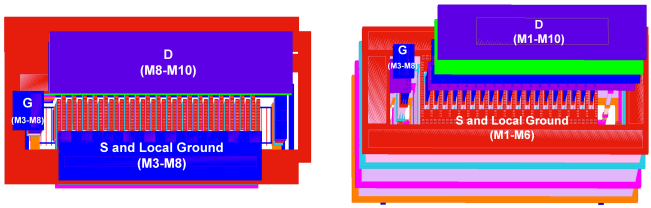
Figure 4.9: Measured 100-MBd and 1-GBd 16-APSK constellation diagrams and spectra at (a) 18.8 GHz and (b) 19.25 GHz of the PA [1]. © IEEE.

V-band is a promising candidate for high-throughput applications, and CMOS technology shows strong capabilities for low-voltage design and high system integration. In the following, detailed design considerations are discussed, and comprehensive experimental results of the fabricated PA are provided.

Circuit Details

The 22-nm FD-SOI process provides a back-end-of-line (BEOL) option of copper 1P10M and one aluminum layer. M8 is a thick metal layer and M9-M10 are both ultra-thick metal layers.

Since the nominal voltage is only 0.8 V per transistor in this technology, a cascode configuration is preferred to provide a high power density for PA designs. However, as previously mentioned, in modern CMOS and SiGe technologies, the parasitic capacitance of the upper device in a cascode may cause negative impedance [TNH13, 12]. To prevent this, a capacitive-neutralized common-



(a) with M8 option (b) with M1 option

Figure 4.10: Layout designs of a single NMOS transistor of the PA core and the EM views. Two metallization options provided by GF are considered [9]. © IEEE.

source (CS) configuration is adopted. In this context, to further increase the output power (P_{out}) of the PA, a transformer-based two-way current-combined topology is utilized.

Super-low Vt NMOS transistors are utilized due to their comprehensive mm-wave models. GF offers three metallization options for designers, which should be considered at the initial stages of PA design. Two of these options, including their electromagnetic (EM) views, are illustrated in Figure 4.10. The single NMOS device is sized with a total gate width of 45.6 µm, consisting of 38 gate fingers with double the gate pitch, and a gate length of 18 nm. With the M8 option, the NMOS model includes metal connections extending up to M8 for the drain (D) and source (S) terminals. For the common-source (CS) configuration, the S terminal is routed to the south side and connected to a thick M3–M8 stacked ground plane and the backgate (Figure 4.10(a)). However, this layout style features the S terminal routed through thin fingers, which may lead to electromigration issues due to increased DC currents in the large-signal operating region of the PA. For improved reliability, similar to the reported PA in advanced CMOS [ZR15], we adopt the layout shown in Figure 4.10(b), ensuring uniform current distribution to the ground on both the south and north sides. To achieve this layout, we use the M1 option, where the NMOS model includes only metal connections limited to the M1 layer for the D and S terminals, while the additional upper metal connections must be modeled separately through EM analysis. Nonetheless, designers should note that the model with M1 option does not partition the multi-finger structure in the schematic-level symbol. As a result, additional parasitic capacitances between

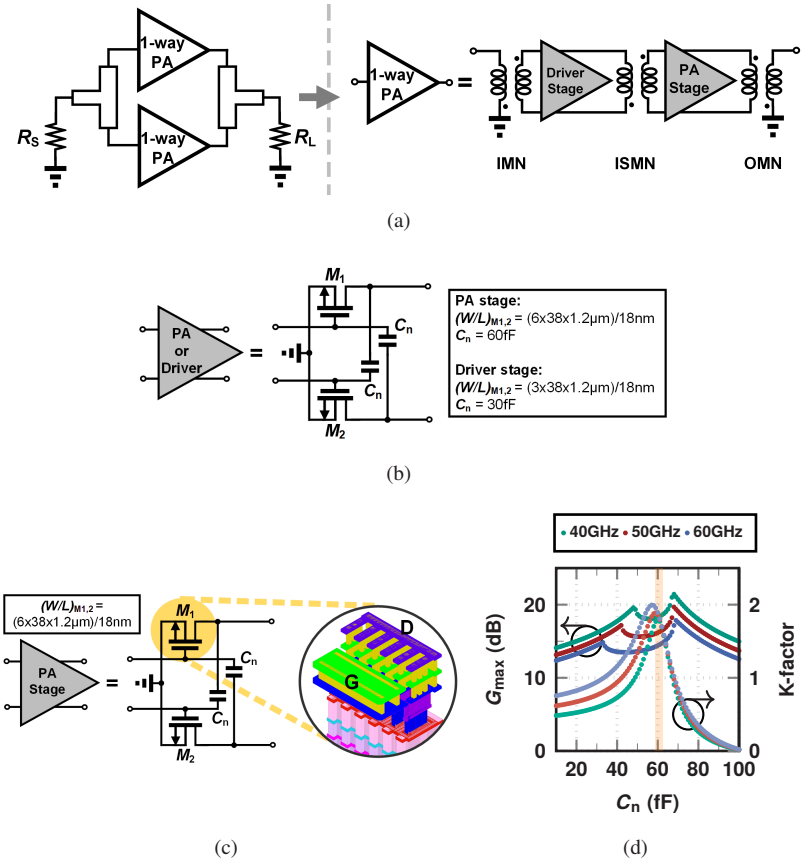


Figure 4.11: Schematics of the two-stage, two-way current-combined PA. (a) Block diagram. (b) Detailed schematic with device sizes for the driver and PA stages [9]. © IEEE. (c) Interdigital layout of single-ended core devices of the PA stage. (d) G_{max} and K-factor simulation versus C_n values. Supply voltage V_{dd} is 0.8 V.

D and S from the M1-M6 metal connections, obtained through EM simulations, remain hidden, leading to inaccuracies. Therefore, the proposed design adopts the layout shown in Figure 4.10(b), while the simulations are conducted using the foundry model illustrated in Figure 4.10(a).

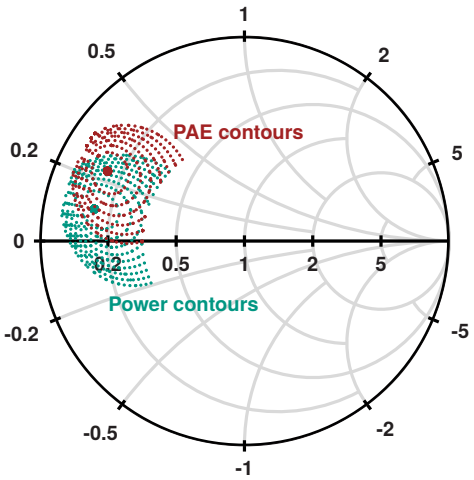
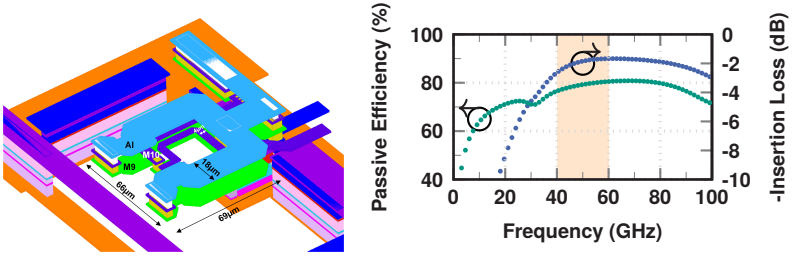


Figure 4.12: Load-pull simulations of the pseudo-differential PA stage at 50 GHz. Both power and PAE contours are shown.

In the two-way PA design, each way consists of two stages—the driver stage and the PA stage—configured to provide sufficient gain for measurement purposes (Figure 4.11(a)). Both stages use pseudo-differential pairs, with the driver stage sized at half the size of the PA stage. The complete schematic of the PA is shown in Figure 4.11(a)–(b), where transformer-based matching networks are utilized. The driver stage is biased under quiescent drain current density (J_D) of 0.28 mA/μm; the PA stage has J_D of 0.29 mA/μm. For one side of the PA stage (i.e., single end), six NMOS devices are used, with one NMOS device illustrated in Figure 4.10(b), resulting in an effective total gate width of 273.6 μm. As illustrated in Figure 4.11(c), for minimizing the core area and reducing extra loss from interconnections, an interdigital layout for the six devices is adopted [ZR15, 6]. The selection of the C_n values is determined by the range of maximum available gain (MAG), where K-factor is greater than unity. As shown in Figure 4.11(d), for the PA stage, the C_n is selected as 60 fF, which guarantees the stability across 40 to 60 GHz. Likewise, C_n value of the driver stage can be selected as 30 fF. Note that, due to the absence of nonlinear diffusion capacitance in CMOS technology, the neutralization technique maintains its validity throughout the entire dynamic range. Subsequently, load-pull simulations are



(a) (b)

Figure 4.13: (a) Layout/EM view of the stacked transformer-based output matching network (OMN). (b) Simulation of passive efficiency and insertion loss (IL) of the OMN [9]. © IEEE.

conducted for the PA stage at 50 GHz, with results shown in Figure 4.12. The maximum P_{out} is 18.3 dBm with $Z_{\text{opt,diff}}$ of $7.2 + \jmath 5.2\ \Omega$; the maximum PAE is 53.4% with $Z_{\text{opt,diff}}$ of $7.5 + \jmath 11.75\ \Omega$. An in-between impedance is selected as a compromise for the output matching network (OMN) design.

Figure 4.13(a) illustrates the transformer-based OMN. To enhance mutual coupling between windings, a stacked structure is utilized [CR19], comprising the top three metal layers (M9, M10, and Al). As observed, the physical number of windings in M10 is designed as two to increase both the self-inductance and mutual inductance, facilitating impedance matching and reducing losses. The EM simulations are performed using Keysight RFPro. As shown in Figure 4.13(b), the OMN achieves a passive efficiency ranging from 76 % to 80 % across the frequency range of 40 GHz to 64.0 GHz. The insertion loss of the OMN is around 2 dB. Regarding input and interstage matching networks, they are also based on transformers.

Experimental Results – CW

Figure 4.14 shows the chip micrograph, which measures 0.27 mm^2 including on-chip decoupling capacitor networks and I/O pads.

S-parameters are characterized with a Keysight N5251A 110-GHz 2-port network analyzer system. The simulated and measured S-parameters are shown

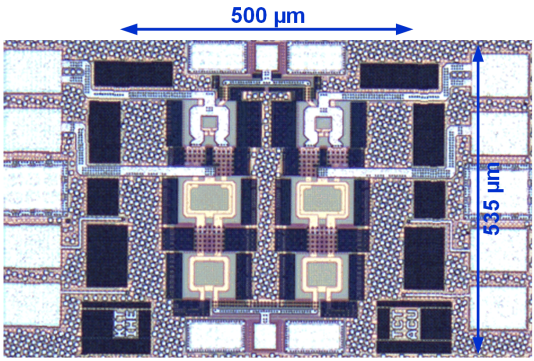


Figure 4.14: Chip micrograph of the V-band PA [9]. © IEEE.

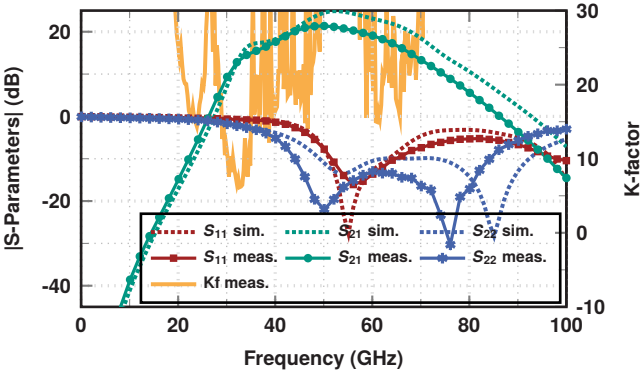
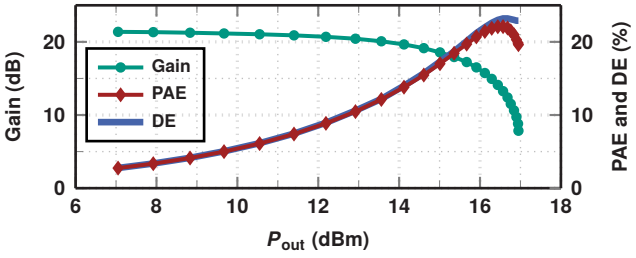
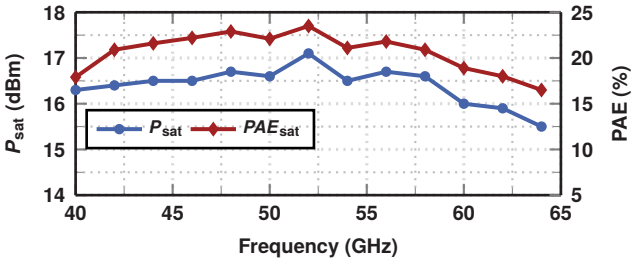


Figure 4.15: Simulated and measured S-parameters [9]. © IEEE.

in Figure 4.15. In the measurement, S_{21} peaks with 21.4 dB at 50.1 GHz and $BW_{\text{-3dB}}$ is 20.7 GHz, ranging from 41.3 GHz to 62.0 GHz. The S_{11} remains below −10 dB from 51.6 GHz to 64.8 GHz. Compared to simulations, the peak of S_{21} has shifted downwards by 3.5 dB from its original value at 52.5 GHz. This shift is likely due to an imprecise modeling from output networks including the drain of the NMOS, as S_{22} shows a similar trend, while S_{11} aligns well between the simulation and measurement. Nevertheless, the measured K-factor remains well above 5.5 across the entire frequency range.



(a)



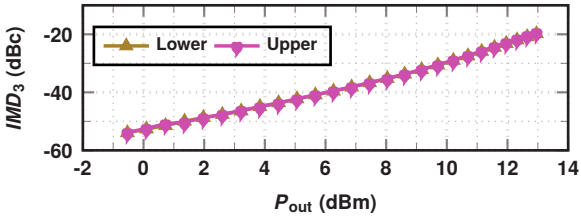
(b)

Figure 4.16: (a) Measured CW large-signal sweep at 50 GHz. (b) Summary of 40 – 64 GHz measured large-signal results of the PA [9]. © IEEE.

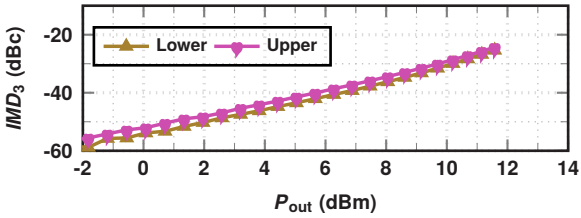
Large-signal measurements are conducted by a Keysight E8257D analog signal generator (ASG) and a 67-GHz N5247B PNA-X in spectrum mode. A U8488A power sensor is adopted for calibration. As shown in Figure 4.16(a), at 50 GHz, the PA delivers saturated power (P_{sat}) of 16.6 dBm with 22.1 % PAE and 23.2 % drain efficiency (DE). Figure 4.16(b) shows that, from 42 to 58 GHz, the PA delivers P_{sat} of >16.5 dBm with >20.9 % PAE. At 52 GHz, the PA delivers a maximum P_{sat} of 17.1 dBm with 23.5 % PAE.

Experimental Results – Third-Order Intermodulation Distortion (IMD_3) and Modulated Signals

For linearity characterizations, a two-tone test is considered. The N5247B PNA-X is exploited with its internal two sources and intermodulation distortion



(a) Δf = 500 MHz



(b) Δf = 2 GHz

Figure 4.17: Measured third-order intermodulation distortion (IMD_3) centered at 50 GHz with tone spacings (Δf) of 500 MHz and 2 GHz [9]. © IEEE.

measurement function. The U8488A power sensor is used again for calibration. Figure 4.17 shows the measured third-order intermodulation distortion (IMD_3) results centered at 50 GHz. With a tone spacing (Δf) of 500 MHz, the PA achieves P_{out} of 9.9 dBm at an IMD_3 level of −30 dBc. When Δf increases to 2 GHz, the PA delivers P_{out} of 9.7 dBm at the same IMD_3 level of −30 dBc. The increased Δf does not heavily worsen the linearity, whereas an asymmetry of upper and lower tones manifests itself in Figure 4.17(b).

Digital IQ modulation signals are considered additionally for PA characterizations. For generation of V-band modulated signals, Keysight M8190A AWG, E8257D ASG and Marki MMIQ-1865L IQ mixer are used at the input. Meanwhile, a SHF 804 TL broadband amplifier and a V-band WR-15 attenuator are also employed to provide sufficient input power (P_{in}) and tuning capabilities. At the output, another IQ mixer is used for downconversion and DSA93204A oscilloscope digitizes the downconverted 15-GHz IF signal for EVM measurements. The PA are tested with 32-APSK and 16-QAM signals with maximal symbol rate of 4 GBd. The roll-off factor (α) of the raised-cosine pulse shaping filter

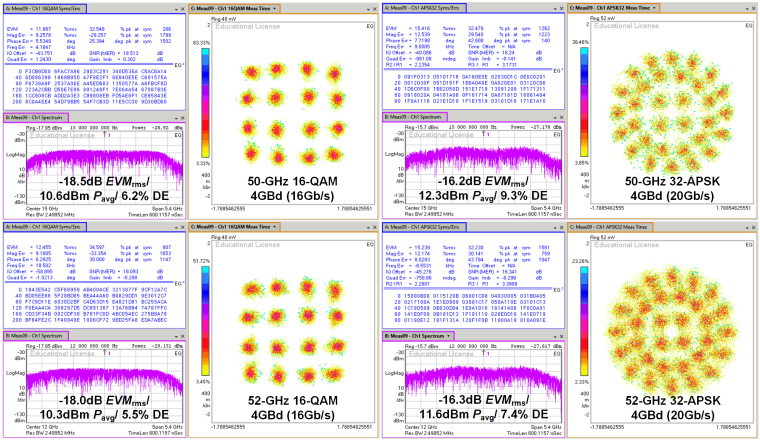


Figure 4.18: Measured constellation diagrams and spectra for 4 GBd 32-APSK and 16-QAM at 50 GHz and 52 GHz [9]. © IEEE.

is selected as 0.35. As illustrated in Figure 4.18, when tested with 32-APSK 4 GBd signal at 50 GHz, this PA achieves average power (P_{avg}) of 12.3 dBm with 9.3 % DE at −16.2 dB EVM. As for 16-QAM 4 GBd signal, the PA has 10.6 dBm P_{avg} with 6.2 % DE at −18.5 dB EVM. When tested with 32-APSK 4 GBd signal at 52 GHz, this PA achieves P_{avg} of 11.6 dBm with 7.4 % DE at −16.3 dB EVM. As for 16-QAM 4 GBd signal, the PA has 10.3 dBm P_{avg} with 5.5 % DE at −18.0 dB EVM. Note that the EVM requirements differ depending on the modulation scheme and application [ZR15, 1]. In addition, due to limited available power at the input in this measurement setup, an input coupler for instantaneous detection of P_{in} was not included. Therefore, only DE, rather than PAE, was measured.

4.1.3 Remarks on Results

TABLE 4.1 presents the performance summary of the 17.3 – 21.2 GHz SiGe PA and comparison with recently published ones in the similar frequency range. This PA achieves 22.8 dBm/22.8 dBm P_{sat} with 37.7 %/37.2 % PAE at 18.8 and 19.25 GHz. At NPR of 15 dB, the PA delivers 18.6-dBm P_{out} with greater than 20 %, at both 18.8 and 19.25 GHz. In the meantime, supporting specific 16-

Table 4.1: Comparison with recently published 16-to-20 GHz SiGe PAs.

	This Work	[LHW18]	[JLC22]	[CKR+22]	[CKA+23]	[KHL+23]
Supply(V)	1.5	1.9	3.6	3.3	4.2	2.4
Freq. (GHz)	18.8	20	16	18	18	17
Gain (dB)	17.5	20	10	13.7	21.4	23.8
P_{sat} (dBm)	22.8	17.4	20.5	25.2	30	14.1*$
PAE_{max} (%)	37.7	37	18	27.2	23.5	23.0*$
P_{out}/PAE at 15-dB NPR (dBm/%)	18.6/20.1	N/A	N/A	N/A	N/A	N/A
Area (mm^2)	0.52	0.29	0.77	1.2	1.1	0.43
Modulation Scheme	16-APSK	64-QAM	64-QAM	N/A	N/A	16-QAM
Freq. (GHz)	18.8	28.5	6	N/A	N/A	24
Symbol Rate (GBd)	1	1	1	N/A	N/A	0.4
EVM (dB)	-16.1	-23.5	-26.1	N/A	N/A	-26.8
P_{avg} (dBm)	21.2	10.7	10.3	N/A	N/A	34.7$^{\$\#}$
PAE (%)	28.1	21.4	6.4	N/A	N/A	N/A

*P_{1dB} and PAE_{1dB} $graphically estimated

#EIRP of 16-element Tx phased array

Table 4.2: Comparison with state-of-the-art V-band PAs in beyond-45nm CMOS/SOI technologies.

	This Work		[CWE24]	[LLLW21]	[CCE20]	[CTF+19]	[ZKR12]
Tech.	22-nm FD-SOI		22-nm FD-SOI	45-nm SOI	22-nm FD-SOI	22-nm FD-SOI	40-nm CMOS
Supply Voltage (V)	0.8		0.8	1.1	1	0.8	1
Frequency (GHz)	50	52	58	55	64	55	60
Gain (dB)	21.4	21.2	15	18.8	31	10.6	21.2
P_{sat} (dBm)	16.6	17.1	11.8	16.3	21.0	15	17.4
PAE_{max} (%)	22.1	23.5	39.8	35.4	28.7	11.8	29.3
Modulation Scheme	32-APSK	16-QAM	N/A	64-QAM	N/A	N/A	N/A
Frequency (GHz)	50		N/A	55	N/A	N/A	N/A
Symbol Rate (GBd)	4		N/A	3	N/A	N/A	N/A
EVM (dB)	-16.2	-18.5	N/A	-24.5	N/A	N/A	N/A
P_{avg} (dBm)	12.3	10.6	N/A	8.1	N/A	N/A	N/A
PAE (%)	9.3*	6.2*	N/A	9.1	N/A	N/A	N/A

*Drain efficiency

APSK signal with 100 MBd, the PA also achieves roughly 22-dBm P_{avg} with greater than 32 %, at EVM level of roughly −16 dB (15.8 %). Note that EVM requirements vary with different modulation schemes. Concerning 4-, 16-, and 64-QAM signals, the possible EVM levels for PA designs can be referenced in [ZR15]. Concerning 16-APSK signals, the EVM level of −16 dB is set to provide a margin for a C/N ratio of 9 to 13.5 dB [ETS15]. In comparison, with the less stringent EVM requirements for 16-APSK, the PA can achieve higher P_{avg} and PAE.

TABLE 4.2 summarizes the performance and compare the proposed 22-nm V-band PA with reported ones in beyond-45nm CMOS/SOI technologies. At a low supply voltage of 0.8 V, this work demonstrates competitive performance across 42 to 58 GHz, achieving P_{sat} of over 16.5 dBm with PAE values exceeding 20.9 %. Furthermore, this V-band PA supports broadband modulation signals up to 4 GBd, achieving a state-of-the-art instantaneous 20 Gb/s data rate with a 32-APSK signal.

4.2 SiGe Linear PA with High Power Density

Parts of the following section were previously published in [6].

This subsection presents a linear and efficient *K*a-band PA, implemented in the IHP SiGe SG13G2 technology, targeting high power density for 28-GHz applications. High power density is a key design consideration for PAs, particularly for compact phased-array system integration, such as in UE, where form-factor limitations restrict the available area for each circuit building block. To overcome this challenge, this design utilizes an ultra-compact, transformer-based neutralized cascode topology.

4.2.1 Design of a *K*a-Band Cascode PA in IHP SG13G2

Considering a PA design for higher power density, a cascode pseudo-differential pair is a top candidate. Firstly, the cascode topology provides sufficient gain while saving area compared to a two-stage amplifier design that includes a driver stage. Secondly, the differential topology enables effective power combining at

the output. By using area-efficient transformer-based output matching networks, a compact PA footprint can be achieved. Thirdly, since CB devices offer higher P_{out} than CE devices, the two-way power combining technique adopted in the previous Section 4.1.1 is not always required, allowing the PA size to be further reduced for a given target P_{out} level.

The same as SG13S, SG13G2 offers one poly layer, seven metal layers (M1-M5, TopM1 and TopM2) and metal-insulator-metal (MIM) capacitor layers. The overall schematic is shown in Fig. 4.19. Detailed PA design considerations are provided as follows, along with experimental results.

Ultra-Compact Neutralized Cascode PA Core

At each single end of the cascode pseudo-differential pair, both the common-emitter cell and common-base cell comprise 60 C-E-B HBT multipliers (Q_{1-4} in Fig. 4.19), resulting in a total effective emitter area of 3.78 µm^2. For minimizing the PA core size and interconnection loss, the devices are arranged interdigitally, as mentioned in Sections 4.1.1 and 4.1.2 for CE and CS devices. This layout concept is also applied to the CB devices. As shown in Fig. 4.20, in the C-E-B unit cells, the emitter terminal metal is located in the center, flanked by the collector and base terminals on the upper and lower sides. Therefore, M2–M4 thick and sufficiently wide metal bars are used to connect the HBT

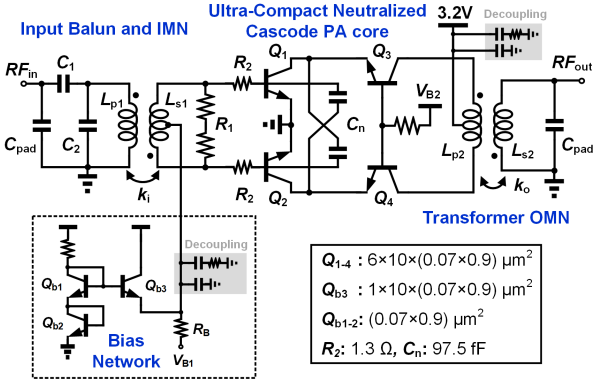
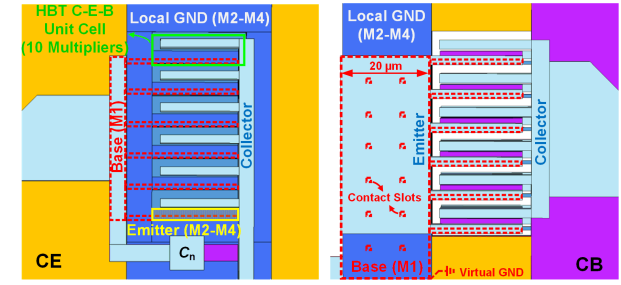
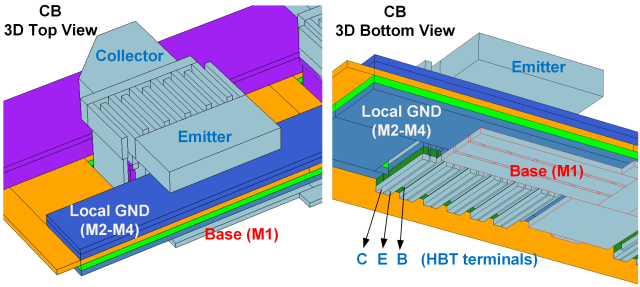


Figure 4.19: The entire schematic [6]. © IEEE.



(a)

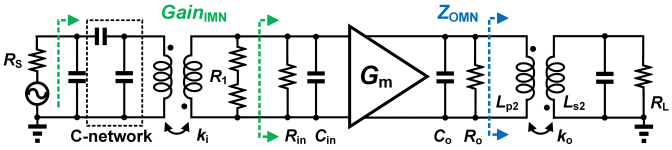


(b)

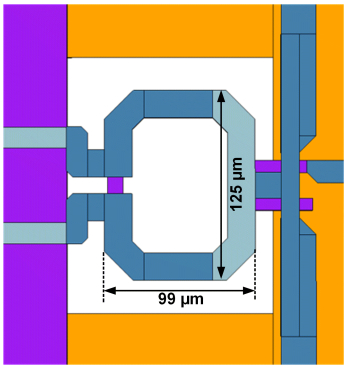
Figure 4.20: (a) Layout of the proposed interdigital common-emitter devices Q_{1-2} (left) and the common-base devices Q_{3-4} (right) [6]. © IEEE. (b) 3D views of the CB devices. Slots on the base 20-µm low-impedance M1 line are made for connections between the local ground and substrate.

emitter terminals to the outer ports, reducing IR drop. For the common-emitter devices, M2–M4 layers are also used for the surrounding local ground, while for the common-base devices, additional M4–TopM1 layers are employed to handle large currents and connect with the collector terminals of the following CE devices.

To improve small-signal stability, poly-silicon resistors R_2 are added (Fig. 4.19). In addition, capacitive neutralization technique is used to enhance differential stability and the neutralization capacitance C_n is chosen as 97.5 fF. Concerning base terminals of the common-base cells, instability emerges if the connection metals are inductive. Using additional capacitors leads to layout complexity



(a)



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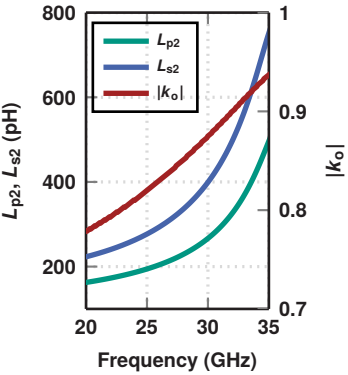

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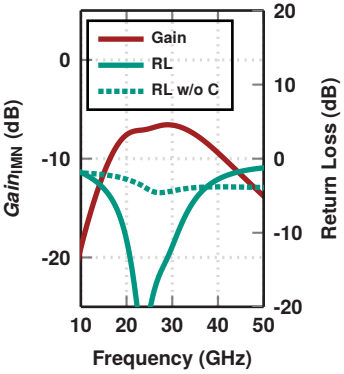
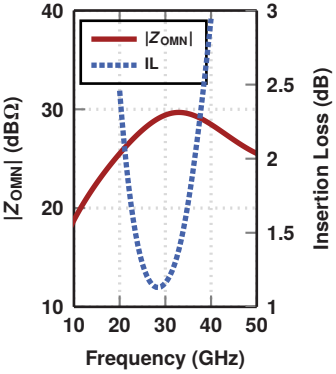


(d)



(e)

Figure 4.21: (a) Simplified schematic, (b) layout of the TF_o, (c) simulated self-inductance and coupling factor of the TF_o, (d) simulated gain and return loss of the input matching network, (e) simulated input impedance and insertion loss of the TF_o [6]. © IEEE.

since the local ground (M2-M4) blocks base terminal (M1) from connecting to higher metal layers. Thus, to ensure stability, a 20-µm low-impedance M1 line is adopted together with the differential virtual ground. Small slots are also made on the line for substrate contacts to avoid uneven local substrate potential around the transistors (see Fig. 4.20(b)).

Output and Input Transformer-based Matching Networks

For Class-AB operation, the optimal output impedance for maximum PAE and maximum output power at 28GHz are $16 + j32.8\Omega$ and $19 + j29.2\Omega$, respectively. An average value $18 + j31\Omega$ is selected as Z_{opt}. Accordingly, an inverting, broadside-coupled TF_o is designed to transform the Z_{opt} to $50\,\Omega$. This TF_o can be modeled as a coupled inductor pair as shown in Fig. 4.21(a). At 28 GHz, the simulated L_{p2}, L_{s2} and $|k_o|$ are 230 pH, 340 pH and 0.85 respectively (Fig. 4.21(c)). The layout is shown in Fig. 4.21(b) where stacked M4–M5 and stacked TopM1–TopM2 are used to minimize the insertion loss. As depicted in Fig. 4.21(e), the TF_o has a simulated 22.3–45.6-GHz wideband input impedance of the output matching network (Z_{OMN}) with a minimal insertion loss (IL) of 1.1 dB at 28.5 GHz. Regarding overall frequency response, input matching network (IMN) also plays a vital role. From source to the differential input of the PA (simplified as G_m in Fig. 4.21(a)), simulated gain of the IMN ($Gain_{IMN}$) is shown in Fig. 4.21(d), where the 3-dB bandwidth is 16.8 – 40.3 GHz. Along with the Z_{OMN} response at output, the PA provides a flat response over n257 band. Moreover, with a standalone input balun, it is hard to achieve an input return loss (RL) <-10 dB. Thus, a C-network (C_{1-2} in Fig. 4.19) and R_1 are designed to satisfy the requirement (Fig. 4.21(d)).

Experimental Results – CW

The chip micrograph is shown in Fig. 4.22. The core area measures 0.162mm^2 including on-chip decoupling capacitors. The PA is characterized through on-wafer probing.

Both small-signal S-parameters and large-signal power measurements are conducted through Keysight N5247A PNA and power meter. Under quiescent collector current density (J_c) of $14\,\text{mA}/\mu\text{m}^2$, the simulated and measured S-

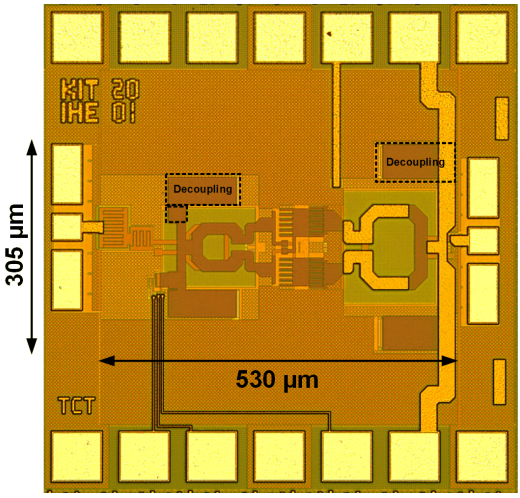


Figure 4.22: Chip micrograph of the *K*a-band PA [6]. © IEEE.

parameters are shown in Fig. 4.23. S_{21} has a peak at 28.9 GHz with 19.4 dB and the BW_{-3dB} is 10.5 GHz from 23.5 to 34 GHz. At the input, S_{11} is lower than −10 dB from 19.2 GHz to 32.5 GHz. The 28- and 29-GHz large-signal measured results are depicted in Fig. 4.24. At 28 and 29 GHz, the PA achieves 22.7 dBm and 22.4 dBm P_{sat} with 38.1 % and 39.8 % PAE respectively.

Experimental Results – Modulated Signals

64-QAM PRBS15 signal with 400 MBd and 800 MBd and 256-QAM PRBS15 signal with 100 MBd are used. The α of the raised-cosine pulse shaping filter is selected as 0.35; the PAPR are 8.3 dB and 7.9 dB for 64- and 256-QAM respectively. As illustrated in Fig. 4.25, when tested with 64-QAM 800 MBd signal at 28 and 29 GHz, this PA achieves P_{avg} levels of 16.2 dBm and 17 dBm with 11 % and 13.3 % PAE, respectively, at −25 dB EVM. As for 256-QAM 100 MBd signal, the PA has 15.4 dBm and 15.8 dBm P_{avg} with 9.4 % and 10.5 % PAE at −30 dB EVM.

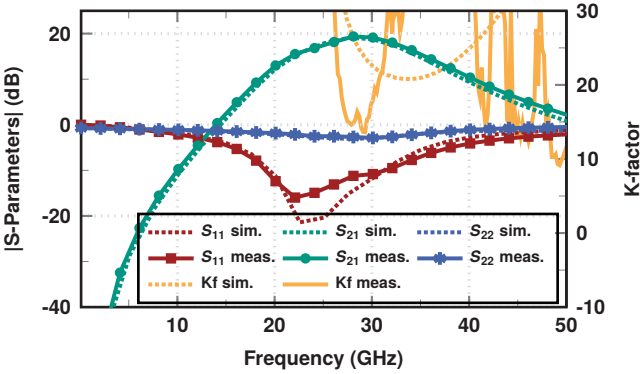


Figure 4.23: Simulated and measured S-parameters and K-factor of the PA [6]. © IEEE.

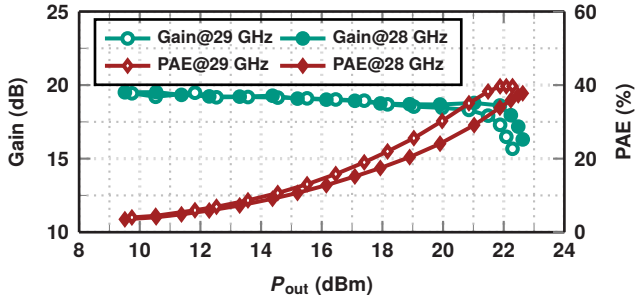


Figure 4.24: Measured CW large-signal sweep at 28 GHz and 29 GHz [6]. © IEEE.

4.2.2 Remarks on Results

This section has presented a compact, transformer-based SiGe PA suitable for 5G phased-array applications. The performance of this design is summarized in Table 4.3 and compared with other high-power-density works. To ensure a consistent evaluation, all designs selected for comparison also provide results from modulation signal tests. With the proposed ultra-compact cascode topology, the PA achieves the highest power density in CW tests and over 26 – 30 GHz, P_{1dB} are greater than 20 dBm with PAE above 30 %. As for 64-QAM 4.8 Gb/s

Table 4.3: Comparison with published Si-based PAs with high power density

	This Work	[WW20]**	[WWW20]	[ZTK+20]**	[HLLW18]
Tech.	130-nm SiGe	130-nm SiGe	90-nm SiGe	22-nm SOI	90-nm CMOS
Supply Voltage (V)	3.2	2	3	2.4	NA
Frequency (GHz)	28	28	24	28	28
Gain (dB)	19.4	20.5	17.4	26.1	16.3
P_{sat} (dBm)	22.7	28.3	20.9	22.5	26
PAE_{max} (%)	38.1	30.4	43.7	28.5	34.1
P_{1dB} (dBm)	22.1	26.8	20.6	21.1	23.2
PAE_{1dB} (%)	35.2	30.2	41.0	26.6	15.0
Core Area (mm^2)	0.162	1.35	0.15	0.2	0.4
Power Density* (mW/mm^2)	1149.4	500.8	820.2	889.1	992.8
Modulation Scheme	64-QAM	64-QAM	64-QAM	64-QAM	256-QAM
Symbol Rate (MBd)	800	200	100	400	100
EVM (dB)	-25.2	-25	-25.1	-25.1	-32.0
P_{avg} (dBm)	16.2	20.9	12.6	10.9	20
PAE (%)	11	18.4	17.5	9.2	NA

*Power Density=P_{sat}/Core Area **Doherty PAs

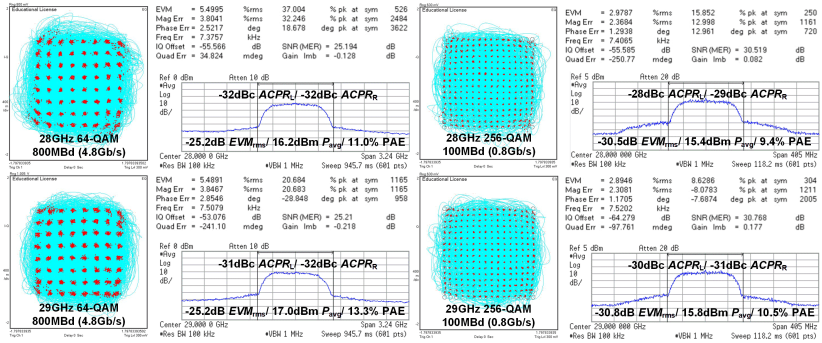


Figure 4.25: Measured constellation diagrams and spectra at 28 GHz and 29 GHz [6]. © IEEE.

modulated signal tests, from 26 to 30 GHz, P_{avg} are continuously greater than 16 dBm with PAE above 11 % at −25 dB EVM.

4.3 SiGe Balanced and Doherty PAs

Parts of the following section were previously published in [11].

In this section, two PA designs are presented to demonstrate the advanced power-combining techniques. The first is a *K*u-band balanced PA, derived from the *K*u-band PA in IHP SG13S, described in Section 4.1.1, and intended for SATCOM large-scale arrays, where insensitivity to antenna impedance variations is a design consideration. The second is a 28-GHz Doherty PA, extended from the *K*a-band PA in IHP SG13G2, discussed in Section 4.2.1, and intended for 5G communications. The design details are presented below.

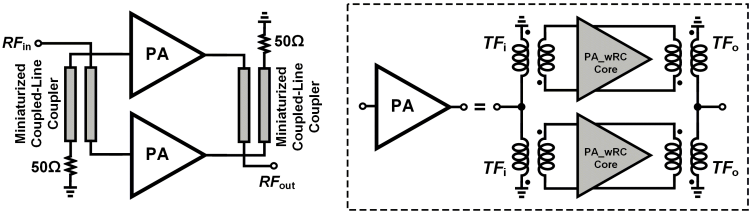


Figure 4.26: The schematic of the balanced PA, incorporating two two-way transformer-combined PA elements, illustrated in Figure 4.1. Miniaturized 90° coupled-line couplers are designed and adopted.

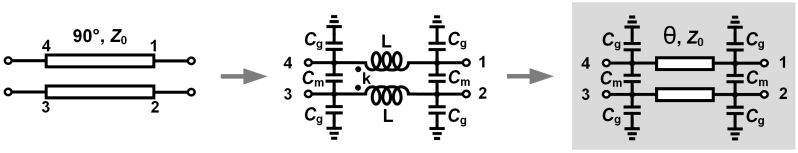
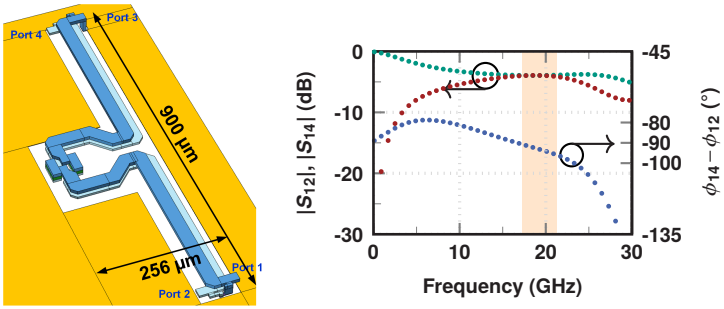


Figure 4.27: Development of the proposed 90° miniaturized coupled-line coupler. By introducing the lumped capacitors C_g and C_m, the distributed coupled line can be effectively shortened, achieving an electrical length of $\theta < 90°$.



(a) (b)

Figure 4.28: (a) Layout/EM view of the miniaturized 90° coupled-line coupler and its (b) simulated results.

4.3.1 Design of a *K*u-Band Balanced PA Using Miniaturized Coupled-Line Couplers

Circuit Details

The schematic of the balanced amplifier is shown in Figure 4.26. The design of the two identical PA elements is elaborated in the previous Section 4.1.1. Further, designing *K*u-band on-chip monolithic 90° hybrid couplers for the balanced configuration is critical, especially in terms of their occupied area. To address this, two miniaturized 90° coupled-line couplers are proposed and implemented.

As shown in Figure 4.27, the original 90° coupled-line coupler can be implemented using lumped capacitors C_g and C_m together with a pair of coupled inductors (transformer) [HCJ97, CMKY18]. The introduction of C_g and C_m allows the transformer to possess a smaller footprint compared to the original coupler. Moreover, the transformer can be regarded and modeled as a coupled-line coupler to account for its distributed characteristic [WW21a]. Consequently, a coupled line with an electrical length of θ is used to represent the miniaturized coupler. With the aid of C_g and C_m, θ smaller than 90° can be readily achieved, reducing the occupied on-chip area.

For the frequency range of 17.3 – 21.2 GHz, with C_g and C_m selected as 61 fF and 100 fF, respectively, the physical length of the coupled line is reduced to 1250 µm, compared to the original 1900 µm. By further adopting a meandered structure, as shown in Figure 4.28(a), the length is shortened to 900 µm, resulting in an area reduction of more than 50 %. The simulated S_{12} and S_{14} magnitudes, together with the phase difference, are presented in Figure 4.28(b). At 18.8 GHz, the insertion loss is 0.94 dB, and the phase difference is 92.6°.

Simulated and Experimental Results

The chip micrograph is shown in Figure 4.29. The core area measures 1.47 mm^2, excluding pads but including the on-chip decoupling networks.

Figure 4.30 presents the simulated and measured S-parameters of the balanced PA. This PA achieves a gain of 13.5 dB at 18.8 GHz with a $BW_{\text{-3dB}}$ of 12 GHz,

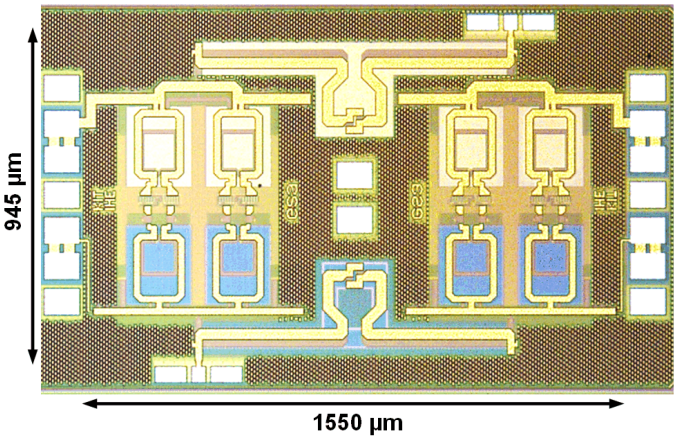


Figure 4.29: Die micrograph.

ranging from 12.3 GHz to 24.3 GHz. The K-factor remains above unity across the frequency range, indicating unconditional small-signal stability. Within the target frequency range of 17.3 – 21.2 GHz, both S_{11} and S_{22} stay below −10 dB. However, at 18.8 GHz, the measured S_{21} is reduced by 2.4 dB compared with the simulated result. The 17.3- and 18.8-GHz large-signal measured results are presented in Fig. 4.31. At 17.3 and 18.8 GHz, the PA achieves P_{sat} of 24.1 dBm with PAE of 24.7 % and 25.3 % PAE, respectively.

In addition, the performance of the balanced PA under load variation was evaluated through simulations. As shown in Fig. 4.32, at 18.8 GHz with a VSWR of 3:1, the small-signal gain ($|S_{21}|$) varies by less than 0.5 dB across the phase sweep, while the P_{sat} varies within 1.8 dB. In comparison, a standalone PA exhibits significantly larger variations of 5.0 dB and 4.0 dB, respectively. Regarding efficiency, the balanced PA shows a peak PAE variation of 10.3 pp across the phase variation.

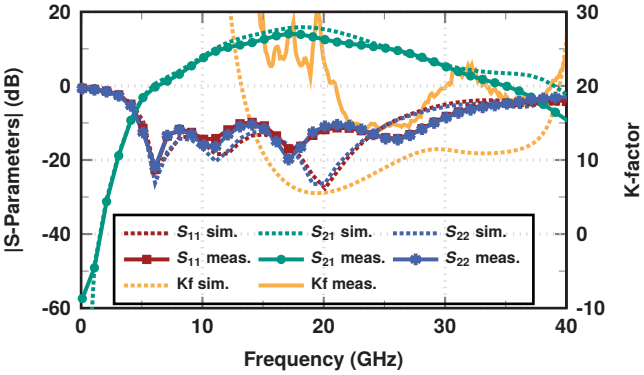


Figure 4.30: Simulated and measured S-parameters and K-factor of the balanced PA.

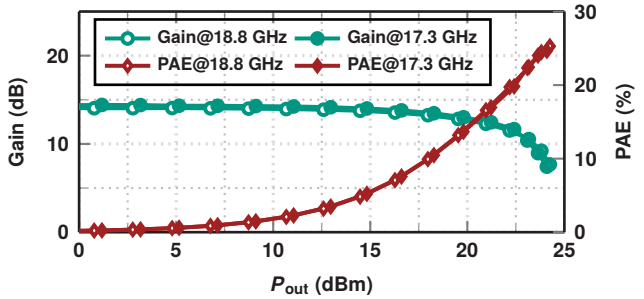


Figure 4.31: Measured CW large-signal sweep at 17.3 GHz and 18.8 GHz.

4.3.2 Design of a 28-GHz Doherty PA Using Meandered Coupled-Line Couplers

Circuit Details

The overall schematic is shown in Figure 4.33(a), where 90° hybrid couplers are employed. At the output, one coupled port (referenced to the amplifier terminals) is left open-circuited to enable Doherty functionality, while the counterpart port of the input coupler is terminated to provide the required 90° phase shift. Both

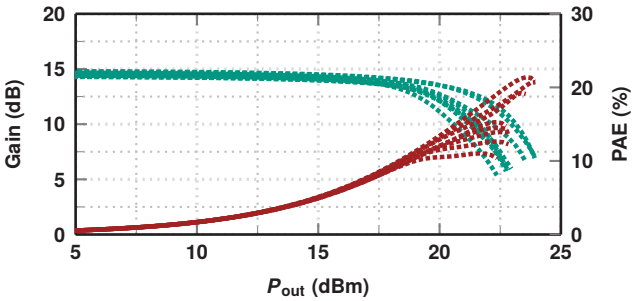
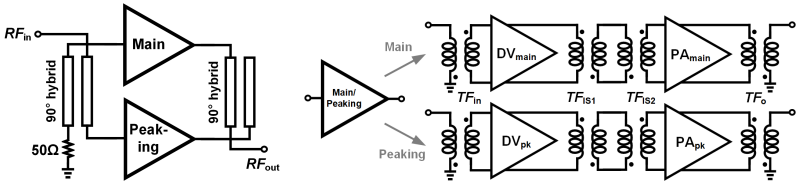


Figure 4.32: Simulated CW large-signal sweep at 18.8 GHz across the phase variation from 0° to 359° for a VSWR of 3:1.



(a) (b)

Figure 4.33: Schematics of the two-stage Doherty PA. (a) Overall schematic. (b) Detailed schematics of the main amplifier and peaking amplifier [11]. © IEEE.

the main and peaking amplifiers share the same structure, consisting of two stages—a driver (DV) stage and a PA stage—as shown in Figure 4.33(b). In Doherty (D) mode, however, the PA stages of the main and peaking amplifiers (PA_{main} and PA_{pk}) are biased differently: PA_{main} operates in Class-AB, while PA_{pk} operates near Class-B. In addition, the overall PA can also be operated in a quasi-balanced (QB) mode, where both PA_{main} and PA_{pk} are biased at Class-AB.

The PA topology with 90° hybrid couplers enables a cascadable design. The PA stages (PA_{main} and PA_{pk}) use the same design as presented in Section 4.2.1, except that the input transformer has been redesigned for fully differential operation, denoted as TF_{IS2} in Figures 4.33(b) and 4.34. This transformer features two windings of 139 pH and 90 pH with a k of 0.53. Unlike the cascode topology used in the PA stages, the DV stages (DV_{main} and DV_{pk}) adopt a CE neutralized pseudo-differential pair with a supply voltage of 1.2 V. The DV

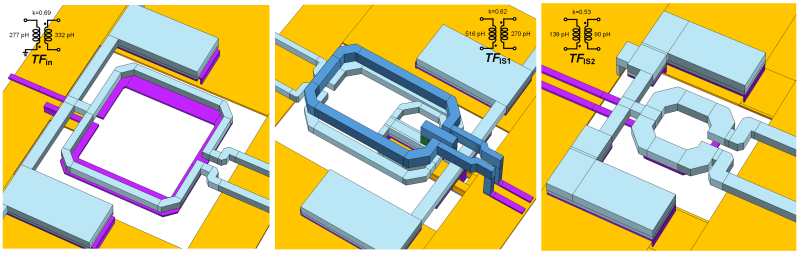


Figure 4.34: Parameters and EM views of the transformer-based input and interstage matching networks (TF_{in}, TF_{IS1} and TF_{IS2}) [11]. © IEEE.

stages provide additional gain and allow tuning of the input power levels that drive PA_{main} and PA_{pk}. Each single-ended device of the DV stages consists of 30 multipliers, which is half the size of the PA stage. The neutralization capacitance is selected as 55 fF to ensure small-signal stability. Two transformers, TF_{in} and TF_{IS1}, are employed as input and interstage matching networks, respectively. TF_{in} matches the DV input impedance to 50 Ω, while TF_{IS1} provides matching to the subsequent TF_{IS2}. The design parameters of TF_{in} and TF_{IS1} are detailed in Figure 4.34.

For the 90° hybrid coupler designs, broadside-coupled lines are adopted. Since the 90° phase shift relies on a quarter-wavelength structure, minimizing the occupied chip area becomes challenging. A miniaturized coupler, as proposed in Section 4.3.1 could be used; however, the additional small-valued MIM capacitors introduce extra process variation, which is a concern for Doherty PAs that are highly sensitive to amplitude and phase imbalances. Therefore, in this design, conventional coupled-line couplers are employed, with the lines meandered to save area. The original and meandered coupled-line couplers are illustrated in Figure 4.35(a), where ports 2 and 4 connect to the PA stages, and ports 1 and 3 serve as the two coupled ports, one of which functions as the output. Compared to the original coupler, the meandered version shortens one side by 635 µm, reducing Δy and thus decreasing the area overhead in the middle region when main and peaking amplifiers are laid out, as illustrated in Figure 4.35(b). Considering the total length of the two-stage amplifiers (935 µm), the use of meandered coupled-line couplers yields an area reduction of 0.52 mm^2. The simulated $|S_{12}|$ and $|S_{14}|$, along with the phase difference, are

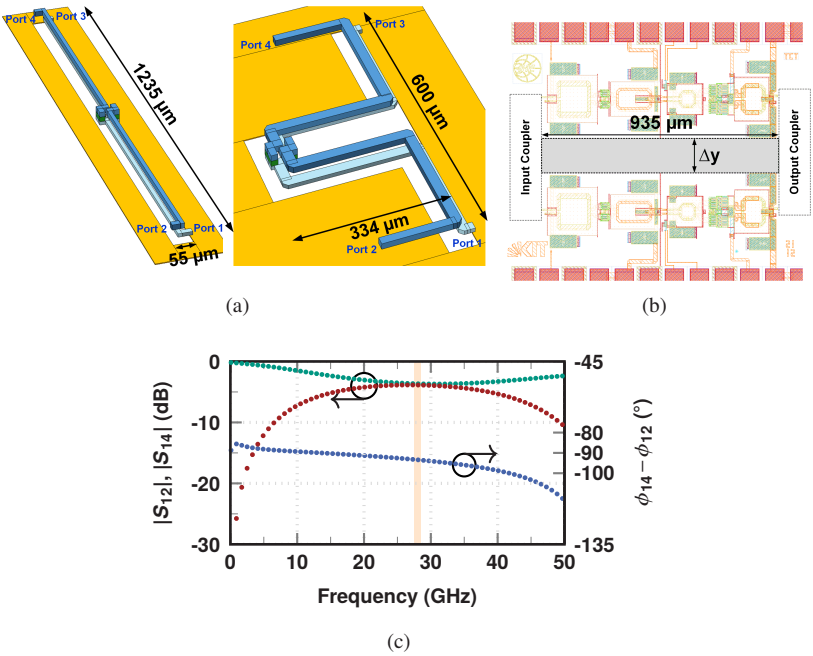
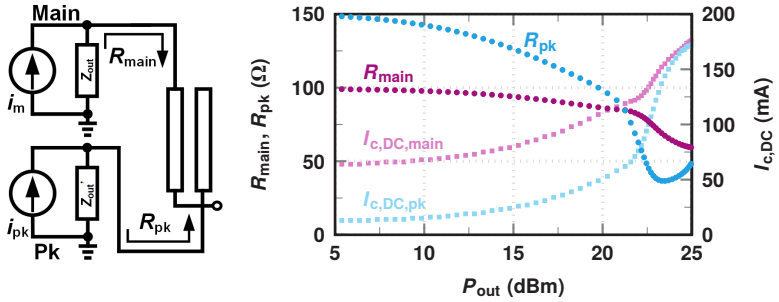


Figure 4.35: (a) Layout/EM view of the 90° coupled-line couplers: original (left) and meandered (right). (b) Consideration of the area overhead caused by the coupler geometry. (c) Simulated results of the meandered coupler [11]. © IEEE.

shown in Figure 4.35(c). At 28 GHz, the coupler exhibits an insertion loss of 0.8 dB and a phase difference of 93.5°.

Figure 4.36 shows the simplified output combining network representing the designed PA and the corresponding simulated results. In Figure 4.36(a), the current source i_m and nonlinear output impedance Z_{out} represent PA_{main} and its transformer TF_o as shown in Figure 4.33(b); likewise, i_{pk} and Z_{out}' represent PA_{pk} and its TF_o. Figure 4.36(b) presents the simulated driving-point load resistance and DC current profiles. Overall, the results agree with the theory depicted in Section 3.4.2. A clear load modulation effect is observed, where the driving-point load resistances R_{main} and R_{pk} eventually decrease to around 50 Ω. In the small-signal region, R_{main} is approximately twice 50 Ω and lower than



(a) (b)

Figure 4.36: (a) Simplified RF signal model of the output Doherty combining network shown in Figures 4.33. (b) Simulated load resistance and DC current profiles illustrating the load modulation effect of the Doherty PA [11]. © IEEE.

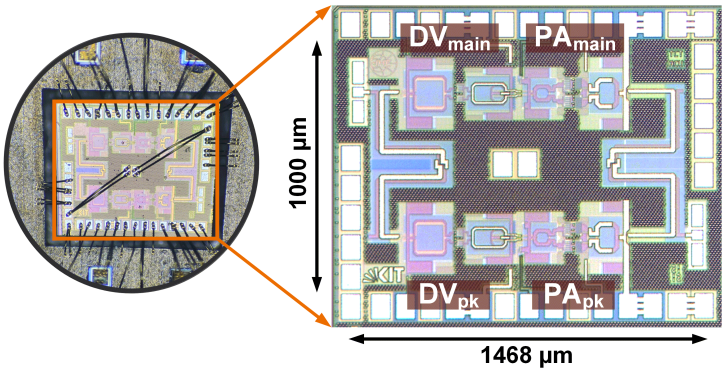


Figure 4.37: Die micrograph [11]. © IEEE.

R_{pk}. Notably, R_{pk} is not infinite in the small-signal region, as this simulation accounts for the finite Z_{out}' and the fact that PA_{pk} is not completely turned off.

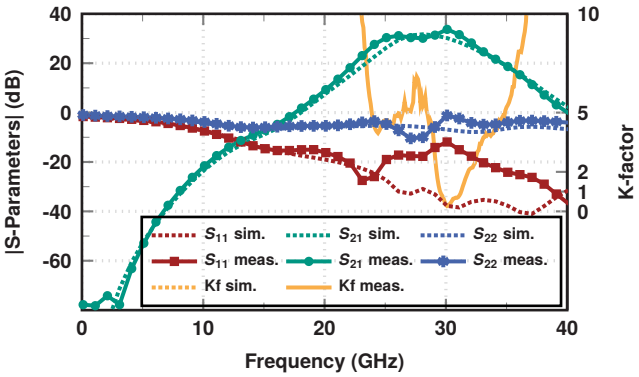


Figure 4.38: Simulated and measured S-parameters and K-factor of the Doherty PA [11]. © IEEE.

Experimental Results

The chip micrograph is shown in Figure 4.37. The core area measures 1.47 mm^2, excluding the DC pads but including the on-chip decoupling networks.

In the measurement of S-parameters shown in Figure 4.38, this Doherty PA achieves gain of 30.1 dB at 28 GHz and a $BW_{\text{-3dB}}$ of 5.9 GHz, ranging from 25.4 GHz to 31.3 GHz. In terms of small-signal stability, the K-factor falls below unity between 29.6 GHz and 31.2 GHz, indicating the PA is not unconditionally stable in this frequency range. This behavior is not observed in the simulation, where the K-factor remains well above 10. A possible cause is that some parasitic effects were not fully captured by the EM simulations of the input and output couplers, as evidenced by the noticeable deviation in S_{11} and S_{22} results. Nevertheless, the $|S_{11}|$ remains below −10 dB, and the $|S_{22}|$ remains below −1 dB. At the target frequency of 28 GHz, the PA also remains unconditionally stable. Compared to the simulation, however, the $|S_{21}|$ value has shifted downwards by 1.6 dB from its original value.

Large-signal measurements at 28 GHz are performed under two quiescent bias conditions for PA_{main} and PA_{pk}. In D-mode, the J_c values of $\{PA_{main}, PA_{pk}\}$ are set to $\{10.85\,mA/\mu m^2, 0.98\,mA/\mu m^2\}$. By contrast, in QB-mode, both are biased at 10.85 $mA/\mu m^2$. As shown in Figure 4.39, the D-mode PA achieves a P_{sat} of 24.6 dBm with a peak PAE of 31.2 %. Around the 2-dB OBO region,

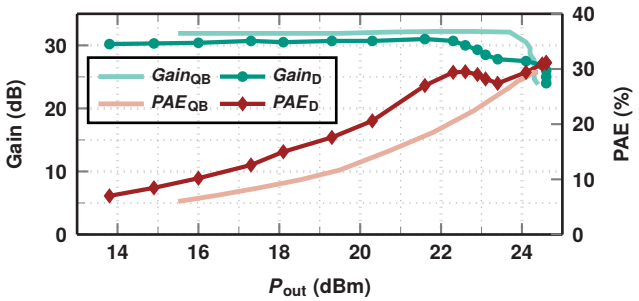


Figure 4.39: Measured CW large-signal sweep at 28 GHz of the PA in Doherty (D) and Quasi-balanced (QB) modes [11]. © IEEE.

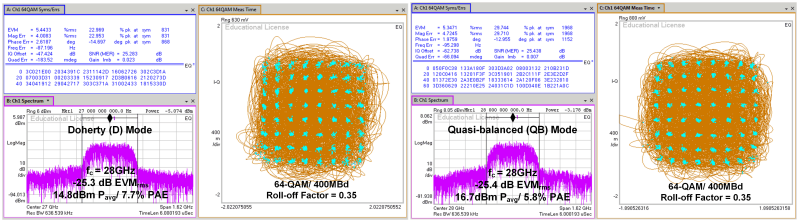


Figure 4.40: Measured constellation diagrams and spectra for 400 MBd 64-QAM at 28 GHz. A comparison is shown between D-mode (left) and QB-mode (right) operations of the PA [11]. © IEEE.

a clear second PAE peak of 29.5 % is observed. Compared to this, the QB-mode offers improved gain and linearity in the OBO region, at the expense of increased DC power consumption and thus reduced PAE.

Further, a typical single-carrier 400-MBd 64-QAM signal is used to characterize the PA in the two different modes. The aforementioned tradeoff between PAE and linearity is clearly demonstrated. In D-mode, the PA achieves P_{avg} of 14.8 dBm with 7.7 % PAE at −25.3 dB EVM. By contrast, QB-mode offers a higher P_{avg} of 16.7 dBm, but with a lower PAE of 5.8 %, at a comparable EVM level.

A performance summary and a comparison with previously reported Si-based 28-GHz Doherty PAs are shown in Table 4.4. In Doherty mode, the PA achieves high gain and moderate back-off PAE. Under a 400-MBd 64-QAM signal, it

delivers P_{avg} of 14.8 dBm with a PAE of 7.7 % at an EVM level of −25.3 dB, without the use of digital predistortion (DPD).

4.4 Chapter Conclusions

This chapter has presented five transformer-based PA designs using silicon technologies, including one implementation in 22-nm CMOS SOI and four in SiGe. Two of these PAs utilize a two-way current-combining technique to boost output power, with designs spanning the *K*u-, *K*a-, and V-bands. A specific design at 28 GHz targets both high linearity and high efficiency while also achieving high power density. The remaining two PAs build upon the previous designs, scaling performance through advanced balanced and Doherty power-combining techniques. Detailed results and performance comparisons are provided for each architecture. Additionally, all PAs were characterized using modulated signals to verify their linearity for practical, real-world communication applications.

Table 4.4: Comparison with published Si-based Doherty PAs at 28 GHz

	This Work	[KWP+25]	[AMAAH+25]	[MMWM22]	[ZTK+20]	[HWW19]
Tech.	130-nm SiGe	40-nm CMOS	90-nm SiGe	55-nm CMOS	22-nm SOI	130-nm SiGe
Supply Voltage (V)	3.1/1.2	2/1	1.8	2.4	2.4	1.5
Frequency (GHz)	28	28	28	28	28	28
Gain (dB)	30.1	25.5	20.4	16.1	26.1	18.2
P_{sat} (dBm)	24.6	25.2	19.9	25.5	22.5	16.8
PAE_{max} (%)	31.2	15.3	37.3	25.2	28.5	20.3
PAE_{6dB} (%)	16.3	8.6	31.1	20.4	22.1	13.9
Core Area (mm^2)	1.47	1.54	0.19	0.54	0.2	1.76
Modulation Scheme	64-QAM	64-QAM OFDM	64-QAM	64-QAM	64-QAM	64-QAM
Symbol Rate (MBd)	400	400	400	250	400	500
EVM (dB)	-25.3	-19	-25.7	-25.2	-25.1	-27
P_{avg} (dBm)	14.8	13.8	8.5	17.7	10.9	9.2
PAE (%)	7.7	5.2*	14.5	17.5	9.2	18.5
DPD	No	No	No	No	No	No

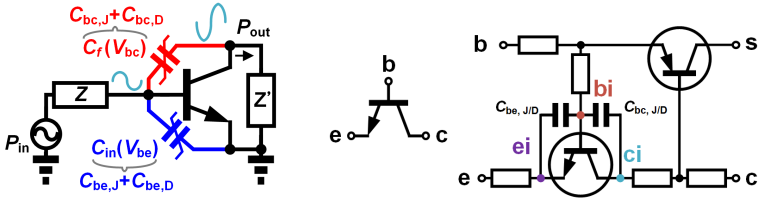
*Drain efficiency

5 SiGe Broadband Linear Power Amplifier Design with Enhanced Stability

Parts of the following section were previously published in [1] and [10].

This chapter focuses on large-signal stability in broadband SiGe PAs, with particular attention to designs covering the 17 – 30 GHz range, which spans both uplink and downlink bands used in next-generation mobile and satellite communications. As the operating bandwidth increases, maintaining stable large-signal operation becomes more challenging, making stability a primary design consideration. As discussed in Section 2.2.2, SiGe PAs achieve improved P_{out} using a CB configuration [RZSM19], which can be implemented either in a cascode or current-clamping CB topology. Current-clamping CB PAs offer linearity advantages, while cascode PAs, incorporating a CE stage, provide higher gain and simplify driver-stage design, making them widely adopted. However, CE devices are prone to large-signal instability, which will be investigated in the following sections, often appearing as sub-harmonic spurs and particularly relevant in broadband CE or cascode designs, necessitating careful stability assessment.

The chapter begins by analyzing the effects of nonlinear capacitances and identifying instability mechanisms using the methods detailed in Section 2.5. A stabilization case study is presented, followed by the design and demonstration of a broadband SiGe PA employing a common-collector–common-base (CC–CB) configuration, which exhibits enhanced large-signal stability and reduced sensitivity to instability phenomena.



(a) (b)

Figure 5.1: (a) Schematic of an HBT common-emitter (CE) RF amplifier and the nonlinear input and feedback capacitors (C_{in} and C_f). The nonlinear capacitances include depletion and diffusion capacitance. (b) A simplified diagram of the VBIC model and internal nodes (bi, ci and ei) of an HBT.

5.1 Nonlinear Capacitances in SiGe-HBTs and the Impact on Stability of PAs

In this section, the impact of nonlinear capacitances on stability is investigated through both theoretical analysis and silicon implementations. In particular, diffusion capacitances become more pronounced than junction capacitances under large-signal operation, thereby disrupting the small-signal stability achieved by neutralization capacitances in common-emitter (pseudo-)differential PAs. While previous discussion about nonlinear capacitances has focused on intermodulation distortion [vdHdGdV02][4], discussions on large-signal instability in modern SiGe PAs are limited in the literature.

5.1.1 Nonlinear Capacitance Effect in SiGe HBTs

In a generic RF amplifier, as shown in Figure 5.1(a), the input capacitance (C_{in}) and feedback capacitance (C_f) depend on the base-emitter voltage (V_{be}) and base-collector voltage (V_{bc}), respectively. These nonlinear capacitances consist of two components: (junction) depletion capacitance (C_J) and diffusion capacitance (C_D), both of which increase when the pn junction is more forward-biased [Rei03, MSB+96]. Due to these capacitances, the amplifier presents

[4] [vdHdGdV02] considered nonlinear C_{in} in the BJT, including both C_J and C_D.

nonlinearity in terms of phase as the input power (P_{in}) increases. It is worth mentioning that the nodes of observation should be set as close as possible to the internal nodes as depicted in Figure 5.1(b), a simplified diagram of the VBIC model of an HBT [MSB+96], since additional parasitic components in the model between internal and external nodes have an impact on the voltage values. In this context, for the following discussion, the voltage swings of V_{bx} is defined as

$$V_{\mathrm{bx}}(t) = V_{\mathrm{bi}}(t) - V_{\mathrm{xi}}(t),\ x = c, e, \tag{5.1}$$

where V_{bi} and V_{xi} are voltages at internal nodes of the base and the collector/emitter[5]. In addition, for describing to what extent the amplifier behaves nonlinearly, the OBO level is adopted.

A depletion capacitance related to the junction voltage (V_{j}) can be modeled as $\frac{C_{\mathrm{J0}}}{(1-V_{\mathrm{j}}/V_0)^m}$, where C_{J0} is the zero-bias depletion capacitance, V_0 is the built-in potential and m is the junction exponential factor. However, if $V_{\mathrm{j}} \geq V_0$ in the large-signal region, the term $(1 - V_{\mathrm{j}}/V_0)^m$ in the denominator becomes zero and complex number, making the model invalid. As an alternative, an extrapolated linear function is used [Rei03]:

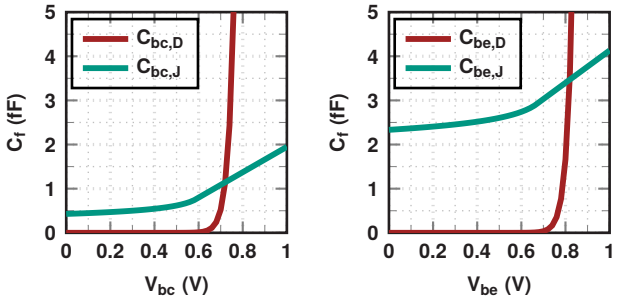
$$C_{\mathrm{J}} \approx mC_{\mathrm{J0}}V_{\mathrm{j}} + b, \tag{5.2}$$

where b is a constant and the slope of the C_{J}-V_{j} relationship depends on the value of m. Referred to the C_{in} in Figure 5.1(a), C_{J} is the base-emitter depletion capacitance ($C_{\mathrm{be,J}}$), with V_{j} applied with the V_{be}. Similarly, base-collector depletion capacitance ($C_{\mathrm{bc,J}}$) can be described in the model with V_{bc}.

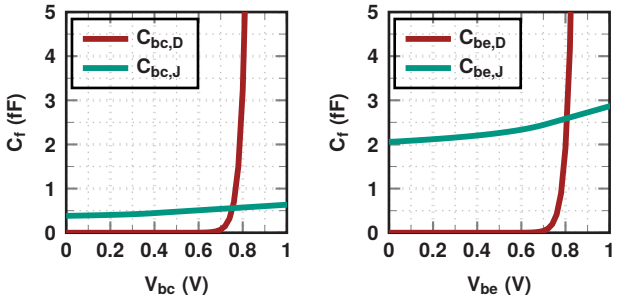
On the other hand, the base-collector diffusion capacitance ($C_{\mathrm{bc,D}}$) related to the reverse transit time (τ_{R}) and V_{bc} can be expressed as [Rei03, MSB+96]

$$C_{\mathrm{bc,D}} = \frac{\mathrm{d}q_{\mathrm{TC}}}{\mathrm{d}V_{\mathrm{bc}}} \approx \frac{\mathrm{d}\tau_{\mathrm{R}} i_{\mathrm{EC}}}{\mathrm{d}V_{\mathrm{bc}}} \approx \frac{\tau_{\mathrm{R}} I_{\mathrm{S}}}{V_{\mathrm{T}}} e^{\frac{V_{\mathrm{bc}}}{V_{\mathrm{T}}}}, \tag{5.3}$$

[5] Extracting V_{bi} and V_{xi} is not trivial, since most of the parasitic resistances are also voltage-dependent. Some resistance values need to be considered constant for achieving the convergence of simulations.



(a) C_{bc} in SG13S (b) C_{be} in SG13S



(c) C_{bc} in SG13G2 (d) C_{be} in SG13G2

Figure 5.2: Simulated parasitic capacitances of IHP SG13S and SG13G2 technologies. The size of HBT is one multiplier; one multiplier stands for emitter area of 0.1 µm^2 and 0.063 µm^2, for SG13S and SG13G2, respectively.

where q_{TC} is the minority stored charge in the base-collector junction, i_{EC} is the reverse current when base-collector junction is forward-biased and I_S is the saturation current. Likewise, the base-emitter diffusion capacitance ($C_{be,D}$) is

$$C_{be,D} = \frac{\partial q_{TE}}{\partial V_{be}} \approx \frac{\tau_F I_S}{V_T} e^{\frac{V_{be}}{V_T}}, \tag{5.4}$$

where τ_F is the forward transit time.

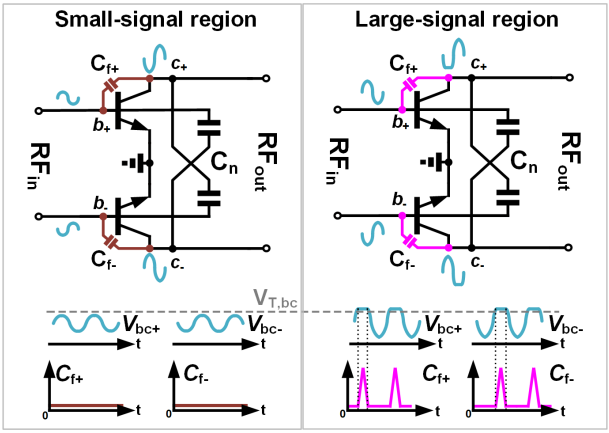
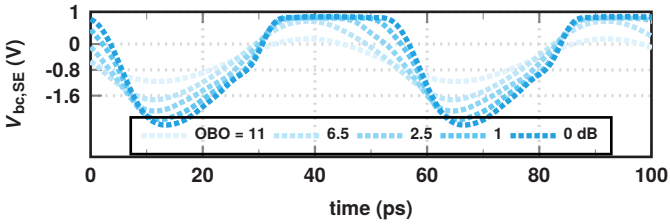


Figure 5.3: Nonlinear base-collector feedback capacitance (C_f) effect in an HBT CE pseudo-differential pair. In the small-signal region, depletion capacitance is predominant and can be counteracted by the neutralization capacitance (C_n). In the large-signal region, diffusion capacitance ($C_\mathrm{bc,D}$) becomes dominant, rendering C_n ineffective [1]. © IEEE.

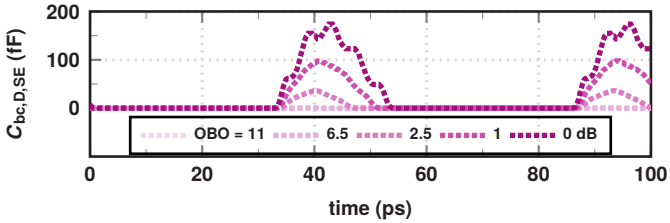
For quantification of practical values of the various nonlinear capacitance, parameters from the VBIC models of IHP SG13S and SG13G2 nodes are extracted and applied in the equations (5.2), (5.3) and (5.4). The size of the npn-HBT is one multiplier (M) and the simulation results are shown in Figure 5.2. As can be seen, by virtue of exponential functions, diffusion capacitance values grow more dramatically as the forward-biased voltage values exceed $0.7-0.8$ V.

Next, we discuss how the nonlinear capacitors react to the dynamics of an amplifier. Let the HBT in the amplifier (Figure 5.1(a)) be in forward-active region, which implies $V_\mathrm{CE} > V_\mathrm{BE}$. In the quiescent state, $C_\mathrm{be,J}$, $C_\mathrm{bc,J}$ and $C_\mathrm{be,D}$ are non-zero. However, since the base-collector junction is reverse-biased, $i_\mathrm{EC} \approx 0$ in equation (5.3) and thus $C_\mathrm{bc,D} \approx 0$. Subsequently, when driven with a small RF signal, the modulation of the capacitances begins but remains small; $C_\mathrm{bc,D} \approx 0$ remains. As the amplifier operates in the large-signal region and exhibits gain compression, the HBT has excursion in the saturation region. This makes $C_\mathrm{bc,D}$ become non-zero, since the base-collector junction experiences forward-bias.

For gaining more insight, HBTs from IHP SG13S are used and the base and collector voltage waveforms at 18.8 GHz are simulated. A testbench is based on



(a)



(b)

Figure 5.4: Nonlinear base-collector diffusion capacitance effect. Single-ended (SE) waveforms of (a) simulated V_{bc} values and (b) the resulting nonlinear $C_{bc,D}$ values at different OBO levels at 18.8 GHz. PAE peaks at the OBO of 0 dB. DC bias: V_{BE}=0.88V, V_{CE}=1.5V [1]. © IEEE.

the pseudo-differential pair shown in Figure 5.3, biased with V_{BE} of 0.88 V and V_{CE} of 1.5 V. The output (RF_{out}) is matched to optimal impedance for maximum output power from a load-pull simulation; the input (RF_{in}) is conjugate matched for the small-signal region. Neutralization capacitors (C_n) are employed to counteract the base-collector feedback capacitance C_f in the small-signal region. With the P_{in} ranging from −20 to −3 dBm, corresponding to the OBO levels from 0 to 11 dB, the single-ended (SE) V_{be} voltage swing is within 250 mVpp. In contrast, the SE V_{bc} swing can go up to 3.3 Vpp, as shown in Figure 5.4(a). According to the VBIC model of the devices and (5.2), with both junction exponential factors (values of m) smaller than 0.3, both $C_{be,J}$ and $C_{bc,J}$ vary within 2 fF (see Figure 5.2).

As for $C_{bc,D}$, the corresponding values are calculated using (5.3) and depicted in Figure 5.4(b). It can be observed that at OBO of 2.5 dB, the HBT already experiences a fraction of $V_{bc} > 0$ in one period, indicating forward-biased

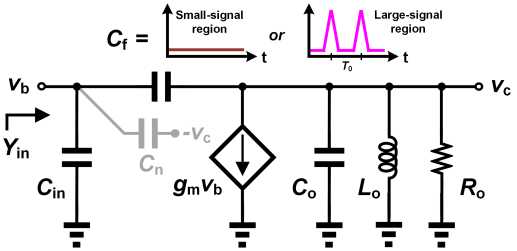


Figure 5.5: A simplified single-ended equivalent model of a SiGe-HBT CE RF amplifier with capacitive neutralization for both small- and large-signal conditions. Due to the nonlinear $C_{bc,D}$, the constant C_n fails to cancel out the C_f in the large-signal region [1]. © IEEE.

base-collector junction. However, due to the coefficient $\frac{\tau_R I_S}{V_T}$ being in the order of 10^{-26} to 10^{-25} in this technology, $C_{bc,D}$ becomes noticeable only when V_{bc} exceeds a certain voltage threshold $V_{T,bc}$, which is roughly 780 mV here. Starting from the OBO of 2.5 dB, triangular pulse trains appear and at the OBO of 0 dB, where power-added-efficiency (PAE) peaks, the maximal $C_{bc,D,SE}$ reaches 170 fF. It can also be seen that the duty cycle of the $C_{bc,D,SE}$ pulse waveform increases with higher gain compression levels as the HBT operates longer in the deep saturation region within each period (Figure 5.4). Concerning $C_{be,D}$, a direct comparison of (5.3) and (5.4) implies that $C_{be,D}$ is smaller than $C_{bc,D}$, due to the much smaller swing of V_{be}. In addition, τ_F is typically smaller than τ_R in an HBT technology. For instance, when considering temperature effects, in IHP SG13S,

$$13\tau_F \lessapprox \tau_R \lessapprox 15\tau_F. \tag{5.5}$$

In brief, the $C_{bc,D}$ is more pronounced than the $C_{be,D}$.

5.1.2 Stability Analysis of CE RF Amplifiers with Nonlinear Base-Collector Diffusion Capacitance Effect

Figure 5.5 is a generic circuit model of a CE amplifier with capacitive neutralization, which also serves as the half-circuit model of a pseudo-differential pair. Only nonlinear C_f is considered due to the smaller variation of C_{in}, as previously discussed. With a specific large-signal driving signal at angular frequency of ω_0, the C_f resembles a triangular pulse train from $C_{bc,D}$, as demonstrated

in Figure 5.4(b). Since C_f becomes non-constant, deriving the input admittance (Y_{in}) in the frequency domain is challenging. Instead, we can describe the circuit in the time domain by first approximating[6] this C_f as

$$C_f \approx \frac{C_1}{1 + m\cos(\omega_0 t)} \tag{5.6}$$

for the triangular pulse train, with appropriate values of C_1 and m, both of which depend on the driving power P_{in}. For example, to model the spike of 170 fF at OBO level of 0 dB in Figure 5.4(b), $C_1 \approx 34$ fF and $m \approx 0.8$ are found for equation (5.6). Then, to proceed with the time-domain derivation based on Figure 5.5 at a fixed large driving power, we assume $\frac{v_c}{v_b} = -g_m R_o$ and $g_m R_o \gg 1$. This allows us to express a second-order differential equation in terms of v_b as

$$\frac{d^2 v_b}{dt^2} + \frac{1}{(C_f + C_o)L_o} v_b = 0. \tag{5.7}$$

Substituting (5.6) into (5.7), the coefficient of the term v_b becomes $\frac{2\pi}{\omega_0}$-periodic and expressed as

$$\frac{1}{(C_f + C_o)L_o} = \frac{1}{L_o C_o} \frac{1 + m\cos(\omega_0 t)}{1 + \frac{C_1}{C_o} + m\cos(\omega_0 t)}. \tag{5.8}$$

With this periodic coefficient, equation (5.7) becomes a Hill's equation, a generalized Mathieu's equation [JS07, KRS18]. Based on Floquet theory, half-frequency ($\omega_0/2$) oscillation is facilitated in the solutions for v_b. In reality, considering additional circuit components (e.g., input matching network and more parasitic components) in the circuit model of Figure 5.5, the circuit complexity readily becomes high. With the periodic modulation of the $C_{bc,D}$ under large-signal conditions, the corresponding Hill's and Mathieu's equation turn higher-order, which facilitates other lower-frequency sub-harmonic (e.g., $\omega_0/3$, $\omega_0/4$, $\omega_0/5$) oscillations in the solutions [BB19, JS07]. Given the high circuit complexity of a practical RF PA design, which includes various passive components and parasitics, these higher-order differential equations are challenging to solve analytically. Therefore, we rely on numerical HB-based mixer-like

[6] This approximation was first introduced in [Loh66] for modeling junction capacitance. In this work, we explicitly use it for modeling diffusion capacitance, as junction capacitance typically represents depletion capacitance in literature [GHL09, MSB+96].

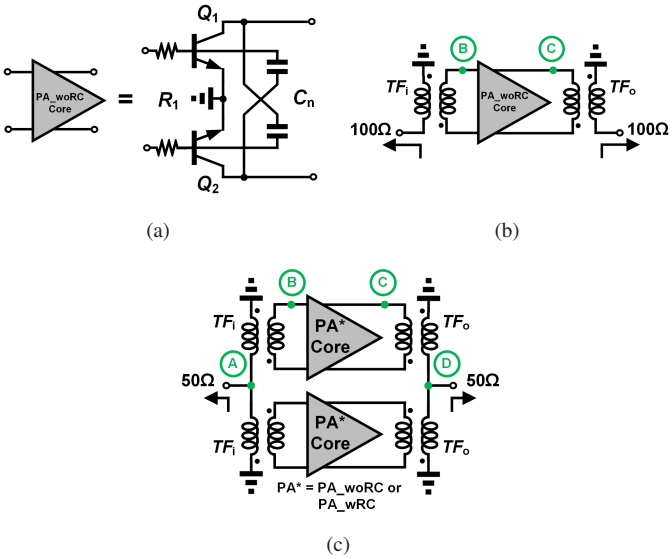


Figure 5.6: (a) Core of the PA_woRC[7], where no RC network is included at the base, compared to Figure 4.1. Location marks of stability simulations of (b) the unit PA of the PA_woRC and (c) both the power-combined PAs, with and without the RC network [1]. © IEEE.

simulations, as elaborated in Section 2.5.2, to verify the derived theoretical impact of $C_{bc,D}$, detect possible low-frequency instabilities in the large-signal region and design stabilization networks.

5.1.3 Verification of the Nonlinear $C_{bc,D}$ Effect on Large-Signal Stability

For verification of the actual nonlinear $C_{bc,D}$ impact on PA in simulation, the *K*u-/*K*a-band SiGe PA design example from Section 4.1.1 is utilized. As shown in Figure 5.6(a), the RC stabilization network at the base is removed for in-

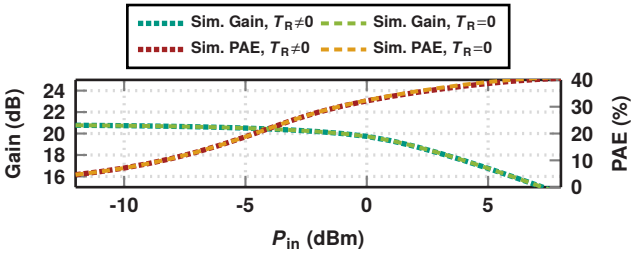
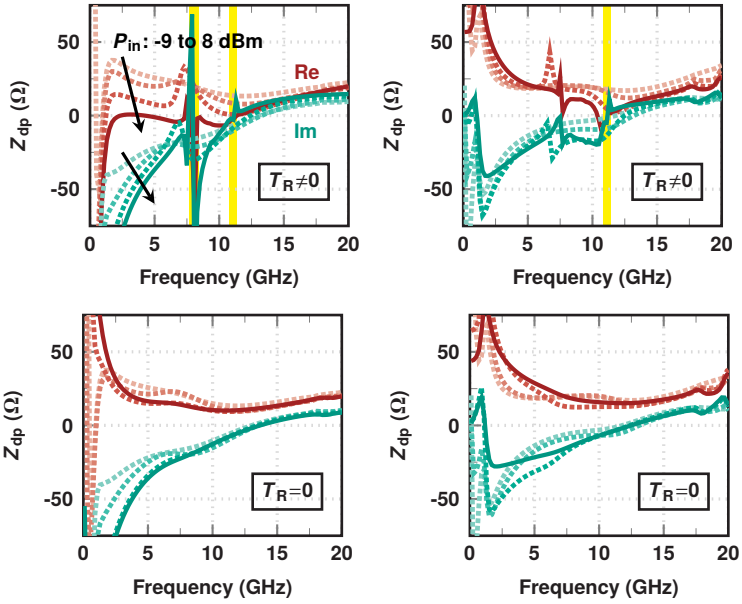


Figure 5.7: Simulated 18.8 GHz CW large-signal sweep of the unit PA, as shown in Fig. 5.6(b). By setting the T_R as default or zero value, the difference between the simulation results is marginal [1]. © IEEE.

tended possible instability[7]. For simplicity, the unit-PA with both input/output 100-Ω terminations is analyzed, as illustrated in Figure 5.6(b). Z_{dp} and Y_{dp}, as elaborated in Section 2.5.2, are examined at sensitive locations in the circuit. Locations Ⓑ and Ⓒ representing the interfaces between transformers and base/collector terminals, are checked. By setting the reverse transit time T_R as default (non-zero) or to zero value in VBIC model, if follows from (5.3) that the $C_{bc,D}$ effect can be controlled in simulations[8]. By 2-port HB simulations, with the driving signal at 18.8 GHz and different P_{in} values, the large-signal sweep simulation results are shown in Figure 5.7, which show that the T_R has little effect. Meanwhile, there is no sign of oscillation from the simulation. However, when the auxiliary sources are adopted with the HB simulator, an impact of T_R on the stability is clearly demonstrated through a Z_{dp} test in Figure 5.8. Instabilities are shown when T_R maintains its default (non-zero) value, where oscillation conditions (2.8) are met in a few frequency regions, highlighted in yellow. The instabilities are found at near 7.5 GHz and 11.2 GHz in the Z_{dp} tests at locations Ⓑ and Ⓒ. These frequencies correspond to $2\omega_0/5$ and $3\omega_0/5$ sub-harmonics. If T_R is set to zero, conditions (2.8) are never fulfilled in these frequencies. In parallel, in Y_{dp} tests, the similar instability is detected when T_R is default, as shown in Figure 5.9. However, compared to Figure 5.8, we can observe that the instability happens earlier at a lower P_{in} level. If T_R is set to zero, no instabilities are found, according to oscillation conditions (2.9).

[7] This PA version is named PA_woRC for comparison with the stable PA version PA_wRC shown in Section 4.1.1 and Figure 4.1.

[8] $T_R \approx \tau_R$.



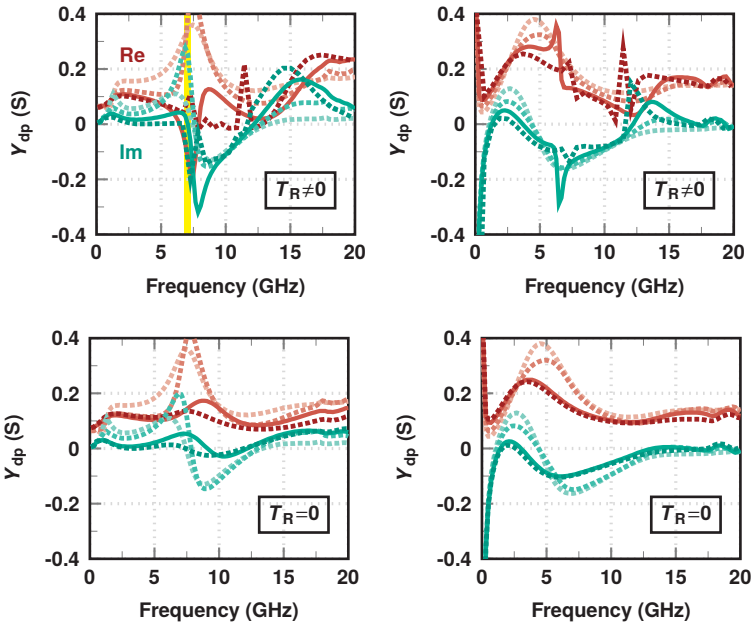
(a) @location Ⓑ (b) @location Ⓒ

Figure 5.8: Verification of the nonlinear $C_{bc,D}$ effect: simulated real and imaginary parts of Z_{dp} of the unit-PA with 18.8-GHz driving signal at different P_{in} levels and at different locations Ⓑ and Ⓒ (see Figure 5.6(b)). When T_R is default and non-zero, $C_{bc,D}$ induces instability and the oscillation conditions (2.8) are met, highlighted in yellow. When $T_R = 0$, there is no sign of instability. The solid lines represent the corresponding P_{in} level, where instabilities occur. Red: real part; green: imaginary part [1]. © IEEE.

In summary, both Z_{dp} and Y_{dp} simulations verify that the decisive role of T_R and equivalently the $C_{bc,D}$ in large-signal oscillations of the SiGe-HBT PA is evident.

5.1.4 Case Study for RC Stabilization Network Design

Here, both power-combined PAs, as depicted in Figure 5.6(c), are compared in terms of stability. Stability checks are performed at different locations over all center frequencies and all input power (P_{in}) levels. As illustrated in Figu-

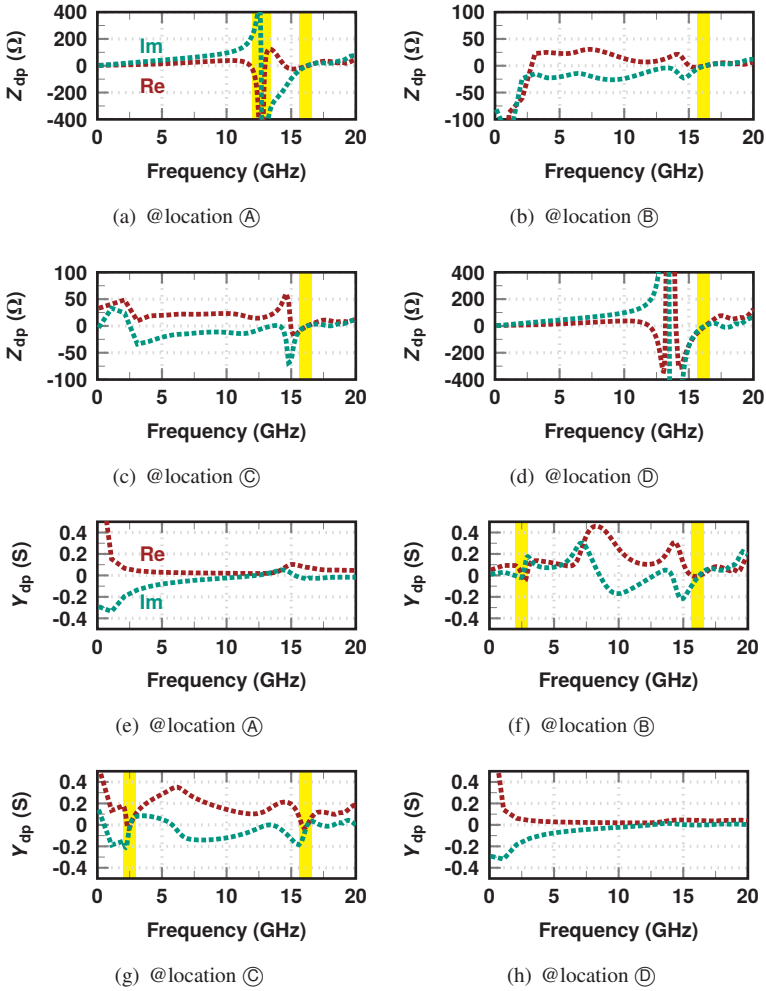


(a) @location Ⓑ (b) @location Ⓒ

Figure 5.9: Verification of the nonlinear $C_{bc,\,D}$ effect: Y_{dp} simulations, the counterpart of Fig. 5.8. Oscillation conditions (2.9) are applied and instability is highlighted in yellow. The solid lines represent the corresponding P_{in} level where instabilities occur. Red: real part; green: imaginary part [1]. © IEEE.

re 5.6(c), Ⓐ and Ⓓ are checked extra for the input and output, respectively. This subsection explains the design procedure of the RC stabilization network, cohering with other design details already stated in Section 4.1.1.

First, PA_woRC is examined and Figure 5.10 presents the analysis results. The Z_{dp} and Y_{dp} tests show no instability in the small-signal region until P_{in} exceeds 1.3 dBm at 18.8 GHz, which corresponds to roughly 2.3-dB OBO level. Z_{dp} tests demonstrate the instability at 16 – 16.5 GHz in all locations (Ⓐ to Ⓓ). Furthermore, Figure 5.10(a) shows additional instability at 12.8 – 12.9 GHz.



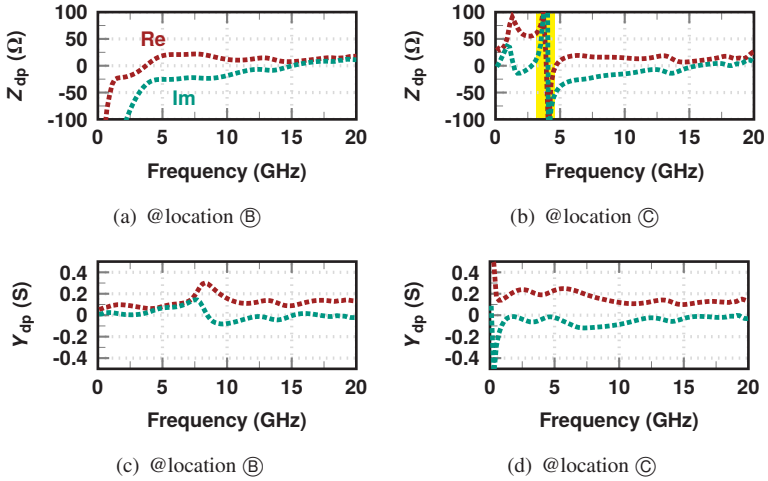
(a) @location Ⓐ (b) @location Ⓑ

(c) @location Ⓒ (d) @location Ⓓ

(e) @location Ⓐ (f) @location Ⓑ

(g) @location Ⓒ (h) @location Ⓓ

Figure 5.10: Simulated Z_{dp} ((a)-(d)) and Y_{dp} ((e)-(h)) of the PA_woRC at the onset of instability with 1.3-dBm P_{in} at 18.8 GHz (corresponding to roughly 2.3-dB OBO level). For Z_{dp} and Y_{dp}, the frequency ranges meeting the oscillation conditions (2.8) and (2.9) are highlighted in yellow. Red: real part; green: imaginary part [1]. © IEEE.



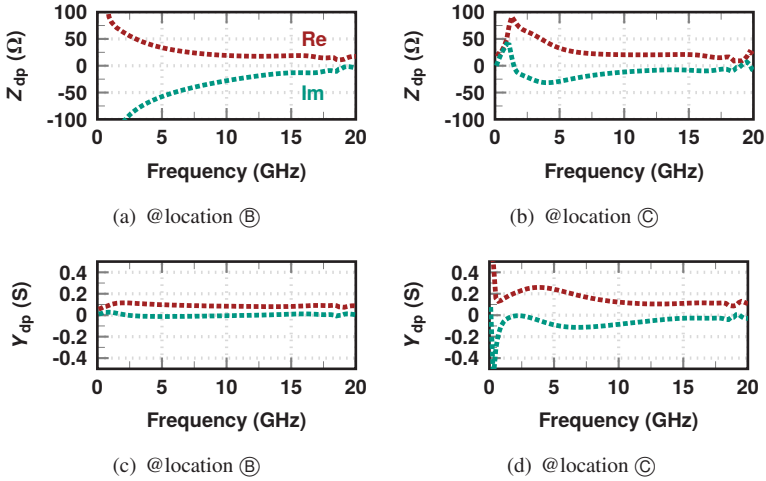
(a) @location Ⓑ (b) @location Ⓒ

(c) @location Ⓑ (d) @location Ⓒ

Figure 5.11: Simulated Z_{dp} and Y_{dp} of the power-combined PA with PA_woRC core, with R_1 increased to 7Ω (see Fig. 5.6(a)) to improve stability at the expense of a 3-dB reduction in small-signal gain. Despite this adjustment, stability is not ensured across the entire dynamic range: when P_{in} is increased to 8 dBm at 18.8 GHz, the oscillation conditions (2.8) are met again and highlighted in yellow in (b). P_{in} of 8 dBm corresponds to 6-dB GC level, where PAE peaks. This indicates that the damping network with only R_1 is ineffective. Red: real part; green: imaginary part [1]. © IEEE.

Figure 5.10(b) indicates large negative resistance at lower-frequency range, whereas there is no zero-crossing in reactance, which means the oscillation conditions are not satisfied. In parallel, from Y_{dp} tests at location Ⓑ and Ⓒ, oscillation conditions are fulfilled at 2.5 – 2.6 GHz and 16 – 16.5 GHz in Figure 5.10(f) and (g), while at location Ⓐ and Ⓓ, no clear instability is shown. We can observe from the simulation results that, instabilities at 12.8 – 12.9 GHz and 2.5 – 2.6 GHz are only shown in either Z_{dp} or Y_{dp} tests. This emphasizes the importance of use of both branch and node analyses.

To stabilize the PA_woRC, a straightforward way is to increase the R_1 in the schematic of Figure 5.6(a), which helps increase the damping factor of a feedback loop formed by the nonlinear $C_{bc,D}$. When a 3-dB compromise of in-band gain reduction is made, R_1 needs to be increased to 7 Ω. However, this measure does not ensure stability across the entire dynamic range. By the tests of Z_{dp}



(a) @location Ⓑ (b) @location Ⓒ

(c) @location Ⓑ (d) @location Ⓒ

Figure 5.12: Simulated Z_{dp} and Y_{dp} of the power-combined PA with PA_wRC core, where additional RC network at the input is applied and R_1 is 1.4Ω (see Fig. 4.1(b)). Compared to Fig. 5.11, there is also a 3-dB reduction in small-signal gain, but stability is maintained across the entire dynamic range. At the same P_{in} level of 8 dBm, where PAE peaks, the oscillation conditions (2.8) and (2.9) are no longer met, demonstrating the effectiveness of the RC damping network. Red: real part; green: imaginary part [1]. © IEEE.

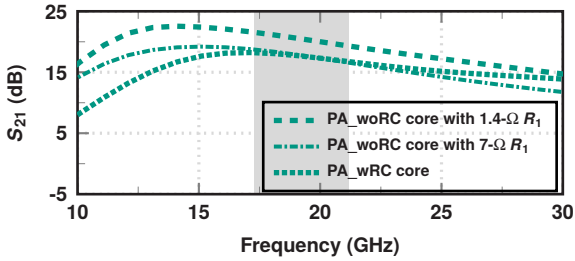


Figure 5.13: Comparison of simulated S_{21} values of power-combined PAs with different stabilization network designs at the input (see Fig. 5.6(a), (c) and Fig. 4.1(b)). A 3-dB compromise is made for stability within the target 17.3 – 21.2 GHz (highlighted in gray). The discussions of the stabilization networks are provided in Fig. 5.11 and 5.12 [1]. © IEEE.

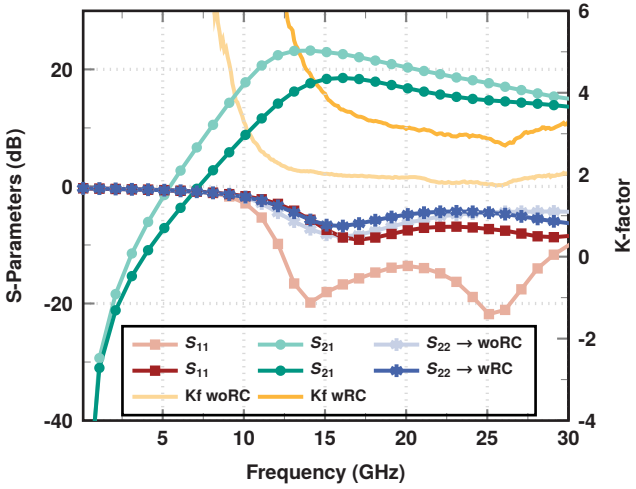


Figure 5.14: Measured S-parameters and K-factor of the unstable example PA_woRC and the stable PA_wRC. The results show that both PAs are stable in the small-signal region [1]. © IEEE.

and Y_{dp} at location Ⓑ and Ⓒ, instability is found again in Z_{dp} at near 5 GHz with 8-dBm P_{in}, as depicted in Figure 5.11(b). This P_{in} level corresponds to 6-dB gain compression level, where PAE peaks.

For avoiding further gain reduction by merely increasing R_1, the empirical RC high-pass network is adopted for PA_wRC. The values of R and C are selected based on Z_{dp} and Y_{dp} tests across the entire P_{in} range, low frequency range and bias variations. Finally, $R = 40\Omega$ and $C = 750fF$ are chosen to completely eliminate oscillation conditions. Figure 5.12(a)-(d) show no further instability at the displayed P_{in} level, where PAE peaks. For brevity, here we do not report all results from different P_{in} levels and checking locations, although they were all examined before the PA was taped out. In addition, the in-band gain compromise of 3 dB is maintained as shown in Figure 5.13. Due to the high-pass function of the RC network, PA_wRC exhibits greater gain degradation at lower frequencies compared to the design with only a 7-Ω R_1.

CW Experimental Comparisons – A Verification of Effectiveness of the Stability Check Method

As the first design iteration, the PA_woRC was fabricated, measured and compared with the PA_wRC. The experimental results are provided for the comparison and the stability study. In S-parameters at 17.3 – 21.2 GHz as shown in Figure 5.14, PA_woRC achieves gain of 19.6 – 22.0 dB while PA_wRC achieves gain of 16.1 – 18.3 dB. In comparison, PA_wRC has 3 – 4 dB decrease of gain in the targeted band. Both PAs are stable in small-signal operation and the K-factors are also greater than unity. Under large-signal operation at 18.8 GHz, PA_woRC begins to exhibit large-signal oscillation when P_{in} exceeds 2.5 dBm. The large-signal sweep is shown in Figure 5.15, where the bifurcation point is observed at a P_{out} of 20.5 – 21.5 dBm.

Spectra at the output of the PA_woRC are shown in Figure 5.16. We can see that in small-signal operation, no spurious signals are found in the lower-frequency region, while they appear when the PA is further driven. Oscillations are found at 10.2 – 10.9 GHz, 12.8 – 13.5 GHz and 15.9 – 16.2 GHz. Compared to the simulated results shown Figure 5.10, the oscillation frequencies are rather accurately predicted in simulation. The measurement results also validate the remark we made about the oscillation conditions in Section 2.5.2. Specifically, the negative slope of X_{T} at 12.8 – 12.9 GHz in Figure 5.10(a) also results in oscillations in the measurement. Moreover, no oscillation at 2.5 – 2.6 GHz is observed in the measurement. This can be explained that the low-frequency spurs are readily filtered out by the output transformer. However, mixed spurious components of 2.5 – 2.6 GHz and 12.8 – 12.9 GHz are found in the measurement where spurs at 10.2 – 10.9 GHz appear in Figure 5.16(b).

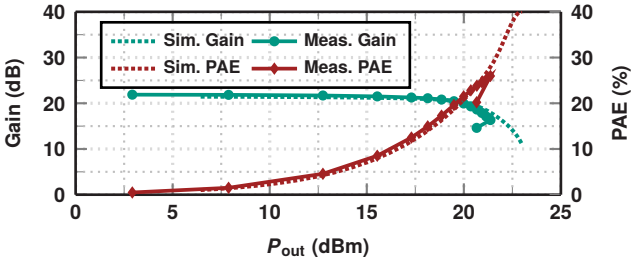
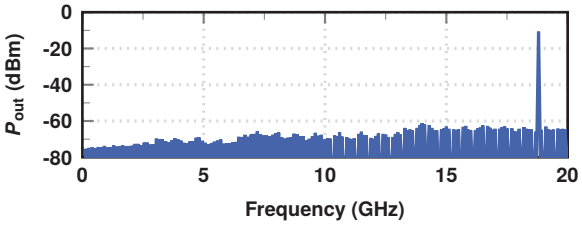
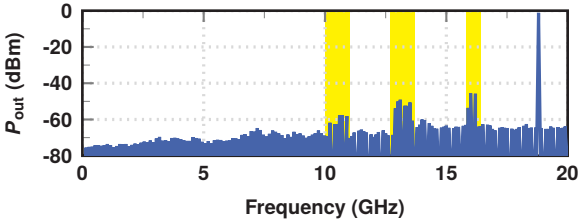


Figure 5.15: Simulated and measured CW large-signal sweep of the the unstable example PA_woRC at 18.8 GHz [12]. © IEEE.

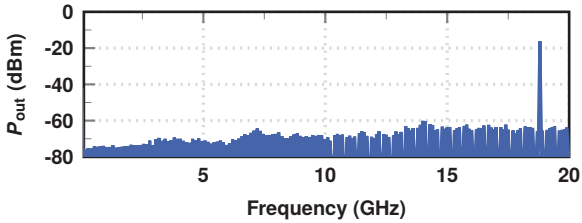


(a) P_{in} = -10 dBm (at 0-dB gain compression)

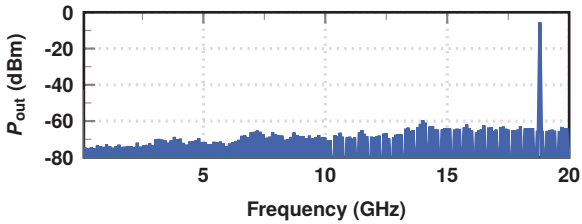


(b) P_{in} = 2.5 dBm (at ≈1-dB gain compression)

Figure 5.16: Measured output spectra of the unstable example PA_woRC with different P_{in} levels at 18.8 GHz: (a) in small-signal region, (b) at the onset of instability. In the small-signal region, the PA is stable, while instability appears when P_{in} exceeds 2.5 dBm. The oscillation frequencies highlighted in yellow show close agreement with those observed in the simulation (see Fig. 5.10). Note that the spectra include the losses from a 110 cm cable and a 10 dB attenuator [1]. © IEEE.



(a) P_{in} = -6 dBm (at 0-dB gain compression)



(b) P_{in} = 6 dBm (at ≈1-dB gain compression)

Figure 5.17: Measured output spectra of the stable PA_wRC with different P_{in} levels at 18.8 GHz are shown. The PA remains stable across the entire dynamic range. For comparison with Fig. 5.16, the same gain compression levels are presented. Note that the spectra include the losses from a 110 cm cable and a 20 dB attenuator [1]. © IEEE.

After the stabilization RC network is applied, PA_wRC shows no oscillation over all dynamic range. The spectra are shown in Figure 5.17. Other detailed measurement results are already demonstrated in Section 4.1.1.

5.2 Broadband Common-Collector–Common-Base (CC–CB) PA with Enhanced and Desensitized Stability

This section presents a stability analysis of SiGe cascode PAs and proposes the use of a CC–CB configuration for broadband PA design, offering enhanced and desensitized large-signal stability.

5.2.1 Stability Assessment of a SiGe Cascode PA

The previous discussion on large-signal instability is based on CE PAs, where the modulation of the $C_{bc,D}$ in SiGe HBTs has been proven to be the cause. Furthermore, large-signal instability may occur in cascode PAs as well; a scrutiny is therefore required.

An example capacitive-neutralized pseudo-differential cascode PA using SG13G2 is shown in Figure 5.18(a). The collector quiescent current density (J_c) is selected as 15.2 mA/μm^2. Without loss of generality, a lossless parallel RL network represents the output load-pull optimal impedance (Z_{opt}) at the center frequency (f_c) and a lossy series RL network at the input represents the conjugate of S_{11} value at f_c, with the inductor having a quality factor (Q) of 10. Node analysis, assisted by an additional shunt auxiliary (Aux.) source in three-port harmonic-balance (HB) simulations, is performed between devices to acquire the Y_{dp}. As shown in Figure 5.18(b), the cascode PA is stable in small-signal region with Rollett's K-factor (Kf)>1; however, with driving signal at f_c of 28 GHz, Y_{dp} tests reveal instabilities at an OBO of 0 dB (i.e., at saturated power P_{sat}). At 10 – 15 GHz, the oscillation conditions are met. Notably, the traditional two-port large-signal simulation fails to detect this instability.

Stabilization Design with Broadband Considerations

As discussed in the previous Section 5.1.4, conventional stabilization networks involve adding an RC at the base to act as a high-pass filter, suppressing low-frequency components. And as we learned, selecting appropriate RC values is an empirical process and is sensitive to bias conditions. Last but not least, the high-pass response also reduces in-band gain due to its limited roll-off. As exemplified in Section 5.1.4, the narrow-band PA design requires a 3-dB in-band gain tradeoff to eliminate large-signal instability in the low-frequency range. This tradeoff is especially unsuitable for broadband PA designs. For instance, as presented in Figure 5.18(d), low-frequency instability occurs near 17 GHz, the lower bound of the target 17 – 30 GHz band. Ensuring complete suppression of instability may require an excessive gain tradeoff at 17 GHz, making the broadband design objective challenging. Therefore, exploring a topology without the

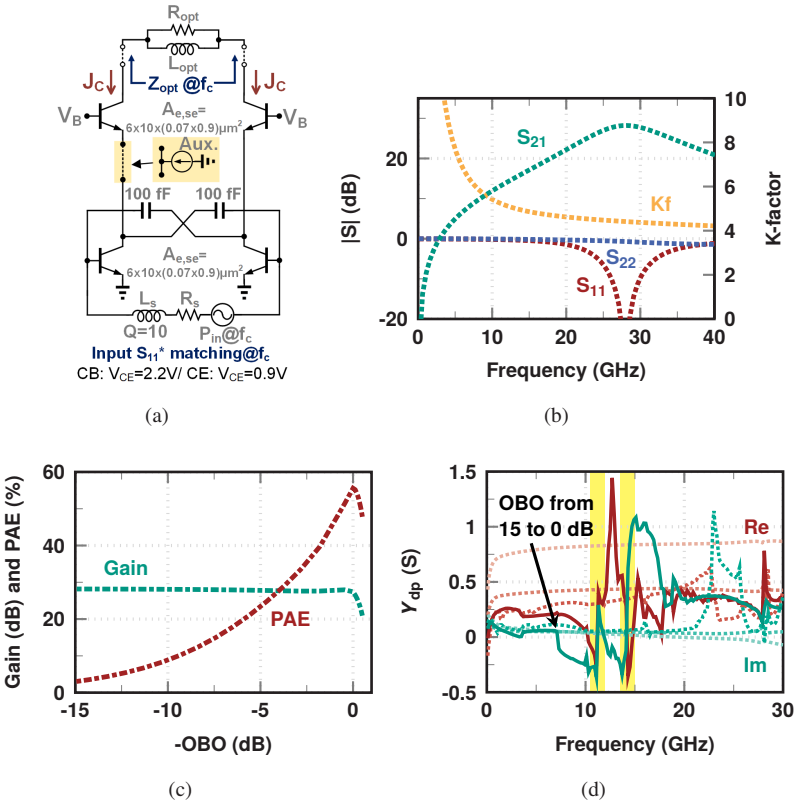


Figure 5.18: (a) A cascode PA example for Y_{dp} examinations and its (b) small- and (c) large-signal simulation results at 28 GHz. (d) The Y_{dp} tests imply instability at OBO of 0 dB [10]. © IEEE.

narrow-band passive RC network, while robustly maintaining stability, becomes a key goal.

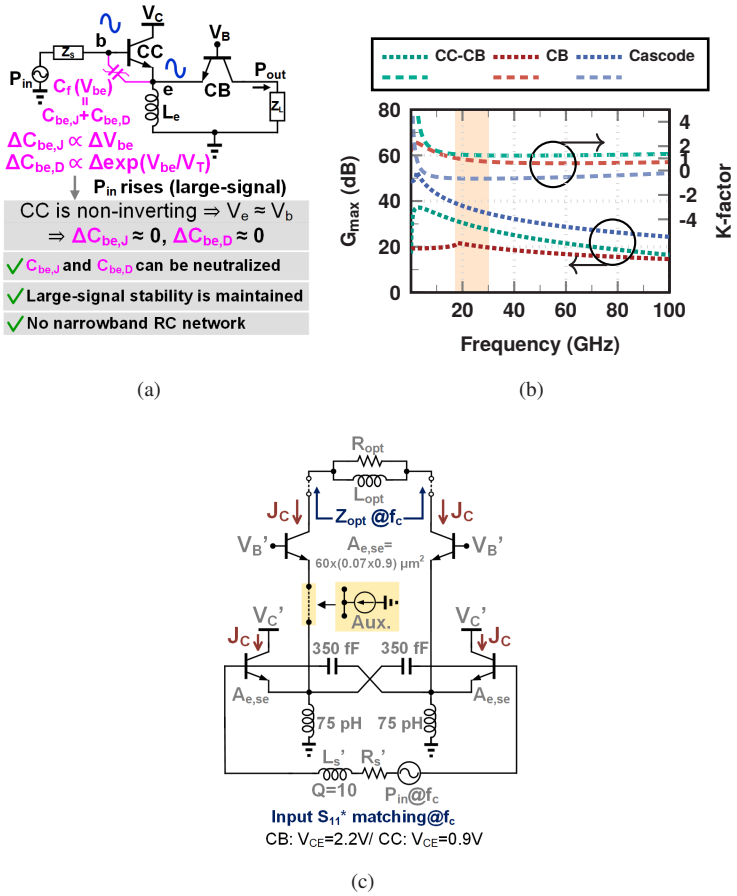


Figure 5.19: (a) Explanation for the adoption of a CC stage. (b) G_{max} comparison. (c) A CC–CB PA example compared to the cascode PA shown in Figure 5.18 [10]. © IEEE.

5.2.2 The Proposed CC–CB PA and Its Stability Assessment

For the aforementioned stability and broadband concerns, this work proposes using a common-collector (CC) stage to replace the CE stage and combining it

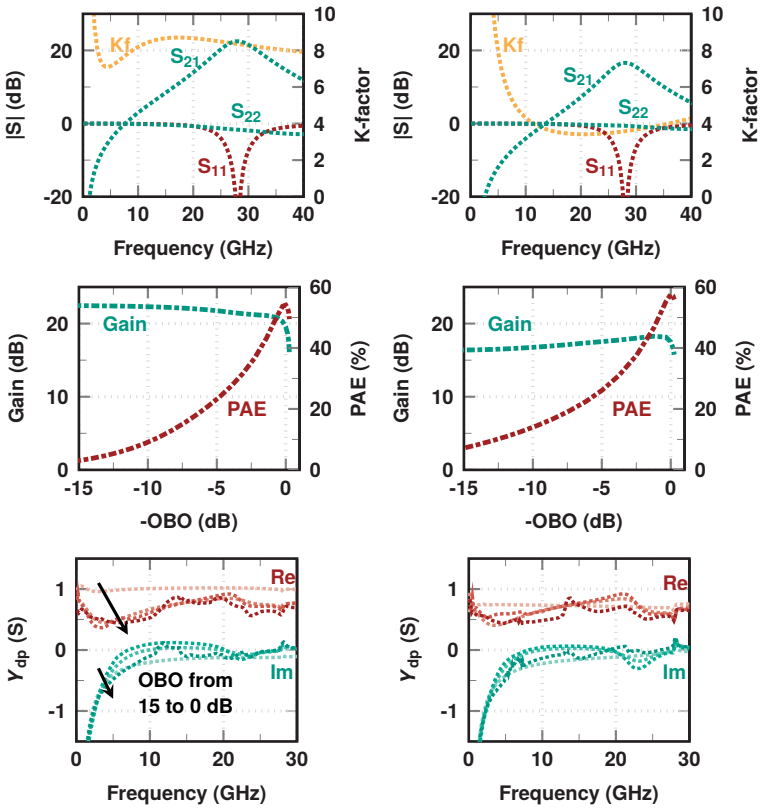


Figure 5.20: Simulation results of the Figure 5.19(c) with bias J_c of (a) 15.2 mA/µm^2 and (b) 3.2 mA/µm^2 [10]. © IEEE.

with a current-clamping CB stage. As illustrated in Figure 5.19(a), in the CC stage, the emitter voltage (V_e) closely follows the base voltage (V_b). Consequently, the base-emitter diffusion capacitance ($C_{be,D}$) and the corresponding C_f do not increase during large-signal operation. As a result, stability in both the small-signal and large-signal regions can be achieved simultaneously by desi-

gning a C_f neutralization network, eliminating the need for an RC stabilization network.

The maximum gain (G_{max}) of single-ended (SE) PAs for three topologies—the proposed CC–CB, cascode, and standalone current-clamping CB PAs—are firstly compared (Figure 5.19(b)). The emitter current-clamping inductor (L_e) is set to 75 pH based on 400-MHz IM3 simulations [RZSM19]. For a fair comparison, the SE emitter area ($A_{e,se}$) and the collector-emitter voltages (V_{CE}) of each HBT are kept consistent as 3.78 μm^2 and matched (V_{CE} of 2.2 V for CB and 0.9 V for CE/CC). J_c is still kept as 15.2 mA/μm^2 for each HBT. The results show that the CC–CB PA achieves at least 8 dB higher G_{max} than the standalone CB PA within the 17 – 30 GHz range, with a Kf>1, ensuring better small-signal stability compared to the other two topologies. For further large-signal evaluations, Figure 5.19(c) presents a capacitive-neutralized pseudo-differential CC–CB PA design. With the same J_c of 15.2 mA/μm^2 and output network, the CC–CB PA achieves the same P_{sat} and PAE values (25.5 dBm and 54%) as the cascode PA, despite having a 5.7 dB lower gain at 28 GHz (see Figures 5.20(a) and 5.18(c)). However, Y_{dp} tests reveal that the cascode PA suffers from large-signal instability and cannot achieve this P_{sat} and PAE performance in practice (Figure 5.18(d)). In contrast, the CC–CB PA remains free from large-signal instability across a range of OBO and J_c values. Figure 5.20(b) presents the results for a J_c of 3.2 mA/μm^2, indicating deep Class-AB operation and showing that the Y_{dp} values do not deviate significantly from those shown in Figure 5.20(a). The stability insensitivity to bias conditions in the CC–CB PA is beneficial for complex PA designs, such as Doherty PAs, where amplifiers with different bias conditions are employed.

5.2.3 Broadband CC–CB PA Design for 17–30 GHz

Figure 5.21(a)-(b) show the schematic of the proposed two-stage PA, where both stages utilize CC–CB pseudo-differential pairs. HBTs Q_1-Q_4 in the driver/PA stages are designed with $A_{e,se}$ of 2.02 μm^2/3.78 μm^2. The values of V_{CE} for the CC/CB devices are chosen as 0.9 V/2.2 V in the PA stage and 0.9 V/1.5 V in the driver (DV) stage. Bias circuits are integrated to provide the CTAT base bias voltage (V_B), as shown in Figure 5.21(c). Unlike those described in Section 4.1.1, the CTAT bias networks are laid out directly alongside the CC and CB devices for improved thermal coupling [JGC20]. The layout/EM view

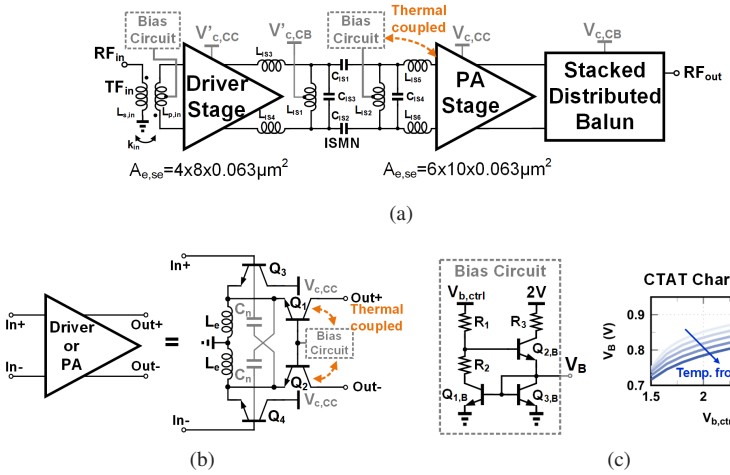
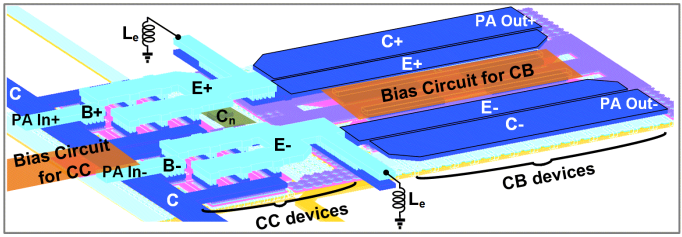


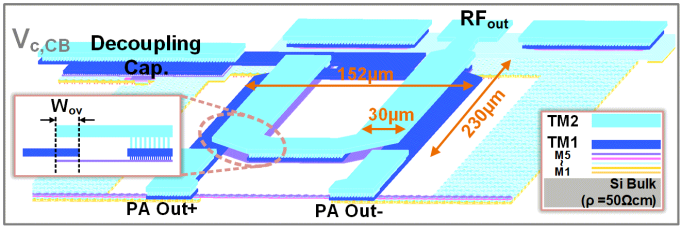
Figure 5.21: (a) Schematic of the proposed two-stage CC–CB power amplifier and (b) the detailed pseudo-differential pair. (c) CTAT bias network characteristic [10]. © IEEE.

of the PA stage is shown in Figure 5.22(a). In addition, R_2 and R_3 are used to avoid any instability loop formed with the amplifiers.

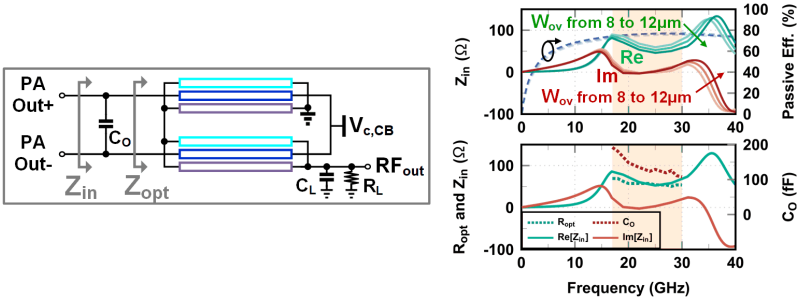
At the PA output, we propose a stacked distributed balun network, as shown in Figure 5.22(b)-(c), to present the broadband optimum load resistance (R_{opt}) given by the load line and to absorb the device output capacitance (C_O) under large-signal conditions. Due to a relatively low Si-bulk resistivity (ρ=50 Ωcm) in this technology, implementing a two-metal-layer distributed balun (such as the one used in SOI technology [WW21a]) is challenging. Instead, a stacked structure using the top three aluminum metals (TM1, TM2, and M5) is employed for better shielding and broadband coupling. TM1 is used for primary winding, connecting the CB devices, and sandwiched between the TM2 and M5, which serve as the secondary winding. The secondary winding is terminated with a load R_L of 50 Ω and a capacitance C_L of ≈170 fF, including the pad. The differential input impedance (Z_{in}) response is adjustable through the overlapping width (W_{ov}) of the stacked structure. Targeting maximum PAE, the simulated R_{opt} and C_O values over the 17 – 30 GHz range vary from 54 to 69 Ω and 110 to 190 fF, respectively. C_O values across the frequency range are used for the Re[Z_{in}] simulations. Accordingly, a W_{ov} of 10 μm is selected to keep



(a)



(b)



(c)

Figure 5.22: (a) Layout/EM view of the PA stage. (b) Layout/EM view of the output stacked distributed balun, and (c) its simplified diagram and simulated network responses [10]. © IEEE.

the deviation between the Re[Z_{in}] and R_{opt} within 20%, and the balun passive efficiency ranges from 73 to 78%. The interstage matching network (ISMN) incorporates two shunt inductors (L_{IS1} and L_{IS2}) and two series DC-block

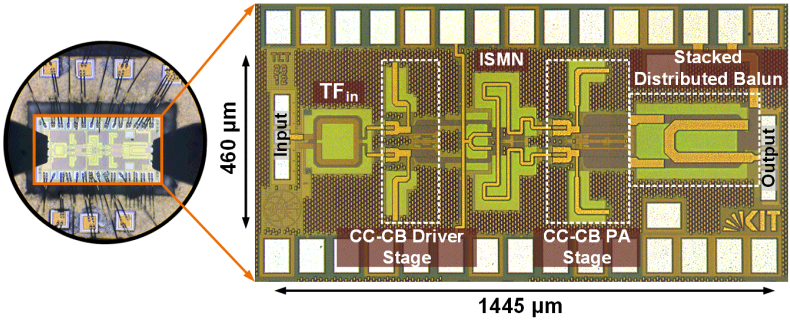


Figure 5.23: Die micrograph [10]. © IEEE.

capacitors (C_{IS1} and C_{IS2}) to provide the biasing for the DV CB and PA CC devices (Figure 5.21(a)). Together with other LC components ($L_{IS3\text{-}6}$ and $C_{IS3\text{-}4}$), the DV stage, and the input transformer (TF_{in}), S_{21} and S_{11} responses are co-designed. The ISMN design ensures that the DV stage delivers sufficient P_{1dB} to the PA stage for operations in the P_{sat} region.

The proposed CC–CB PA is prototyped, and Figure 5.23 shows the die micrograph. The core area, including RF pads, measures 0.67mm^2.

Experimental Results – CW

The J_c values of the CB devices in both the DV and PA stages are set to 15.2 mA/µm^2, while for the CC devices, they are set to 3.2 mA/µm^2. Measurements indicate no instability in either the small-signal or large-signal regions, confirmed by a spectrum analyzer connected to the output. No spurs and discontinuities were observed in the spectra and large-signal sweep results. The measured S-parameters and large-signal results are shown in Figure 5.24. The measured S_{21} ranges from 16.2 to 23.2 dB over 17 to 30 GHz, peaking at 18.3 GHz. The $S_{11}<-10$ dB bandwidth is from 19.9 to 26.8 GHz. The higher ripple in the S_{21} measurement is primarily due to variations in the output network, where deviations between simulated and measured S_{22} can be observed. Across the 17 – 30 GHz range, the measured P_{sat} varies from 19.3 to 23.3 dBm, with PAE_{max} ranging from 10.4 to 28.6%; P_{1dB} varies from 15.1 to 21.5 dBm, with PAE_{1dB} ranging from 6.0 to 22.1%. Despite the ripple in S_{21}, P_{sat} shows a

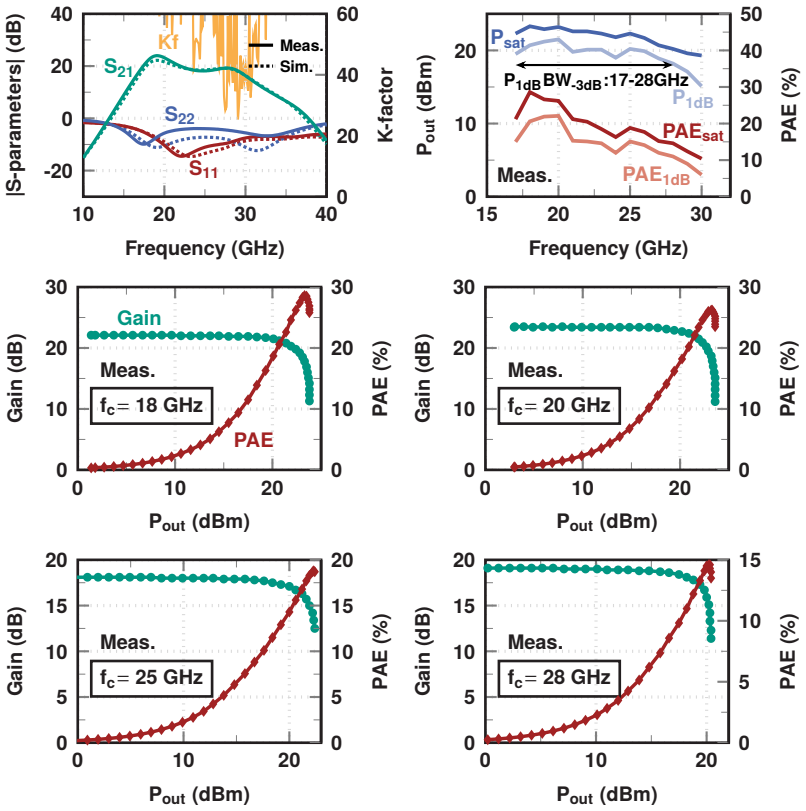


Figure 5.24: Small-signal and large-signal measurement results [10]. © IEEE.

relatively stable variation of 4 dB, and P_{1dB} has a $BW_{\text{-3dB}}$ from 17 to 28 GHz, with PAE_{1dB} ranging from 11.0 to 22.1%.

Experimental Results – Modulated Signals

The PA is further characterized using 400-MBd modulated signals (Figure 5.25). No DPD is applied. With a roll-off factor (α) of the raised-cosine filter of 0.25, the 32-APSK signal has an ≈8.2 dB PAPR. At 20 and 28 GHz, the

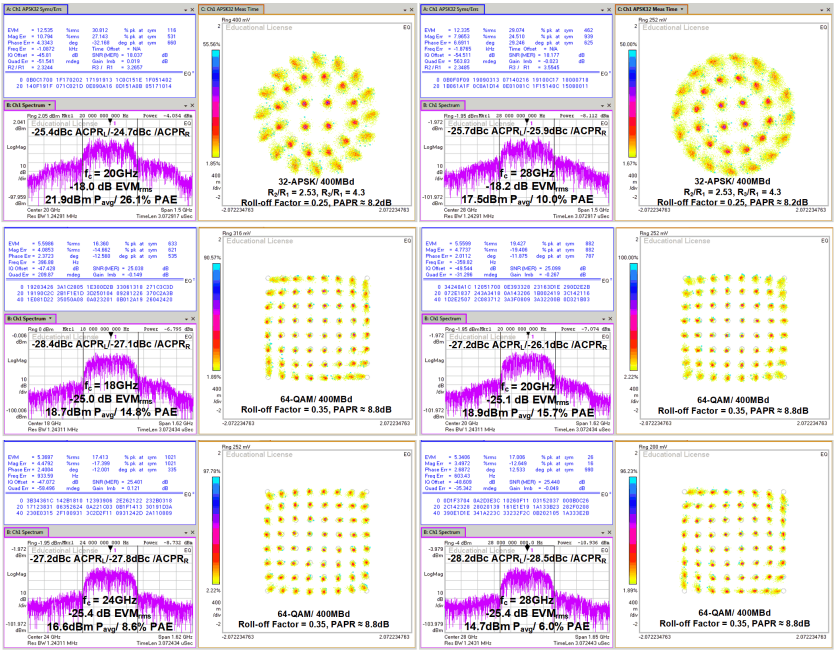


Figure 5.25: Modulation measurement results of the PA: 400-MHz single-carrier 32-APSK and 64-QAM signals [10]. © IEEE.

PA achieves average P_{out} (P_{avg}) of 21.9 and 17.5 dBm with PAE of 26.1% and 10.0%, respectively, at an EVM_{rms} of −18.0 dB. The ACPR is maintained below −25.0 dB. In addition, a 64-QAM signal with $\alpha = 0.35$ and PAPR ≈8.8 dB is used for evaluation from 18 to 28 GHz, showing P_{avg} values ranging from 14.7 to 18.9 dBm, with PAE from 6.0 to 15.7%. In comparison, for APSK signals, due to a relaxed EVM requirement [1], the PA achieves better performance.

5.2.4 Remark on Results

Focusing on large-signal stability enhancement, this work presents a broadband SiGe CC–CB linear PA. Table 5.1 summarizes the performance, along with the recent broadband works across 5 to 60 GHz [YHKJ24, LHJ24, KHL+23,

Table 5.1: Comparison with state-of-the-art broadband PAs across 5 − 60 GHz.

	This Work				[YHK+24]	[LHJ24]	[KHL+23]		[WW21b]	[6]	[ZGS+23]			[VR18]		[WW21a]		[GMW21]		[LLLW24]
Technology	130nm SiGe				130nm SiGe	130nm SiGe	90nm SiGe		130nm SiGe	130nm SiGe	28nm CMOS			28nm CMOS		45nm SOI		45nm SOI		16nm FinFET
Supply Voltage (V)	0.9 (DV-CC) & PA-CC)/ 1.5 (DV-CB)/ 2.2 (PA-CB)				1.8	3.6	2.4		2.0	3.2	0.9 (DV)/ 1.8 (PA)			0.9		2.0		1.9		1.6
Presented P_{sat} BW (GHz)	17–30				8.7–14.7	24–32	5–33		23–31	26–30	19.7–43.8			26–58		22–44		23–36		21–28
Freq. (GHz)	18	20	25	28	11.7	14.7	28	17	20	28	28	20	25	28	28	30	24	28	23	28	21	24
Gain (dB)	22.1	23.4	18.0	19.2	26.2	23.8	26.5	23.8	23.8	22.0	20.5	19.4	20.5	17.8		13.0	20.5	N/A	20.4	17.5	22.4
P_{sat} (dBm)	23.3	23.2	22.3	20.2	24.4	23.9	22.6	N/A		28.3	22.7	17.7	19.8	20.3	16.4	16.6	20.0	20.4	18.8	20.1	17.8	18.0
PAE_{max} (%)	28.6	26.6	18.8	14.6	32.1	26.2	40	N/A		30.4	38.1	18.0	32.2	33.6	23.8	24.2	38.9	45.0	35.0	48.3	25.1	31.0
P_{1dB} (dBm)	20.7	21.5	20.2	18.2	22.7	20.6	21.6	14.1	12.5	11.0	26.8	22.1	13.5	18.2	19.0	13.2	13.4	19.6	19.1	18.0	19.1	17.5	17.1
PAE_{1dB} (%)	20.6	22.1	15.1	11.0		N/A	N/A	23.0	17.7	10.0	30.2	35.2	9.5	26.2	29.7	12.0	12.6	38.9	42.5	32.5	45.5	24.9	29.2
Freq. (GHz)	20	28	20	28	11.7		28		24		28	28	20	25	28	28	32	24	28	28		24	25	
Modulation Scheme	32-APSK		64-QAM		DVB-S2X 64-APSK	5GNR 64-QAM OFDM	16-QAM		5GNR 64-QAM OFDM	64-QAM	5GNR 64-QAM OFDM			64-QAM		5GNR 64-QAM OFDM		5GNR 64-QAM OFDM		5GNR 64-QAM OFDM	
Symbol Rate (MBd)	400				250	400	400		200	800	200			500		400		200		100	400	
PAPR (dB)	8.2		8.8		7.4	9.7	6.6		9.6	8.3	9.7			8.3		9.6		9.6		9.6		
EVM (dB)	-18.0	-18.2	-25.1	-25.4	-25.0	-25.0	-26.8		-25.1	-25.2	-25.0	-25.1		-25.0		-25.4		-25.0		-25.1	-25.0	
ACPR (dB)	-24.7	-25.7	-26.1	-28.2	-25.2	-27.5	N/A		-28.8	-32.0	-22.0	-23.9		-23.9	-37.6	-34.2	-27.5	-29.6	-26.6	-27.6	-30.7	
P_{avg} (dBm)	21.9	17.5	18.9	14.7	18.6	15.6	34.7*		18.1	16.2	7.0	10.6	10.9	6.8	8.1	13.0	13.2	10.7		10.7	8.3	
PAE (%)	26.1	10.0	15.7	6.0	16.0	16.3	N/A		13.8	11.0	3.5	8.0	8.8	2.9	3.9	19.0	21.1	15.5		13.7	8.6	

*EIRP of a 16-element Tx phased array.

WW21b, ZGS+23, VR18, WW21a, GMW21, LLLW24, 6]. For the 17—30-GHz broadband purpose, this PA demonstrates a 17—28-GHz (49 %) P_{1dB} BW_{-3dB} and comparable or even higher P_{out}/PAE, including performance with modulation signals.

5.3 Chapter Conclusions

The chapter begins with a study investigating the impact of nonlinear capacitances in SiGe technology on the stability of PA designs for 17.3 – 21.2 GHz Satcom applications. Various nonlinear capacitances are considered and compared. Various nonlinear capacitance components are considered and compared. In particular, the pronounced influence of the nonlinear base-collector diffusion capacitance ($C_{bc,D}$) on the large-signal stability of PAs is analyzed and mathematically derived using simplified circuit models. Then the advanced stability analysis techniques based on HB are employed for verification and for the design of stabilization networks in a fabricated unstable PA.

Subsequently, a broader operating band of 17 – 30 GHz is targeted to support both Satcom and mobile applications. Based on the insights gained into stability behavior, enhanced and desensitized stability is established as a primary design objective, and the use of a CC–CB configuration is proposed. The implemented CC–CB PA demonstrates broadband stability and robust performance, achieving a 17—28-GHz (49 %) P_{1dB} BW_{-3dB}.

6 High-Speed Linear Optical Modulator Driver for Short-Reach Links

Parts of the following section were previously published in [7].

This chapter presents the design considerations and an illustrative example of a SiGe high-speed, linear optical modulator driver intended for short-reach optical backhaul links, which form a critical part of the infrastructure supporting modern wireless communication systems.

6.1 Design Considerations

High-speed optical transmit links deliver digital data first in the electrical domain, after which the data are transferred to the optical domain by optical

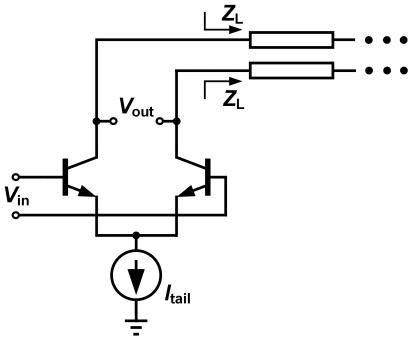


Figure 6.1: A generic current-mode modulator driver.

modulators. The output-stage amplifier (i.e., the modulator driver), which interfaces the electrical circuitry with the optical modulator, must provide broad bandwidth and sufficient output voltage swing according to the modulator type. The bandwidth requirement is outlined and elaborated in Section 1.2 and Figure 1.3. The design rationale for the target output voltage swing ($V_{\mathrm{out,TGT}}$) is discussed in Section 2.4.

Considering a generic current-mode modulator driver as shown in Figure 6.1, to reach $V_{\mathrm{out,TGT}}$, the required tail current I_{tail} must satisfy

$$I_{\mathrm{tail}} \geq \frac{V_{\mathrm{ppd,TGT}}}{2Z_{\mathrm{L}}}, \tag{6.1}$$

where $V_{\mathrm{ppd,TGT}}$ denotes the peak-to-peak differential value of $V_{\mathrm{out,TGT}}$. The term $\frac{V_{\mathrm{ppd,TGT}}}{2Z_{\mathrm{L}}}$ indicates the boundary for full switching, which is a useful reference for NRZ signals. However, for modulation formats requiring stricter linearity, such as PAM-4, an I_{tail} that merely meets this boundary is not sufficient. Moreover, $V_{\mathrm{out,TGT}}$ depends on the type of optical modulator. Conventional Mach–Zehnder modulators (MZMs) exhibit a high π-voltage (V_π), which consequently necessitates a large output swing from the driver, e.g., differential $4\,V_{\mathrm{pp}}$ [RGLA+17]. In contrast, silicon-organic hybrid (SOH) MZMs supporting 100-GBd operation have been demonstrated [UKA+21, KFZ+20], and their reduced V_π (e.g., single-ended $1.3\,V_{\mathrm{pp}}$ in [UKA+21]) significantly eases driver design and improves overall efficiency. Electro-absorption modulators (EAMs), which typically require low drive voltages as well—e.g., differential $2\,V_{\mathrm{pp}}$—are also widely adopted in high-speed EO systems [RLV+19].

6.2 Design of a 100-GBd Optical Modulator Driver in IHP SG13G2

This section presents key circuit design details and experimental results for a 100-GBd optical modulator driver implemented in IHP SG13G2.

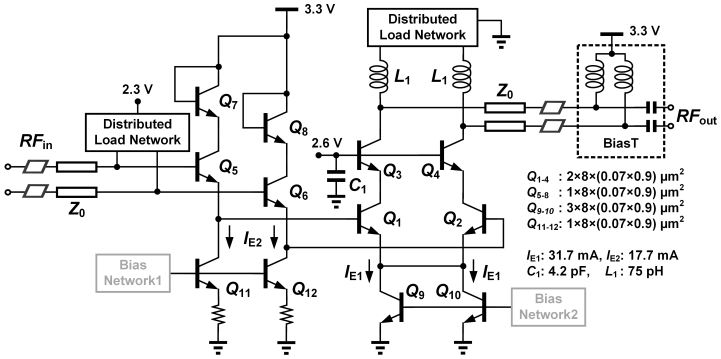
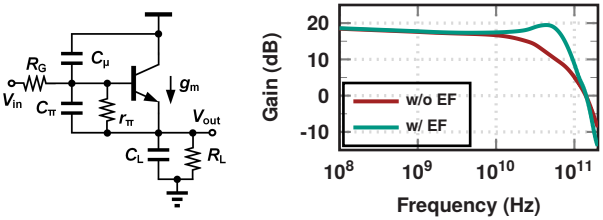


Figure 6.2: Schematic of the proposed 100-GBd modulator driver [7]. © IEEE.

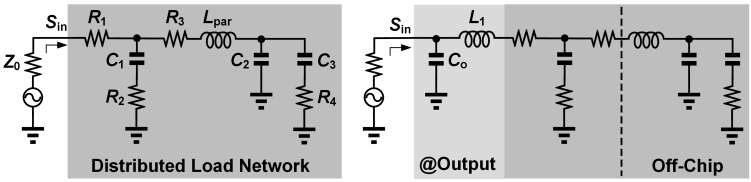


(a) (b)

Figure 6.3: (a) Small-signal model of an EF. (b) Improvement of the simulated bandwidth by a preceding EF [7]. © IEEE.

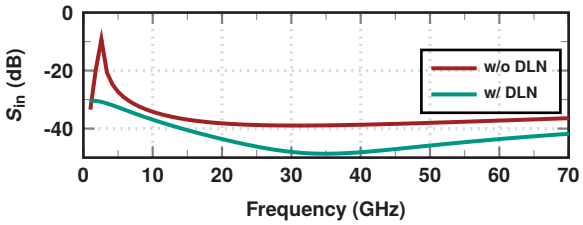
6.2.1 Circuit Design

The complete schematic is shown in Figure 6.2. The driver is composed of a cascode differential pair to minimize the Miller effect, as bandwidth is critical for 100-GBd data transmission. To account for packaging parasitics of the subsequent modulator, a near-end termination—used to absorb reflections [Beh12]—is implemented at the output. In addition, an open-collector topology is used to reduce power consumption. Considering EAMs or low-drive-voltage MZMs, and using (6.1) with a Z_L (and the near-end termination) of 50 Ω, the $V_{ppd,TGT}$ requirement is 2.5 V_{pp}-3.0 V_{pp}.

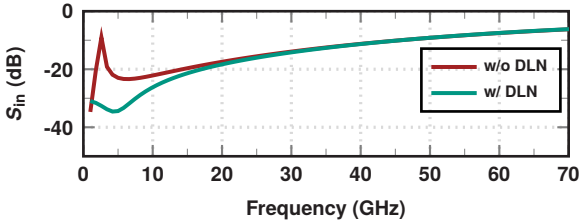


(a) (b)

Figure 6.4: (a) Distributed load network (DLN) and test benches for S_{in}. (b) Inclusion of output collector parasitic capacitance (C_o) and peaking inductance (L_1) [7]. © IEEE.



(a)



(b)

Figure 6.5: Simulated S_{in} with DLN (R_1 = 40Ω, R_2 = R_3 = 10Ω) and without DLN (R_1 = 50Ω, R_2 = R_3 = 0Ω). (a) Directly seen into the network. (b) Including C_0 and L_1 at the output. (See the test benches shown in Fig. 6.4.) [7], © IEEE.

In terms of bandwidth, because the input capacitance of the CE devices is large, the bandwidth is dominated by the input pole. It can be improved by selecting the cascode differential core (Q_{1-4}) to be slightly smaller than the

tail-current devices (Q_{9-10}). Furthermore, a preceding emitter-follower (EF) stage is adopted, serving as a buffer and extending the overall driver bandwidth [TKA+07]. The small-signal model of a capacitive-loaded EF is shown in Figure 6.3(a), exhibiting a second-order gain response with one zero and a pair of complex-conjugate poles. The natural frequency is given by

$$\omega_{\mathrm{n}} \approx \sqrt{\frac{g_{\mathrm{m}}}{R_{\mathrm{G}}[(C_\pi + C_\mu)C_{\mathrm{L}} + C_\pi C_\mu]}}, \tag{6.2}$$

which indicates that the gain-peaking frequency can be adjusted through I_{E2} and the device sizes of Q_{5-6}. A higher ω_{n} can be achieved with higher I_{E2}, but this reduces the damping factor [TKA+07] and increases DC power consumption. As shown in Figure 6.3(b), without EFs, the cascode differential pair suffers from a dominant input pole at 15.5 GHz in simulation. With the designed EF pair, this dominant pole is eliminated and replaced by a gain peaking at 44 GHz. The resulting 3-dB bandwidth extends to 78 GHz. It is worth mentioning that while distributed amplifiers have been investigated as a means to increase bandwidth and appear promising [RGLA+17, BHSV17, EAR19], they typically suffer from larger chip area and higher complexity. Especially for multi-channel optical transmitter integration, the smaller required chip area makes a lumped driver preferable; thus, an EF-based broadband driver remains competitive.

In parallel, to ensure the quality of a 100-GBd eye diagram, the near-end DC-block termination network including on-chip load, on/off-chip decoupling capacitors and parasitic effects must be carefully treated. As shown in Figure 6.2 and Figure 6.4, a distributed load network (DLN) is designed at the driver output. The on-chip part includes R_{1-3} and C_1, while C_{2-3}, R_4 and the parasitic L_{par} represent the off-chip decoupling network and package parasitics. In the DLN, the termination resistance (i.e., 50 Ω) is distributed into both $(R_1 + R_2)$ and $(R_1 + R_3)$, rather than implemented as a standalone R_1 (i.e., $R_2 = R_3 = 0$). In this design, $R_1 = 40\Omega$ and $R_2 = R_3 = 10\Omega$. For the decoupling network, $C_1 = 9.6\mathrm{pF}$, $C_2 = 120\mathrm{pF}$, $C_3 = 100\mathrm{nF}$, $R_4 = 5\Omega$ and L_{par} is estimated as 500 pH due to wire bonding.

Figure 6.4 also shows the test benches for input reflection coefficient S_{in} with a source impedance Z_0 of 50 Ω. Two conditions are considered: one with a standalone DLN, and the other including additional device output capacitance C_{o} and the designed peaking inductance L_1 at the collector node of Q_3 or Q_4 (Figure 6.2). In simulation, C_{o} is extracted as 70 fF, and L_1 is designed as

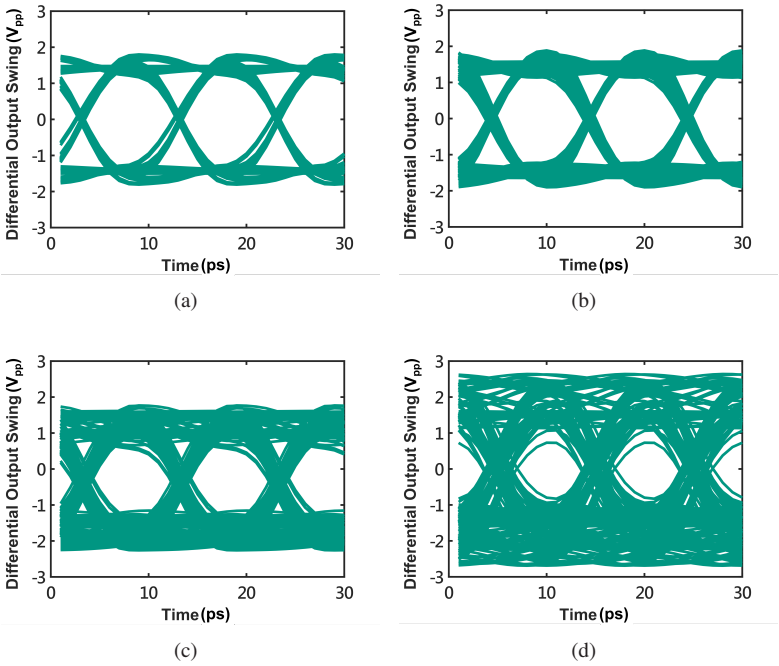


Figure 6.6: Simulated 100-GBd NRZ differential output eye diagrams of the driver under conditions: (a) with DLN, (b) without DLN, (c) without off-chip decoupling ($L_{\text{par}} \rightarrow \infty$) and (d) without on-chip decoupling ($C_1 = 0, R_1 = 50\Omega$) [7]. © IEEE.

75 pH to optimize the bandwidth. Figure 6.5 demonstrates the corresponding simulation results. Figure 6.5(a) indicates that the DLN improves the overall frequency response. When output parasitics C_{o} and L_1 are taken into account, the DLN still offers improvement at lower frequencies (Figure 6.5(b)), while the large C_{o} dominates and degrades performance at higher frequencies. Under the condition of a standalone R_1, denoted as w/o DLN in Figure 6.5, a peak in S_{in} appears at low frequencies, primarily caused by L_{par}. This unwanted S_{in} peak emerges even when L_{par} is as small as 50 pH, indicating that countermeasures are necessary. Figure 6.5 demonstrates that a DLN with R_3 of 10 Ω effectively suppresses the abnormal resonance induced by L_{par}. The DLN has

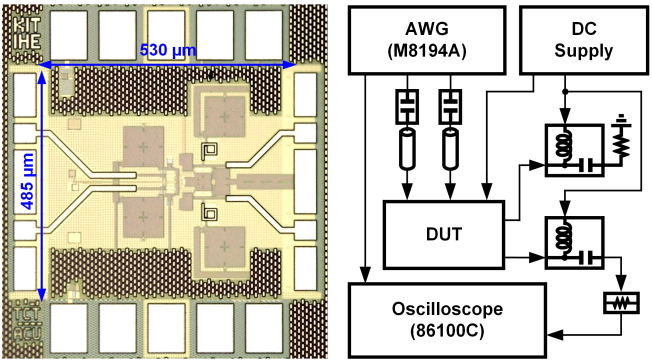


Figure 6.7: (a) Chip micrograph and (b) time-domain testing setup [7]. © IEEE.

also been proposed as a line-termination approach in distributed amplifiers to avoid unnecessary power dissipation at the termination [Boh24].

Figure 6.6 illustrates how the designed termination network affects time-domain simulation results. Figure 6.6(a) shows the 100-GBd NRZ differential output eye of the driver with the DLN applied. As seen in Figure 6.6(b), the eye becomes noticeably noisier when the DLN is not used. Furthermore, Figure 6.6(c) and (d) show the impact of removing the off-chip and on-chip decoupling networks, respectively. A large on-chip decoupling capacitor C_1 often helps prevent eye degradation, as depicted in Figure 6.6(d); however, this improvement comes at the cost of increased chip area.

6.2.2 Experimental Results

Figure 6.7(a) shows the chip micrograph which measures 0.26 mm^2 excluding pads.

True-mode differential S-parameters are characterized using a 67-GHz 4-port vector signal analyzer (VNA). The simulated and measured differential S-parameters are shown in Figure 6.8. In measurement, a gain of 19.3 dB is achieved and the $BW_{-3\text{dB}}$ exceeds 67 GHz. The measured $S_{\text{dd11}}/S_{\text{dd22}}$ remain

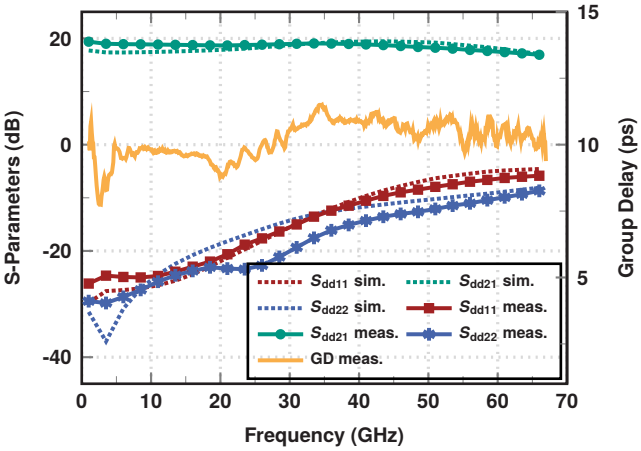


Figure 6.8: Simulated and measured differential S-parameters. Measured group delay [7]. © IEEE.

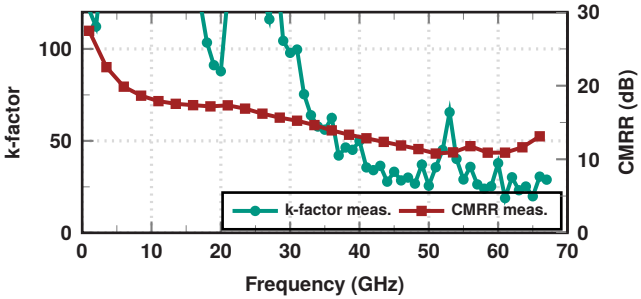
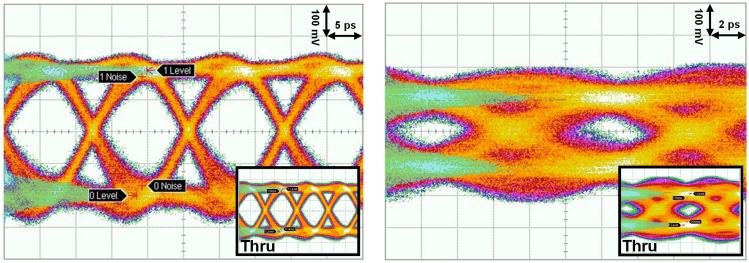


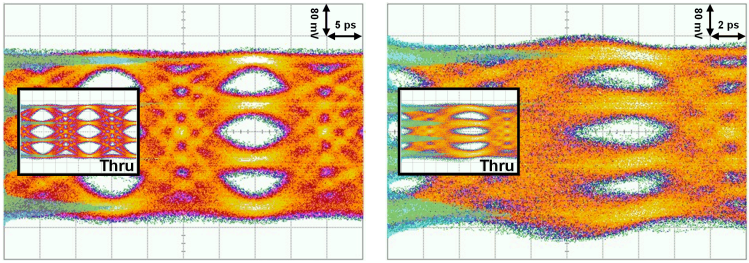
Figure 6.9: Measured k-factor and CMRR [7]. © IEEE.

below −10 dB up to 42.4/60.6 GHz. The group delay (GD) derived from S_{dd21} varies by less than 4 ps up to 67 GHz. Moreover, across the entire measured frequency range, the stability k-factor is well above unity and the CMRR remains greater than 10 dB (Figure 6.9). Large-signal stability is not a concern in this driver design, since the broadband termination is applied, which is particularly effective in the lower-frequency range.



(a) (b)

Figure 6.10: Measured single-ended NRZ eye diagrams with (a) 75 GBd and (b) 100 GBd [7]. © IEEE.



(a) (b)

Figure 6.11: Measured single-ended PAM4 eye diagrams with (a) 50 GBd (100 Gb/s) and (b) 75 GBd (150 Gb/s) [7]. © IEEE.

Eye diagrams are measured using the setup shown in Figure 6.7(b). At the input, a 120-GSa/s AWG generates of high-speed differential random NRZ and PAM4 signals. DC-blocks, 30-cm cables, and differential probes are pre-characterized using the VNA, and their responses are cascaded and fed back to the AWG for input-channel equalization. At the output, a sampling oscilloscope with a precision timebase reference is used. Due to display limitations of the oscilloscope, a 10-dB attenuator is added. In addition, because the samplers cannot capture both differential outputs simultaneously, only one side is sampled while the other port is terminated with 50 Ω. This, however, degrades the

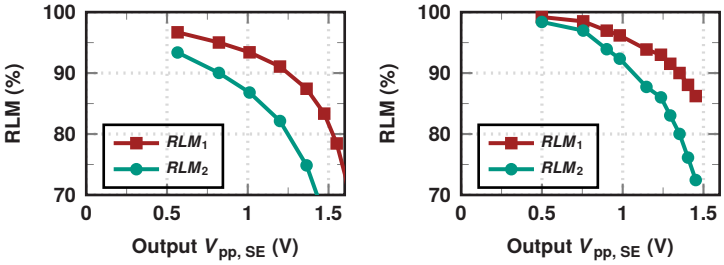


Figure 6.12: Measured RLM with (a) 50 GBd- and (b) 75 GBd- PAM4 signals [7]. © IEEE.

measurement performance, since a true differential acquisition suppresses even-order distortion effects.

Single-ended output eye diagrams of NRZ and PAM4 signals are shown in Figure 6.10 and Figure 6.11. The insets display the input signals measured through a thru test structure. In Figure 6.10(a), with a 75-GBd NRZ signal, the single-ended output voltage swing is 1.23 V_{pp}, with a peak-to-peak jitter (J_{pp}) of 4.11 ps and an SNR of 8.19. For 100-GBd NRZ, the output voltage swing is 670 mV_{pp}, with J_{pp} of 8.18 ps and an SNR of 3.87 (Figure 6.10(b)). It is worth mentioning that for 100-GBd NRZ, the output swing is limited by the input-channel equalization—specifically, the additional loss at the AWG output ports—as the AWG cannot generate a larger voltage amplitude.

For PAM4 signals, a measurement up to 75 GBd (150 Gb/s) is accomplished. The attempt at 100-GBd PAM4 test is unsuccessful because the eye is already closed at the thru test. Figure 6.11(a)-(b) show the output eyes at 50 and 75 GBd, where the single-ended output swings are 1.2 V_{pp} and 1.3 V_{pp}, respectively. In addition, to assess and quantify linearity of the modulator driver, ratio of level mismatch (RLM) is also evaluated. Two definitions of RLM (RLM_1 and RLM_2), as described in Section 2.1 are used. As shown in Figure 6.12, at an RLM_1 of 91 %, the driver provides 1.2 V_{pp}/1.3 V_{pp} single-ended output voltage swing for 50-GBd/75-GBd PAM4 signals. In comparison, at the same voltage swing level, RLM_2 reaches only 82 %.

6.3 Chapter Conclusions

A compact 100-GBd linear modulator driver in 130-nm SiGe BiCMOS process has been demonstrated for short-reach IM/DD optical links, together with the associated design considerations. By leveraging a pair of EFs, a differential small-signal gain $BW_{-3\text{dB}}$ exceeding 67 GHz is achieved. A detailed description of the proposed DLN is also provided to address the adverse effects introduced by packaging parasitics.

The driver performance is summarized and compared with recently reported Si-based implementations in Table 6.1. The driver delivers a differential swing of $2.6\,V_{\text{pp}}$ at RLM_1 of 91 % for a 75-GBd PAM4 signal, making it well suited for low-drive-voltage MZMs and EAMs.

Table 6.1: Comparison with State-of-the-art Si-based Modulator Drivers

	This Work	[IMK+22]	[JNO+21]	[EAR19]	[RLV+19]	[RGLA+17]	[ZSV17]	[BHSV17]
Technology	130-nm SiGe	130-nm SiGe	90-nm SiGe	45-nm SOI CMOS	55-nm SiGe	0.13-µm SiGe	55-nm SiGe	55-nm SiGe
f_T/f_{max} (GHz)	300/500	380/520	310/370	290/250	N/A	320/350	380/340	380/340
BW_{-3dB} (GHz)	>67	>115	>67	108	38**	90	57.5	>70
Gain (dB)	19.3	18	21	23	15**	12.5	18.8	20.75
Data Rate (GBd)	100	128	96	56	70	120	56	120
Output Swing (V_{ppd})	2.6♯	2	4.5*	3.6‡	2	4***	3.8	4.8
P_{dc} (mW)	336	280	350	890	61	550	820	1100
Chip Area (mm^2)	0.26	0.24†	1.16	0.31	0.37	1.2	0.6	1.34

♯Due to AWG limitation, only with 75-GBd PAM4 at RLM1=91% *Derived from 1-GHz one-tone test at P_{1dB}
**Originally designed not for 50Ω ***With visible distortion †Graphically estimated ‡Single-ended

7 Concluding Remarks

This dissertation explores the design of high-frequency and broadband output-stage amplifiers, resulting in several silicon implementations for wireless and optical transmitters. The research focuses on the essential challenges of bandwidth, linearity, efficiency, and stability, which are increasingly important in modern high-speed communication systems.

The study began by addressing the fundamentals of digital modulation and amplifier design, with a focus on how transistor configurations and differential architectures perform across different scenarios. The principles of silicon power amplifiers (PAs) were also summarized, specifically looking at transformer-based power combining for integrated designs. Based on these considerations, several linear PAs were developed in SiGe and CMOS technologies covering the *K*u-, *K*a-, and V-bands. Among these, two PAs used current power combining to increase output power (P_{out}) while maintaining moderate to high power-added efficiency (PAE). One 28-GHz PA was designed for high power density, achieving 22.7 dBm saturated P_{out} and 38.1 % peak PAE. To explore the advanced power-combining technique, balanced and Doherty PAs were developed to handle antenna variations and improve back-off efficiency, while using specific strategies to keep the coupler area small.

Another key part of this work was the investigation of large-signal stability in broadband SiGe PAs. By analyzing how nonlinear capacitances affect stability, the causes of instability were identified and verified with a fabricated PA. These findings guided the design of a *K*u/*K*a-band broadband SiGe PA using a common-collector–common-base (CC–CB) configuration. This design showed reduced sensitivity to large-signal instability and achieved a $17-28$ GHz (49 %) P_{1dB} 3-dB bandwidth.

Finally, the dissertation demonstrated a 100-GBd linear SiGe optical modulator driver for short-reach links. These links are essential for both wireless backhaul and AI-related data centers. The driver provides a differential swing of $2.6\,V_{\text{pp}}$

with a 91 % ratio of level mismatch for a 75-GBd PAM4 signal. Overall, the methods and designs presented in this work provide practical solutions for the next generation of high-speed communication transmitters.

A Appendix

A.1 Linearity of Bipolar Differential and Pseudo-Differential Pairs

First, we consider a differential pair with a tail current I_{tail}. The collector currents I_{cp} and I_{cn} on the two sides are then expressed as

$$I_{\text{cp}} = \frac{\alpha I_{\text{tail}}}{1 + \exp\{(-v_{\text{id}}/V_{\text{T}})\}} \tag{A.1}$$

$$I_{\text{cn}} = \frac{\alpha I_{\text{tail}}}{1 + \exp\{(v_{\text{id}}/V_{\text{T}})\}}. \tag{A.2}$$

Then the output differential current I_{id} becomes

$$I_{\text{id}} = I_{\text{cp}} - I_{\text{cn}} = \alpha I_{\text{tail}} \tanh\left(\frac{v_{\text{id}}}{2V_{\text{T}}}\right), \tag{A.3}$$

where v_{id} is the input differential voltage excluding common mode. Equation (A.3) can be further Taylor expanded near $v_{\text{id}} = 0$ as

$$\alpha I_{\text{tail}}\left(\frac{x}{2} - \frac{x^3}{24} + \frac{x^5}{240} + \ldots\right), \tag{A.4}$$

where $x = v_{\text{id}}/V_{\text{T}}$. Equation (A.4) indicates that $\alpha_1 = \alpha I_{\text{tail}}/(2V_{\text{T}})$ and $\alpha_3 = \alpha I_{\text{tail}}/(24V_{\text{T}}^3)$. Therefore, the corresponding A_{IIP3} is calculated as

$$A_{\text{IIP3}} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|} = 4V_{\text{T}}. \tag{A.5}$$

Next, a pseudo-differential pair is considered. The device size is kept and both transistors are biased with a same common-mode level V_{CM} to ensure an identical quiescent biasing current $\frac{I_{tail}}{2}$ per each transistor. Then the I_{id} is expressed as

$$\begin{aligned} I_{id} = I_{cp} - I_{cn} &= \alpha I_S \exp\left\{\left(\frac{V_{CM}}{V_T}\right)\right\}\left[\exp\left\{\left(\frac{v_{ip}}{V_T}\right)\right\} - \exp\left\{\left(\frac{v_{in}}{V_T}\right)\right\}\right] \\ &= 2\alpha I_S \exp\left\{\left(\frac{V_{CM}}{V_T}\right)\right\} \sinh\left(\frac{v_{id}}{2V_T}\right), \end{aligned} \tag{A.6}$$

where $v_{ip} = -v_{in} = \frac{v_{id}}{2}$ and the term $\alpha I_S \exp\left\{\left(\frac{V_{CM}}{V_T}\right)\right\}$ corresponds to $\frac{\alpha I_{tail}}{2}$.

Equation (A.6) can be further Taylor expanded near $v_{id} = 0$ as

$$\alpha I_S \exp\left\{\left(\frac{V_{CM}}{V_T}\right)\right\}\left(2x + \frac{x^3}{3} + \frac{x^5}{60} + \ldots\right), \tag{A.7}$$

where $x = \frac{v_{id}}{2V_T}$. This indicates $\alpha_1 = \alpha I_{tail}/(2V_T)$ and $\alpha_3 = \alpha I_{tail}/(48V_T^3)$ and the A_{IIP3} is

$$A_{IIP3} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|} \approx 5.7V_T, \tag{A.8}$$

which is higher than the counterpart from (A.5), showing a better linearity.

Figure A.1: A balun network.

A.2 CMRR of Balun Networks

First, we use a balun as a power splitter. As shown in Fig. A.1, port 3 is the input port, and ports 1 and 2 are the balanced ports. By Z-parameters, voltage V_1 and V_2 at ports 1 and 2 can be expressed as

$$\begin{aligned} V_1 &= Z_{11}I_1 + Z_{12}I_2 + Z_{13}I_3, \\ V_2 &= Z_{21}I_1 + Z_{22}I_2 + Z_{23}I_3. \end{aligned} \tag{A.9}$$

Let ports 1 and 2 be open, the V_1 and V_2 collapse to

$$V_1 = Z_{13}I_3 \quad and \quad V_2 = Z_{23}I_3. \tag{A.10}$$

Then, the differential voltage V_{diff} and common-mode voltage V_{cm} follow

$$\begin{aligned} V_{\text{diff}} &= V_1 - V_2 = (Z_{13} - Z_{23})I_3, \\ V_{\text{cm}} &= \frac{V_1 + V_2}{2} = \frac{Z_{13} + Z_{23}}{2}I_3. \end{aligned} \tag{A.11}$$

Hence, the CMRR of the 3-port power splitter is derived as

$$CMRR = \frac{V_{\text{diff}}}{V_{\text{cm}}} = \frac{2(Z_{13} - Z_{23})}{Z_{13} + Z_{23}}. \tag{A.12}$$

Next, if the balun network is used reversely as a power combiner, we derive the CMRR by assuming currents I_1 and I_2 enter the network and port 3 is open. Consequently,

$$V_3 = Z_{31}I_1 + Z_{32}I_2. \tag{A.13}$$

With the definition of differential current I_{diff} and common-mode current I_{cm} as

$$I_{\text{diff}} = \frac{I_1 - I_2}{2} \quad and \quad I_{\text{cm}} = I_1 + I_2, \tag{A.14}$$

V_3 can be further derived as

$$\begin{aligned} V_3 &= (Z_{31} - Z_{32})I_{\text{diff}} + \frac{(Z_{31} + Z_{32})}{2}I_{\text{cm}} \\ &= V_{\text{diff},3} + V_{\text{cm},3}. \end{aligned} \tag{A.15}$$

Therefore, the CMRR of the 3-port power combiner is derived as

$$CMRR' = \frac{V_{\text{diff},3}}{V_{\text{cm},3}} = \frac{2(Z_{13} - Z_{23})}{Z_{13} + Z_{23}} \frac{I_{\text{diff}}}{I_{\text{cm}}} = CMRR \cdot \frac{I_{\text{diff}}}{I_{\text{cm}}}, \tag{A.16}$$

given the balun is a reciprocal network (i.e., $Z_{31} = Z_{13}$ and $Z_{32} = Z_{23}$). The ratio $\frac{I_{\text{diff}}}{I_{\text{cm}}}$ in (A.16) comes from the preceding differential amplifier; if a pseudo-differential pair is used, this ratio becomes unity and (A.16) is equal to (A.12).

Equation (A.12) can be also expressed in Y-parameters. By letting $I_1 = I_2 = 0$, the CMRR can be equivalently expressed as

$$CMRR = \frac{2[(Y_{11} + Y_{12})Y_{23} - (Y_{21} + Y_{22})Y_{13}]}{(-Y_{11} + Y_{12})Y_{23} + (Y_{21} - Y_{22})Y_{13}}. \tag{A.17}$$

To summarize, equations (A.12) and (A.17) are indices for evaluating the CMRR of a balun network. They are represented by Z-parameters and Y-parameters, respectively, and are independent of any loading effects.

A.3 Generalized Kurokawa Conditions

The following section was previously published in [1].

Considering both frequency ω and amplitude A dependences, Z_{L} and Z_{in} are re-denoted as $Z_{\text{L}}(\omega, A)$ and $Z_{\text{in}}(\omega, A)$ which are expressed as

$$Z_{\text{L}}(\omega, A) = R_{\text{L}}(\omega, A) + \jmath X_{\text{L}}(\omega, A) \tag{A.18}$$

$$Z_{\text{in}}(\omega, A) = R_{\text{in}}(\omega, A) + \jmath X_{\text{in}}(\omega, A). \tag{A.19}$$

In the branch analysis, let branch current i_{b}(t) be equal to

$$\mathfrak{Re}\{A(t) \exp[\jmath(\omega t + \theta(t))]\}, \tag{A.20}$$

then the equivalent frequency $\omega_{\text{eq}} = \omega + \Delta\omega$ can be deduced by the slow time-varying amplitude $A(t) = A + \Delta A(t)$ and phase $\theta(t)$ where

$$\Delta\omega = \frac{\mathrm{d}\theta(t)}{\mathrm{d}t} - J\frac{1}{A(t)}\frac{\mathrm{d}A(t)}{\mathrm{d}t}. \tag{A.21}$$

The $Z_{\text{L}}(\omega_{\text{eq}}, A(t))$ and $Z_{\text{in}}(\omega_{\text{eq}}, A(t))$ are then Taylor's expanded firstly at ω as

$$Z_{\text{L}}(\omega_{\text{eq}}, A(t)) \approx Z_{\text{L}}(\omega, A(t)) + \frac{\partial Z_{\text{L}}(\omega, A(t))}{\partial\omega}\Delta\omega \tag{A.22}$$

and

$$Z_{\text{in}}(\omega_{\text{eq}}, A(t)) \approx Z_{\text{in}}(\omega, A(t)) + \frac{\partial Z_{\text{in}}(\omega, A(t))}{\partial\omega}\Delta\omega. \tag{A.23}$$

By equating the voltage across Z_{L} and Z_{in} from (A.22)-(A.23) and using elimination [Kur69, Gui06], the following equation is shown:

$$\begin{aligned} &R_{\text{T}}(\omega, A(t))\frac{\partial X_{\text{L}}(\omega, A(t))}{\partial\omega} - X_{\text{T}}(\omega, A(t))\frac{\partial R_{\text{L}}(\omega, A(t))}{\partial\omega} \\ &+P(\omega, A(t))\frac{1}{A(t)}\frac{\mathrm{d}A(t)}{\mathrm{d}t} + Q(\omega, A(t))\frac{\mathrm{d}\theta}{\mathrm{d}t} = 0 \end{aligned} \tag{A.24}$$

where $R_{\text{T}} = R_{\text{L}} + R_{\text{in}}$, $X_{\text{T}} = X_{\text{L}} + X_{\text{in}}$ and

$$\begin{aligned} P(\omega, A(t)) = &\frac{\partial X_{\text{L}}(\omega, A(t))}{\partial\omega}\frac{\partial X_{\text{T}}(\omega, A(t))}{\partial\omega} \\ &+ \frac{\partial R_{\text{L}}(\omega, A(t))}{\partial\omega}\frac{\partial R_{\text{T}}(\omega, A(t))}{\partial\omega}. \end{aligned} \tag{A.25}$$

In steady-state oscillation with ω_0, A_0, we have

$$R_{\text{T}}(\omega_0, A_0) = X_{\text{T}}(\omega_0, A_0) = 0. \tag{A.26}$$

Now if a small variation of A as ΔA based on the A_0 is considered, the total impedance can be expanded as

$$R_{\text{T}}(\omega_0, A_0 + \Delta A) \approx R_{\text{T}}(\omega_0, A_0) + \frac{\partial R_{\text{T}}(\omega, A)}{\partial A}|_{\omega_0, A_0}\Delta A \tag{A.27}$$

and

$$X_{\mathrm{T}}(\omega_0, A_0 + \Delta A) \approx X_{\mathrm{T}}(\omega_0, A_0) + \frac{\partial X_{\mathrm{T}}(\omega, A)}{\partial A}|_{\omega_0, A_0}\Delta A. \tag{A.28}$$

Assuming θ does not vary and substituting (A.26), (A.27) and (A.28) into (A.24) gives

$$P(\omega_0, A_0)\frac{1}{A_0}\frac{\mathrm{d}\Delta A}{\mathrm{d}t} + (\frac{\partial R_{\mathrm{T}}}{\partial A}\frac{\partial X_{\mathrm{L}}}{\partial \omega} - \frac{\partial X_{\mathrm{T}}}{\partial A}\frac{\partial R_{\mathrm{L}}}{\partial \omega})|_{\omega_0, A_0}\Delta A = 0. \tag{A.29}$$

For a stable oscillation, the ΔA should decay over time [Kur69, Gui06], and (2.10) follows. In the case of node analysis, let the node voltage $v_{\mathrm{n}}(\mathrm{t})$ be equal to $\mathfrak{Re}\{A(t)\exp[\jmath(\omega t + \theta(t))]\}$. Following a similar derivation as above, equation (2.11) is consequently derived.

A.4 Load Modulation Analysis of Doherty Current-Combiner Using a 90° Hybrid Couplers

Figure A.2 illustrates the simplified power-combining network using an open-circuited 90° hybrid coupler, where the current sources i_{m} and i_{pk} model the main and peaking amplifiers, respectively.

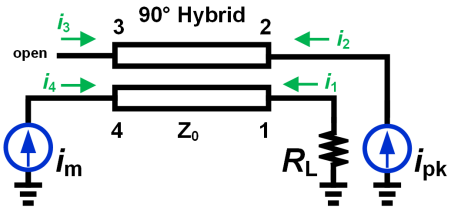


Figure A.2: Simplified power-combining model using an open-circuited 90° hybrid coupler.

From the 4-port Z-matrix of a 90° coupler with characteristic impedance Z_0,

$$\begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} = -\jmath Z_0 \begin{bmatrix} 0 & 0 & 1 & \sqrt{2} \\ 0 & 0 & \sqrt{2} & 1 \\ 1 & \sqrt{2} & 0 & 0 \\ \sqrt{2} & 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix}, \tag{A.30}$$

the voltage and current relationships for the network in Figure A.2 can be expressed as

$$\begin{aligned} v_1 &= -\jmath\sqrt{2} Z_0\, i_4, \\ v_2 &= -\jmath Z_0\, i_4, \\ v_3 &= -\jmath Z_0\,(i_1 + \sqrt{2}\, i_2) \quad \textit{and} \quad v_4 = -\jmath Z_0\,(\sqrt{2}\, i_1 + i_2), \end{aligned} \tag{A.31}$$

with additional conditions $i_3 = 0$ and $v_1 = -Z_0 i_1$. Therefore, the voltages across i_m and i_pk become

$$\begin{aligned} v_4 &= -\jmath Z_0 \left(-\sqrt{2}\,\frac{v_1}{R_\mathrm{L}} + i_2\right) = -\jmath Z_0 \left[-\sqrt{2}\,\frac{(-\jmath\sqrt{2} Z_0\, i_4)}{R_\mathrm{L}} + i_2\right] \\ &= Z_0 \left(\frac{2Z_0}{R_\mathrm{L}} i_4 - \jmath\, i_2\right) \quad \textit{and} \\ v_2 &= -\jmath Z_0\, i_4. \end{aligned} \tag{A.32}$$

In the power backoff region, the peaking amplifier is turned off, so the peaking amplifier current at port-2 satisfies $i_\mathrm{pk} = i_2 = 0$. Assuming $R_\mathrm{L} = Z_0$, the driving point impedance seen by the main amplifier becomes

$$Z_\mathrm{m} = \frac{|v_4|}{|i_4|} = \frac{-\jmath\sqrt{2} Z_0\, i_1}{-\jmath\frac{1}{\sqrt{2}}\, i_1} = 2Z_0. \tag{A.33}$$

When both amplifiers operate with the maximum drive voltage and the peaking amplifier is delayed by 90°, it follows that $i_\mathrm{m} = i_4 = \jmath\, i_\mathrm{pk} = \jmath\, i_2 = i_\mathrm{max}$. With

$R_L = Z_0$ and the resulting $i_1 = \jmath\sqrt{2}\, i_4$, the driving point impedances seen by the main and the peaking amplifiers become

$$\begin{aligned} Z_m &= \frac{|v_4|}{|i_4|} = \frac{-\jmath Z_0\,(\sqrt{2}\, i_1 + i_2)}{i_4} = Z_0 \quad \textit{and} \\ Z_{pk} &= \frac{|v_2|}{|i_2|} = \frac{-\jmath Z_0\, i_4}{i_2} = Z_0. \end{aligned} \tag{A.34}$$

Bibliography

[AAC+08] Natanael Ayllon, Aitziber Anakabe, Juan Mari Collantes, Geoffroy Soubercaze-Pun, and Stephane Forestier. Sensitivity Enhancement in Pole-Zero Identification Based Stability Analysis of Microwave Circuits. In *2008 Workshop on Integrated Nonlinear Microwave and Millimetre-Wave Circuits*, pages 75–78, 2008.

[ACA+11] Natanael Ayllon, Juan-Mari Collantes, Aitziber Anakabe, Ibone Lizarraga, Geoffroy Soubercaze-Pun, and Stephane Forestier. Systematic Approach to the Stabilization of Multitransistor Circuits. *IEEE Trans. Microw. Theory Techn.*, 59(8):2073–2082, 2011.

[ACC+23] Giandomenico Amendola, Daniele Cavallo, Tobias Chaloun, Nicolas Defrance, George Goussetis, Marc Margalef-Rovira, Enrica Martini, Oscar Quevedo-Teruel, Václav Valenta, Nelson J.G. Fonseca, and Mauro Ettorre. Low-Earth Orbit User Segment in the Ku and Ka-Band: An Overview of Antennas and RF Front-End Technologies. *IEEE Microw. Mag.*, 24(2):32–48, 2023.

[ACP+02] A. Anakabe, J.-M. Collantes, J. Portilla, J. Jugo, A. Mallet, L. Lapierre, and J.-P. Fraysse. Analysis and elimination of parametric oscillations in monolithic power amplifiers. In *2002 IEEE MTT-S International Microwave Symposium Digest*, volume 3, pages 2181–2184 vol.3, 2002.

[AKGR22] Abdulrahman Alhamed, Oguz Kazan, Gökhan Gültepe, and Gabriel M. Rebeiz. A Multiband/Multistandard 15–57 GHz Receive Phased-Array Module Based on 4 × 1 Beamformer IC and Supporting 5G NR FR2 Operation. *IEEE Trans. Microw. Theory Techn.*, 70(3):1732–1744, 2022.

[AKRH02] I. Aoki, S.D. Kee, D.B. Rutledge, and A. Hajimiri. Distributed Active Transformer – A New Power-Combining and

Impedance-Transformation Technique. *IEEE Trans. Microw. Theory Techn.*, 50(1):316–331, 2002.

[Ali11] Ali. M. Niknejad. *Electromagnetics for High-Speed Analog and Digital Communication Circuits*. Cambridge University Press, 2011.

[All25] Ethernet Alliance. 2025 Ethernet Roadmap. `https://ethernetalliance.org/technology/ethernet-roadmap`, 2025. [Online].

[Alm09] Almudena Suarez. *Analysis and Design of Autonomous Microwave Circuits*. Wiley-IEEE Press, 2009.

[AMAAH+25] Mohammad Ali Mokri, Emad Afshar, Md Aminul Hoque, Soodeh Miraslani, Shahriar Mirabbasi, and Deukhyoun Heo. A Compact Single-Ended Common-Base Doherty PA in 90-nm BiCMOS With 37.3% Peak PAE for 5G Beamforming Arrays. *IEEE Trans. Microw. Theory Techn.*, 73(1):540–552, 2025.

[AWZ+20] Khalid Aldubaikhy, Wen Wu, Ning Zhang, Nan Cheng, and Xuemin Shen. mmWave IEEE 802.11ay for 5G Fixed Wireless Access. *IEEE Wireless Communications*, 27(2):88–95, 2020.

[BB19] Subhadip Biswas and Jayanta K Bhattacharjee. On the properties of a class of higher-order Mathieu equations originating from a parametric quantum oscillator. *Nonlinear Dynamics*, 96:737–750, Apr 2019.

[BCS06] G. Berretta, D. Cristaudo, and S. Scaccianoce. A Balanced CDMA2000 SiGe HBT Load Insensitive Power Amplifier. In *2006 IEEE Radio and Wireless Symposium*, pages 523–526, 2006.

[BE95] D.E. Bockelman and W.R. Eisenstadt. Combined Differential and Common-Mode Analysis of Power Splitters and Combiners. *IEEE Trans. Microw. Theory Techn.*, 43(11):2627–2632, 1995.

[Beh11] Behzad Razavi. *RF Microelectronics*. Prentice Hall Press, 2nd edition, 2011.

[Beh12] Behzad Razavi. *Design of Integrated Circuits for Optical Communications*. Wiley, 2nd edition, 2012.

[BHSV17] Robert J. A. Baker, James Hoffman, Peter Schvan, and Sorin P. Voinigescu. SiGe BiCMOS linear modulator drivers with 4.8-V_{pp} differential output swing for 120-GBaud applications. In *2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 260–263, 2017.

[Boh24] Christian Bohn. *Broadband Circuits for High-Speed Short Reach Optical Transceivers*. Dissertation, Karlsruher Institut für Technologie (KIT), Karlsruhe, 2024. Online Resource.

[BSTSN15] A. Basaligheh, P. Saffari, M. Taherzadeh-Sani, and F. Nabki. A Highly Efficient and Linear Broadband Common-Drain CMOS Power Amplifier With Transformer-Based Input-Matching Network. *IEEE Microw. Wireless Compon. Lett.*, 25(12):814–816, 2015.

[Cam18] T. Cameron. Bits to Beams: RF Technology Evolution for 5G Millimeter Wave Radios. `https://www.analog.com/en/signals/thought-leadership/bits-to-beams-rf-tech-evolution-5g-milli-wave-radios.html`, 2018. [Online].

[CCE20] M. Cui, C. Carta, and F. Ellinger. A 21-dBm 3.7 W/mm² 28.7% PAE 64-GHz Power Amplifier in 22-nm FD-SOI. *IEEE Solid-State Circuits Letters*, 3:386–389, 2020.

[CCL+21] Sergio Colangeli, Walter Ciccognani, Patrick E. Longhi, Leonardo Pantoli, Giorgio Leuzzi, and Ernesto Limiti. Extending the Ohtomo Stability Test to Large-Signal Solutions in a Commercial Circuit Simulator. *IEEE Trans. Microw. Theory Techn.*, 69(10):4437–4447, 2021.

[Cha19] Mathieu Chagnon. Optical Communications for Short Reach. *J. Lightw. Technol.*, 37(8):1779–1797, 2019.

[CHW+16] Cheng-Feng Chou, Yuan-Hung Hsiao, Yi-Ching Wu, Yu-Hsuan Lin, Chen-Wei Wu, and Huei Wang. Design of a V-Band 20-dBm Wideband Power Amplifier Using Transformer-Based Radial Power Combining in 90-nm CMOS. *IEEE Trans. Microw. Theory Techn.*, 64(12):4545–4560, 2016.

[CKA+23] Benjamin Coquillas, Eric Kerhervé, Anne-Charlotte Amiaud, Samuel Redois, Laurent Roussel, Bruno Louis, Thomas Merlet, and Vincent Petit. Ku Band SiGe Power Amplifier With High

Output Power and SWR Robustness Up to 120 °C. *IEEE Trans. Circuits Syst. I*, 70(7):2744–2751, 2023.

[CKR+22] B. Coquillas, E. Kerhervé, S. Redois, AC. Amiaud, L. Roussel, B. Louis, E. Itcia, and T. Merlet. A 27dBm Ku-Band SiGe Power Amplifier Working up to 90°C with High Robustness to the 2:1 SWR. In *2021 16th European Microwave Integrated Circuits Conference (EuMIC)*, pages 152–155, 2022.

[CMA+19] Juan-Mari Collantes, Libe Mori, Aitziber Anakabe, Nerea Otegi, Ibone Lizarraga, Natanael Ayllon, Franco Ramírez, Vincent Armengaud, and Geoffroy Soubercaze-Pun. Pole-Zero Identification: Unveiling the Critical Dynamics of Microwave Circuits Beyond Stability Analysis. *IEEE Microwave Magazine*, 20(7):36–54, 2019.

[CMKY18] Peng Siew Chew, Kaixue Ma, Zhi Hui Kong, and Kiat Seng Yeo. Miniaturized Wideband Coupler for 60-GHz Band in 65-nm CMOS Technology. *IEEE Microw. Wireless Compon. Lett.*, 28(12):1089–1091, 2018.

[CR19] U. Celik and P. Reynaert. An E-Band Compact Power Amplifier for Future Array-Based Backhaul Networks in 22nm FD-SOI. In *2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 187–190, 2019.

[Cre13] John D. Cressler. Radiation Effects in SiGe Technology. *IEEE Transactions on Nuclear Science*, 60(3):1992–2014, 2013.

[Cri06] Steve Cripps. *RF Power Amplifiers for Wireless Communications*. Artech, 2nd edition, 2006.

[CRN09] Debopriyo Chowdhury, Patrick Reynaert, and Ali M. Niknejad. Design Considerations for 60 GHz Transformer-Coupled CMOS Power Amplifiers. *IEEE J. Solid-State Circuits*, 44(10):2733–2744, 2009.

[CS13] Nuno Borges Carvalho and Dominique Schreurs. *Microwave and Wireless Measurement Techniques*. Cambridge University Press, 2013.

[CTF+19] M. Cui, Z. Tibenszky, D. Fritsche, C. Carta, and F. Ellinger. An Area Efficient 48 - 62 GHz Stacked Power Amplifier in 22nm FD-SOI. In *2019 14th European Microwave Integrated Circuits Conference (EuMIC)*, pages 120–123, 2019.

[CWE24] M. Cui, J. Wagner, and F. Ellinger. A Class-J/F 60 GHz Power Amplifier with 42.3% Power Added Efficiency in FD-SOI CMOS. In *2024 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 123–126, 2024.

[CWW19] Yang Chang, Yunshan Wang, and Huei Wang. A K-Band High-OP1dB Common-Drain Power Amplifier With Neutralization Technique in 90-nm CMOS Technology. *IEEE Microw. Wireless Compon. Lett.*, 29(12):795–797, 2019.

[DDT+19] Kaushik Dasgupta, Saeid Daneshgar, Chintan Thakkar, James Jaussi, and Bryan Casper. A 26 dBm 39 GHz Power Amplifier with 26.6% PAE for 5G Applications in 28nm bulk CMOS. In *2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 235–238, 2019.

[DR14] Noël Deferm and Patrick Reynaert. Differential and common mode stability analysis of differential mm-wave CMOS amplifiers with capacitive neutralization. *Analog Integr. Circuits Signal Process.*, 80(1):1–12, Jul 2014.

[DZM+04] Lei Ding, G.T. Zhou, D.R. Morgan, Zhengxiang Ma, J.S. Kenney, Jaehyeong Kim, and C.R. Giardina. A Robust Digital Baseband Predistorter Constructed Using Memory Polynomials. *IEEE Transactions on Communications*, 52(1):159–165, 2004.

[EAR19] Omar El-Aassar and Gabriel M. Rebeiz. A DC-to-108-GHz CMOS SOI Distributed Power Amplifier and Modulator Driver Leveraging Multi-Drive Complementary Stacked Cells. *IEEE J. Solid-State Circuits*, 54(12):3437–3451, 2019.

[Edw23] Terry Edwards. V-Band and E-Band Radio Links Are Becoming Important for 5G Fixed Wireless Access and xHaul. `https://www.microwavejournal.com/articles/40630-v-band-and-e-band-radio-links-are-becoming-important-for-5g-fixed-wireless-access-and-xhaul`, 2023. [Online].

[ETS15] ETSI. Technical Report ETSI TR 102 376-1 V1.2.1 (2015-11), 2015.

[FPdC+04] C. Fager, J.C. Pedro, N.B. de Carvalho, H. Zirath, F. Fortes, and M.J. Rosario. A Comprehensive Analysis of IMD Behavior

in RF CMOS Power Amplifiers. *IEEE J. Solid-State Circuits*, 39(1):24–34, 2004.

[GHL09] Paul R. Gray, Paul J. Hurst, and Stephen H. Lewis. *Analysis and Design of Analog Integrated Circuits*. Wiley, 5th edition, 2009.

[GMW21] Edgar Felipe Garay, David Joseph Munzer, and Hua Wang. 26.3 A mm-Wave Power Amplifier for 5G Communication Using a Dual-Drive Topology Exhibiting a Maximum PAE of 5030GHz. In *2021 IEEE International Solid-State Circuits Conference (ISSCC)*, volume 64, pages 258–260, 2021.

[GS99] B. Gustavsen and A. Semlyen. Rational Approximation of Frequency Domain Responses by Vector Fitting. *IEEE Transactions on Power Delivery*, 14(3):1052–1061, 1999.

[Gui97] Guillermo Gonzalez. *Microwave Transistor Amplifiers: Analysis and Design*. Prentice Hall, 2nd edition, 1997.

[Gui06] Guillermo Gonzalez. *Foundations of Oscillator Circuit Design*. Artech, 2006.

[GXC12] Q. J. Gu, Z. Xu, and M. C. F. Chang. Two-Way Current-Combining W-Band Power Amplifier in 65-nm CMOS. *IEEE Trans. Microw. Theory Techn.*, 60(5):1365–1374, 2012.

[HBD+20] Jonathan Hill, Michel Bellemare, Yves Demers, Nicholas Boudreau, Jean-Daniel Dea, and Eric Amyotte. Active Antennas Radiated Spurious. In *2020 14th European Conference on Antennas and Propagation (EuCAP)*, pages 1–5, 2020.

[HBS04] K. M. Hangos, J. Bokor, and G. Szederkényi. *Analysis and Control of Nonlinear Process Systems*. Springer, 2004.

[HCJ97] J. Hogerheiden, M. Ciminera, and G. Jue. Improved Planar Spiral Transformer Theory Applied to a Miniature Lumped Element Quadrature Hybrid. *IEEE Trans. Microw. Theory Techn.*, 45(4):543–545, 1997.

[Hey17] Payam Heydari. Neutralization Techniques for High-Frequency Amplifiers: An Overview. *IEEE Solid-State Circuits Mag.*, 9(4):82–89, 2017.

[HLKR24] Zhaoxin Hu, Linjie Li, Oguz Kazan, and Gabriel M. Rebeiz. A 16-Channel 3.1–25.5-GHz Phased-Array Receive Beamformer IC With Two Simultaneous Beams and 2.0–2.4-dB NF

for C/X/Ku/Ka-Band SATCOM. *IEEE Trans. Microw. Theory Techn.*, 72(5):2773–2785, 2024.

[HLLW18] W. C. Huang, J. Lin, Y. Lin, and H. Wang. A K-band power amplifier with 26-dBm output power and 34% PAE with novel inductance-based neutralization in 90-nm CMOS. In *IEEE RFIC*, pages 228–231, Philadelphia, PA, USA, June 2018.

[H.W45] H.W. Bode. *Network Analysis and Feedback Amplifier Design*. D. Van Nostrand Company, 1945.

[HWW19] Song Hu, Fei Wang, and Hua Wang. A 28-/37-/39-GHz Linear Doherty Power Amplifier in Silicon for 5G Applications. *IEEE Journal of Solid-State Circuits*, 54(6):1586–1599, 2019.

[IEE18a] IEEE Standard for Ethernet SECTION EIGHT. In *IEEE Std 802.3-2018 (Revision of IEEE Std 802.3-2015)*, pages 366–384. 2018.

[IEE18b] IEEE Standard for Ethernet SECTION SIX. In *IEEE Std 802.3-2018 (Revision of IEEE Std 802.3-2015)*, pages 489–546. 2018.

[IEE18c] SECTION EIGHT. *IEEE Std 802.3-2018 (Revision of IEEE Std 802.3-2015)*, pages 366–384, 2018.

[IEE18d] SECTION SIX. *IEEE Std 802.3-2018 (Revision of IEEE Std 802.3-2015)*, pages 489–546, 2018.

[IMK+22] Festim Iseini, Andrea Malignaggi, Falk Korndörfer, Mesut Inac, and Gerhard Kahmen. Lumped Ultra-Broadband Linear Driver in 130 nm SiGe SG13G3 Technology. In *2022 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, pages 136–139, 2022.

[JGC20] I. Ju, Y. Gong, and J. D. Cressler. Highly Linear High-Power 802.11ac/ax WLAN SiGe HBT Power Amplifiers With a Compact 2nd-Harmonic-Shorted Four-Way Transformer and a Thermally Compensating Dynamic Bias Circuit. *IEEE J. Solid-State Circuits*, 55(9):2356–2370, 2020.

[JLC22] I. Ju, S. Lee, and J. D. Cressler. An Efficient, Broadband SiGe HBT Non-Uniform Distributed Power Amplifier Leveraging a Compact, Two-Section $\lambda/4$ Output Impedance Transformer. *IEEE Trans. Microw. Theory Techn.*, 70(7):3524–3533, 2022.

[JNO+21] Teruo Jyo, Munehiko Nagatani, Yoshihiro Ogiso, Shogo Yamanaka, and Hideyuki Nosaka. An Over 67-GHz Bandwidth 21-dB Gain 4.5-V_{pp} Linear Modulator Driver for 100-GBd Coherent Optical Transmitter. *IEEE Microw. Wireless Compon. Lett.*, 31(6):705–708, 2021.

[Joh07] John G. Proakis, Masoud Salehi. *Digital Communications*. McGraw Hill, 5th edition, 2007.

[JS07] Dominic Jordan and Peter Smith. *Nonlinear Ordinary Differential Equations: An Introduction for Scientists and Engineers*. OUP Oxford, 2007.

[KFZ+20] Clemens Kieninger, Christoph Füllner, Heiner Zwickel, Yasar Kutuvantavida, Juned N. Kemal, Carsten Eschenbaum, Delwin L. Elder, Larry R. Dalton, Wolfgang Freude, Sebastian Randel, and Christian Koos. Silicon-organic hybrid (SOH) Mach-Zehnder modulators for 100 GBd PAM4 signaling with sub-1dB phase-shifter loss. *Opt. Express*, 28(17):24693–24707, Aug 2020.

[KHL+23] Oguz Kazan, Zhaoxin Hu, Linjie Li, Abdulrahman Alhamed, and Gabriel M. Rebeiz. An 8-Channel 5–33-GHz Transmit Phased Array Beamforming IC With 10.8–14.7-dBm Psat for C-, X-, Ku-, and Ka-Band SATCOM. *IEEE Trans. Microw. Theory Techn.*, 71(5):2029–2039, 2023.

[KRS18] Ivana Kovacic, Richard Rand, and Si Mohamed Sah. Mathieu's Equation and Its Generalizations: Overview of Stability Charts and Their Features. *Applied Mechanics Reviews*, 70(2):020802, Feb 2018.

[Kur65] K. Kurokawa. Power Waves and the Scattering Matrix. *IEEE Trans. Microw. Theory Techn.*, 13(2):194–202, 1965.

[Kur69] K. Kurokawa. Some Basic Characteristics of Broadband Negative Resistance Oscillator Circuits. *Bell System Technical Journal*, 48(6):1937–1955, 1969.

[KWP+25] Anil Kumar Kumaran, Yizhuo Wu, Masoud Pashaeifar, Hamza Nachouane, Chang Gao, Leonardus Cornelis Nicolaas de Vreede, and Morteza S. Alavi. A 4×Two-Way mm-Wave Doherty CMOS PA. *IEEE Trans. Microw. Theory Techn.*, 73(10):7482–7499, 2025.

[LC20] Haifeng Lyu and Kenle Chen. Balanced-to-Doherty Mode-Reconfigurable Power Amplifier With High Efficiency and Linearity Against Load Mismatch. *IEEE Trans. Microw. Theory Techn.*, 68(5):1717–1728, 2020.

[LHJ24] Hanjung Lee, Insu Han, and Inchan Ju. A Highly Efficient, Linear Ka-Band SiGe HBT Cascode Power Amplifier With a Compact Lumped Element Coupled Line Impedance Inverting Balun. *IEEE Trans. Microw. Theory Techn.*, 72(10):5799–5808, 2024.

[LHW18] Tso-Wei Li, Ming-Yu Huang, and Hua Wang. A continuous-mode harmonically tuned 19-to-29.5GHz ultra-linear PA supporting 18Gb/s at 18.4% modulation PAE and 43.5% peak PAE. In *2018 IEEE International Solid-State Circuits Conference - (ISSCC)*, pages 410–412, 2018.

[LLLW21] T. W. Li, S. Li, H. M. Lavasani, and H. Wang. A V-Band Doubly Hybrid NMOS/PMOS Four-Way Distributed-Active-Transformer Power Amplifier for Nonlinearity Cancellation and Joint Linearity/Efficiency Optimization. In *2021 IEEE MTT-S International Microwave Symposium (IMS)*, pages 382–385, 2021.

[LLLW24] Edward Liu, Boce Lin, Cho-Ying Lu, and Hua Wang. Compact K/Ka-Band Frontend PA and LNA in 16nm FinFET for Next Generation Digitally Intensive Arrays. In *2024 IEEE/MTT-S International Microwave Symposium - IMS 2024*, pages 858–861, 2024.

[Loh66] D.R. Lohrmann. Parametric oscillations in VHF transistor power amplifiers. *Proceedings of the IEEE*, 54(3):409–410, 1966.

[Lon00] J.R. Long. Monolithic Transformers for Silicon RF IC design. *IEEE J. Solid-State Circuits*, 35(9):1368–1382, 2000.

[LR21] Siwei Li and Gabriel M. Rebeiz. A 130-151 GHz 8-Way Power Amplifier with 16.8-17.5 dBm Psat and 11.7-13.4% PAE Using CMOS 45nm RFSOI. In *2021 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 115–118, 2021.

[MHHW20] Naga Sasikanth Mannem, Min-Yu Huang, Tzu-Yuan Huang, and Hua Wang. A Reconfigurable Hybrid Series/Parallel Do-

herty Power Amplifier With Antenna VSWR Resilient Performance for MIMO Arrays. *IEEE J. Solid-State Circuits*, 55(12):3335–3348, 2020.

[MKQ+25] Susnata Mondal, Sashank Krishnamurthy, Junyi Qiu, Tolga Acikalin, Soumya Bose, Shuhei Yamada, James Jaussi, and Mozhgan Mansuri. A 108 Gb/s PAM-4 VCSEL-Based Direct-Drive Optical Engine for Co-Packaged Optics Applications. *IEEE J. Solid-State Circuits*, pages 1–14, 2025.

[MMWM22] Zonglin Ma, Kaixue Ma, Keping Wang, and Fanyi Meng. A 28GHz Compact 3-Way Transformer-Based Parallel-Series Doherty Power Amplifier With 20.4%/14.2% PAE at 6-/12-dB Power Back-off and 25.5dBm PSAT in 55nm Bulk CMOS. In *2022 IEEE International Solid-State Circuits Conference (ISSCC)*, volume 65, pages 320–322, 2022.

[MSB+96] C.C. McAndrew, J.A. Seitchik, D.F. Bowers, M. Dunn, M. Foisy, I. Getreu, M. McSwain, S. Moinian, J. Parker, D.J. Roulston, M. Schroter, P. van Wijnen, and L.F. Wagner. VBIC95, the vertical bipolar inter-company model. *IEEE J. Solid-State Circuits*, 31(10):1476–1483, 1996.

[NC17] Roberto Nebuloni and Carlo Capsoni. Fade mitigation in future Q/V-band high-throughput satellites. In *2017 XXXIInd General Assembly and Scientific Symposium of the International Union of Radio Science (URSI GASS)*, pages 1–4, 2017.

[Nyq28] H. Nyquist. Certain Topics in Telegraph Transmission Theory. *Transactions of the American Institute of Electrical Engineers*, 47(2):617–644, 1928.

[PdVA21] Masoud Pashaeifar, Leo C. N. de Vreede, and Morteza S. Alavi. A Millimeter-Wave Mutual-Coupling-Resilient Double-Quadrature Transmitter for 5G Applications. *IEEE J. Solid-State Circuits*, 56(12):3784–3798, 2021.

[PHFB18] Prathamesh H. Pednekar, William Hallberg, Christian Fager, and Taylor Wallis Barton. Analysis and Design of a Doherty-Like RF-Input Load Modulated Balanced Amplifier. *IEEE Trans. Microw. Theory Techn.*, 66(12):5322–5335, 2018.

[PLSF16] Leonardo Pantoli, Giorgio Leuzzi, Alberto Santarelli, and Fabio Filicori. Stability Analysis and Design Criteria of

Paralleled-Device Power Amplifiers Under Large-Signal Regime. *IEEE Trans. Microw. Theory Techn.*, 64(5):1442–1455, 2016.

[PRC+21] Anna Piacibello, Chiara Ramella, Vittorio Camarchia, Roberto Quaglia, and Marco Pirola. A Simple Method to Identify Parametric Oscillations in Power Amplifiers Using Harmonic Balance Solvers. *IEEE Microw. Wireless Compon. Lett.*, 31(3):269–271, 2021.

[PSH93] A. Platzker, W. Struble, and K.T. Hetzler. Instabilities Diagnosis And The Role of K in Microwave Circuits. In *1993 IEEE MTT-S International Microwave Symposium Digest*, pages 1185–1188 vol.3, 1993.

[QR21] Valdrin Qunaj and Patrick Reynaert. A Ka-Band Doherty-Like LMBA for High-Speed Wireless Communication in 28-nm CMOS. *IEEE J. Solid-State Circuits*, 56(12):3694–3703, 2021.

[Rei03] Michael Reisch. *High-Frequency Bipolar Transistors*. Springer Berlin Heidelberg, 2003.

[RGLA+17] Pedro Rito, Iria García López, Ahmed Awny, Minsu Ko, Ahmet Cagri Ulusoy, and Dietmar Kissinger. A DC-90-GHz 4-V_{pp} Modulator Driver in a 0.13-μm SiGe:C BiCMOS Process. *IEEE Trans. Microw. Theory Techn.*, 65(12):5192–5202, 2017.

[RLV+19] Hannes Ramon, Joris Lambrecht, Jochem Verbist, Michael Vanhoecke, Srinivasan Ashwyn Srinivasan, Peter De Heyn, Joris Van Campenhout, Peter Ossieur, Xin Yin, and Johan Bauwelinck. 70 Gb/s Low-Power DC-Coupled NRZ Differential Electro-Absorption Modulator Driver in 55 nm SiGe BiCMOS. *J. Lightw. Technol.*, 37(5):1504–1514, 2019.

[Rol62] J. Rollett. Stability and Power-Gain Invariants of Linear Two-ports. *IRE Transactions on Circuit Theory*, 9(1):29–32, 1962.

[RZSM19] Elham Rahimi, Junlei Zhao, Francesco Svelto, and Andrea Mazzanti. High-Efficiency SiGe-BiCMOS E-Band Power Amplifiers Exploiting Current Clamping in the Common-Base Stage. *IEEE J. Solid-State Circuits*, 54(8):2175–2185, 2019.

[She21] Sudip Shekhar. Silicon photonics: A brief tutorial. *IEEE Solid-State Circuits Mag.*, 13(3):22–32, 2021.

[SJR06] Almudena Suarez, Sanggeun Jeon, and David Rutledge. Stability Analysis and Stabilization of Power Amplifiers. *IEEE Microwave Magazine*, 7(5):51–65, 2006.

[SP93] W. Struble and A. Platzker. A Rigorous Yet Simple Method for Determining Stability of Linear N-port Networks [and MMIC Application]. In *15th Annual GaAs IC Symposium*, pages 251–254, 1993.

[SPC16] Daniel J. Shepphard, Jeffrey Powell, and Steve C. Cripps. An Efficient Broadband Reconfigurable Power Amplifier Using Active Load Modulation. *IEEE Microw. Wireless Compon. Lett.*, 26(6):443–445, 2016.

[SPD+16] Sherif Shakib, Hyun-Chul Park, Jeremy Dunworth, Vladimir Aparin, and Kamran Entesari. A Highly Efficient and Linear Power Amplifier for 28-GHz 5G Phased Array Radios in 28-nm CMOS. *IEEE J. Solid-State Circuits*, 51(12):3020–3036, 2016.

[SR21] Almudena Suarez and Franco Ramírez. Two-Level Stability Analysis of Complex Circuits. *IEEE Trans. Microw. Theory Techn.*, 69(1):132–146, 2021.

[SSCG20] Adel S. Sedra, Kenneth C. Smith, Tony Chan Carusone, and Vincent Gaudet. *Microelectronic Circuits*. Oxford University Press, 2020.

[Sua15] Almudena Suarez. Check the Stability: Stability Analysis Methods for Microwave Circuits. *IEEE Microwave Magazine*, 16(5):69–90, 2015.

[SWWH99] W. Simburger, H.-D. Wohlmuth, P. Weger, and A. Heinz. A Monolithic Transformer Coupled 5-W Silicon Power Amplifier with 59% PAE at 0.9 GHz. *IEEE J. Solid-State Circuits*, 34(12):1881–1892, 1999.

[TIT+21] Jeffrey W. Teng, Adrian Ildefonso, George N. Tzintzarov, Hanbin Ying, Arya Moradinia, Peng Fei Wang, Xun Li, En Xia Zhang, Daniel M. Fleetwood, and John D. Cressler. Variability in Total-Ionizing-Dose Response of Fourth-Generation SiGe HBTs. *IEEE Transactions on Nuclear Science*, 68(5):949–957, 2021.

[TKA+07] Saverio Trotta, Herbert Knapp, Klaus Aufinger, Thomas F. Meister, Josef Bock, Bernhard Dehlink, Werner Simburger, and Arpad L. Scholtz. An 84 GHz Bandwidth and 20 dB Gain Broadband Amplifier in SiGe Bipolar Technology. *IEEE J. Solid-State Circuits*, 42(10):2099–2106, 2007.

[TNH13] S. V. Thyagarajan, A. M. Niknejad, and C. D. Hull. A 60 GHz Linear Wideband Power Amplifier using Cascode Neutralization in 28 nm CMOS. In *Proceedings of the IEEE 2013 Custom Integrated Circuits Conference*, pages 1–4, 2013.

[TP20] Van-Son Trinh and Jung-Dong Park. Common-Mode Stability Test and Design Guidelines for a Transformer-Based Push-Pull Power Amplifier. *IEEE Access*, 8:42243–42250, 2020.

[TPB99] D. Teeter, A. Platzker, and R. Bourque. A Compact Network for Eliminating Parametric Oscillations in High Power MMIC Amplifiers. In *1999 IEEE MTT-S International Microwave Symposium Digest (Cat. No.99CH36282)*, volume 3, pages 967–970 vol.3, 1999.

[TVHK01] M. Tian, V. Visvanathan, J. Hantgan, and K. Kundert. Striving for Small-Signal Stability. *IEEE Circuits and Devices Magazine*, 17(1):31–41, 2001.

[UKA+21] Sandeep Ummethala, Juned N. Kemal, Ahmed S. Alam, Matthias Lauermann, Artem Kuzmin, Yasar Kutuvantavida, Sree H. Nandam, Lothar Hahn, Delwin L. Elder, Larry R. Dalton, Thomas Zwick, Sebastian Randel, Wolfgang Freude, and Christian Koos. Hybrid electro-optic modulator combining silicon photonic slot waveguides with high-k radio-frequency slotlines. *Optica*, 8(4):511–519, Apr 2021.

[vdHdGdV02] M.P. van der Heijden, H.C. de Graaff, and L.C.N. de Vreede. A Novel Frequency-Independent Third-Order Intermodulation Distortion Cancellation Technique for BJT Amplifiers. *IEEE J. Solid-State Circuits*, 37(9):1176–1183, 2002.

[VMR17] Marco Vigilante, Earl McCune, and Patrick Reynaert. To EVM or Two EVMs?: An Answer to the Question. *IEEE Solid-State Circuits Magazine*, 9(3):36–39, 2017.

[VR18] Marco Vigilante and Patrick Reynaert. A Wideband Class-AB Power Amplifier With 29–57-GHz AM–PM Compensation

in 0.9-V 28-nm Bulk CMOS. *IEEE J. Solid-State Circuits*, 53(5):1288–1301, 2018.

[WMT+17] Rui Wu, Ryo Minami, Yuuki Tsukui, Seitaro Kawai, Yuuki Seo, Shinji Sato, Kento Kimura, Satoshi Kondo, Tomohiro Ueno, Nurul Fajri, Shoutarou Maki, Noriaki Nagashima, Yasuaki Takeuchi, Tatsuya Yamaguchi, Ahmed Musa, Korkut Kaan Tokgoz, Teerachot Siriburanon, Bangan Liu, Yun Wang, Jian Pang, Ning Li, Masaya Miyahara, Kenichi Okada, and Akira Matsuzawa. 64-QAM 60-GHz CMOS Transceivers for IEEE 802.11ad/ay. *IEEE J. Solid-State Circuits*, 52(11):2871–2891, 2017.

[WSH10] Hua Wang, Constantine Sideris, and Ali Hajimiri. A CMOS Broadband Power Amplifier With a Transformer-Based High-Order Output Matching Network. *IEEE J. Solid-State Circuits*, 45(12):2709–2722, 2010.

[WW20] F. Wang and H. Wang. A 24-to-30GHz watt-level broadband linear doherty power amplifier with multi-primary distributed-active-transformer power-combining supporting 5G NR FR2 64-QAM with >19dBm average P_{out} and >19% average PAE. In *IEEE ISSCC*, pages 362–364, San Francisco, CA, USA, February 2020.

[WW21a] Fei Wang and Hua Wang. A Broadband Linear Ultra-Compact mm-Wave Power Amplifier With Distributed-Balun Output Network: Analysis and Design. *IEEE J. Solid-State Circuits*, 56(8):2308–2323, 2021.

[WW21b] Fei Wang and Hua Wang. A High-Power Broadband Multi-Primary DAT-Based Doherty Power Amplifier for mm-Wave 5G Applications. *IEEE J. Solid-State Circuits*, 56(6):1668–1681, 2021.

[WWW20] F. Wang, A. Wang, and H. Wang. A 22-37 GHz broadband compact linear mm-wave power amplifier supporting 64-/256-/512-QAM modulations for 5G communications. In *IEEE/MTT-S IMS*, pages 1105–1108, Los Angeles, CA, USA, August 2020.

[WYF+22] Yun Wang, Dongwon You, Xi Fu, Takeshi Nakamura, Ashbir Aviat Fadila, Teruki Someya, Atsuhiro Kawaguchi, Junjun Qiu, Jian Pang, Kiyoshi Yanagisawa, Bangan Liu, Yuncheng

Zhang, Haosheng Zhang, Rui Wu, Shunichiro Masaki, Daisuke Yamazaki, Atsushi Shirane, and Kenichi Okada. A Ka-Band SATCOM Transceiver in 65-nm CMOS With High-Linearity TX and Dual-Channel Wide-Dynamic-Range RX for Terrestrial Terminal. *IEEE J. Solid-State Circuits*, 57(2):356–370, 2022.

[YHKJ24] Byeongcheol Yoon, In Su Han, Junghyun Kim, and Inchan Ju. A Compact, Highly Linear Ku-Band SiGe HBT Power Amplifier Using Shared Single Center-Tap Four-Way Output Transformer Balun for Emerging Low Earth Orbit SATCOM Phased-Array Transmitter. In *2024 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 295–298, 2024.

[ZGS+23] Weisen Zeng, Li Gao, Ningzheng Sun, Hongtao Xu, Quan Xue, and Xiuyin Zhang. 25.2 A 19.7-to-43.8GHz Power Amplifier with Broadband Linearization Technique in 28nm Bulk CMOS. In *2023 IEEE International Solid-State Circuits Conference (ISSCC)*, pages 372–374, 2023.

[ZKR12] D. Zhao, S. Kulkarni, and P. Reynaert. A 60 GHz dual-mode power amplifier with 17.4 dBm output power and 29.3% PAE in 40-nm CMOS. In *2012 Proceedings of the ESSCIRC (ESSCIRC)*, pages 337–340, 2012.

[ZR15] D. Zhao and P. Reynaert. An E-Band Power Amplifier With Broadband Parallel-Series Power Combiner in 40-nm CMOS. *IEEE Trans. Microw. Theory Techn.*, 63(2):683–690, 2015.

[ZSV17] Alireza Zandieh, Peter Schvan, and Sorin P. Voinigescu. Linear Large-Swing Push–Pull SiGe BiCMOS Drivers for Silicon Photonics Modulators. *IEEE Trans. Microw. Theory Techn.*, 65(12):5355–5366, 2017.

[ZTK+20] Zhiwei Zong, Xinyan Tang, Khaled Khalaf, Dongyang Yan, Giovanni Mangraviti, Johan Nguyen, Yao Liu, and Piet Wambacq. A 28GHz Voltage-Combined Doherty Power Amplifier with a Compact Transformer-based Output Combiner in 22nm FD-SOI. In *2020 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 299–302, 2020.

[ZZ19] Dixian Zhao and Jiecheng Zhong. Design and Modeling of Millimeter-Wave Transformer in Silicon: A Tutorial (Invited).

In *2019 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*, pages 1–3, 2019.

Own Publications

Journal articles

[1] **Tsung-Ching Tsai**, Václav Valenta, and Ahmet Çağrı Ulusoy. Nonlinear Capacitance Effect on Stability and Stabilization of SiGe Power Amplifiers for 17.3–21.2 GHz SATCOM. *IEEE Trans. Circuits Syst. I*, 72(7):3176–3189, 2025.

Conference proceedings

[2] Yen-Wei Chang, **Tsung-Ching Tsai**, Jie-Ying Zhong, Jeng-Han Tsai, and Tian-Wei Huang. A 28 GHz Linear and Efficient Power Amplifier Supporting Wideband OFDM for 5G in 28nm CMOS. In *2020 IEEE/MTT-S International Microwave Symposium (IMS)*, pages 1093–1096, 2020.

[3] Yu-Chun Chen, **Tsung-Ching Tsai**, Jeng-Han Tsai, and Tian-Wei Huang. A 38-GHz-Band Power Amplifier with Analog Pre-distortion for 1600-MHz Transmission Bandwidth 64-QAM OFDM Modulated Signal. In *2019 IEEE MTT-S International Microwave Symposium (IMS)*, pages 312–315, 2019.

[4] Kun-Chan Chiang, **Tsung-Ching Tsai**, Ian Huang, Jeng-Han Tsai, and Tian-Wei Huang. A 27-GHz Transformer Based Power Amplifier with 513.8-mW/mm2 Output Power Density and 40.7% Peak PAE in 1-V 28-nm CMOS. In *2019 IEEE MTT-S International Microwave Symposium (IMS)*, pages 1283–1286, 2019.

[5] Tai-Yu Kuo, **Tsung-Ching Tsai**, and Ahmet Çağrı Ulusoy. A D-Band Mixer-First Receiver in 22-nm FD-SOI CMOS with Back-Gate Biasing for I/Q Imbalance Optimization. In *2024 19th European Microwave Integrated Circuits Conference (EuMIC)*, pages 134–137, 2024.

[6] **Tsung-Ching Tsai**, Christian Bohn, Joachim Hebeler, Mehmet Kaynak, and Ahmet Çağrı Ulusoy. A Linear and Efficient Power Amplifier Supporting Wideband 64-QAM for 5G Applications from 26 to 30 GHz in SiGe:C BiCMOS. In *2021 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 127–130, 2021.

[7] **Tsung-Ching Tsai**, Christian Bohn, and Ahmet Çağrı Ulusoy. 100-GBd Linear Optical Modulator Driver for Short-Reach Links in 130-nm SiGe:C BiCMOS. In *2023 18th European Microwave Integrated Circuits Conference (EuMIC)*, pages 113–116, 2023.

[8] **Tsung-Ching Tsai**, Ian Huang, Jeng-Han Tsai, Abdulelah Alshehri, Mazen Almalki, Abdulhamid Saved, and Tian-Wei Huang. A Ka-Band Sub-Harmonically Pumped Mixer Using Diode-Connected MOSFET for 5G MM-Wave Transceivers. In *2018 Asia-Pacific Microwave Conference (APMC)*, pages 488–490, 2018.

[9] **Tsung-Ching Tsai** and Ahmet Çağrı Ulusoy. A V-band Power Amplifier in 22-nm FD-SOI Supporting Instantaneous Broadband Data Transmission at 20 Gb/s. In *2025 16th German Microwave Conference (GeMiC)*, pages 459–462, 2025.

[10] **Tsung-Ching Tsai** and Ahmet Çağrı Ulusoy. A SiGe Common-Collector-Common-Base Linear Power Amplifier with 17–28-GHz P1dB 3-dB Bandwidth and Enhanced Large-Signal Stability. In *2025 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 287–290, 2025.

[11] **Tsung-Ching Tsai** and Ahmet Çağrı Ulusoy. Design of a 28-GHz SiGe Doherty Power Amplifier Using Meandered Coupled-Line Couplers. In *2026 17th German Microwave Conference (GeMiC)*, 2026.

[12] **Tsung-Ching Tsai**, Václav Valenta, and Ahmet Çağrı Ulusoy. Parametric-Oscillation-Free Efficient SiGe:C Power Amplifier Design for Ku-/Ka-Band SATCOM. In *2024 IEEE 24th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, pages 60–62, 2024.