

**An ultra-fast switch technology concept for future beam
transfer at CERN using impact ionization triggering of high
voltage thyristors**

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Kurzfassung

Im CERN-Teilchenbeschleunigerkomplex übertragen schnell gepulste Magnetsysteme den Teilchenstrahl zwischen den Beschleunigerstufen. Viele dieser Systeme verwenden Kickermagneten vom Typ Übertragungsleitung, um geladene Teilchen mit einem Magnetfeldpuls zu lenken, der eine gut definierte flache Spitze sowie schnelle Anstiegs- und Abfallzeiten aufweist. Einige Kickermagneten sind mit einem Kurzschluss abgeschlossen, um die Kickstärke für eine gegebene Systemimpedanz, Aperturgröße und Magnetlänge zu verdoppeln, indem der Strom im Kickermagneten verdoppelt wird. Die Impulsgeneratoren, die derzeit diese Kickermagneten antreiben, basieren auf Impulsformungsleitungen oder Impulsformungsnetzwerken und Thyatron-Schaltern. Aufgrund der Obsoleszenz der verwendeten Thyatron-Schalter müssen diese Impulsgeneratoren jedoch in naher Zukunft ersetzt werden.

In jüngsten Studien wurde gezeigt, dass die Aktivierung industrieller Thyristoren (die relativ langsame Schaltgeräte sind) im Überspannungsmodus, auch bekannt als Stoßionisationsmodus, ihre dU/dt - und dI/dt -Eigenschaften erheblich verbessern kann. Diese neue Aktivierungstechnik erfordert die Anwendung einer erheblichen Überspannung zwischen Anode und Kathode des Thyristors, die mit einer schnellen Anstiegsgeschwindigkeit von mehr als 1 kV/ns geliefert wird. Durch die Verwendung kompakter Impulsgeneratoren, die aus handelsüblichen Standardkomponenten (COTS) hergestellt werden, hat sich die Technologie neue Anwendungsmöglichkeiten in verschiedenen Bereichen eröffnet, einschließlich des Einsatzes von Hochgeschwindigkeits-Kickergeneratoren in Teilchenbeschleunigern.

In meiner Methodik habe ich handelsübliche Hochspannungs-SiC-MOSFETs zusammen mit einem speziell entwickelten schnellen Gate-Treiber verwendet. Dieser Treiber wurde auf der Grundlage neuer Gate-Boosting-Techniken konzipiert und bietet eine Treiberspannung von über 600 V. Der Gate-Treiber für diese MOSFETs besteht aus drei Hauptkomponenten: einem Pegelwandler mit NMOS- und PMOS-Transistoren, einem kompakten Marx-Generator mit zwei Lawinentransistoren und einem GaN-HEMT in einer Konfiguration mit hoher Eingangs- und niedriger Ausgangsimpedanz. Der vorgeschlagene Gate-Boosting-Treiber erreicht eine Anstiegsgeschwindigkeit von mehr als 1 kV/ns für den Treiberpuls.

Darüber hinaus zeige ich, dass ein mit diesem Treiber betriebener SiC-MOSFET mit einer Nennspannung von 1.7 kV einen Ausgangspuls von 1.45 kV und eine maximale Anstiegsgeschwindigkeit von etwa 2.5 kV/ns erzeugen kann. Dieser Gate-Boosting-Treiber zielt darauf ab, Schaltzeiten zu minimieren, eine Anstiegsgeschwindigkeit von über 1 kV/ns zu erreichen und höhere Lasten zu bewältigen. Der erzeugte Ausgangspuls wird dann in einem vierstufigen Marx-Generator, der aus kleinen, mit 1.2 kV bewerteten D2PAK-Thyristoren besteht, verstärkt und geschärft. Diese Konfiguration erzeugt einen Ausgangspuls mit einer Amplitude von 11 kV und einer Anstiegsgeschwindigkeit von 6.6 kV/ns.

Abstract

In the CERN particle accelerator complex, fast pulsed magnet systems transfer the particle beam between accelerator stages. Many of these systems use transmission line type kicker magnets to deflect charged particles with a magnetic field pulse that has a well-defined flat top and rapid rise and fall times. Some kicker magnets are terminated with a short-circuit to double the kick-strength for a given system impedance, aperture size, and magnet length by doubling the current in the kicker magnet. The pulse generators currently driving these kicker magnets are based on pulse forming lines or pulse forming networks and thyatron switches. However, due to the obsolescence of the thyatron switches, these pulse generators need to be replaced in the near future.

In recent studies, it has been shown that activating industrial thyristors (which are relatively slow switching devices) in overvoltage mode, also known as impact ionization mode, can significantly improve their dU/dt and dI/dt characteristics. This new activation technique requires the application of a substantial overvoltage between the thyristor's anode and cathode, delivered with a swift slew rate exceeding 1 kV/ns . By using compact pulse generators constructed from commercially available off-the-shelf components (COTS), the technology has opened up new possibilities for applying this technology in various fields, including the use of high-speed kicker generators in particle accelerators.

In my methodology, I employed commercially available high-voltage SiC MOSFETs along with a custom-designed fast gate driver. This driver was conceptualized based on recent gate boosting techniques, featuring a driving voltage exceeding 600 V . The gate driver for these MOSFETs comprises three key components: a level-shifter with NMOS and PMOS transistors, a compact Marx

generator with two avalanche transistors, and a GaN HEMT in a high input and low output impedance configuration. The proposed gate-boosting driver achieves a slew rate exceeding 1 kV/ns for the driving pulse.

Furthermore, I demonstrate that with this driver, a 1.7 kV rated SiC MOSFET can produce an output pulse of 1.45 kV with a maximum slew rate of approximately 2.5 kV/ns . This gate-boosting driver aims to minimize commutation times, achieve a slew rate over 1 kV/ns , and handle higher loads. The generated output pulse is then amplified and sharpened in a four-stage Marx generator composed of small, 1.2 kV rated D2PAK thyristors. This configuration yields an output pulse with an amplitude of 11 kV and a slew rate of 6.6 kV/ns .

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Acronyms and symbols

Acronyms

CERN	European Organization for Nuclear Research
COTS	Commercial Off-The-Shelf
CP	Capacitive Probe
CT	(X-ray) Computed Tomography
D2PAK	Double Decawatt Package (TO-263)
DFN	Dual Flat No-lead package
DSRD	Drift Step Recovery Diode
FCC	Future Circular Collider
FEMM	Finite Element Method Magnetics
FR4	Glass-epoxy PCB laminate (FR-4)
GaAs	Gallium Arsenide
GaN	Gallium Nitride
GaNPX	GaN Systems “GaN PX” package family
HEB	High Energy Booster
HEMT	High Electron Mobility Transistor

HF	High Frequency
HV	High Voltage
IGBT	Insulated-Gate Bipolar Transistor
IHE	Institute for High Frequency Technology and Electronics
II	Impact Ionization
LHC	Large Hadron Collider
LTspice	LTspice circuit simulator
MARX	Marx generator (impulse-adding topology)
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
PCB	Printed Circuit Board
PFL	Pulse Forming Line
PFN	Pulse Forming Network
RC	Resistor–Capacitor (network)
RCPS	Resonant Charging Power Supply
RG58	RG58 coaxial cable
RO4350B	Rogers 4350B high-frequency PCB laminate
SiC	Silicon Carbide
Si	Silicon
SMA	SubMiniature version A (RF connector)
SOA	Safe Operating Area
SPS	Super Proton Synchrotron

SEB	Single Event Burnout
SOS	Semiconductor Opening Switch
TRAPATT	Trapped Plasma Avalanche Triggered Transit (diode)

Constants

ε_0	Vacuum permittivity ($\approx 8.854 \times 10^{-12} \text{ F m}^{-1}$)
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Latin symbols and variables

A	Area
C	Capacitance
C_p	Probe capacitance (capacitive divider island)
C_c	Coupling/series capacitor in probe chain
d	Distance / gap spacing
E	Electric field strength
f	Frequency
I	Current
L	Inductance
ℓ	Length (line/trace/lead)
N	Number of stages / samples
P	Power
Q	Charge
R	Resistance

R_L	Load resistance (e.g., 50 Ω)
t	Time
t_r	Rise time (10–90 %)
U	Voltage (node/pulse amplitude)
U_{bias}	Bias voltage
U_{out}	Output voltage
V_{pp}	Peak-to-peak voltage
w	Width (e.g., microstrip)
x, y, z	Cartesian coordinates
Z	Impedance (complex)
Z_0	Characteristic impedance of a line
dU/dt	Voltage slew rate
dI/dt	Current slew rate

Greek symbols and variables

Γ	Reflection factor
ε_r	Relative permittivity
λ	Wavelength

Operators and math symbols

$\cdot$	Dot product
$\approx$	Approximately equal

<, >

Less/greater than

1 Introduction and motivation

Geneva, 1954: The European Organization for Nuclear Research (CERN) was founded. 22 member states from all over the world contribute to the scientific feat of improving our understanding of the world we live in. In order to support this mission, powerful tools like particle accelerators and colliders are built. These machines can accelerate particles to nearly the speed of light and collide them, to analyse the collision products and draw further scientific conclusions about the structure of matter. Over the years of CERN's existence several particle accelerators have been built, creating a chain of accelerators with increasing nominal energy at each step.

A single circular accelerator can only accelerate particles within a certain range of energy, which is why a chain of accelerators is needed to accelerate particles from rest energy up to 7 TeV (Breskin and Voss (2009)). An overview of the accelerator complex at CERN is drawn in Figure 1.1. Different machines of different sizes enable this complex to recreate a variety of experiments also by accelerating a versatile range of particles.

At its peak, the Large Hadron Collider (LHC), currently the biggest and most powerful particle accelerator in the world. Its nominal center of mass energy is 14 TeV (7 TeV for each of the counter rotating beams), and its planned operation time runs beyond 2030. Knowing that the design and construction of all the constituting elements spanned for about 30 years (Breskin and Voss (2009)), it seems reasonable that the planning of an accelerator post LHC time should already be starting shortly after the LHC commissioning.

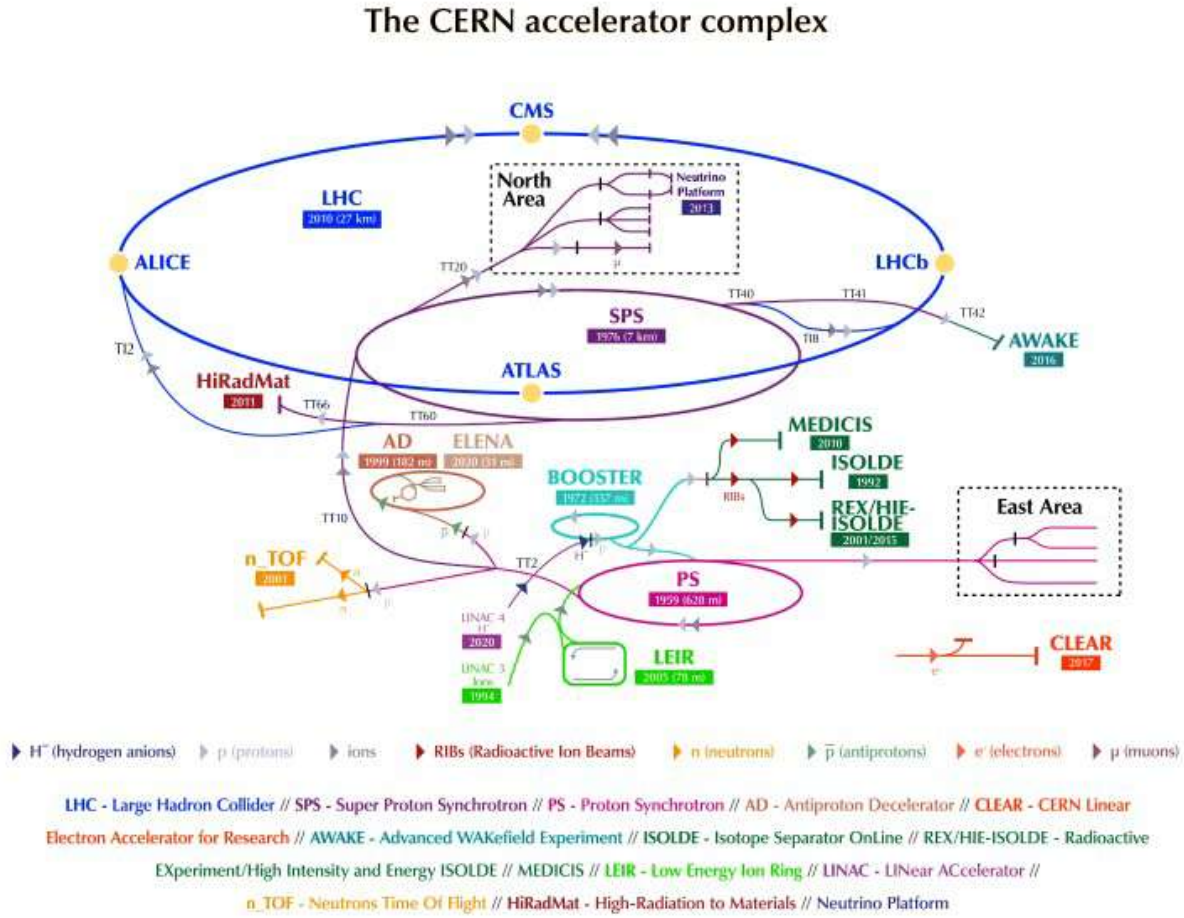


Figure 1.1: Accelerator complex at CERN (CERN (2025))

Said LHC successor is called the future circular collider (FCC), with a center of mass energy of 100 TeV. The FCC study, started in 2013, investigates the challenges of such a high energy hadron-hadron (hh) collider.

At such grand center of mass energies, one of the big challenges for this new accelerator will be the injection of the particle beams from the pre-accelerator, also called high energy booster (HEB), into the FCC. Different HEB options are studied, with respective pros and cons: LHC's beam energy of 3.3 TeV, upgrading the super proton synchrotron (SPS) superconducting magnets to reach an energy of up to 3.3 TeV, and finally a pre-accelerator, placed in the same tunnel as the FCC. The baseline is an injection energy of 3.3 TeV provided from the LHC (Benedikt et al. (2019), Renner and et al. (2018)).

Accounting for machine protection, a fast and reliable injection system as well as extraction and disposal systems are key components in any accelerator complex. Injection and extraction of the beams rely on very fast and high power pulse generators. At CERN's complex, the energies reached call for unconventional solutions, fundamentally different from traditional ones.

The conventional pulse generators employed at CERN, such as Pulse Forming Lines (PFL) and Pulse Forming Networks (PFN), typically utilize thyratrons for switching high voltage and high current pulses.

A PFL serves as a transmission line that shapes and delivers high-voltage pulses to the intended load. It comprises various components, including energy storage elements, switching elements, and pulse shaping components. The primary function of the PFL is to store electrical energy and transmit it to the load in a controlled manner. By manipulating impedance, timing, and other parameters along the transmission line, the PFL shapes the pulse waveform (Bluhm (2006)). Conversely, a PFN refers specifically to an energy storage and shaping circuit commonly employed within a pulse forming line. It consists of a network configuration comprising inductors, capacitors, and other components. The PFN stores electrical energy from a power source, such as a charging capacitor bank, and delivers it to the load in the form of a shaped pulse. The components within the PFN are designed to adjust the rise time, duration, and amplitude of the pulse.

Thyratrons, being plasma switching devices, can experience pre-triggering, leading to an inadvertent kick of the beam. As the energy of the accelerator increases, the potential danger posed by a mis-kick of the beam escalates, necessitating its prevention to avoid any subsequent damage to downstream equipment. To address this concern, a novel design for a pulse generator is proposed, utilizing solid-state semiconductor switches as a viable alternative to thyratrons.

Recent investigations have shown that standard thyristors triggered in impact ionization (II) mode can outperform thyratrons (Gusev et al. (2019b)) for low repetition rate applications. Impact ionisation is achieved by applying a high dU/dt , which creates an ionisation wavefront in the depletion zone moving at the

speed higher than charge carriers velocity and leaving behind it dense electron-hole plasma homogeneously spread over the volume of the semiconductor. This phenomenon will be further described in Section 2.5.

By implementing Impact Ionization on out-of-the-shelf, industrial thyristors, their commutation speed would outperform that of a thyatron; whilst allowing higher current than similarly sized thyatrons. Another advantage of the use of thyristors in this mode is a significantly lower price compared to the traditional solutions.

To trigger such a device in II mode, the voltage applied to the thyristor needs to reach more than double of its static breakdown voltage with a slew rate of $\geq 1\text{ kV/ns}$, while providing an output current sufficient to charge the parasitic capacitance of the thyristor with the required dU/dt (Gusev et al. (2019a), Lavrinovich et al. (2022)).

To sum up, the aforementioned advantages of this new approach make the impact ionization-based approach not only interesting for kicker systems in future accelerators but also as a replacement in pre-existing systems to reduce maintenance costs and profit from this new technology.

This dissertation documents the development, design and construction as well as the initial testing of an innovative pulse generator, reports the results and gives an overview of the challenges faced throughout the process. Finally this work outlines future leads for this project.

1.1 Outline of the document

The document begins with Chapter 1, Introduction and Motivation, providing an overview of the thesis and its objectives.

Chapter 2 focuses on Pulsed Systems, discussing various components such as Thyatron Switches, Pulse Forming Line or Network, Marx Generator, and Semiconductor-based Designs and their limitations. The Impact Ionization (II)

Principle is explored, along with the concept of Ultra-Gate Boosting of Semiconductors.

Following that, Chapter 3, Conceptual Design, elaborates on the design aspects of the thesis. It covers the different parts of the design, including the Booster, Driver, High Voltage Super-Boosted SiC MOSFET, and Marx Generator. Chapter 3.5 examines the use of Thyristors in impact ionization, and Chapter 3.6 proposes a future prototype.

Chapter 4, Measurement Results on the Prototype, presents the findings from the measurements conducted on the prototype, specifically focusing on the Booster, Driver, SiC MOSFET, GaAs Diode/Thyristor Marx generator, and the challenges faced during the measurements.

Finally, Chapter 5, Conclusions and Outlook, summarizes the key findings and provides an outlook for future developments.

2 State of the art

2.1 Pulsed systems

Pulsed power can be defined as the technology that accumulates a certain amount of energy and then releases it in very short times, resulting in a significant increase in the instantaneous power of a system.

Particle accelerator facilities, such as those at the European Organization for Nuclear Research (CERN), depend heavily on pulse generators to effectively transfer particle beams. These systems require high voltage levels exceeding 20 kV and high current levels surpassing 10 kA. The accelerator chain at CERN operates in stages, with each one progressively increasing the particle energy before passing them to the next accelerator. As a consequence, the pulsed magnets in the transfer lines must generate extremely fast and precisely controlled magnetic fields, with rise times of less than 100 ns for the fastest magnets (Barnes (2018)). Reaching this degree of speed and accuracy requires the use of ultra-fast pulse generators.

This work presents an innovative approach to such pulse generators, with the objective of exploring their applications within CERN's systems—particularly in the injection and extraction lines. These systems rely on kicker magnets, which require precise pulsed magnetic fields to deflect the particle beam either toward the next accelerator stage or into a beam dump. To meet the diverse requirements of different kicker systems, various pulse generator designs based on different technologies are employed. Some of these designs are discussed in the following sections.

While the ultimate goal is to develop a solution for application in CERN's beam transfer systems, the current focus is on fundamental research, proposing a novel approach for triggering in the sub-nanosecond scale.

2.2 Thyatron switches and pulse forming line or network

A practical and common way to generate a pulse is by storing energy in a network of inductors and capacitors and discharging it via a switch—in this case, a thyatron. The energy storage can either be in a coaxial cable, known as a pulse forming line (PFL), or implemented with lumped elements, then called a pulse forming network (PFN).

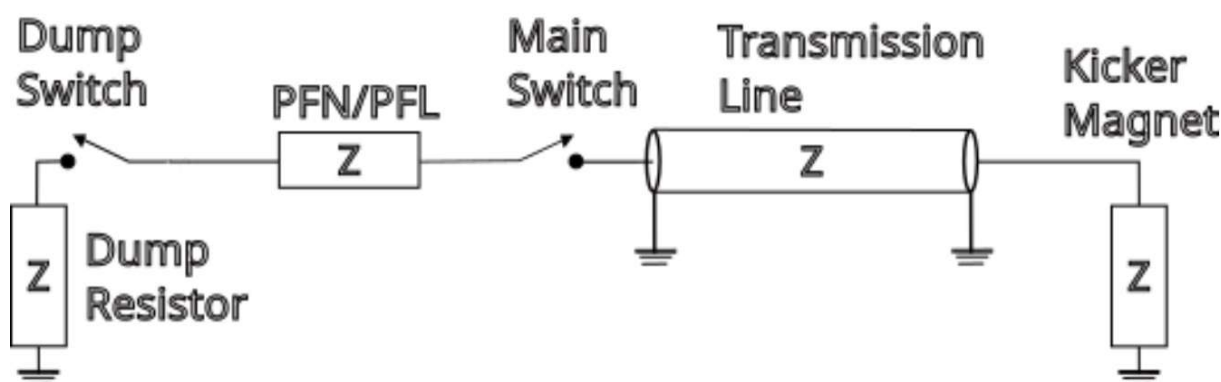


Figure 2.1: Schematic drawing of a kicker system with a PFN or PFL in short-circuit operation with dump switch and dump resistor (Barnes (2017))

Historically, pulse power systems at CERN have relied on PFLs and PFNs to supply energy to kicker magnets (Benedikt et al. (2004)). As illustrated in Figure 2.1, once the resonant charging power supply (RCPS) charges the energy storage element to its working voltage, the main switch connects it via a transmission line to the kicker magnet. An essential component of any PFN/PFL-based pulse generator is the high-voltage closing switch that discharges the energy storage into the load.

Such setups generally incorporate at least one high-voltage switch, which may be an IGBT module, a thyristor, or a thyatron (Bordry et al. (2020)). Thyatrons, in particular, stand out for their ability to control switching characteristics with precision. Combined with their rapid switching times and strong reliability, this

makes them well-suited for applications requiring both high current and high voltage.

These benefits, however, come with notable drawbacks. Thyratrons require intricate triggering and biasing circuits, are relatively expensive, and are increasingly difficult to source due to limited market availability. Additionally, they tend to be bulky, often require oil cooling, and pose a risk of erratic triggering events (Frank et al. (2007), Barnes et al. (2015a), Senaj et al. (2021a)).

As a result of these limitations, there is growing interest in exploring alternative systems that use solid-state devices or other switching technologies capable of providing more reliable, compact, and cost-effective solutions for pulsed power applications.

2.3 Semiconductor based designs

The common point for all pulse generators is their dependence on the switch for overall performance. It is evident that the energy stored in a system cannot be delivered faster than the switching device and circuit layout allow.

Semiconductor devices such as thyristors, IGBTs, and MOSFETs offer a new range of possibilities for pulsed power systems. While individually these components may have lower voltage and current ratings than traditional gas-based switches, such as thyratrons, their performance can be enhanced through parallel or series configurations. As a result, semiconductor-based systems are emerging as strong candidates to replace thyratrons in many applications. The continued advancement in Si and SiC device manufacturing has led to faster switching speeds and improved characteristics (Fujimoto et al. (2017)), with modern components capable of handling pulsed currents up to several hundred amperes and blocking voltages up to 3.3 kV (Masuda et al. (2018)).

In comparison to silicon devices of similar voltage class—particularly Si IGBTs with a fixed on-state voltage and earlier-generation Si MOSFETs—modern SiC MOSFETs exhibit a significantly lower effective on-state drop (i.e., reduced $R_{DS(on)}$ at the same current), which minimizes conduction loss and pulse droop; this is especially advantageous in low-impedance kicker pulse generators (Barnes and et al. (2018), Barnes (2018)).

Insulated-Gate Bipolar Transistors (IGBTs), for example, are widely used in high-power switching applications due to their capability to perform both opening and closing operations (Lehr and Ron (2017)). Although their rise time is not optimal for ultra-fast switching, they excel in power electronics where moderate switching speeds are acceptable. A nanosecond-pulse generator using IGBTs in parallel has been proposed for generating high-voltage nanosecond pulses (Huiskamp et al. (2013)). While effective in managing high power for rapid and repeated pulses, such solutions become impractical for applications demanding tens of kilovolts and kiloamperes due to their increased size and complexity.

Another approach to high-voltage pulse generation is the inductive adder, as described in Barnes et al. (2015a,b). This solid-state modulator uses multiple transformers with 1:1 turn ratios connected in series. It combines key components such as semiconductor switches (e.g., IGBTs or MOSFETs), capacitors for energy storage, diode clamps to suppress voltage spikes, and gate drivers for switch control. The inductive adder's modular architecture simplifies maintenance and customization, but its bulkiness and susceptibility to transformer magnetic saturation limit its application in constrained environments. Additionally, increasing the number of modules raises the system's impedance, making impedance matching and system tuning more complex.

A third method involves Marx generators based on SiC MOSFETs, which are optimized for extremely fast switching. These systems can achieve nanosecond-scale rise and fall times while delivering high voltage and current (Redondo et al. (2019)). A major benefit is the use of compact, off-the-shelf (COTS) components, which reduce parasitic inductance and facilitate high-speed operation. Nonetheless, component stress and synchronization challenges grow with each added stage, complicating scalability and potentially affecting reliability and lifespan.

Solid-state thyristor switches have also demonstrated dependable performance in accelerator applications (Sanders et al. (2012)). They offer a combination of moderate switching speeds, low conduction losses, high reliability, and long operational lifetimes (Hegeler et al. (2011)). Their ability to handle significantly higher currents than other semiconductor devices makes them ideal for power-heavy applications. However, integrating them effectively requires a sophisticated support system, including snubbers, fast gate drivers, and tailored triggering mechanisms. Kicker systems demand sub-100 ns field rise times (Barnes (2018)). Standard industrial thyristors—i.e., phase-control/inverter-grade SCRs operated in their conventional gate-triggered mode—have turn-on/settling times in the microsecond range and therefore cannot meet this requirement (Littelfuse (2022)).

To address this limitation, recent studies have explored triggering thyristors using overvoltage, or impact ionization mode (Gusev et al. (2019b)). These methods have shown potential for enabling sub-nanosecond switching times by applying

fast-rising pulses that temporarily exceed the device's nominal breakdown voltage. This technique facilitates a near-instantaneous transition from blocking to conducting state, making it promising for high-speed, high-voltage applications. A more detailed explanation of this mode of operation is provided in Section 2.5.

2.4 Limitations

Slowly during the past decades, the pulse generators at CERN have faced increasing difficulties to source various components, namely for thyratrons. Their cost has increased significantly ($\approx 20,000$ CHF) due to the pricing policy of the manufacturer and the very limited number of suppliers (Woog et al. (2018)). Additionally, the possibility of erratic triggering is a limitation of thyatron-based pulse generators. Plasma switches such as thyratrons carry a risk of spontaneous ignition even without a trigger signal, leading to non-synchronized pulse generation (Huang et al. (2013)) and potentially causing a mis-kick in the accelerator. In high-energy machines like the LHC, where the beam stores enormous energy (350 MJ per beam at 7 TeV luminosity, Holma et al. (2012)), such mis-kicks are unacceptable and pose a serious risk to machine protection and availability (Barnes et al. (2015a), Kramer et al. (2016)).

Aside from erratic behavior, thyratrons also suffer from inherent physical drawbacks. These include bulky designs due to the need for gas-filled enclosures, high-voltage insulation, and oil cooling systems. Their operational lifetime is limited by electrode wear and gas contamination, leading to high maintenance demands and relatively frequent replacement cycles. Moreover, the long turn-on delay and jitter compromise the precise timing requirements of modern accelerator systems.

As a result, there is increasing motivation to transition to solid-state alternatives. The semiconductor industry has made significant strides in recent years, with modern Si and SiC-based switches now reaching current ratings of several hundred amperes and blocking voltages of up to 3.3 kV. Additionally, switching speeds have improved significantly, bringing them into a range suitable for accelerator applications. These advancements, paired with the aforementioned limitations of gas-based switches, make solid-state topologies highly attractive for the design of robust, low-maintenance, and high-performance pulse generators.

However, solid-state solutions also face challenges. Achieving extremely fast rise times often demands series and/or parallel configurations of switching devices,

which introduces complexity in trigger synchronization and increased design overhead. In Marx-type topologies or pulse forming networks using semiconductor switches, precise and simultaneous turn-on of multiple stages is critical to preserve pulse shape and timing. Improper synchronization can lead to voltage sharing issues, pulse distortion, or even device failure.

Moreover, transmission line-based pulse generators are subject to signal degradation due to magnetic interference and parasitic capacitance—effects that are especially problematic in high-frequency regimes (Ranjan et al. (2024)). These parasitic phenomena introduce losses, reduce edge sharpness, and compromise pulse integrity. To mitigate these issues, this thesis employs microstrip transmission lines, which offer reduced parasitic capacitance and improved impedance control compared to conventional coaxial or parallel-plate structures. This choice helps ensure minimal signal distortion and precise timing in fast-switching circuits.

In response to the limitations discussed above, this thesis explores an innovative approach for building a semiconductor-based pulse generator that relies on the principle of impact ionization wave triggering in commercial thyristors. This method enables sub-nanosecond switching by applying high-voltage, high- dU/dt trigger pulses capable of initiating an ionization front within the device. Such a mechanism enables ultra-fast transitions from the blocking to the conducting state, making it suitable for applications requiring high voltage, high current, and extremely fast rise times.

While not intended as a complete turnkey replacement for existing kicker systems, the proposed design is intended to demonstrate the feasibility of such a solution, and to show its suitability for demanding high-power, fast-switching environments, such as those found in CERN's accelerator complex.

The design and construction of the prototype are detailed by the author in the publications listed in the List of Publications (A.2).

2.5 The Impact Ionization (II) principle

Impact ionization is a carrier multiplication process that occurs in regions of high electric field. When charge carriers are exposed to such fields, they gain significant energy and can collide with bound electrons in the valence band, liberating them and generating additional free carriers (Triebl (2012)). For this to occur, the electric field must exceed a threshold that enables carriers to break atomic bonds. Once triggered, this process can result in an avalanche effect, where the carrier density increases rapidly. The likelihood of initiating this process depends on parameters such as the local electric field strength, which directly influences the ionization rate (Hasan et al. (2019)).

Impact ionization was first observed at the Ioffe Institute in 1979, when a fast-rising reverse voltage was applied to a silicon structure. This caused the formation of an ionization front that rapidly generated a dense electron-hole plasma, rapidly driving a reverse-biased p-n junction into conduction within sub-nanosecond time scales (Rodin et al. (2007)).

Since its discovery, impact ionization triggering has been demonstrated in numerous semiconductor devices, including dynistors, TRAPATT diodes, thyristors, Si and SiC diodes, and GaAs diodes. This phenomenon continues to be a subject of active research, particularly for its role in ultra-fast switching applications.

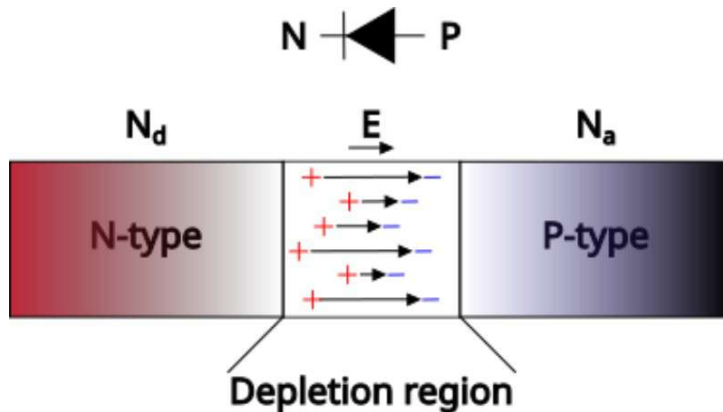


Figure 2.2: Idealized pn junction. Space charge (depletion) region at equilibrium; E represents the electric field (El-Kareh and Hutter (2020))

To understand front propagation in this context, consider two ideally uniform N- and P-type silicon regions brought into contact. As shown in Fig.2.2, a depletion region forms at the abrupt junction due to carrier diffusion, which establishes a built-in electric field E and potential V_{bi} . This depletion region contains relatively few free carriers and is dominated by ionized dopants, which generate the space charge. When an impact ionization front propagates into this region, it does so by rapidly multiplying carriers through avalanche breakdown, effectively collapsing the electric field in its path (Rodin et al. (2007)).

While this process can cause permanent damage under some conditions—due to localized heating and high current densities—recent studies show that, when operated at high switching frequencies with sharp voltage ramps, semiconductor devices can survive the triggering process without structural damage (Gusev et al. (2019a), Rodin et al. (2010)).

This triggering technique involves applying a fast voltage ramp (dU/dt) together with an over-voltage—typically more than twice the DC breakdown voltage—across the thyristor. This initiates an avalanche multiplication process that generates an ionization front (Grekhov (2010)). If the front propagates faster than the drift velocity of carriers, the phenomenon is referred to as **impact ionization**.

The result is ultra-fast switching using commercially available thyristors that can rival or surpass the performance of gas-based devices like thyratrons in both speed and current density handling (Grekhov et al. (2008b), Nakamura et al. (1993)). Once triggered, thyristors can conduct continuously, making them more efficient for sustained high-current applications compared to thyratrons, which are limited by gas volume and require bulky enclosures.

To initiate impact ionization in four-layer devices like thyristors, the triggering circuit must apply a voltage exceeding twice the breakdown voltage and achieve slew rates beyond 1 kV/ns (Gusev et al. (2014), Shahriari et al. (2023)). The driver must also provide sufficient current to charge the parasitic capacitance at this rate.

Several studies have investigated fast opening switches—like Drift Step Recovery Diodes (DSRDs) and Semiconductor Opening Switch (SOS) diodes—as potential trigger sources for impact ionization (Grekhov and Mesyats (1999), Degnon et al. (2023)). However, these technologies are hindered by limited commercial availability, bulky designs, and long pre-charging times that introduce delays exceeding 500 ns (Yan et al. (2020)).

Alternative solutions, such as the spiral generator, leverage compact spiral/vector inversion stripline architectures to generate high-speed pulses (Lavrinovich et al. (2022), Yan et al. (2021)). Although more compact than other high-voltage generators, scaling them remains challenging due to size and efficiency tradeoffs.

Parallel to the present work, a different driver-centric approach has arisen. The work by Shang et al. (2023) includes the use of a 60-stage avalanche transistor Marx generator to achieve the necessary high dU/dt trigger signal for impact ionization wave mode on thyristors. While the aforementioned work synthesizes the required over-voltage with a high-stage avalanche-transistor Marx driver, the hereby presented driver is constituted by a compact hybrid chain (avalanche pre-driver $\rightarrow$ GaN current booster $\rightarrow$ super-boosted SiC MOSFET), reducing stage count (del Barrio Montañés et al. (2023), Senaj et al. (2021b, 2022), del Barrio Montañés et al. (2024a)). This driver chain is capable of achieving output pulses of 1.45 kV and slew rates up to 2.5 kV/ns (del Barrio Montañés et al. (2024b)). These enhancements aim to improve voltage, current, and edge speed, ultimately supporting thyristor triggering via impact ionization wave mode (Shahriari et al. (2023, 2024)).

The primary motivation behind the research at hand is to develop a reliable, compact, and ultra-fast alternative to thyratrons for high-power pulse applications. In such systems, trigger timing is critical, as misfires can lead to operational failures. The objective is to minimize the delay between the trigger signal and the energy delivery event. While alternatives such as spiral generators or SOS-based architectures exist, a comparative analysis shows that these solutions are not optimal for applications such as emergency beam dumps at CERN. In particular, SOS diode-based generators introduce delays due to the time needed for plasma

formation (Kim et al. (2020)), which makes them unsuitable for trigger systems that demand immediate reaction. Spiral generators, on the other hand, pose challenges in terms of integration and scalability.

Recognizing these limitations, this ongoing research aims to further develop triggering methods specifically tailored to large commercial thyristors. Previous results have shown the feasibility of impact ionization wave switching, and the current focus lies in increasing output voltage and slew rate to ensure reliable, repeatable triggering.

Ultimately, this approach targets sub-nanosecond response and switching times with dU/dt values exceeding 1 kV/ns, fully aligning with requirements for impact ionization triggering in thyristors (Grekhov (2010), Shahriari et al. (2023), Gusev et al. (2014, 2019b)). The hereby presented research builds on prior works and sets the foundation for further development of solid-state replacements for traditional gas-based switches.

In summary, the conditions required to induce impact ionization in a device are:

- An applied bias voltage significantly exceeding the static breakdown voltage.
- A fast voltage ramp (high dU/dt)—typically in the range of 1 kV/ns or more.
- Sufficient available current to sustain the initiation and propagation of the ionization front.

2.6 Gate boosting of semiconductors

The following section discusses the issue of parasitic inductance in MOSFET devices, which hinders fast gate charging and thus limits the speed of turning the device on. In addition to inductive effects, parasitic capacitances inherent to the device's MOS structure also play a significant role by requiring rapid charge transfer to reach the necessary gate voltage. Various methodologies have been proposed to mitigate these parasitic elements, though they often introduce additional complexity to the circuit. The proposed design focuses on an ultra-gate boosting circuit that addresses both inductive and capacitive parasitics without the need for extra active components.

Problematic: When triggering a MOSFET device, its leads and bond wires introduce additional parasitic inductance into the gate drive circuit. This conforms a second order low-pass filter because of the parasitic inductance and the gate capacitance. As such, it hinders fast gate charging, which would allow for a faster turn-on of the device.

This issue has been addressed before in Hochberg et al. (2016), with two predominant methodologies:

- Higher gate-drive voltage (charge-boosting): a brief, elevated-voltage pulse into the gate (e.g., from a charged capacitor) followed by a lower steady-state level, to accelerate charge transfer during the Miller plateau.
- Current-source gate drivers: drivers that impose a controlled gate current (often different for turn-on and turn-off) to set dU/dt and dI/dt precisely (Fu et al. (2012), Shahane and et al. (2024)).

The downside of CSG approaches, as implemented in the literature, is the need for additional active circuitry—typically a high-speed error amplifier or transconductance stage, current mirrors, sensing elements, and sometimes auxiliary supplies or level shifting—which increases complexity and component count. By contrast, the driver used in Hochberg et al. (2016) achieves the required gate-charge

injection with a higher gate-driver voltage. The commutation speed of silicon IGBTs and MOS transistors is increased by triggering pulses with up to 80 V amplitude. This high amplitude is necessary to counterbalance the effects of their leads inductance and internal parasitic capacitances.

In this work, this effect is enhanced by a charge-boosting chain (avalanche pre-driver → GaN current booster → super-boosted SiC MOSFET); which, similarly to the original gate-boosting concept, does not include additional active elements besides the drive voltage source.

Since the target applications for this project —CERN kicker systems— reach up to 10^8 pulses during their entire working lifetime, a more aggressive triggering approach can be considered. In exchange, this would potentially reduce the component lifetime, making it necessary to find a tradeoff between its fast performance, its lifetime and compatibility with the kicker system lifetime.

2.6.1 Design rule and sizing of the series coupling capacitor

In the MOS triggering methodology, the only parameter that is strictly observed is the total injected MOS gate charge (Q_{tot}). It is limited to a value extrapolated from the component datasheet Q_{tot} curve at its maximum authorised gate-source voltage (U_{gs}) (see Fig. 2.4). This condition can be automatically fulfilled by a series capacitor (C_s in Fig.2.3) between the driver output and the MOS gate.

As C_s is in series with the MOS gate, the charge stored on it is equal to the charge delivered to the gate. This ensures that all the energy initially stored in the capacitor is transferred to the MOS gate during the switching event. Equation 2.1 describes the calculation method for the value of C_s . Said method is then adapted for each one of the devices, that have been used in gate-boosting configuration.

$$(U_{dr_{max}} - U_{g_{max}}) \cdot C_s = Q_{tot}(@U_{g_{max}}) \quad (2.1)$$

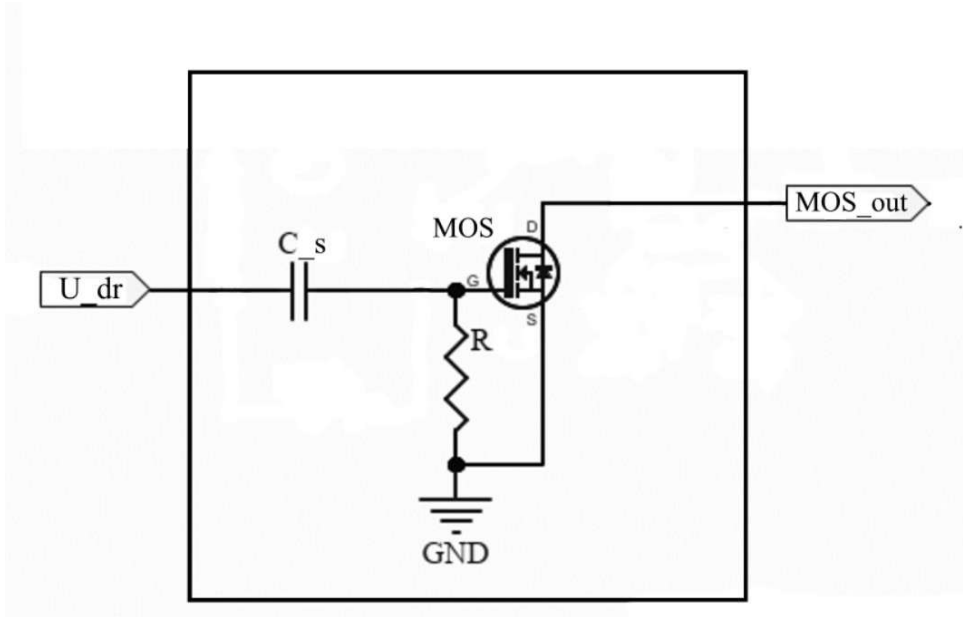


Figure 2.3: Minimal schematic of the gate-boosting method with a series capacitor. The driver injects charge through the series capacitor into the gate.

where:

1. $U_{dr_{max}}$ represents the maximum output voltage of the gate driver circuit.
2. $U_{g_{max}}$ is the absolute maximum allowable gate-source voltage (derived from the corresponding datasheet).
3. C_s is the value of the series capacitor between the driver output and the corresponding MOS gate.
4. $Q_{tot}(@U_{g_{max}})$ denotes the total gate charge extrapolated from the datasheet curve at the maximum gate voltage (Figure 2.4).

This equation is based on three assumptions (Senaj et al. (2021a)):

1. Q_{tot} follows a linear progression with the gate-applied voltage and can be extrapolated as per Infineon (2020).
2. All relevant voltages are initially zero before triggering.
3. After the MOS reaches complete turn-on, the driver output voltage becomes $U_{dr_{max}}$, the MOS transistor gate-source voltage reaches $U_{g_{max}}$, and the

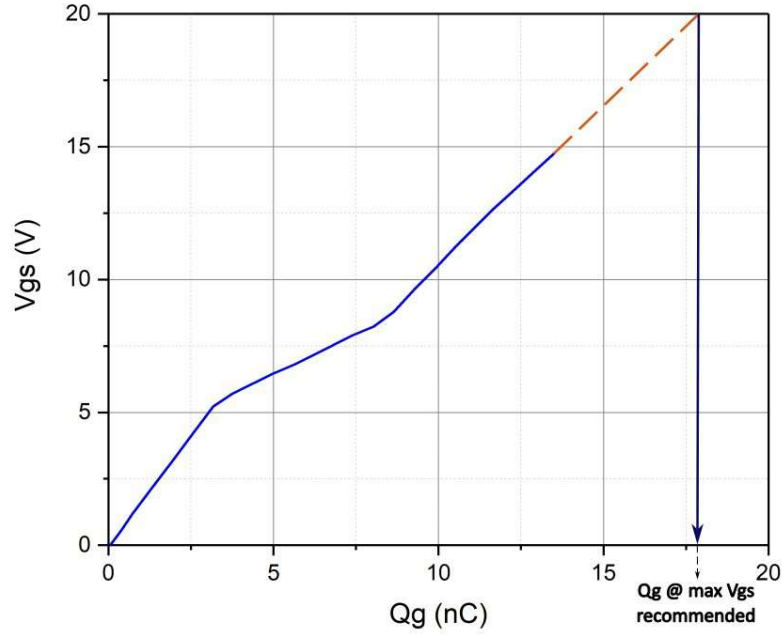


Figure 2.4: Extrapolation of values of Q_g at 20 V Infineon (2020)

series capacitor accumulates a charge of $(U_{dr_{max}} - U_{g_{max}}) \cdot C_s$. Since C_s is in series with the MOS gate, an equivalent charge is delivered to the MOS gate. While acknowledging a transient period and brief over-voltage on the gate, these are considered acceptable.

The transient period is defined as the short interval immediately after the driver edge during which the series capacitor C_s injects a bounded charge packet into the gate so that U_{gs} briefly exceeds its steady drive level, and then naturally decays as the coupling capacitor re-biases. This is the intended behaviour of AC-coupled/series- C gate drives: they deliver a transient overdrive while blocking DC, which has been used explicitly in earlier AC-coupled gate-driver implementations for fast Si/SiC devices (Lehmann et al. (2012)).

Gate-oxide wear-out follows time-dependent dielectric breakdown (TDDB) kinetics, where lifetime decreases strongly with electric field stress and stress duration (Baliga (2018), Borja et al. (2016)). Keeping the over-voltage pulse extremely short minimizes the time-integral of oxide stress and the injected/transported

charge, reducing TDDDB risk while still providing the fast charge delivery needed for $> 1 \text{ kV/ns}$ switching. A limited duration of the over-voltage on the gate-source insulator ($< 1 \text{ ns}$) is accepted.

In order to achieve an efficient gate boosting by this principle, the driver output slew rate needs to be very high. By implementing this approach, a suitably high voltage at the gate of the MOS device is guaranteed.

2.7 Marx generator

The Marx generator, patented by Erwin Marx in 1923, is a widely used multi-stage pulse generator designed to deliver high-voltage pulses by charging capacitors in parallel and subsequently discharging them in series (Marx (1923)). A typical configuration is depicted in Figure 2.5. In this setup, each stage contains a capacitor C_i that is charged through resistors R_{i1} and R_{i3} . Once the spark gaps (SG) are triggered, the capacitors discharge through R_{i2} , producing an output voltage equal to the cumulative sum of all n individual stages (Beyer et al. (1986)).

During its early development, triggered spark gaps were the dominant switching elements in Marx generators, delivering nanosecond-scale pulses with typical rise times in the tens of nanoseconds (application-dependent geometry and gas), while modern variants achieve few-nanosecond and even sub-nanosecond transitions (Excelitas (2011), Yang et al. (2008), Tang et al. (1981)).

For accelerator kicker modulators and similar high-reliability pulsed-power systems, the balance increasingly favors solid-state switching because it offers deterministic timing/jitter, high repetition-rate control, and lower maintenance; accordingly, the FCC injection and extraction systems specify solid-state generators for reliability (Barnes et al. (2019)). In parallel, reviews of Marx technology document a broad shift toward solid-state Marx generators (MOSFETs, IGBTs, thyristors) driven by device advances and the need for flexible pulse shaping—while noting that the optimal switch still depends on the application and load (Zhong et al. (2021)).

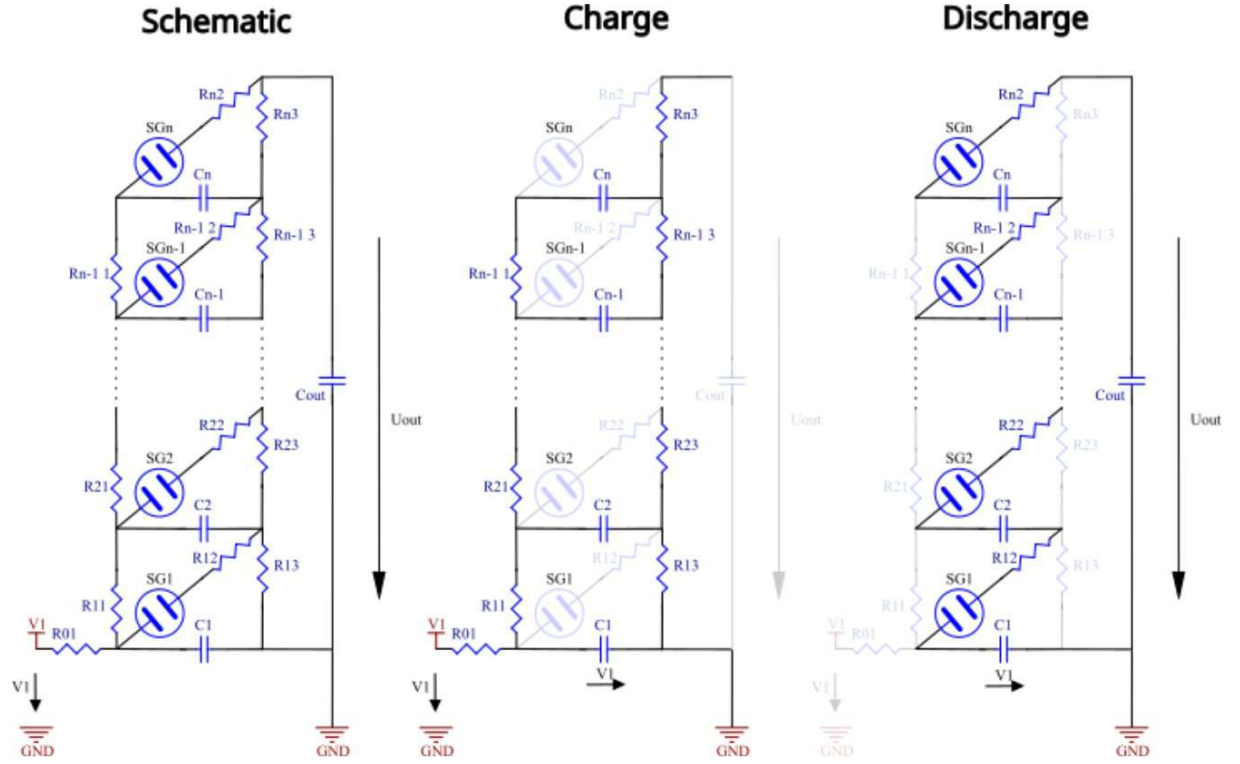


Figure 2.5: Schematic of a Marx generator, with its charge and discharge phases

Through innovative configurations and careful design, these solid-state Marx generators can match or even exceed the performance of traditional gas-based switches like thyratrons in terms of voltage output, current handling, and fast rise times (Perez et al. (2018)).

In the context of this thesis, the Marx generator serves as the voltage-boosting stage for the stripline-based pulse generator described in Chapter 4. By replacing the spark gaps with semiconductor components, a Marx-like topology is implemented using off-the-shelf devices such as silicon (Si) thyristors. This approach enables the delivery of high voltage and current with sub-nanosecond switching times (del Barrio et al. (2021), del Barrio Montañés et al. (2023, 2024a,b)). A more detailed discussion of the implementation is provided in Chapter 4.

3 High voltage measurement - the Capacitive Probe

3.1 Measurement Approach and Justification

During the testing of the pulse generator, the measuring equipment presented significant challenges, particularly with the standard high-voltage (HV) and high-frequency (HF) attenuators. These devices began to experience breakdowns when subject to output voltages surpassing 6 kV, as explained in Senaj et al. (2022).

To address this issue cost-effectively, an alternative method is used, namely capacitive probes, to measure the output voltages. This adjustment mitigated escalating voltage levels and provided a more suitable and robust measurement configuration, as capacitive probes are capable of withstanding elevated voltage thresholds. This approach ensures the preservation of the oscilloscope's and attenuator's integrity by reducing the voltage that reaches said measurement equipment.

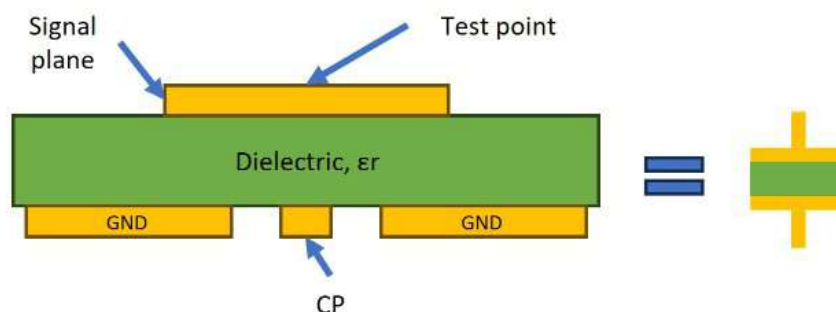


Figure 3.1: A capacitive probe on a PCB can be interpreted as a capacitor.

Capacitive probes offer the advantage of non-contact voltage measurement, thereby preserving the integrity of the oscilloscope and attenuator by reducing the voltage that reaches these sensitive instruments (Baxter (1997)). Their application is well-established within the pulsed power community for testing high-voltage, fast pulses (Novac et al. (2018)), and they have been successfully developed in laboratories utilizing printed circuit board techniques (van Oorschot and Huiskamp (2023)).

Beyond the aforementioned techniques, the present implementation includes several details tailored to sub-nanosecond, kilovolt-class pulses and to this Marx environment: (i) a PCB-integrated pickup with fixed geometry and a deliberately short return to limit loop inductance and ringing at the test node; (ii) a mid-band equalization by pairing the probe's first-order high-pass with digital integration on the oscilloscope, chosen and verified so that the composite transfer is flat over the bandwidth actually used; (iii) an in-situ calibration routine performed before each measurement series that nulls the oscilloscope offset and sets the integration window to minimize drift and noise in the reconstructed waveform; and (iv) an experimental material check (FR4 vs. RO4350B) showing no measurable rise-time benefit for these conditions, which justifies the continued use of FR4 without compromising probe bandwidth. These adaptations, although incremental, were required to obtain valid waveforms for the analysis presented in this thesis.

3.2 PCB Implementation and Parameter Optimization

The integration of capacitive sensor plates into the existing PCB design eliminates the need for additional components, leveraging the intrinsic capacitance between the probe and the test point. This non-contact approach significantly reduces the risk of arcing and damage to delicate components, thereby ensuring a safer measurement environment. The 2 mm diameter capacitive probe is positioned beneath the much larger target signal plane, allowing for effective voltage measurement without direct electrical contact.

It is recognized that the accuracy of the capacitive probe measurements may be influenced not only by the voltage amplitude and signal frequency—due to the frequency-dependent limitations of FR4, as documented in recent studies (Cai et al. (2020), Hsu et al. (2021), Paleček et al. (2013))—but also by the characteristics of the signal processing chain. In particular, the integration of the probe signal depends on the bandwidth and resolution of the oscilloscope, and is susceptible to low-frequency drift and high-frequency noise. To mitigate these issues, consistent geometrical dimensions are maintained for the capacitive probe and its associated high-voltage island, following the recommendations from the aforementioned literature to ensure reproducible coupling. Additionally, an optimisation of the integration window and pre-processing steps is introduced, to reduce the impact of noise and baseline offset, enhancing the fidelity of the reconstructed signal.

In this setup, the capacitive probe functions as a first-order high-pass filter. Its cutoff frequency (f) is defined in Equation 3.1, below which signals are attenuated. The RC time constant establishes the high-pass filter behavior.

$$f = \frac{1}{2 \cdot \pi \cdot C_{probe} \cdot R_{load}} \quad (3.1)$$

- The capacitance of the probe (C_{probe}) is primarily serving as a way to transfer the signal from the point of measurement to the measurement equipment without significantly disturbing the circuit being measured. As per the schematic in Figure 3.1, it is an inherent property of the probe determined by the dimensions of the copper plates and the dielectric material of the PCB.
- The load resistance (R_{load}) is the resistance across which the probe measures the voltage. In the present application, this is the $50 \, \Omega$ coaxial cable (RG58) connected to a $50 \, \Omega$ attenuator at the input of the oscilloscope.

- The product $C_{probe} \cdot R_{load}$ represents the time constant (τ) of the RC circuit. This time constant determines how quickly the circuit can respond to changes in voltage.

Regarding these signals, for an expected rise time of $t_{rise} < 200ps$, Eq. 3.2 (Johnson and Graham (1993)) gives a minimal required value of ≥ 700 MHz. This equation originates from the characteristics of a single-pole filter, where faster transitions require proportionally higher bandwidth to avoid signal distortion.

$$f_{low} \geq \frac{0.35}{t_{rise}} \quad (3.2)$$

Equation 3.1 describes the lower cut-off frequency of a first-order high-pass RC filter, which corresponds to the low-frequency limit of the capacitive probe. Below this frequency, the probe's response attenuates rapidly, with a typical slope of +20 dB/decade. In the mid-frequency region, this results in the differentiation of the high-voltage signal. To reconstruct the original waveform, a digital integration is applied using the oscilloscope's built-in math function, which introduces a compensating -20 dB/decade slope. Thus, in the overlapping region, the system's overall transfer function becomes flat, enabling accurate signal reconstruction.

However, it is important to note that at very high frequencies, the probe no longer maintains the +20 dB/decade slope due to the influence of parasitic elements, such as inductance in the measurement loop, dielectric losses, and bandwidth limitations of the measurement equipment. These effects constrain the upper usable frequency of the probe, which in this case is limited by the oscilloscope bandwidth (6 GHz).

To model the system's mid-band behavior, the following transfer functions apply: the RC high-pass filter of the probe (Eq.3.3), the integrator (Eq.3.4), and the overall system response (Eq.3.5):

$$H_{HP}(f) = \frac{j2\pi f C_{probe} R_{load}}{1 + j2\pi f C_{probe} R_{load}} \quad (3.3)$$

$$H_{Int}(f) = \frac{K}{j2\pi f} \quad (3.4)$$

$$H_{sys}(f) = H_{HP}(f) \cdot H_{Int}(f) = \frac{K C_{probe} R_{load}}{1 + j2\pi f C_{probe} R_{load}} \quad (3.5)$$

The probe's coupling capacitance, approximately 0.2 pF, defines its high-frequency limit at 16 GHz. However, the assumption of an integrator gain of 0 dB at 16 GHz is purely hypothetical and intended to simplify calculations, as the actual bandwidth of the oscilloscope at hand is limited to 6 GHz. Together with a 18 GHz attenuator and an oscilloscope bandwidth of 6 GHz, this ensures sufficient bandwidth for the capacitive pickup-based high-voltage measurement system, all at negligible cost.

The constant K in Eq. 3.4 is chosen to set the integrator's gain to 0 dB at 16 GHz, thereby balancing the high-pass filter's response over a wide frequency range. For instance, at 500 MHz, the high-pass filter introduces approximately 30 dB of attenuation, while the integrator provides a complementary gain of 30 dB. The combined system response H_{sys} is thus flat at 500 MHz, allowing this signal to be accurately captured. While the probe itself has a high-pass nature, the integrator's compensation results in a stable, broad frequency response that accurately reflects the signal across the desired bandwidth.

The choice of FR4 as the PCB material could potentially limit high-frequency measurements as the choice of material affects the upper frequency limit due to dielectric losses. Comparative measurements of the driver output using both the current FR4 PCB and a high-frequency PCB material (RO4350B) (Rogers Corporation (2022)) are shown in Figure 3.2 (del Barrio Montañés et al. (2025)).

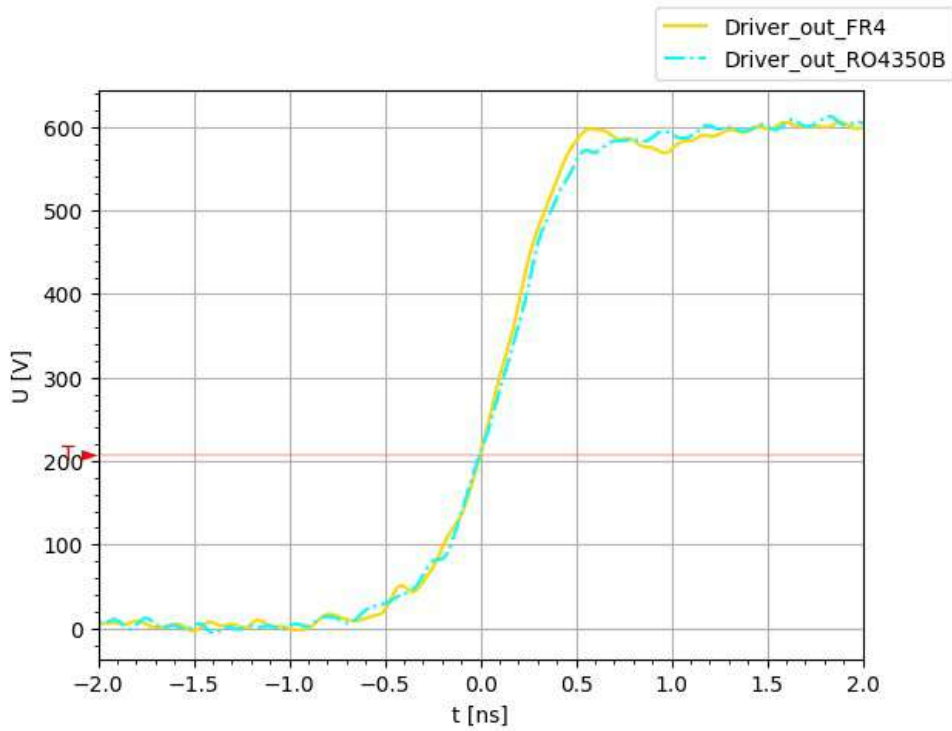


Figure 3.2: Driver output measurement. Comparison between FR4 and RO4350B PCB materials.

The results indicated no significant improvement in rise time (FR4: 680 ps; RO4350B: 768 ps), leading us to continue using FR4 for further measurements as it meets the present requirements without imposing limitations on the bandwidth of the capacitive probe while having the added advantage of being more economically priced.

The functioning principle of the capacitive probe operates through a series of steps:

1. **Current Injection:** Injecting a current $i(t)$ proportional to the rate of voltage change ($du(t)/dt$) through the capacitive pickup's inherent capacitance (C_{probe}).

$$i(t) = C_{probe} \cdot \frac{du(t)}{dt} \quad (3.6)$$

2. Voltage Generation: This injected current generates a voltage $u_{scope}(t)$ across a $50\ \Omega$ load (attenuator) due to the load's resistance (R_{load}).

$$u_{scope}(t) = i(t) \cdot R_{load} \quad (3.7)$$

3. Voltage Reconstruction and Calibration: The original voltage on the top PCB plane ($u(t)$) is then reconstructed by integrating $u_{scope}(t)$.

$$u(t) = \frac{1}{C_{probe} \cdot R_{load}} \cdot \int_0^t u_{scope}(t) dt \quad (3.8)$$

The integration process can result in an error due to a DC offset in the oscilloscope. To compensate for this potential error, before each set of pulse measurements, the capacitive probe was set at 0 V, compensating the oscilloscope's input offset. This involved observing the integrated signal at zero input voltage to determine any existing offset. If an offset was detected, it was quantified and by either adding or subtracting the necessary amount based on the observed offset, this ensured that the measurements accurately reflected the true signal without the influence of the DC offset.

Regarding the RC constant ($C_{probe} \cdot R_{load}$), the load for these measurements presents a $R=50\ \Omega$ impedance. Consequently, in equation 3.8, the only unknown value is denoted as C.

3.3 Electrostatic Field Analysis of the Capacitive Probe Geometry

To evaluate the electric behavior of the capacitive probe, an electrostatic field simulation was performed using CST Studio Suite. The electric field distribution results provide insight into the effectiveness and confinement of the coupling between the high-voltage pad (HV) and the capacitive pickup (CP). As illustrated

in the field magnitude plots (Fig. 3.3, 3.4a, and 3.4b), the electric field is concentrated in the vertical region directly between the HV and CP electrodes. The simulation reveals a radially symmetric distribution around the CP pad, with a peak in field strength along the edges of the pickup electrode, indicative of fringing effects typical in planar capacitive coupling geometries.

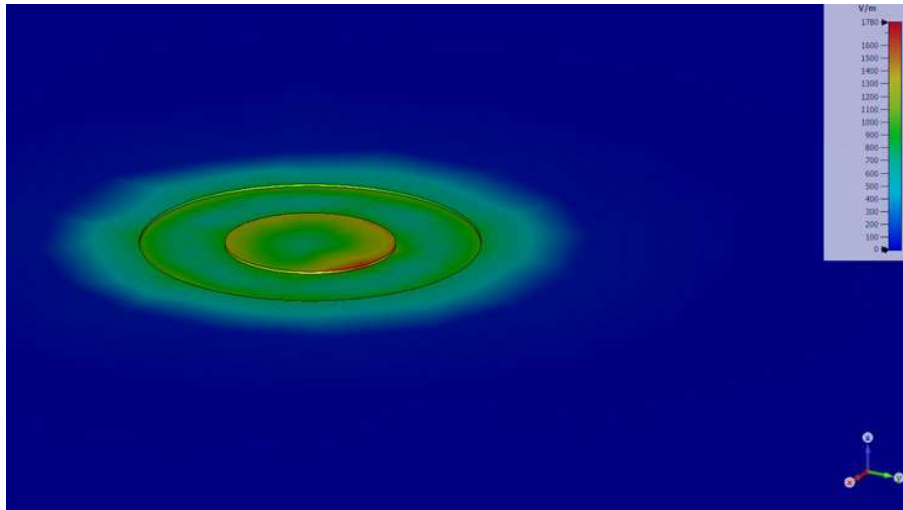
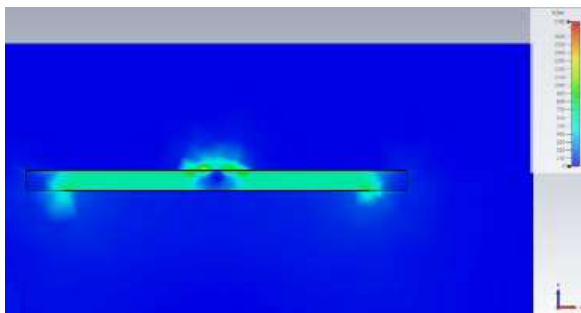
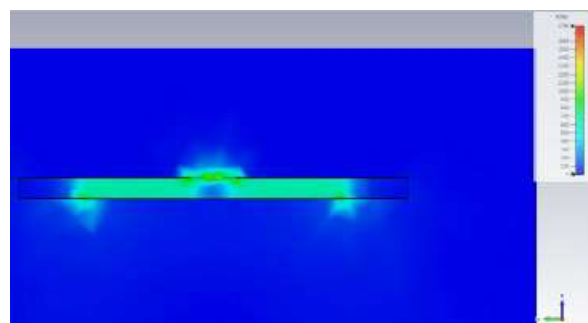


Figure 3.3: Electric field magnitude in the vicinity of the probe tip. The fringing field around the circular pad is clearly visible, indicating a significant deviation from the ideal parallel-plate model and highlighting the influence of edge effects.



(a) Cross-sectional electric field distribution along the X-axis. The field lines reveal asymmetric fringing and varying field intensity across the dielectric, influenced by the finite geometry of the probe pad and surrounding ground plane.



(b) Cross-sectional electric field distribution along the Y-axis. The fringing profile is similar to the X-direction, with added influence from nearby copper structures, highlighting three-dimensional effects.

Figure 3.4: Electric field distribution along orthogonal cross-sections of the capacitive probe. These cuts illustrate the non-uniformity and 3D nature of the field around the probe pad.

The field extends predominantly from the HV pad upward toward the CP and downward toward the ground plane. This confirms that the CP is primarily sensitive to the vertical component of the electric field, with the strongest coupling occurring in the central axis of the geometry. The fields remain well-confined in the vertical direction with limited lateral spread, ensuring that the CP responds to a localized electric field without significant interference from the surrounding ground region. Furthermore, the separation of field regions suggests that the CP is minimally influenced by the HV-to-ground coupling path, supporting the selectivity and isolation of the measurement.

Overall, these field simulations confirm the suitability of the CP geometry for capturing fast transients in the HV signal. The field confinement, symmetry, and intensity distribution validate the probe's design for localized and reproducible signal acquisition, with minimal parasitic effects from the surrounding PCB structures.

In addition to the field plots, the solver provides a quantitative capacitance matrix for the modeled conductors (self- and mutual capacitances). This is particularly well suited to this geometry: the matrix inherently accounts for full 3-D fringing, finite ground apertures, nearby copper, solder mask and air regions. By reading the matrix entry corresponding to the sensing pad and its facing return plane, a direct and geometry-faithful estimate of the coupling capacitance is obtained.

From the capacitance matrix, the capacitance between the central probe pad (CP) and the plane above it is approximately 0.15 pF.

3.4 Capacitance of the Probe: Microstrip Calculation and Bench Measurement

The analytical estimation of the value of this capacitance is outlined in Bahl and Garg (1977). The authors proposed a simple way to include conductor thickness effects in microstrip calculations by replacing a finite-thickness strip of width w and thickness t over a substrate of height h with an equivalent zero-thickness strip

of enlarged width $w_{eq} = w + \Delta w$. The increment Δw is given by closed-form expressions that depend on t/h and w/h and capture the fringing of fields around the strip edges. Once w_{eq} is obtained, any standard zero-thickness formulas (e.g., for characteristic impedance Z_0 and effective permittivity ϵ_{eff}) can be used unchanged by substituting $w \rightarrow w_{eq}$. This yields accurate results for practical ranges of w/h and moderate conductor thicknesses (typically $t/h \ll 1$), with errors on the order of a few percent relative to full-wave solutions, while keeping the method analytical and fast (Bahl and Garg (1977)).

As per this method, the capacitance per unit length (C') of a microstrip with a finite strip thickness is given by:

$$C' = \frac{\epsilon_0 \cdot \epsilon_r}{\pi} \cdot \left(\ln \left(\frac{4h}{t} \right) + 1 \right) \quad (3.9)$$

where:

- ϵ_0 is the permittivity of free space
- ϵ_r is the relative permittivity of the dielectric material
- h is the dielectric thickness
- t is the thickness of the microstrip conductor

Given the parameters for the hereby presented system:

- Dielectric thickness $h = 1.55mm$
- Relative permittivity $\epsilon_r = 4.5$
- Copper thickness of the pad and ground plane $t = 35\mu m$
- Radius of the pad $r = 1mm$

The total capacitance of the pad (C_{probe}) can be approximated by multiplying the capacitance per unit length by the effective length of the pad area, and it amounts to 0.18 pF.

Upon comparing this estimated value to the one obtained during the test measurements, achieved by a comparative analysis similar to that illustrated in Fig. 3.6, a measured capacitance value of 0.19 pF is met. First, the measurement was taken on the capacitive probe island at the back of the PCB, and the resulting signal was integrated on the oscilloscope. This integrated signal was then adjusted by varying the RC value to match the reference measurement obtained using a coaxial cable and a 50-ohm attenuator. The final measured capacitance of 0.19 pF aligns with the calculated value, confirming the reliability of this measurement system.

The capacitive probe could be exposed to high voltage if the $RC \cdot dU/dt$ (eq. 3.7) value is excessively high. The SMA socket that in use has a voltage limitation of 500V, which corresponds to a rate of 50 kV/ns with a 0.19 pF capacitive probe and 50 Ω load. Therefore, it is crucial to maintain a low CP capacitance to ensure safe and effective operation.

3.5 Capacitance Comparison Summary

A summary of the values obtained using the four approaches:

- Analytical (fringe-corrected): 0.6 pF
- CST simulation: 0.15 pF (Section 3.3)
- Microstrip-based calculation: 0.18 pF (Section 3.4)
- Experimental measurement: 0.19 pF (Section 3.4)

The results confirm that the analytical model significantly overestimates the probe capacitance, while the simulated, microstrip-derived, and measured values are in close agreement.

3.5.1 Voltage Reduction and Loading Model

While the capacitive probe can be approximated as part of a capacitive voltage divider—formed between the probe capacitance and the input capacitance of the measurement system (e.g., oscilloscope or attenuator)—this model is frequency-dependent. At high frequencies, the capacitive impedance of the probe (~ 0.15 pF) becomes comparable to or smaller than that of the measurement input (typically ~ 10 pF), which justifies using a capacitive divider model for estimating signal attenuation.

The voltage reduction obtained with the capacitive probe of this size can be calculated using the voltage divider principle for capacitors:

$$V_{out} = V_{in} \cdot \frac{C_{load}}{C_{probe} + C_{load}} \quad (3.10)$$

where:

- V_{in} is the input voltage
- V_{out} is the output voltage (voltage across the load)
- C_{probe} is the capacitance of the probe, 0.15 pF, as per the CST simulation in Section 3.3
- C_{load} is the load capacitance (input capacitance of the measurement device), 10 pF

Resulting in a Voltage Reduction Ratio ≈ 0.98 .

Therefore, while the capacitive voltage divider model offers a useful first-order approximation, particularly for quick estimation of voltage attenuation at high frequencies, the actual measurement system is better represented by a resistively loaded capacitive coupling circuit. This hybrid perspective aligns with both analytical expectations and practical implementation constraints.

3.6 Measurement validation

The final PCB setup, illustrated in Fig. 3.5, consists of a 2 mm diameter sensing pad connected to an SMA plug for the measurement cable, with a local copper shield to stabilize the field and reduce pickup (del Barrio Montañés et al. (2025)).



Figure 3.5: Capacitive probe implementation on the back side of the PCB (del Barrio Montañés et al. (2025)).

To assess accuracy and robustness, the capacitive probe was compared against a conventional coaxial measurement chain (RG58 into a $50\ \Omega$ attenuator), with both signals acquired simultaneously from the same node. Because of the attenuator's voltage rating, comparisons were performed so that the resulting outputs did not exceed 2.7 kV. The side-by-side acquisition enables a direct consistency check between the non-contact probe and the reference attenuator method.

In Fig. 3.5, the probe appears on the rear side of the board with an SMA launch and copper shielding around the test point. Figure 3.6 compares both measurement paths at the input node (G-B SiC MOS out, Fig. 4.24); the bias for the SiC MOSFETs is 1.3 kV, chosen as a compromise between fast commutation and device stress.

During preliminary trials, it became clear that the available attenuator for calibrating the capacitive probe at TP2 would be stressed by repetitive pulsing at the intended amplitude. The comparison point was therefore moved upstream to the input node, where the signal magnitude remains within the attenuator limit, allowing a safe and repeatable cross-check.

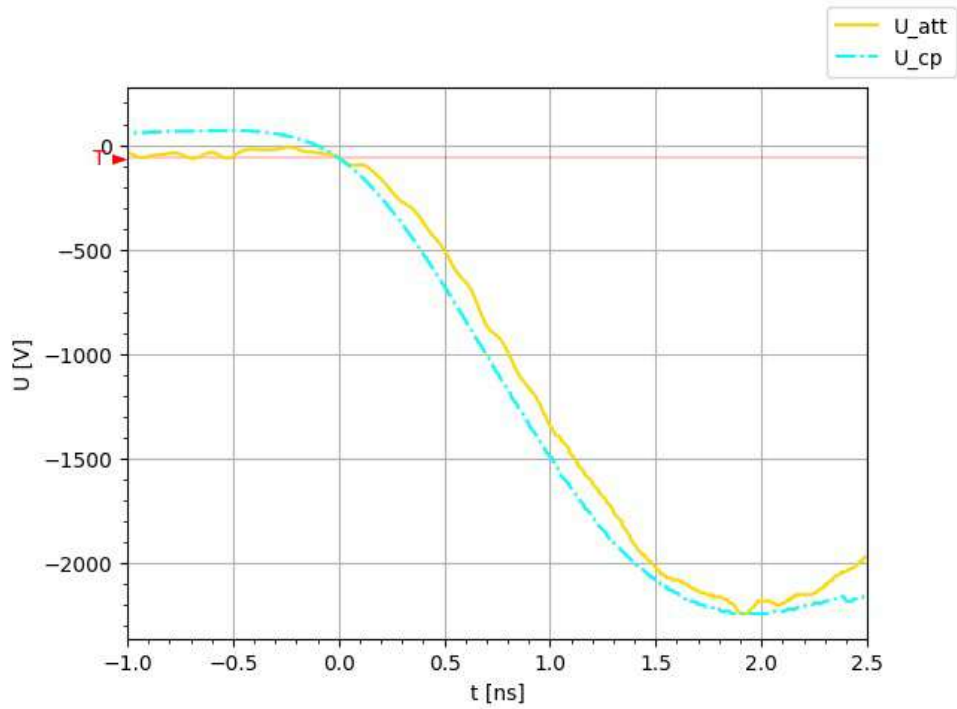


Figure 3.6: Simultaneous measurement at the Marx input (G-B SiC MOS out, Fig. 4.24): capacitive probe vs. attenuator (color mapping as in the legend).

A quantitative agreement check was performed using the coefficient of determination r^2 (Eq. 3.12) across two sets of five measurements acquired at different bias levels (Fig. 3.7).

$$C_v = \frac{\sigma}{\mu_{att}} \cdot 100$$

$$\sigma = \sqrt{\frac{1}{N} \sum_{i=1}^N ((att_i - cp_i) - \mu_{error})^2} \quad (3.11)$$

Where:

- C_v is the Coefficient of Variation, a normalized measure (in %) of the spread of the difference between the two methods.

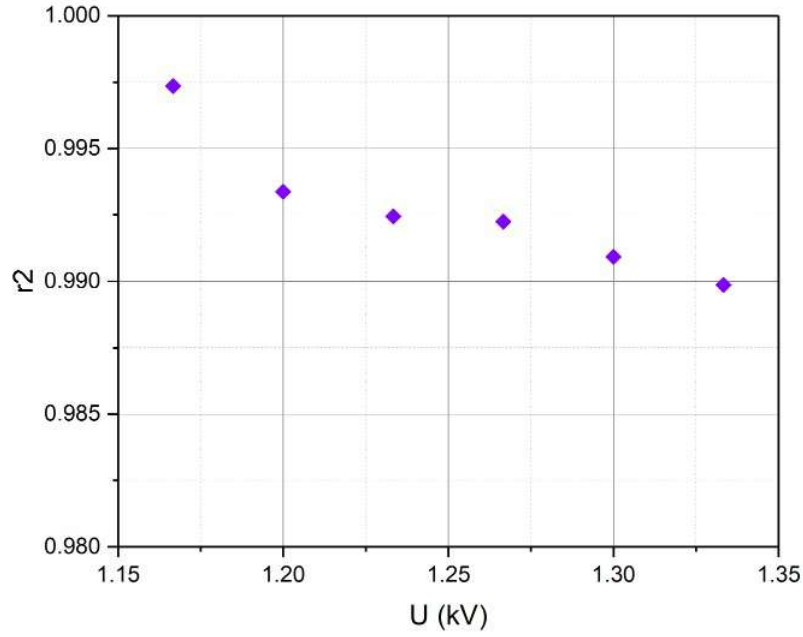


Figure 3.7: Coefficient of determination (r^2 , Eq. 3.12) for five measurement pairs at the input node and at different bias voltages (cf. Fig. 4.24).

- σ is the standard deviation of the difference between the attenuator measurements (att_i) and the capacitive probe ones (cp_i).
- μ_{error} is the mean value of the difference between the attenuator measurements (att_i) and the capacitive probe ones (cp_i).
- μ_{att} is the mean value of the attenuator measurement dataset.

$$r^2 = 1 - \frac{\sum_{i=1}^n (y_i - \hat{y}_i)^2}{\sum_{i=1}^n (y_i - \bar{y})^2} \quad (3.12)$$

Where:

- r^2 is the coefficient of determination, i.e., the fraction of variance in the capacitive probe data that is explained by the reference (attenuator) data.
- y_i are the data points obtained with the attenuator measurement.

- $\hat{y}_i$ are the data points obtained with the capacitive probe measurement.
- $\bar{y}$ is the mean value of the attenuator dataset.
- n is the number of points.

An r^2 value close to 1 indicates strong agreement between methods; in these measurements, after applying the integration and calibration procedure for the capacitive probe signal (Eqs. 3.6, 3.7, 3.8), the two records overlap closely across the tested bias range. In other words, within the range exercised here, the non-contact probe reproduces the reference result with accuracy sufficient for the analyses presented in this thesis (see also the discussion of agreement metrics in del Barrio Montañés et al. (2025)).

Overall, the measurement chain used throughout this thesis was verified to meet the accuracy needed in both amplitude and timing over the voltage and bandwidth ranges actually employed. The additional linearity extension to higher voltages is identified as subsequent work and is not a prerequisite for the results presented here.

4 Design

Following the literature-based assessment of thyristor triggering in impact ionization mode, as presented in the preceding chapters, the design of a pulse generator is undertaken.

This phase aims to practically apply the theoretical findings by implementing impact ionization triggering on commercially available off-the-shelf (COTS) thyristors.

In this chapter, a comprehensive exploration of the pulse generator is presented, breaking down its components and offering detailed descriptions for each. This chapter is organized as follows: it begins with the target design of a thyristor stack, detailing the selected thyristor model and its specific requirements. From there, the discussion progresses through each stage of the system, starting with the output pulse that will be delivered to the thyristor stack. Next, it examines the Marx generator responsible for producing this pulse, followed by the SiC MOSFET stage, which provides the necessary current to trigger the Marx generator's thyristors in avalanche mode. The chapter then addresses the driver circuit that activates the parallel SiC MOSFETs and concludes with an explanation of the pulse booster, which refines and sharpens the input from the pulse generator.

4.1 Thyristor Capacitance Measurement

Previous literature establishes that ultra-fast thyristor triggering requires a significant slew rate and an overvoltage at least twice the static breakdown voltage of the thyristor (Gusev et al. (2019b), Grekhov (2010), Grekhov et al. (2008b), Gusev et al. (2014)); all whilst ensuring that enough current is available to guarantee the charging of the thyristor's internal parasitic capacitance at the required dU/dt . Therefore, the parasitic capacitance of the thyristors used must first be determined.

To assess the relationship between the internal parasitic capacitance and voltage for the 2.4 kV rated thyristor MPPCT750D240 (Multicomp Pro (2020)), a test was conducted as depicted in Figure 4.1a. The biasing voltage applied via the DC power supply was gradually increased to facilitate the charging of both the thyristor's parasitic capacitance and the series coupling capacitor. Placing a resistor R_p in parallel with the RLC meter is intended to protect it from the charging current of the coupling capacitor during voltage changes. It should be noted that this resistance will only be active during voltage transitions, serving as a protective measure for the RLC meter.

The thyristor's parasitic capacitance was measured by applying a blocking DC voltage on the anode–cathode of the component, on a range from 200 V to 3 kV. The RLC meter measurement was set at 10 kHz. A coupling capacitor was incorporated between the thyristor anode (at positive U_{bias}) and the RLC meter. If the coupling capacitance is chosen to be significantly larger than the parasitic capacitance of the thyristor under investigation, its effect can be considered through the series capacitance relation, yielding $C_c = 3.3$ nF (del Barrio Montañés et al. (2024b)).

The voltage dependence of the thyristor's parasitic capacitance is shown in Fig. 4.1b.

To address radiation tolerance—specifically to lower the probability of single-event burnout (SEB) under bias—the limit of the operating DC blocking voltage is set to at most $0.6 V_{rating}$ (here: 1.4 kV for a 2.4 kV device), at which the

device exhibits a parasitic capacitance of about 220 pF. This 60% choice is motivated by SEB physics and practice: the SEB cross-section rises steeply with blocking voltage, guidance for unqualified parts commonly recommends strong voltage derating (often $\lesssim 50\%$ of the rating), and SEB has been observed even below half the nominal rating; therefore the DC bias needs to remain conservative and any additional electric field is generated only as sub-nanosecond transients with the driver Fernández-Martínez and Papadopoulou (2023), Radiation (2023), Lauenstein et al. (2019).

The sweep in Fig. 4.1b extends to 3 kV solely to bound $C(V)$ for modeling and does not imply a service bias of 3 kV in a radiation environment.

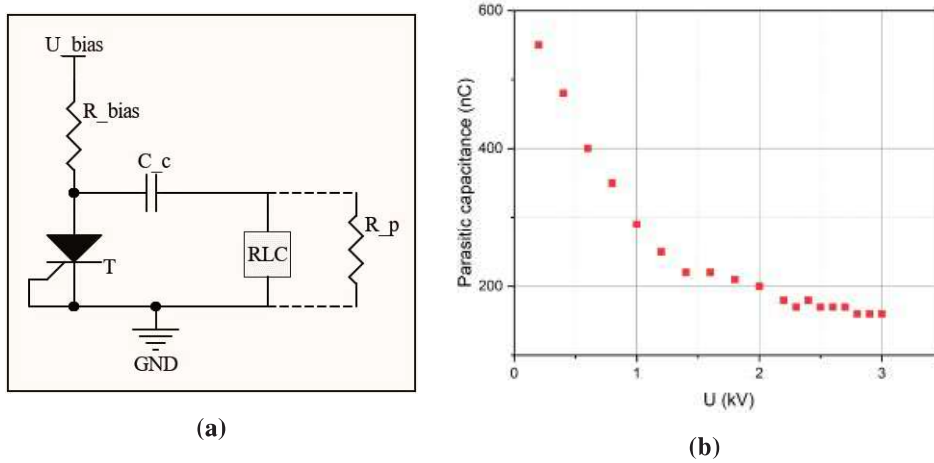


Figure 4.1: Assessing the thyristor's parasitic capacitance. (a) Setup to measure the parasitic capacitance of a thyristor in relation to bias voltage using an RLC meter. (b) Voltage dependance of the MPPCT750D240 thyristor's parasitic capacitance.

Taking as a starting point a small thyristor stack generator, with the previously studied thyristors, the operating point that the present pulse generator needs to reach is given by:

1. Slew rate at turn-on $\frac{dU}{dt} > 1 \text{ kV/ns}$.
2. Considering the static breakdown voltage $U_{BD} = 3 \text{ kV}$, doubling it and subtracting the biasing voltage $U_{bias} = 1.4 \text{ kV}$, the output voltage needs to be $U_{out} > 4.6 \text{ kV}$.

3. Current $I = C_{\text{parasitic}} \cdot \frac{dU}{dt} = 200 \text{ A}$.

In this work U_{BD} denotes the DC breakdown voltage of the thyristor in blocking state. It is determined $U_{BD} = 3 \text{ kV}$ experimentally on the devices used here by sweeping the DC bias up to breakdown under current-limited conditions and defining breakdown as the onset of irreversible conduction (sharp increase of leakage beyond the compliance limit and a pronounced knee in the $I-V$ curve). Figure 4.1b therefore extends to 3 kV and reaches the breakdown point on the same setup used for the $C(V)$ measurement (Fig. 4.1a).

Because the thyristor's parasitic capacitance in blocking state is voltage dependent, the edge-current is estimated on the differential capacitance, $C_d(V) = dQ/dV$, extracted from Fig. 4.1b; and the displacement current during the leading edge can be estimated as

$$i(t) = C_d(V(t)) \frac{dU}{dt}. \quad (4.1)$$

For a compact design model, an effective capacitance averaged over the blocking-voltage range covered during edge build-up is employed,

$$C_{\text{eff}} = \frac{1}{\Delta V} \int_{V_{\text{bias}}}^{V_{\text{bias}} + \Delta V} C_d(V) dV, \quad (4.2)$$

with $V_{\text{bias}} = 1.4 \text{ kV}$ and $\Delta V \approx 1 \text{ kV}$. From Fig. 4.1b, $C_d(1.4 \text{ kV}) \approx 220 \text{ pF}$ and a modest decrease can be observed with increasing voltage; averaging $C_d(V)$ over $V \in [1.4 \text{ kV}, 2.4 \text{ kV}]$ yields $C_{\text{eff}} \approx 200 \text{ pF}$. The corresponding design headline current for the target slew is then

$$I_{\text{edge}} \approx C_{\text{eff}} \cdot \left. \frac{dU}{dt} \right|_{\text{target}} = 200 \text{ pF} \times 1 \text{ kV/ns} \approx 200 \text{ A}. \quad (4.3)$$

This choice avoids overstating the requirement (the instantaneous peak at the very start of the edge—where C_d is largest near V_{bias} —would be slightly higher,

~ 220 A) while remaining faithful to the measured $C(V)$ dependence used for sizing.

To provide a comprehensive overview of how this can be achieved, the methods, materials, and results are presented as follows: starting from a low-voltage pulse generator (Section 4.2), progressing through pulse edge sharpening and voltage amplification steps (Sections 4.3 to 4.6), and culminating in the triggering of a D2PAK thyristor in impact ionization mode (Section 4.5).

4.2 Boosting the Pulse Generator Signal

In the first step towards meeting the demanding requirements of nanosecond switching, the principle of gate boosting is employed to enhance the output of a standard function generator. A Philips PM5786B pulse generator (Philips (1999)) is used. Its output signal undergoes a custom voltage level-shifting and boosting process that results in a significant sharpening and amplitude amplification. The same booster topology and sizing rules are detailed and reused in earlier publications (del Barrio Montañés et al. (2023, 2024a,b)).

4.2.1 Component-Level Operation of the Booster Stage

Figure 4.2 shows the booster schematic used for the PM5786B pulse generator. The PM5786B provides a 10 V step with 2 ns rise time (10–90%); this is level-shifted and boosted by a two-stage MOSFET gate-booster dimensioned for a low-inductance loop by choosing small-packaged components. The booster supply was 45 V (del Barrio Montañés et al. (2024b)).

In the booster of Fig. 4.2, the first level shift is performed by NMOS NMO_1 (2N7002K, Onsemi (2024)). Its gate is driven from the PM5786B through the series/input resistor R0_1 with a gate bleed/damper R0_2 to ground. The capacitor C0_1 acts as a speed-up capacitor: it injects a brief extra charge into the NMO_1 gate so the device commutates faster. By contrast, PMOS PM0_1 already uses gate boosting; its series capacitor C0_2 was sized according to the method described in Section 2.6.1. The same boosting approach is then applied to the following stage with NMO_2 and PM0_2, using C0_4 and C0_5, respectively.

The resulting low-side transition controls the PMOS PM0_1 (NVR5124PL, Onsemi (2019)), whose source is tied to the 45 V voltage source (decoupled by C0_3). The gate of PM0_1 is biased by the divider R0_4–R0_3 and edge-shaped by the series capacitor C0_2; together they realize a brief gate overdrive and then settle to the steady level, keeping the gate–source voltage within the recommended limits (Onsemi (2019)).

The second stage repeats the concept at a higher drive level: NMO_2 (2N7002K, Onsemi (2024)) is driven via R0_6 with a pull-down R0_7. The series capacitor C0_4 meters charge into the NMO_2 gate to sharpen the transition, while R0_8 provides damping from the stage output back to the gate node. The high-side device PM0_2 (NVR5124PL, Onsemi (2019)) is placed at the 45 V voltage source (decoupled by C0_5); its gate is biased from it via R0_9. The output node is lightly biased through R0_10 and is delivered to a 50 Ω load for a matched measurement.

The capacitors C0_2, C0_4 and C0_5 are intentionally chosen larger than a strict charge-metering design (which would size them just from the devices' Q_g). In this low-voltage booster, their role is to inject extra transient charge so the gate nodes traverse the necessary ΔU quickly despite the finite loop R and stray L , avoiding slow RC charging through the bias resistors. Because the absolute gate voltages in this stage remain modest, this “more-capacitance for more charge” choice prioritizes edge speed and current-loop compensation over minimal capacitor sizing; steady-state gate levels are still set by the resistive dividers (R0_1 / R0_2 for NMO_1, R0_4 / R0_3 for PM0_1, R0_6 / R0_7 and R0_9 for NMO_2 / PM0_2), so DC stress remains controlled while the transient edges are significantly sharpened.

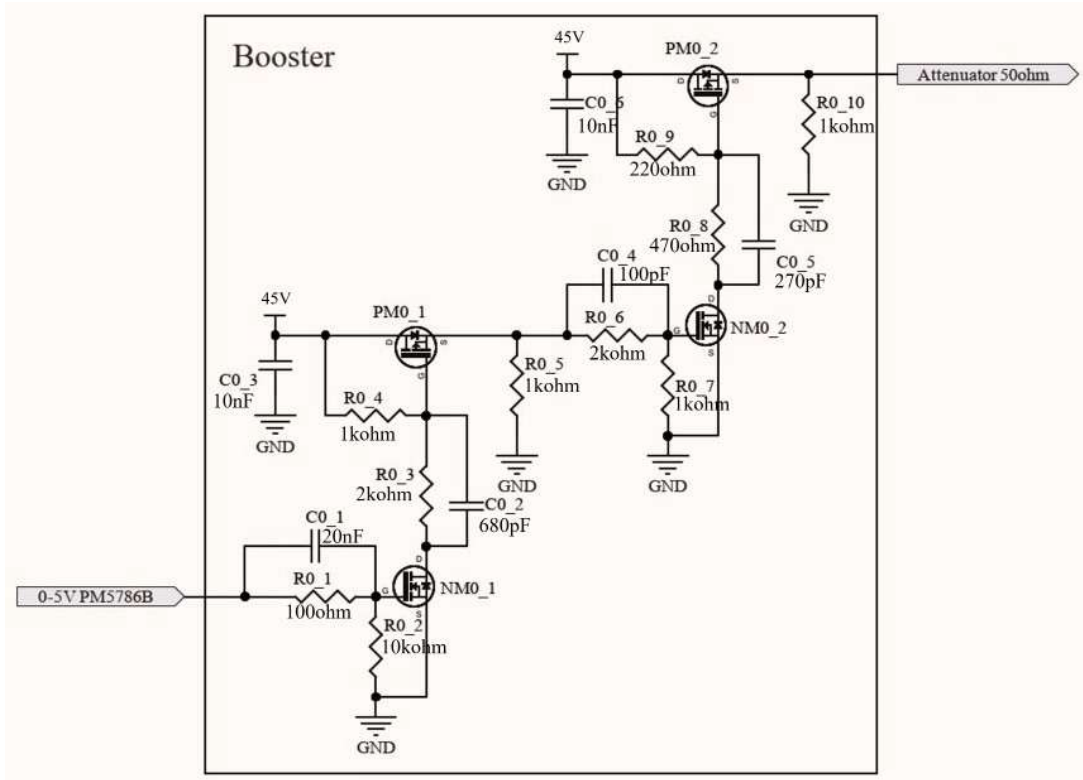


Figure 4.2: Schematic of the pulse booster for the Philips PM5786B pulse generator.

4.2.2 Measurement Results

The waveform in Fig.4.3 was recorded into a matched $50\ \Omega$ load using a $50\ \Omega$ coaxial path and the oscilloscope's $50\ \Omega$ input. The scope bandwidth was $\geq 6\ \text{GHz}$ (rise-time limit $\leq 60\ \text{ps}$); sample rate $20\ \text{GSa/s}$. A $20\ \text{dB}$ DC-to- $18\ \text{GHz}$ coaxial attenuator was inserted at the scope to improve match and protect the input. The load was a through $50\ \Omega$ termination at the scope front-end.

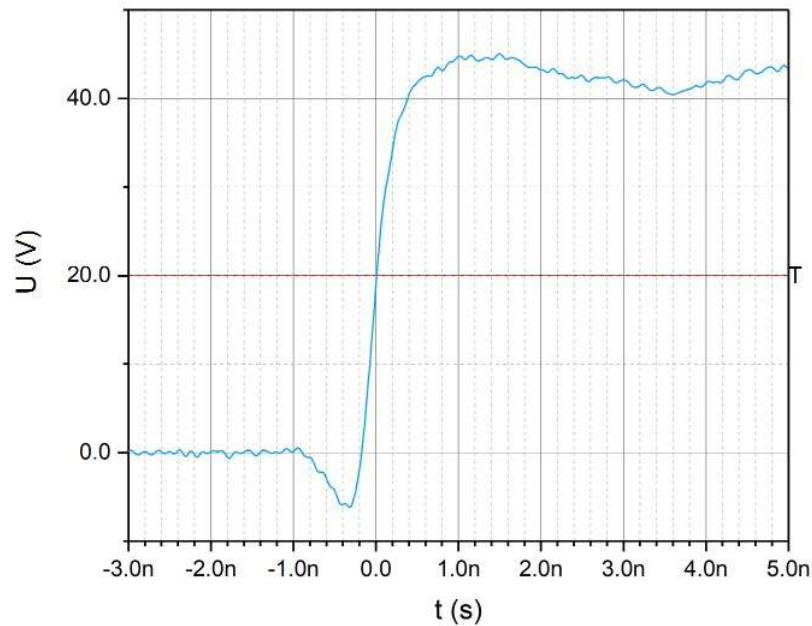


Figure 4.3: Booster output pulse on a $50\ \Omega$ load. Maximum amplitude: 45 V, rise time: 425 ps.

The resulting pulse, shown in Fig. 4.3, achieves a final amplitude of 45 V, a 10–90% rise time of 425 ps, and a slew rate of approximately 80 V/ns. This enhanced signal enables the reliable triggering of subsequent stages in the system, surpassing the inherent limitations of the original function generator.

4.3 Enhanced Driver Stage for HV MOS

After the booster stage, the generated pulse advances to the driver stage, which further enhances the pulse characteristics by sharpening it and increasing the amplitude (del Barrio Montañés et al. (2024b)).

The initial gate driver topology consisted of a compact NMOS/PMOS stage, supplied with 150 V (Senaj et al. (2021)). This version served as the foundation for the subsequent designs and demonstrated promising switching behaviour. Measurements taken at the output of this driver, terminated with a resistive $50\ \Omega$ load and recorded using an 18 GHz attenuator, are shown in Fig. 4.4. The driver achieved a voltage slew rate of approximately $200\ \text{V/ns}$ and $t_r = 800\ \text{ps}$, measured between 10–90%, and a maximum of 160 V (del Barrio Montañés et al. (2024b)).

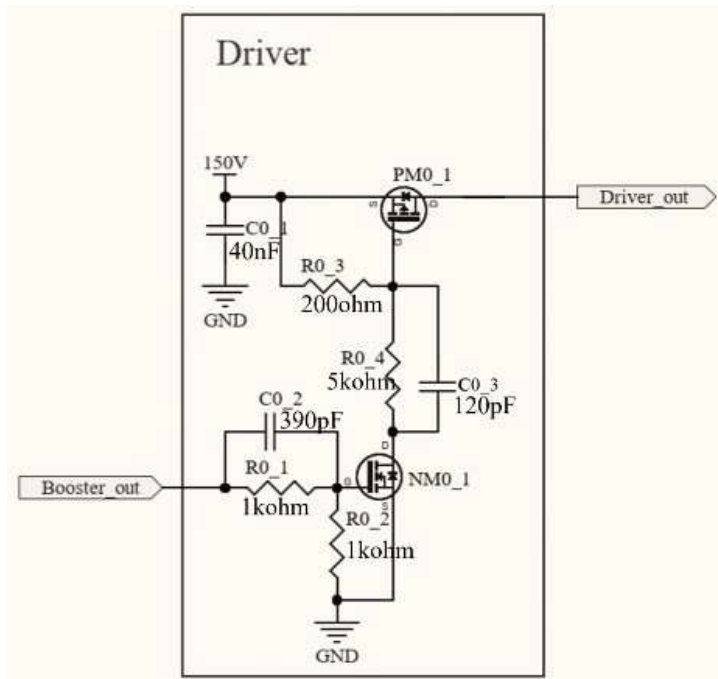


Figure 4.4: Schematic of the earlier version of the SiC MOSFET gate-boosting driver.

An interesting transient was observed just before the voltage rise: a brief negative dip caused by capacitive coupling through the parasitic gate-drain capacitance

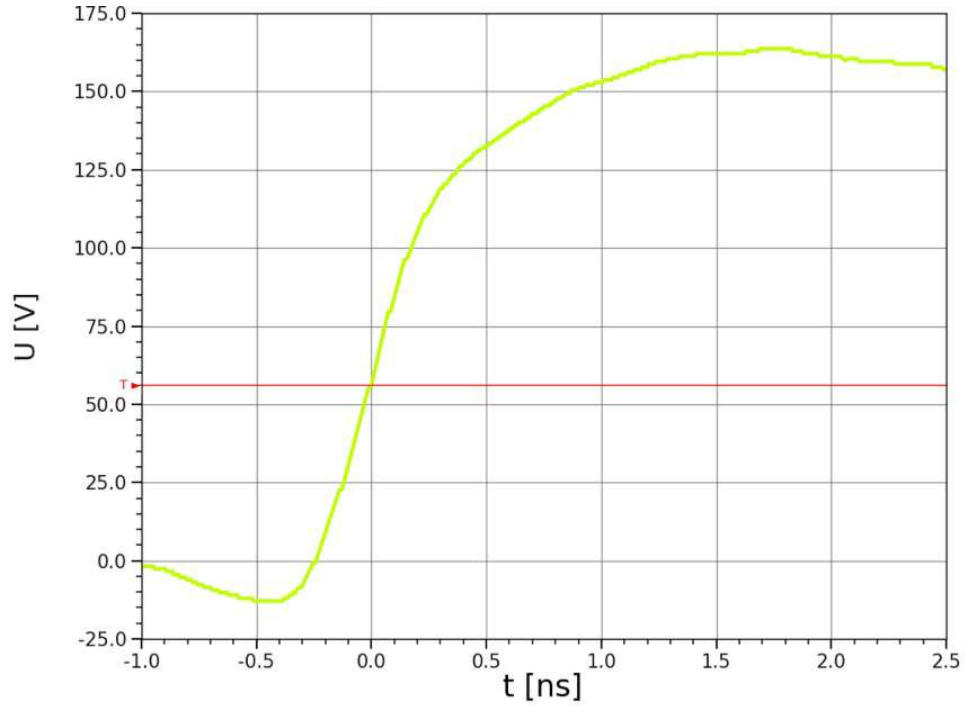


Figure 4.5: Output voltage of the gate-boosting driver on Figure 4.4, on a $50\ \Omega$ load at a charging voltage of 160 V. Maximum amplitude of 160 V and $t_r = 800$ ps, measured between 10–90%.

of the PMOS device. This effect occurs before the PMOS turns on, and it is a consequence of the aggressive gate boosting employed in this design.

A previous design of this driver (Figure 4.6) was capable of delivering $430\ \text{V/ns}$ to a $50\ \Omega$ load, with a maximum output voltage of 300 V. The resulting output voltage was first presented in del Barrio Montañés et al. (2023), as seen in Figure 4.7. It profits from the rapid switching capability of an avalanche transistor (Av0_1, Diodes Incorporated (2015a)) to increase the output pulse dU/dt .

A key component of this driver stage is the utilization of avalanche transistors, which significantly sharpen the pulse waveform and enable higher output voltage. Avalanche-transistor pulsers are a well-established technique dating back to the 1950s–60s: the device physics and avalanche-mode operation were documented by Miller and Ebers (1955), with practical avalanche-switching circuits and nanosecond pulse generators compiled in Meiling and Stary (1969); series-stacked avalanche banks for higher voltage were already analyzed at SLAC in the late 1960s Pellegrin (1969).

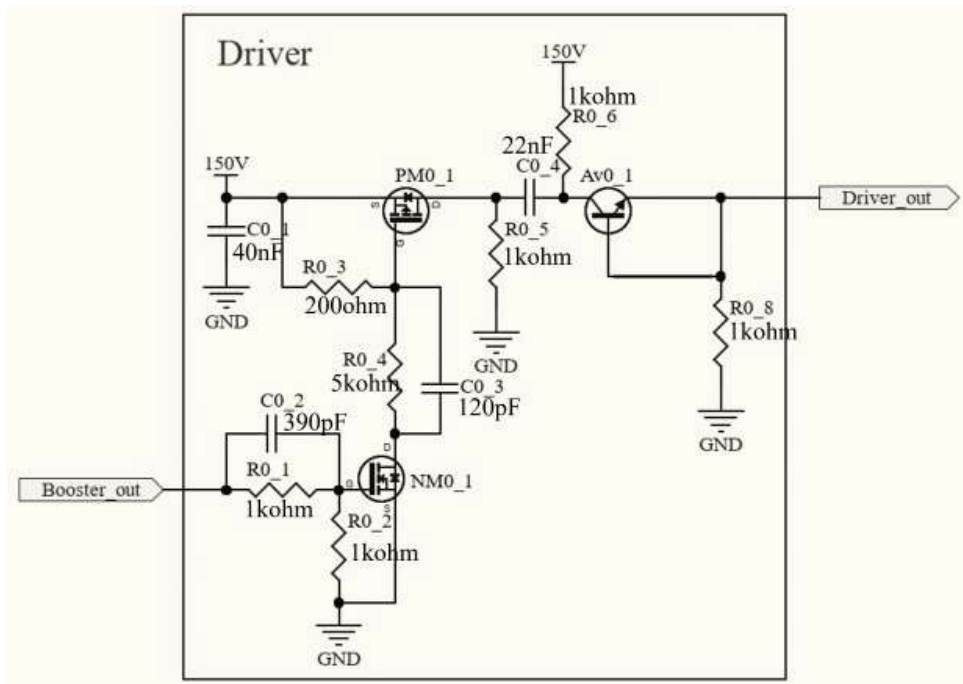


Figure 4.6: Schematic of the first version of the SiC MOSFET gate-driving driver utilizing an avalanche transistor.

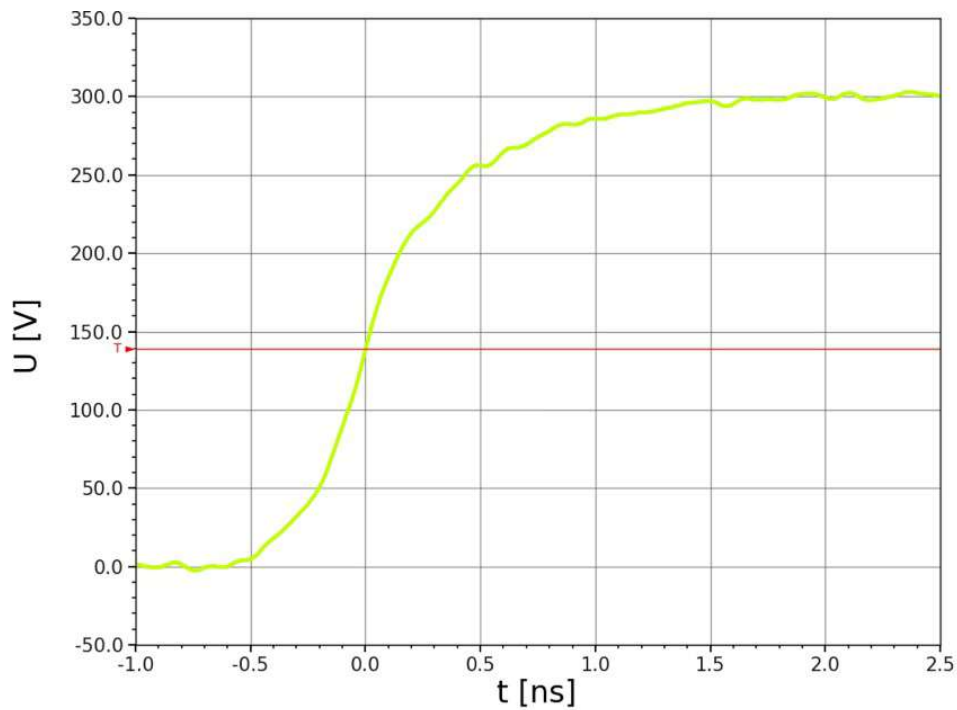


Figure 4.7: Output voltage of the gate-driving driver on Figure 4.6, on a $50\ \Omega$ load at a charging voltage of 320 V. Maximum amplitude of 300 V and $t_r = 1\text{ ns}$, measured between 10–90%.

These transistors are optimized for avalanche mode operation, exhibiting strong performance characteristics. In this context, avalanche mode operation refers to a phenomenon where a bipolar transistor is intentionally biased so that a junction enters avalanche multiplication; a single particle initiates a cascade of ionization events, generating multiple charge carriers (Miller and Ebers (1955)). Each charge carrier gains energy from the accelerating field, producing additional carriers and creating a self-sustaining chain reaction. This fast electrical trigger therefore forces a snap transition that discharges the junction and any added capacitance into a low-inductance load, creating a very steep voltage step.

In the driver chain, inserting these avalanche transistors produces exactly those signatures: each stage generates a short, unipolar step that sharpens the edge delivered to the next stage and increases the peak gate amplitude (Fig. 4.5, without avalanche transistors, vs. Fig. 4.7, with a single avalanche transistor stage).

Moving from the avalanche stage to the remaining transistors in this design, the MOS devices in the driver must satisfy a few practical criteria. Since their switching speed is largely set by gate charge and Miller behavior, the first selection metric is the datasheet rise time: the faster the device, the higher the attainable dU/dt , and thus the greater the likelihood that the resulting pulse will drive the next stage into gate-boosting mode. The second metric is the total gate charge Q_g ; devices with lower Q_g switch faster and impose less demand on the preceding driver stage, because less current is required to charge and discharge the gate.

After reviewing prior research (del Barrio et al. (2021)), a potential limitation in the driver's output current was pinpointed, when driving one or multiple parallel SiC MOS devices with high gate charge. To overcome this limitation and further enhance the performance of the driver stage, a driver upgrade incorporating a GaN FET (GaN Systems (2020)) current boosting stage in a source follower configuration is proposed, as illustrated in Fig. 4.8 (del Barrio Montañés et al. (2024b)). This enhancement amplifies the output current, reduces the output stage's impedance, and minimizes stray inductance and loop surface area, resulting in improved driving capability and reliable operation of the SiC MOSFETs under

demanding load conditions. Consequently, one of the criteria in choosing the driver's transistors is based on the shape and size of the package.

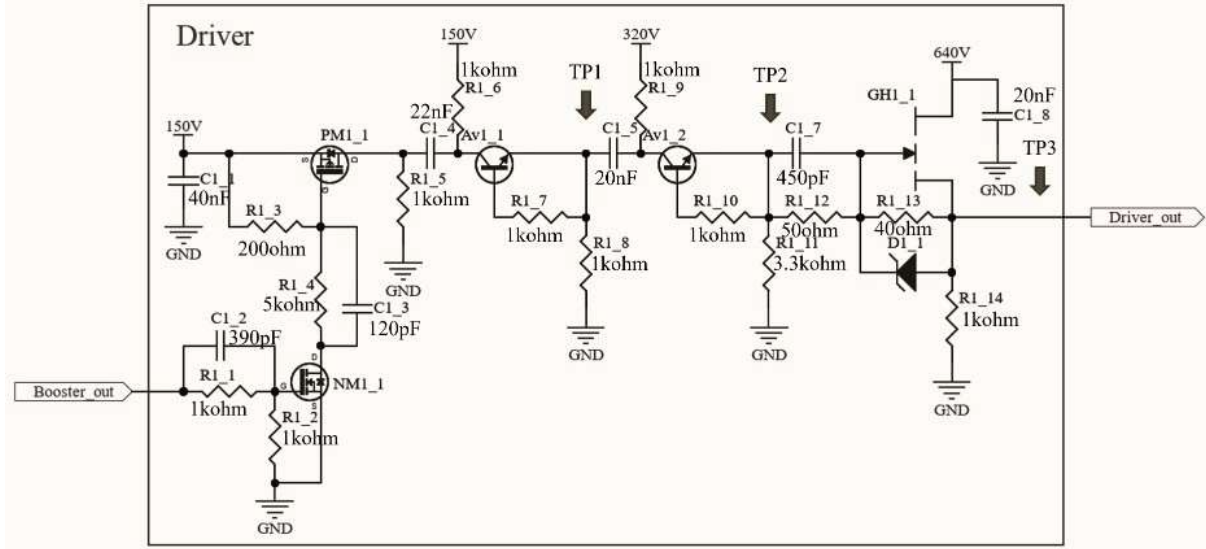


Figure 4.8: Schematic of the driver.

4.3.1 Component-Level Operation of the Driver Stages

Similar to what was described in Section 4.2.1 for the Booster stage, the input pulse follows a series of gate-boosting, pulse-sharpening stages. These are outlined as follows:

The NMOS transistor (Onsemi (2023)) NM1_1 in Figure 4.8 serves as the first level-shifting element, activated by a 45 V pulse at the Booster_out terminal. The capacitor C1_2 is in series with the gate capacitance of the NMOS, which serves as a gate-boosting element to ensure fast switching. The considerations to define its value are described in Section 2.6.1. The resistors R1_1 and R1_2 form a voltage divider that keeps the voltage in the steady state at <20 V. Following this, a similar configuration for the PMOS transistor (Onsemi (2015)) PM1_1 is set, with capacitor C1_3 acting as a gate-boosting element for the PMOS like C1_2 does for the NMOS, in series with its gate capacitance (and, same as for the NMOS, its value is given by the considerations in Section 2.6.1), and resistors

R1_3, R1_4 and R1_5 as the voltage divider that keeps the steady state voltage <25 V in this case. The capacitor C1_4 serves as the bias voltage decoupling capacitor, whereas C1_1 is placed to add the output signal of PM_1 to the 150 V feeding voltage of the avalanche transistor Av1_1 that follows.

The avalanche transistors Av1_1 (Diodes Incorporated (2015a)) and Av1_2 (Diodes Incorporated (2015b)) work in a two-stage Marx generator configuration. Accordingly, the fast-rising pulse of the PMOS drain (voltage on C1_1 = 150 V) is added to the collector–emitter voltage of the avalanche transistor Av1_1 (biased to 150 V, which is the voltage on its energy storage capacitor C1_4) and triggers it in avalanche. The sum of voltages of C1_1 and C1_4 is then added to the collector–emitter voltage of the avalanche transistor Av1_2 (biased to 320 V, which is the voltage on its energy storage capacitor C1_5) and triggers it also in avalanche. At the end, the sum of the voltages on C1_1, C1_4, and C1_5 appears on the Av1_2 emitter, minus the corresponding voltage drops on PM_1, Av1_1, Av1_2 and on the series resistances of the energy storage capacitors C1_1, C1_4 and C1_5. It should be noted that the actual limitation of Av1_1 is approximately 165 V, as determined through laboratory testing. However, this is not the recommended producer use (Incorporated (2015a), maximal ratings for U_{CE} and U_{CB} , 150 V) and therefore the biasing is limited to 150 V (del Barrio Montañés et al. (2024b)).

After this two-stage Marx generator, its output voltage drives the 650 V rated GaN HEMT (GaN Systems (2020)) via its coupling capacitor C1_7 and resistor R_12. A decoupling capacitor for the GaN HEMT drain biasing C1_8 is grounded as close as possible to the SiC MOSFET (Infineon (2020)) source to reduce its gate current loop length and, therefore, inductance. This is carried out to maximize the speed of the SiC MOSFET gate charging.

The decision to employ this specific GaN HEMT in the setup on Figure 4.8 is driven by comparing the parameters detailed in Table 4.1. In comparison to alternative options with identical datasheet drain-source voltage and continuous drain current, the GaN HEMT demonstrates a significantly reduced total gate charge; which corresponds to faster switching. During the switching process, the

gate charge is required to be supplied to the switch's gate. Regarding the package size criterion, the smaller form factor of the GaN HEMT results in decreased stray inductance. Overall, it is the most suitable component to meet the aforementioned requirements (del Barrio Montañés et al. (2024b)).

Table 4.1: Comparison of choice criteria for GaN HEMT (GaN Systems (2020)), Si MOSFET (Toshiba (2019)), and SiC MOSFET (Onsemi (2022a)) devices.

Parameter	GaN GS66508T	Si TK099V65Z	SiC NVBG095N065SC1
Package	GaNPX®	DFN8×8	D2PAK7L
U_{DS} (V)	650	650	650
I_D (25 °C) (A)	30	30	30
I_{DM} (25 °C) (A)	60	120	79
$Q_{g_{tot}}$ (nC)	6.1	47	50

A Zener diode (Taiwan Semiconductor (2023), $V_Z = 5.6V$) D1_1 together with R1_14 implements a bidirectional, window-clamp on the last driver node (and thus on the gate of the GaN HEMT it feeds). For positive polarities the diode conducts in Zener breakdown and diverts current to ground, limiting the node to:

$$U_{\text{clamp}+} \approx U_{\text{Zener}} + I_{\text{Zener}} R1_14 \quad (4.4)$$

while for negative polarities it conducts forward, limiting the node to the diode's forward voltage:

$$U_{\text{clamp}-} \approx -U_{\text{fwd}} \quad (\text{current limited by } R1_14) \quad (4.5)$$

This protects the gate oxide (caps the positive over-voltage), prevents excessive negative U_{GS} , provides a low-impedance discharge path for Miller/gate charge, and thereby improves turn-off and ringing.

4.3.2 Measurement Results and Performance Limits

At the first avalanche transistor level, the output features a pulse with an amplitude of 300 V and a rise time of 1.2 ns. At the second avalanche transistor level, the pulse reaches an amplitude of 540 V with a rise time of 1.5 ns (Fig. 4.9). These measurements are taken at the corresponding test points marked "TP" in Fig. 4.8, with a 50 Ω attenuator. At the time of these measurements, the remainder of the circuit was disconnected – i.e., the driver stage was terminated at the respective test point – ensuring that the observed signal characteristics reflect the standalone behaviour of the driver circuit without influence from subsequent stages. The pulse at TP2 level still does not rise rapidly enough for the purposes of impact ionization, likely due to increased loop inductance and series resistance, which limit the effective current transfer. To mitigate this effect, a source follower with high input impedance is implemented in the subsequent design stages.

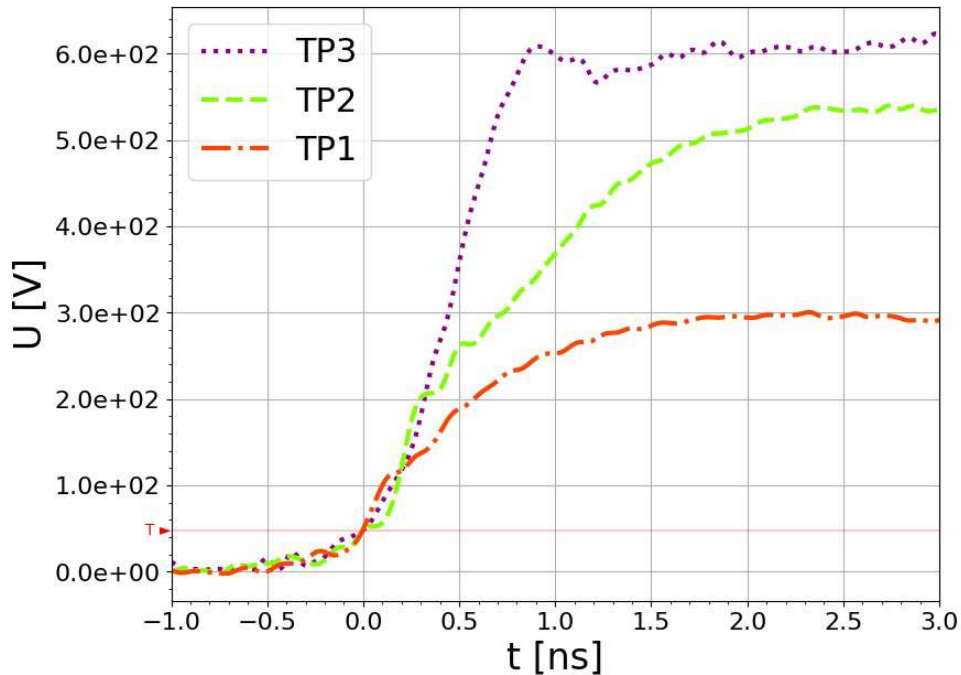


Figure 4.9: Output voltage of the first and second avalanche transistors (red and green respectively) and the GaN FET (purple), respectively on a 50 Ω load.

Therefore, a GaN FET (GaN Systems (2020)) is introduced, operated at 650 V after the two avalanche transistors. This modification enables the driver to deliver

>620 V to a $50\ \Omega$ load (Fig. 4.9), at a rate of approximately 900 V/ns (10%-90%). These conditions are highly conducive to triggering MOS components in ultra-boosted mode.

In an attempt to find the limit of this approach, this setup is operated above the recommended derated voltage in irradiated facilities (Scheick (2008)). It can be considered operating at 640 V as safe since the GaN HEMT has a significant drain-source voltage margin ($\approx 30\%$), as stated in its datasheet (GaN Systems (2020)), and GaN technology devices are supposed to be often more robust against the single-event burnout (SEB) phenomenon than Si/SiC counterparts (Mizuta and et al. (2018), Zhou and et al. (2023)). This is an abrupt failure caused by a high-energy hadron (proton or neutron), such as cosmic rays or, in accelerator facilities, stray radiation from the accelerator, striking a power semiconductor device, triggering an instantaneous breakdown of the device and compromising its reliability. Consequently, SEB immunity cannot be assumed; instead, as hereby previously described, it is recommended to minimize the risk of such events by limiting the U_{DS} operating stress, constraining the gate overdrive with a Zener diode, and keeping nanosecond transients short and current-limited (del Barrio Montañés et al. (2024b)).

4.3.3 PCB Design and Layout Considerations

In summary, employing two avalanche transistors and a GaN FET in series as the driving section results in an exceptionally sharp rising edge, leading to slew rates that can surpass 1 kV/ns for the driving pulse. This is crucial for subsequently triggering high-voltage MOS components in ultra-boosted mode.

During the design process of the PCB, particular care was taken to minimise the loop inductance in the critical current paths of the gate driving network. The most important loop in this setup is the one driving the SiC MOSFET gate (Infineon (2020), "Driver_out" on Fig. 4.8), which starts at the GaN decoupling capacitor ground, flows through the GaN HEMT, the boosting capacitor, into the gate of the SiC MOSFET, and returns via the source connection and PCB ground plane back

to the GaN decoupling capacitor ground. This loop was prioritised in the layout to ensure minimal inductance and optimal switching speed.

Other significant current paths include (labels referenced to Figure 4.8 and 4.10):

1. NMOS gate drive loop: booster ground $\rightarrow$ booster output $\rightarrow$ boosting capacitor $\rightarrow$ NMOS gate $\rightarrow$ NMOS source $\rightarrow$ return to booster ground.
2. PMOS gate drive loop: NMOS source ground $\rightarrow$ NMOS drain $\rightarrow$ boosting capacitor $\rightarrow$ PMOS gate $\rightarrow$ PMOS source $\rightarrow$ decoupling capacitor $\rightarrow$ return to NMOS source ground.
3. SiC MOSFET triggering loop: ground of capacitor C1_1 $\rightarrow$ C1_1 $\rightarrow$ PMOS source $\rightarrow$ PMOS drain $\rightarrow$ C1_4 $\rightarrow$ Av1_1 $\rightarrow$ C1_5 $\rightarrow$ Av1_2 $\rightarrow$ C1_7 and R1_12 $\rightarrow$ Zener and R1_13 $\rightarrow$ GaN gate $\rightarrow$ GaN source $\rightarrow$ boosting capacitor $\rightarrow$ SiC gate $\rightarrow$ SiC source $\rightarrow$ ground $\rightarrow$ back to C1_1 ground via the PCB ground plane.

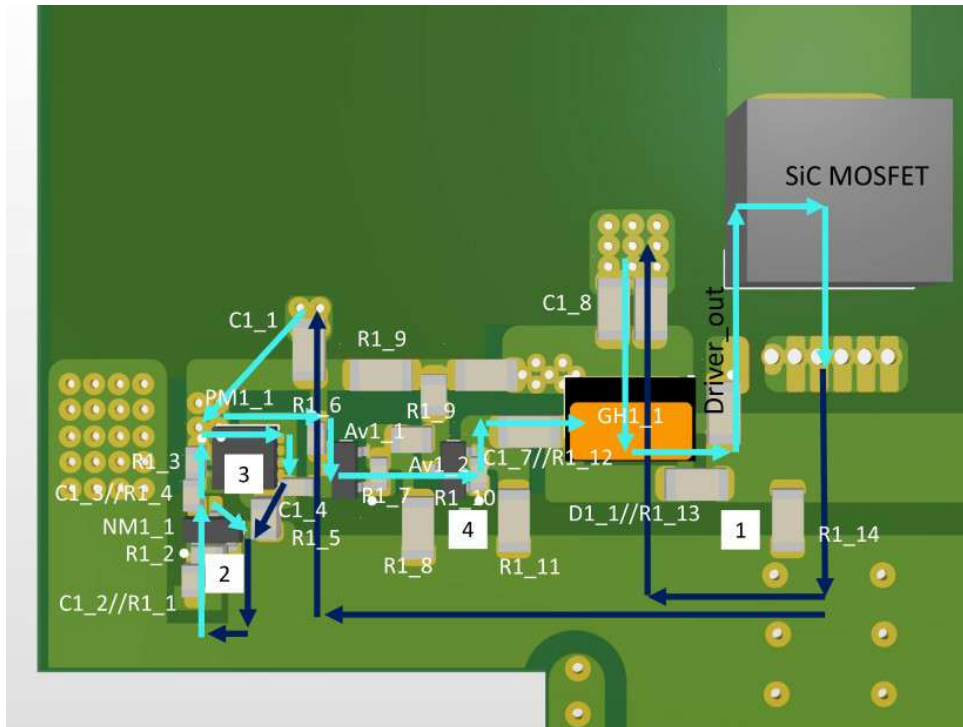


Figure 4.10: 3D rendering of the driver on the PCB. Light blue indicates the driving current path on the top plane, and dark blue the return path on the bottom plane.

The selection of small component casings and their strategic placement not only minimizes the length of the triggering loop but also contributes to the overall compactness of the PCB. Consequently, one of the criteria in choosing the driver's transistors is based on the shape and size of the package.

A 3D rendering of the driver layout is shown in Figure 4.10, where the highlighted traces represent these critical current paths. The compact arrangement of components and the emphasis on short, direct routing for both high-side and low-side loops contributes to the improved overall performance of the gate driver and enhances signal integrity.

4.4 SiC MOSFETs with Gate Ultra-Boosting for Enhanced Slew Rate

The utilization of gate boosting technology, aimed at enhancing the commutation speed of silicon IGBTs and MOS transistors, has yielded significant results, as discussed in Chapter 2. Earlier studies (Hochberg et al. (2016)) demonstrated a reduction in rise time (T_r) by a factor of approximately eight on IGBTs, confirming the effectiveness of this approach. Building on this foundation, more recent research has achieved a tenfold T_r reduction specifically for SiC MOSFETs (Azizi et al. (2020)).

Gate boosting operates by applying a controlled overvoltage to the gate terminal during the switching transition. This technique counters the limitations imposed by internal lead inductance and parasitic capacitances within the semiconductor structure, all while avoiding permanent damage to the device. Its effectiveness has been validated in experimental work (Hochberg et al. (2016)), and previous publications demonstrated successful gate boosting on a single SiC MOSFET in earlier studies (del Barrio Montañés et al. (2023), Senaj et al. (2021b, 2022), del Barrio Montañés et al. (2024a,b, 2025)).

Following this initial validation phase, the focus shifts to a more demanding configuration: triggering multiple SiC MOSFETs in parallel. This step aims to significantly increase the pulse generator's output current to 200 A, in accordance with the requirements outlined in Section 4.1.

4.4.1 Parallel Configuration and Schematic Overview

To achieve the current levels necessary for triggering medium-sized thyristors—whose ratings exceed 200 A—a dedicated setup has been implemented, as illustrated in Figure 4.11. This configuration consists of N SiC MOSFETs connected in parallel, all driven by a common gate driver described in Section 4.3. The

resulting increase in output current is essential for reliably triggering the thyristor stack at the final stage of the pulse generator (del Barrio Montañés et al. (2025)).

With N parallel devices and a current-sharing factor $\gamma \in (0, 1]$ to account for tolerances, the per-device peak current is:

$$N \geq \frac{I_{\text{req}}}{\gamma I_{D,\text{ns-pulse}}}. \quad (4.6)$$

Using $I_{\text{req}} = 200$ A (Section 4.1), a sharing factor $\gamma = 0.8$ for a symmetric, short-return layout, and the device's ns-scale pulsed capability $I_{D,\text{pulse}}$, the required number of devices N is inferred from the equations above. The concrete numbers for the chosen switch are worked out in Section 4.4.1.1.

This design approach ensures that the current supply is available to effectively trigger these thyristors. Additionally, the use of multiple parallel MOS transistors offers scalability and flexibility, allowing for the accommodation of an even greater number of paralleled MOS transistors if needed. By combining multiple SiC MOS transistors in parallel, the overall current-carrying capacity is significantly increased, ensuring that the triggering requirements of medium-sized thyristors are met efficiently.

4.4.1.1 Device Selection and Characterization

To achieve a slew rate exceeding 1 kV/ns, it is essential to select a high-voltage (HV) MOS transistor that can be efficiently driven by the output of the pulse generator's driver stage. For this purpose, a range of silicon and silicon carbide (Si and SiC) MOSFETs were tested and evaluated to determine the most suitable candidate for the application. Table 4.2 provides a summary of the key parameters considered during this selection process, including rated drain-source voltage, pulsed current capacity, total gate charge, and datasheet rise time.

The key features sought in a suitable MOSFET, based on datasheet specifications and practical considerations, included:

	U_{ds} (V)	$Q_{g_{total}}$ (nC)	t_{rise} (ns)
SCT3080KL (ROHM Semiconductor (2022))	1200	60	22
NVHL080N120SC1 (Onsemi (2022b))	1200	56	20
APT12057LFLL (Microchip Technology (2004))	1200	185	20
IMBF170R450M1 (Infineon (2020))	1700	11	20
NTHL160N120SC1 (Onsemi (2023b))	1200	34	19
IMBF170R650 (Infineon (2025))	1700	8	16
IPB60R120P7 (Infineon (2018))	650	36	14
NTBG160N120SC1 (Onsemi (2023a))	1200	33.8	11
C2M0080170P (Wolfspeed (2018))	1700	120	9
C3M0016120J (Wolfspeed (2024))	1200	24	8
SCTH40N120G2V7AG (STM (2021))	1200	63	5

Table 4.2: Summary of high voltage Si and SiC MOS transistors tested

- Datasheet rise time as low as possible (under comparable triggering conditions).
- Lowest Q_g total possible.
- Estimated Q_g for $V_{GS} = 20$ V (“Typical gate charge” graph) as low as possible.
- Smallest package possible (low-inductance body and short leads for soldering).
- Lowest $R_{DS(on)}$ possible.

After evaluation of these factors, the IMBF170R450M1 (Infineon (2020)) was selected. Its electrical characteristics—particularly its voltage and current ratings—aligned well with the demands of the pulse generator. Furthermore, its fast-switching performance, when driven by the gate driver described in Section 4.3, confirmed its suitability for this application.

For this device, the datasheet lists $I_{D,pulse} = 24.8$ A (defined for μs pulses and a specified case temperature). The edge is ~ 1 ns into a predominantly capacitive load, so the relevant constraint is not the μs $I_{D,pulse}$ but rather the per-device current share during the 1 ns edge and the instantaneous energy in the channel

and inductive overshoot. With $N = 6$ devices and a sharing factor $\gamma = 0.8$, the per-device peak current is

$$I_{\text{dev,pk}} = \frac{I_{\text{req}}}{N \gamma} = \frac{200}{6 \times 0.8} \approx 41.7 \text{ A}. \quad (4.7)$$

The corresponding instantaneous channel energy over a ~ 1 ns edge is

$$E_{\text{ch}} \approx I_{\text{dev,pk}}^2 R_{\text{DS(on)}} t_{\text{edge}}, \quad (4.8)$$

which, using the device's room-temperature $R_{\text{DS(on)}}$ (order 0.45Ω), yields

$$E_{\text{ch}} \approx (41.7 \text{ A})^2 \times 0.45 \Omega \times 1 \text{ ns} \approx 0.8 \mu\text{J per device}, \quad (4.9)$$

i.e., negligible thermal rise at ns timescales. The per-device inductive kick remains within the clamp budget:

$$V_{L,s} = L_s \frac{I_{\text{req}}/N}{t_{\text{edge}}} \approx 0.8 \text{ nH} \times \frac{200/6}{1 \text{ ns}} \approx 26.7 \text{ V}. \quad (4.10)$$

Thus, despite the μs $I_{D,\text{pulse}}$ value of 24.8 A, the ns-scale operation with current-limited, capacitive loading justifies the choice $N = 6$ without violating device limits. Therefore, N is determined from (4.7)–(4.10) (ns regime) rather than from the datasheet-specified long-pulse $I_{D,\text{pulse}}$.

The decision was made to trigger all parallel SiC MOSFETs using a common driver to simplify the system and avoid synchronization issues that could arise from using individual drivers for each transistor. To address the potential coupling problems between the six parallel transistors, a microstrip was added to each branch (del Barrio Montañés et al. (2024b)). A microstrip is a transmission line configuration consisting of a conductive trace mounted on a dielectric substrate, with a ground plane on the reverse side (Hoffmann and Howe (1987)). This setup facilitates

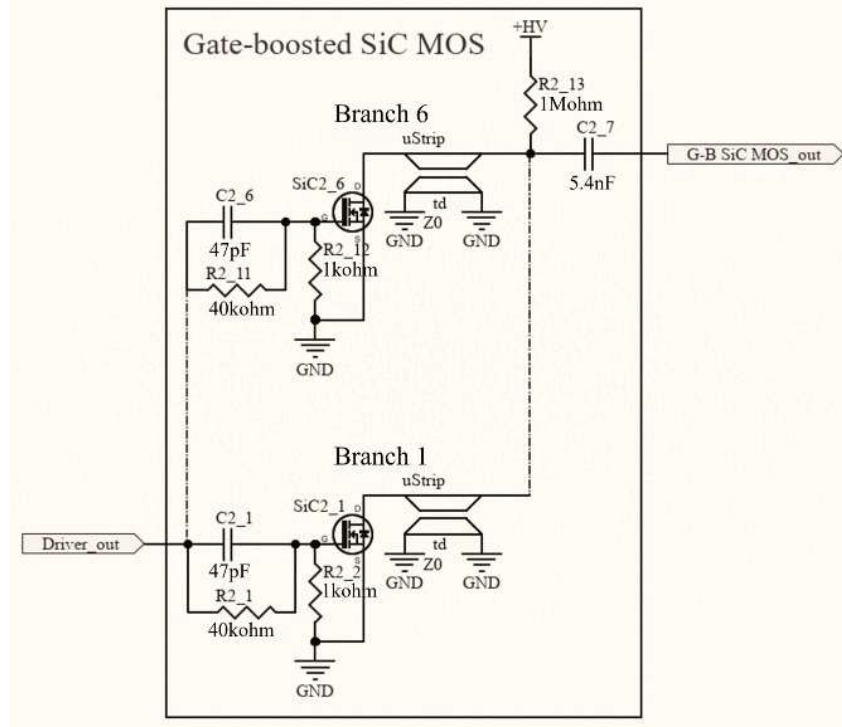


Figure 4.11: Schematic of the six SiC MOSFETs ($SiC2_1$ to $SiC2_6$), with the corresponding microstrips, in parallel.

controlled impedance and signal propagation delay, physically decoupling the respective drains of the SiC MOSFETs and introducing a time delay, which is compensated by the geometric properties of the connection. Figure 4.11 shows the schematic including the six gate-boosted SiC MOSFETs and the corresponding microstrips acting as transmission lines, and Figure 4.12 shows a 3D rendering of the PCB layout.

To ensure gate boosting of these devices, the values of capacitors $C2_1$ through $C2_6$ are adjusted. These capacitors counteract the effects of both input capacitance and reverse transfer (Miller) capacitance inherent in the SiC MOSFETs being triggered. The strategy prioritizes controlling the total injected MOS gate charge (Q_{tot}) rather than measuring or restricting the gate-source voltage at the wafer level (del Barrio Montañés et al. (2024b)).

To maintain adherence to this criterion, a capacitor ($C2_1$ to $C2_6$) is placed in series between the driver output and the MOS gate. The value of these capacitors follows 2.1:

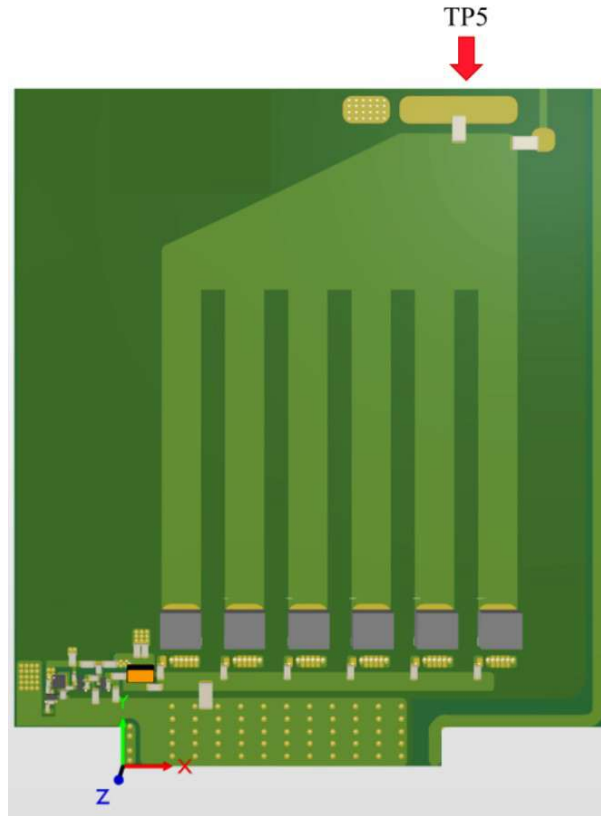


Figure 4.12: PCB 3D rendering representing the six SiC MOSFETs and microstrip branches of the pulse generator. The propagation delay of the individual SiC gate driving signal is mostly compensated by the geometry of their drain transmission lines layout and the placement of the output feeding point on the opposite extremity.

Regarding the gate resistors R2_1,3,5,7,9,11 and R2_2,4,6,8,10,12, they form a voltage divider aimed at fixing the DC gate voltage to less than 20 V at $U_{drV_{max}}$ as per Infineon (2020). Any momentary spikes in the gate voltage exceeding this threshold during the commutation time have limited effects given the sub-nanosecond timescales involved. Some destructive effect of the transient over-voltage is acceptable on the SiC gate (greater than 100 V at package level, "TP3" in Fig. 4.8, which is also labeled as "Driver_out" in Fig. 4.11; not measured at wafer level), provided the required lifetime is respected.

4.4.2 Micro CT Scan of Components

A focused CT scan study was conducted, primarily to verify working hypotheses about how specific package features control lead inductance and current paths. The intent was not an exhaustive metrology campaign but a practical check to validate design assumptions relevant to the fast, high- dU/dt driver stages.

CT scanning is a non-destructive method that reveals internal structures without chemically or mechanically opening the devices. In this context, this avoided destructive teardowns of the SiC MOSFET and thyristor packages while still exposing the current-carrying geometry that dominates parasitics.

4.4.2.1 Qualitative findings

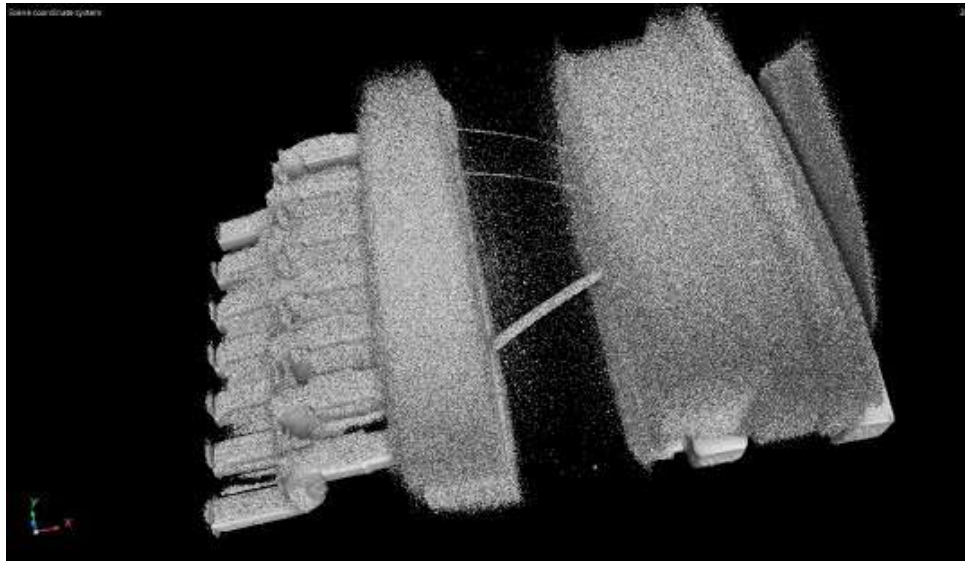


Figure 4.13: CT scan of a SiC MOS IMBF170R650M1XTMA1. Courtesy of CERN MME Group.

From the reconstructed slices and volume renders in Figs. 4.13–4.14, the following internal features were identified that directly impact series inductance and switching behaviour:

The scans in Figs. 4.13–4.14 reveal internal features consistent with lower package inductance—e.g., multiple short parallel bond wires, compact source return paths,

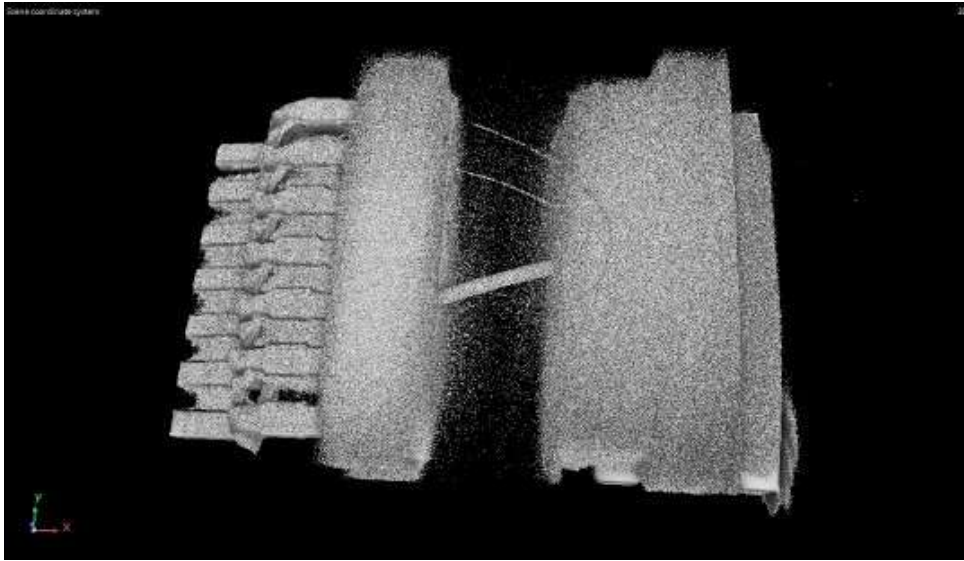


Figure 4.14: CT scan of a SiC MOS IMBF170R450M1XTMA1. Courtesy of CERN MME Group.

and direct leadframe routing. These observations are illustrative rather than exhaustive and align with the ringing and edge-rate differences seen on the bench.

The micro-CT scans were used qualitatively on the chosen SiC MOSFET (Infineon (2020)) to visualize internal features that plausibly affect lead inductance. Component choices in Chapter 4 were made primarily from datasheet parameters (e.g., Q_g , t_r , $R_{DS(on)}$, package) and bench performance; CT images serve only to corroborate and interpret observed behavior.

4.4.2.2 Limitations

The CT voxel size was insufficient to derive precise bond diameters or to extract absolute inductance values; therefore the analysis is qualitative. Nevertheless, the geometric trends (bond count/loop height, leadframe width/length, and source return separation) are resolved well enough to support the design choices and explain differences seen in ringing and turn-on reproducibility.

All CT images were provided by CERN’s Mechanical and Materials Engineering (MME) Group and are reproduced here with permission.

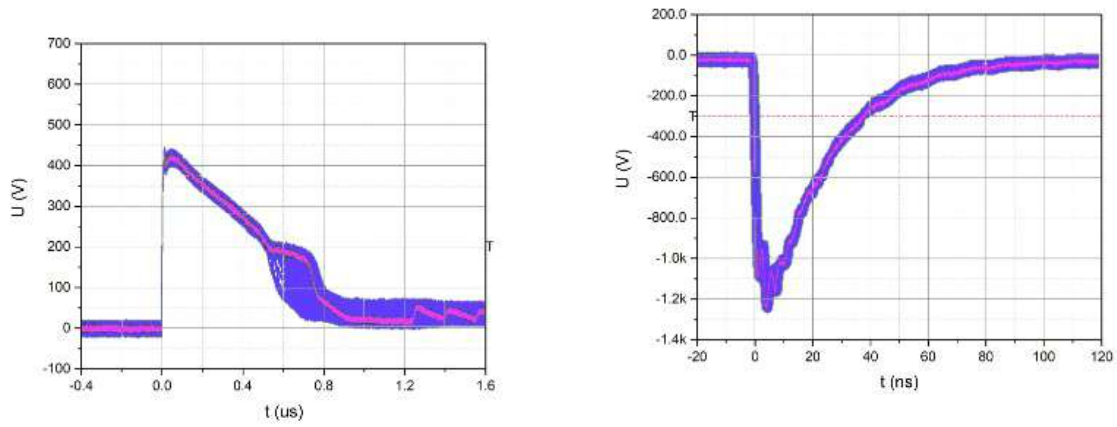
4.4.3 Lifetime Tests

These sub-nanosecond over-voltages have limited effects in the sense that the time-integral of oxide stress and the injected charge are very small. With a series- C gate boost the charge delivered to the gate is bounded by $Q_{inj} \approx C_s \Delta V$. Gate-oxide wear-out in Si/SiC follows time-dependent dielectric breakdown (TDDB) kinetics in which lifetime scales super-linearly with reduced stress time and strongly with electric field; very short, low-duty transients contribute negligibly to cumulative damage compared to longer stresses at the same field (Baliga (2018), Borja et al. (2016)). Consistent with this, the endurance operation (repetitive triggering) showed no measurable drift in gate threshold or waveform shape within the test duration; therefore a brief, sub-nanosecond over-voltage is accepted while meeting the required lifetime.

An aggressive triggering approach has been adopted, which impacts the component's operational lifespan but remains within acceptable limits for the system's overall lifetime. A lifetime of more than 10^5 pulses is deemed sufficient for the kicker systems considered in these investigations (Kramer (2011)). Although this approach has the potential to reduce component lifespan, it is still compatible with the expected use for the kicker systems, given that the present target applications, specifically CERN kicker systems, are expected to perform up to 10^8 pulses throughout their lifetime (del Barrio Montañés et al. (2024b)).

It is important to note that the gate-source voltage at the wafer level was not measured nor limited. Instead, strict adherence was given to the total injected MOS gate charge (Q_{tot}) parameter. This prioritization ensures that the system meets the performance and durability requirements of the kicker systems.

The driver achieved a cumulative endurance of 2×10^6 switching events (Fig. 4.15a). For this test, the output was connected to a representative load formed by 180 pF (six 30 pF coupling capacitors in parallel) in series with 3.5Ω (the parallel combination of the six 20Ω internal gate resistors of the SiC MOSFETs). When the driver was subsequently coupled to the bank of six parallel SiC MOSFETs, a lifetime of at least 1×10^6 pulses was demonstrated on a 4Ω load (Fig. 4.15b).



- (a) Driver lifetime test, "TP3" in Fig. 4.8, total $2 \cdot 10^6$ pulses. Loaded with 180 pF and 3.5Ω to reproduce the six SiC MOSFET loading; charging voltage 640 V.
- (b) 6x SiC MOSFET lifetime test, "G-B SiC MOS_out" in Fig. 4.11, total $1 \cdot 10^6$ pulses. Loaded with 4Ω to reproduce the condition of an output current >220 A (calculated output current >300 A); charging voltage 1.3 kV.

Figure 4.15: Lifetime test

Taken together, these endurance runs indicate that the pulse generator meets the commissioning requirements for a kicker-magnet modulator in the beam-dump system at CERN (Kramer (2011)). These results are preliminary, as a full statistical lifetime qualification has not yet been performed.

Because the application features negligible steady-state power dissipation and an extremely low duty cycle ($< 0.0001\%$), the dynamic thermal load is minimal; accordingly, no dedicated thermal management study was carried out for these devices.

4.4.4 Measurement Results for Parallel SiC MOSFETs

The different tests have been done using a 6 GHz oscilloscope with a series of 10 to 18 GHz, 50Ω attenuators used as output loads.

The results for a single IMBF170R450M1 SiC MOSFET (as per del Barrio Montañés et al. (2024a)) are depicted in Figure 4.16, illustrating three charging voltages

in the range representing the later operation from 1.3 kV to 1.5 kV. The measurements were performed using a $50\ \Omega$ load and with an identical driver to the one detailed in Section 4.3 (del Barrio Montañés et al. (2024b)).

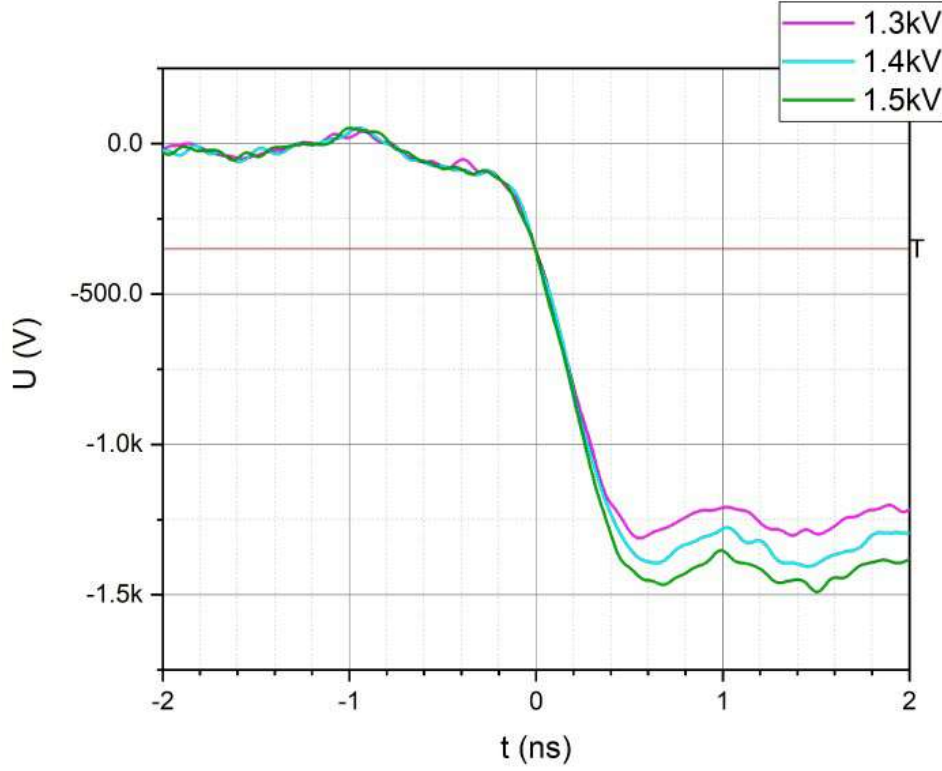


Figure 4.16: Output voltages obtained on a single IMBF170R450M1 SiC MOSFET on a $50\ \Omega$ load, at different charging voltages.

As previously described in Section 4.4, and represented in Figure 4.12, presently each SiC MOSFET has its own microstrip with $\approx 21\ \Omega$ impedance (FEMM calculation (Meeker (2023))) and $\approx 0.78\ \text{ns}$ length which aims to mutually decouple the individual drains of the SiC MOSFET triggered by a common driver to cope with the spread of the switching times of each individual SiC MOSFET (Figure 4.12).

$$\begin{aligned}
v_p(outer) &= \frac{v_c}{\sqrt{\epsilon_{reff}}} \\
t_d(outer) &= \frac{length}{v_p} \\
\epsilon_{reff} &= \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \cdot (1 + 12 \cdot \frac{h}{W})^{-\frac{1}{2}} - \frac{\epsilon_r - 1}{4.6} \cdot \frac{t/h}{\sqrt{W/h}}
\end{aligned} \tag{4.11}$$

The delay calculation on an outer stripline on a PCB is described in Equation 4.11 (Bahl and Garg (1977)), where

- v_p is the propagation speed, in this case on the outer layer of the PCB.
- v_c is the speed of light in vacuum.
- ϵ_{reff} is effective dielectric constant for microstrips.
- ϵ_r is the dielectric constant of the PCB material.
- h is the height of the substrate.
- t and W are respectively the thickness and width of the microstrip.
- t_d is the propagation delay due to the length of the microstrips in the outer layer of the PCB.

The outcome of this step is depicted in Figure 4.17, capturing the performance characteristics of this pulse generator with six SiC MOSFET transistors operating simultaneously. This test was performed with a charging voltage ranging from 1.2 kV to 1.7 kV on an attenuator's 50Ω load. The maximum amplitude of the output voltage is 3.2 kV and a 10–90% slew rate of 2 kV/ns (del Barrio Montañés et al. (2024b)).

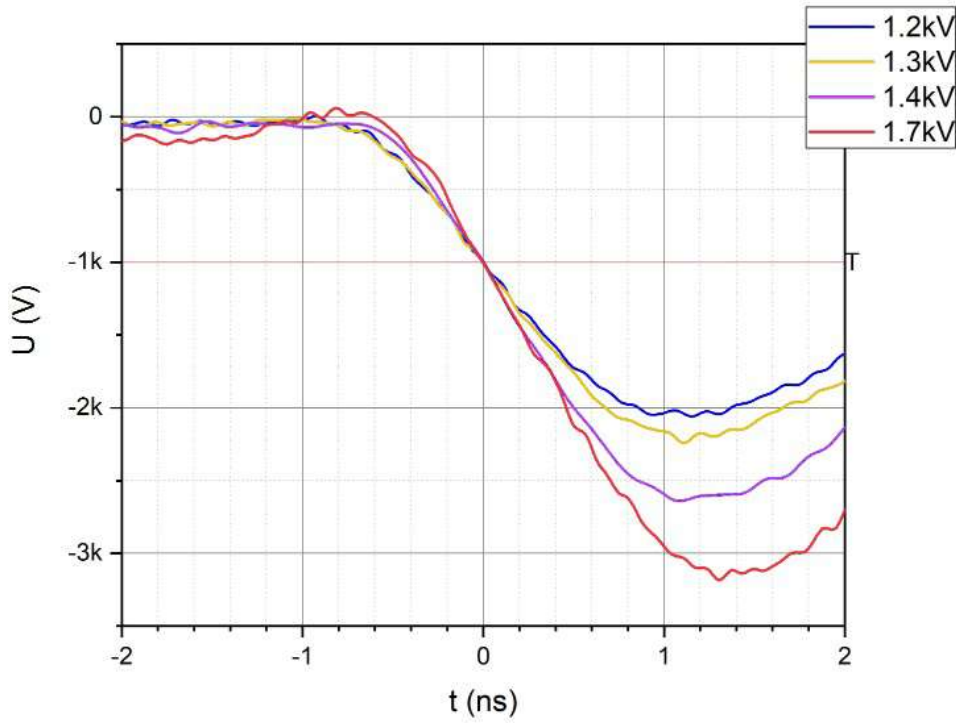


Figure 4.17: Output voltage of the six parallel IMBF170R450M1 SiC MOSFETs on a $50\ \Omega$ load (TP5, Figure 4.12), different charging voltages. At a 1.7 kV charging voltage, the maximum voltage amplitude is 3.2 kV and a 10–90% slew rate of 2 kV/ns.

The impedance mismatch of the microstrips with respect to the $50\ \Omega$ output load causes the reflection of the signal, almost doubling its voltage due to the superposition of the incident and reflected waves (reflection factor $\Gamma = 0.9$). This is the reason why the output voltage is higher than the feeding voltage of the SiC MOSFETs.

Given that the core intention of increasing the quantity of SiC MOSFETs primarily aims to amplify the output current of the pulse generator's driving phase, a focused experiment was undertaken specifically under the condition of a $4\ \Omega$ load (del Barrio Montañés et al. (2024b)). This testing procedure was performed to comprehensively evaluate the performance enhancement attributed to the increased number of SiC MOSFETs.

The obtained results, for a test at 1.7 kV charging voltage on a $4\ \Omega$ resistive load with minimized inductive elements, graphically represented in Figure 4.18, show this. The output voltage on a less mismatched load ($4\ \Omega$ for six $15\ \Omega$ microstripes

in parallel) is reduced. However, the output curve exceeds the threshold of 220 A after calculation, delivering 400 A, making it 66 A per SiC MOSFET. According to its datasheet, this implies a $2.6\times$ greater surge output current per SiC MOSFET than the datasheet established 24.8 A (Infineon (2020)), lasting in the range of tens of nanoseconds. This upsurge in output current validates the effectiveness of incorporating additional SiC MOSFETs to the setup.

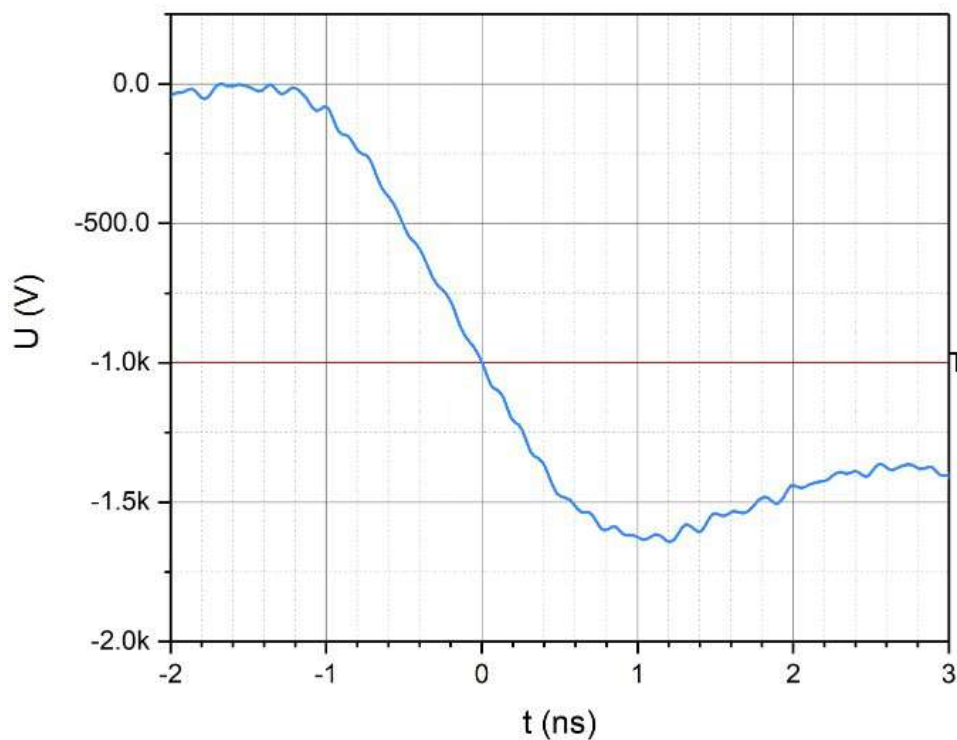


Figure 4.18: The output voltage of the six parallel IMBF170R450M1 SiC MOSFETs on a 4Ω load (TP5, Figure 4.12), charging voltage 1.7 kV. The maximum voltage amplitude is 1.6 kV; hence, there is a calculated output current of 400 A.

4.5 Triggering of a thyristor in impact ionization mode

Prior to advancing to the full thyristor stack, an initial experiment was conducted to validate the feasibility of Impact Ionization triggering using a single thyristor. For this purpose, a topology as shown in Fig.4.19 was implemented, employing a Vishay D2PAK, 1.2 kV-rated thyristor (Vishay (2021)) —the same device intended for the Marx generator implementation. The thyristor was reverse-biased at -1 kV through a 500 k Ω resistor. A 100 nF coupling capacitor (C_{out}) was used between the thyristor node and the probe input to block the -1 kV DC bias while passing the nanosecond pulse with negligible droop. The triggering concept for this last test follows the same principle as in the thyristor-based Marx generator (Section 4.6), where a fast voltage pulse generated by the driver circuit initiates the commutation process through impact ionization, leading to conduction in less than a nanosecond.

The implementation of the full thyristor stack, however, falls outside the scope of this thesis and is left for future work.

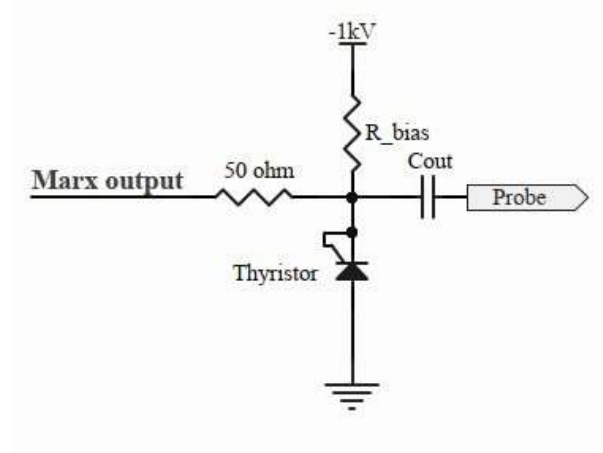


Figure 4.19: Schematic of biased thyristor triggered by a Marx generator

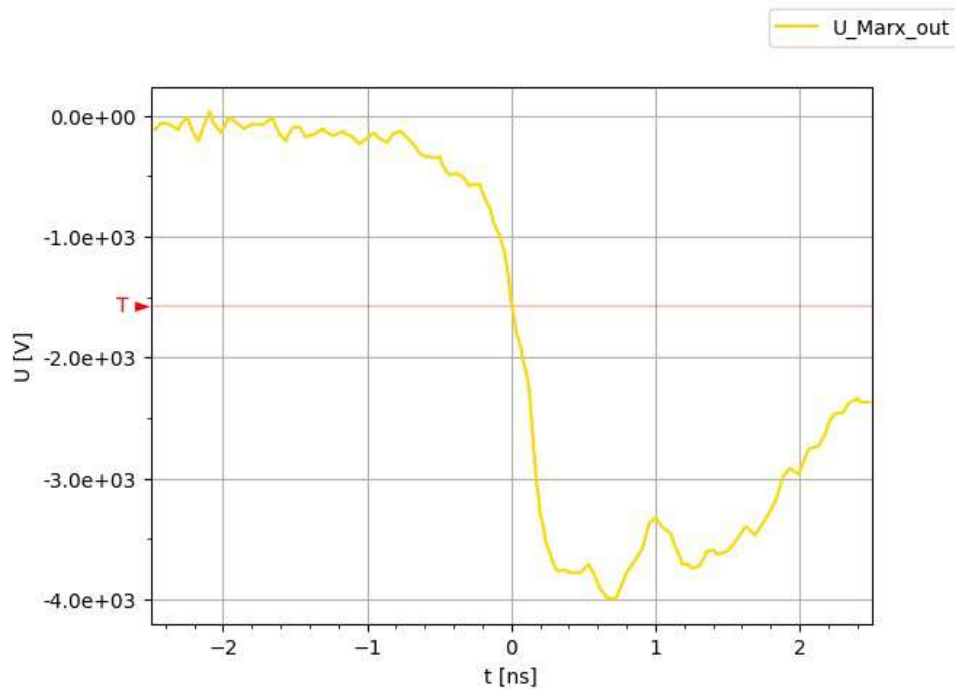


Figure 4.20: Output from the Marx stage; trigger signal for impact ionization on a single thyristor, onto $50\ \Omega$ load

Figure 4.20 shows the output voltage of the Marx generator across a $50\ \Omega$ load. The waveform exhibits a steep negative voltage transition, with an amplitude exceeding 4 kV and a rise time on the order of sub-nanoseconds. This fast transient ensures a voltage slew rate greater than 1 kV/ns, fulfilling the conditions required for initiating impact ionization in the thyristor's junction. The subsequent damped oscillations are attributed to parasitic effects and impedance mismatches in the circuit.

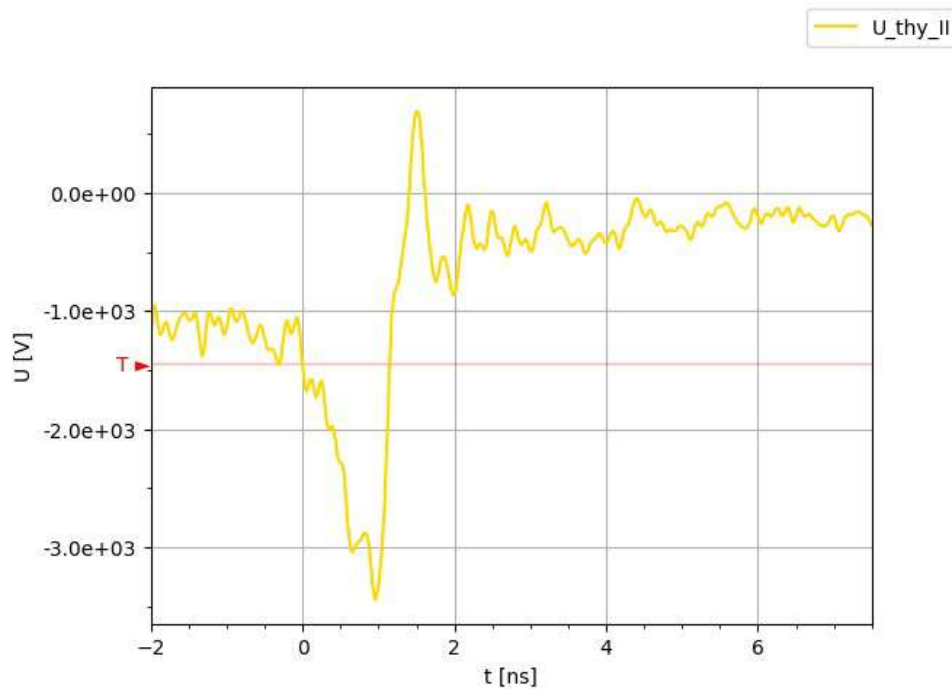


Figure 4.21: Impact ionization triggering of a thyristor onto 50 Ω load

The phenomenon of impact ionization on the thyristor is seen on Figure 4.21. The thyristor commutation time (10% to 90% of the peak to peak amplitude ≈ 4 kV) is of ≈ 250 ps. The voltage waveform shows a rapid transition from a blocking state to conduction, initiated by the steep negative voltage pulse from Figure 4.20 added to the biasing voltage. The sharp recovery and overshoot peaking above 0 V confirm the abrupt nature of the switching process. After commutation, the voltage stabilizes near zero, indicating the thyristor is fully conducting. The oscillations following the transition are attributed to parasitic inductance and capacitance in the layout, but do not impair the successful triggering of the device.

4.6 Design and Architecture of the Thyristor Marx generator

The third stage of this setup encompasses an ultra-fast Marx generator, which operates by utilizing thyristors. The complete system that will be presented in this chapter is illustrated in Figure 4.22, comprising four key stages: the input signal generated by an external pulse generator, which drives the Driver stage, followed by the Gate-Boosted (G-B) SiC MOS, and finally the Thyristor Marx Generator (del Barrio Montañés et al. (2025)).

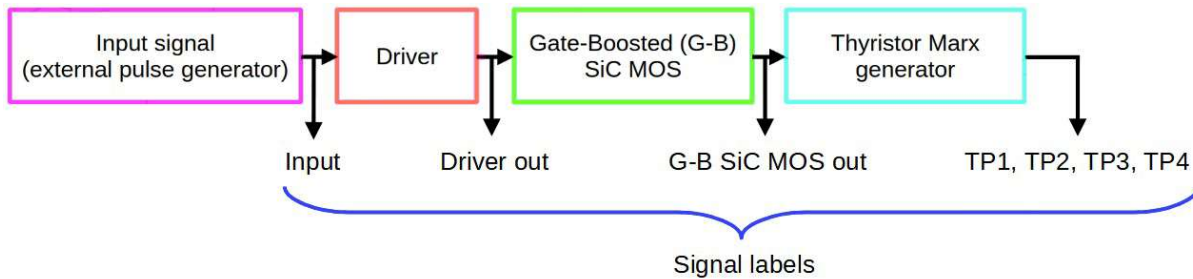


Figure 4.22: Diagram illustration of the complete system.

Our Marx generator comprises multiple stages of thyristors with a voltage rating of 1.2 kV (Vishay (2021)). The number of stages employed depends on the desired output voltage amplitude. In this configuration, the triggering of the Marx generator is accomplished by leveraging the capabilities of the driving stages described in previous Sections (4.2, 4.3, 4.4). The negative voltage generated by the MOSFET stage is now applied to the cathode of the thyristors, initiating the operation of the Marx generator. Each stage of the Marx generator effectively adds its storage capacitor voltage while simultaneously sharpening the pulse's rise time to achieve the power required for a successful impact ionization triggering.

According to the datasheet of the D2PAK thyristors (Vishay (2021)), these devices can handle extremely short pulses with peak currents reaching nearly 100 times their RMS rating for nanosecond-scale durations. The thyristors chosen for this application are specified for 16 A RMS, but can withstand peak currents above

1 kA, with a parasitic capacitance of 14 pF. For the present phase of testing, a 4-stage Marx generator has been implemented, as shown in Figure 4.24.

4.6.1 Breakdown Voltage Evaluation through Leakage Current

To identify the most suitable thyristor for high-voltage pulse applications using impact ionization triggering, a comparative study was conducted of leakage currents across a selection of commercially available D2PAK-packaged thyristors. Leakage current is a critical parameter, as it directly impacts the voltage-sharing behavior in series-stacked configurations and can influence triggering reliability. Each device was tested over a range of reverse voltages until breakdown.

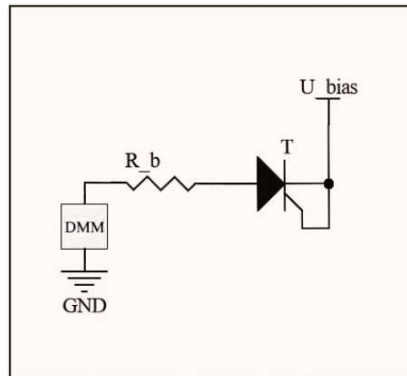


Figure 4.23: Reverse-bias leakage and breakdown test for small-packaged thyristors; leakage is read by a DMM used as a low-side series ammeter. A sustained current rise marks breakdown.

Each D2PAK thyristor was reverse-biased on a simple HV bench and its DC leakage measured with the digital multimeter (DMM) in ammeter mode placed in series with the device (Figure 4.23). A programmable negative HV supply fed the DUT anode through a ballast resistor R_b (1 M Ω) to limit current and energy at breakdown. The return path at ground contained the DMM (series ammeter); this low-side placement kept the instrument near ground potential. The measured current was read directly as I_{leak} .

Bias was increased in small steps (1–2 s dwell) until a sustained current jump indicated breakdown; R_b protected both DUT and instruments during this event. The fixture used short, guarded connections to minimize surface leakage. This procedure produced the leakage-versus-voltage curves and breakdown onsets reported in Tables A.1 to A.5 (Appendix 4.6.1), which were then used for device selection. Based on the combination of breakdown voltage margin and consistently low leakage current values; as well as the highest voltage rating possible, the VS-16TTS12S-M3 thyristor (Vishay (2021)) was selected for use in these experiments. Its leakage current measurement is reported here in Table 4.3.

Table 4.3: Reverse-leakage measurements for VS-16TTS12S-M3.

VS-16TTS12S-M3 (Vishay (2021))	
V_{RRM} (V)	1200
I_{RMS} (A)	16
I_{TSM} (A)	200
U (V)	I_{leak} (μA)
200	0.36
400	0.45
600	0.55
700	0.58
800	0.64
900	0.70
1000	0.76
1100	0.86
1200	0.95
1300	1.11
1400	1.30
1500	1.73
1600	1.70
1700	BD

4.6.2 Triggering Mechanism and Impedance Study

The first stage of the Marx generator employs a single thyristor rated at 1.2 kV (VS-16TTS12-M3 (Vishay (2021))). To trigger this device in impact ionization mode, a voltage at least twice its breakdown level is required (breakdown voltage for this component 1.6 kV, Table 4.3). This triggering signal is generated by the output of six parallel SiC MOSFETs, as per Section 4.4, combined with the charge stored in capacitor C3_1 (Figure 4.24) to reach the necessary overvoltage.

As the pulse propagates through the stages, additional thyristors are introduced to withstand the increasing voltage. In principle, a partial “natural” voltage sharing can occur in a series string because device leakage currents are voltage dependent Rashid (2014); however, this design does not rely on this effect. In the present design Fig. 4.24), each stage capacitor (C3_2 to C3_5) contributes a voltage increment HV_i (HV_1 , HV_2 and HV_3 on Figure 4.24, through the biasing resistors R3_1, 3, 5, 7 and 9), and the steady-state voltage distribution across the series thyristors is actively set by parallel equalizing resistors (potential control). This resistive grading defines the intended DC voltage division and provides a controlled discharge path, while the dynamic sharing during fast edges is handled by the driver timing and the layout’s low stray inductance (del Barrio Montañés et al. (2025)).

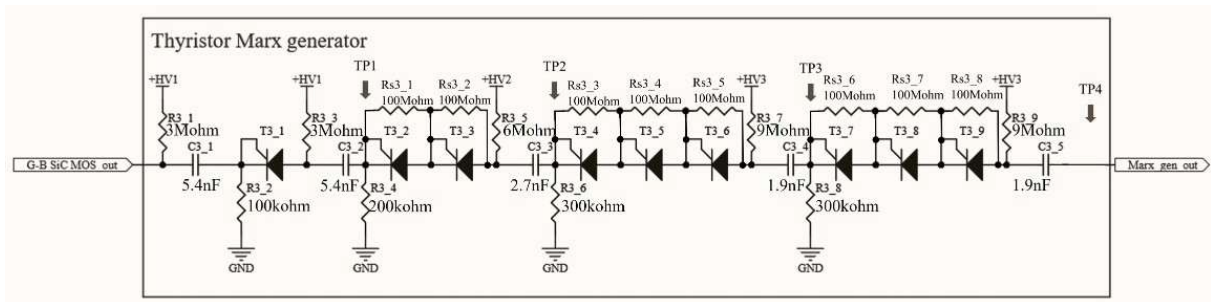


Figure 4.24: Schematic of the four stages Marx generator with D2PAK thyristors

To reinforce this voltage balancing mechanism, resistors (Rs3_1 to Rs3_8, Figure 4.25) are connected in parallel with each thyristor. These resistors provide a balancing current of approximately 13 μ A at a maximum charging voltage of

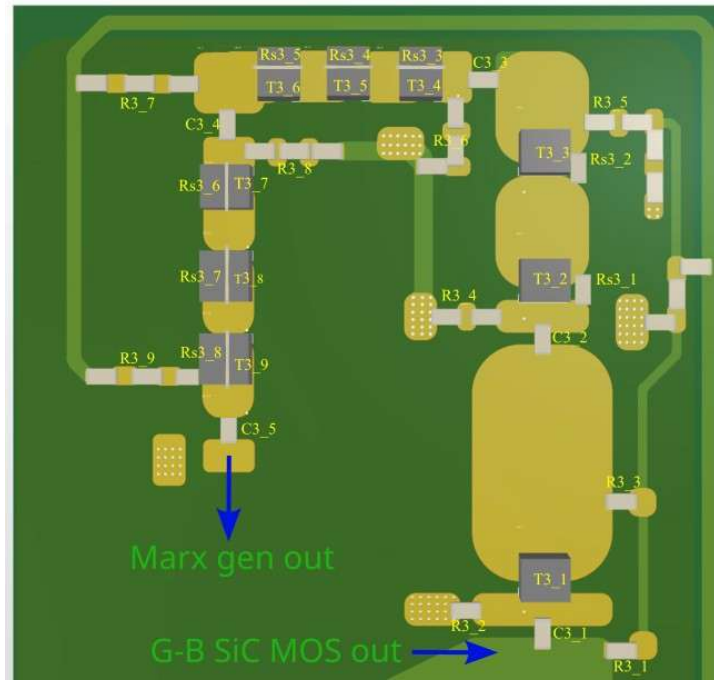


Figure 4.25: PCB 3D cut of the Marx generator setup

1.3 kV, significantly exceeding the typical leakage current of around $1\ \mu\text{A}$. Resistors Rs3_3 to Rs3_8 are depicted in Figure 4.25 as thin white lines above the thyristors because they were added during the experimental phase after the PCB had already been fabricated. Due to the limited remaining copper area around the thyristor footprints, these components were implemented using short leads mounted above the devices.

In the presented design, the most significant source of reflection occurs at the output of the six SiC MOSFET stage, where the incoming signal encounters an untriggered thyristor. In its off-state, the thyristor presents a very high impedance, with only a small parasitic capacitance of approximately 14 pF. This limits the current flow to about 14 A for a voltage slope of 1 kV/ns, effectively making the thyristor appear as an open circuit during the early stages of the pulse (del Barrio Montañés et al. (2025)). As a result, a strong positive reflection is generated, which enhances the amplitude and sharpness of the voltage pulse at the thyristor input—conditions that support triggering in impact ionization mode (as further discussed in Section 4.4).

In summary, the initial, intentional reflection at the open thyristor is exploited only to steepen the incident edge and raise the local field for triggering. Beyond this interface, however, further reflections are undesirable: the pulse must traverse the stack with smooth current flow and without overshoot at the output (del Barrio Montañés et al. (2025)).

4.6.2.1 PCB Implementation and Parameter Optimization

To achieve this smooth propagation, a graded-impedance strategy at the PCB level is implemented (del Barrio Montañés et al. (2025)). Instead of leaving successive stages as abrupt discontinuities, the effective source impedance of each higher-voltage stage was adjusted so that the traveling current front remains continuous. After leveraging the beneficial front-end reflection, the per-stage impedance is progressively increased along the Marx stack (see Table 4.5). This graded transition helps reduce signal reflections at the output and prevents high-voltage overshoots that could otherwise stress or damage the thyristors.

PCB Parameter	Value
Dielectric constant (FR4)	4.5
FR4 thickness (mm)	1.55
Copper thickness (μm)	35

Table 4.4: PCB parameters used in impedance calculations.

	Width (mm)	Length (mm)	$Z_{\text{calculation}}$ (Ω)	Z_{femm} (Ω)	Delay (ps)
1x SiC MOS trace	10	120	21	21	780
6x SiC MOS traces	6×10	120	3.5	4	780
First Marx stage	30	60	7	8	125
Second Marx stage	20	60	14	12	226
Third Marx stage	13	60	24.5	17	345

Table 4.5: Impedance values from LTSpice calculations ($Z_{\text{calculation}}$) and field solutions using FEMM (Z_{femm}) for various PCB traces.

The optimal impedance values for each stage were identified through LTSpice simulations. In the model, all parameters were fixed based on the schematic except for the impedance values of the transmission lines (denoted as Z in Fig. 4.26). These impedances were swept systematically to determine the configuration that minimized reflections and improved current continuity. The time delay (T_d) for each stage, determined by the physical layout, was held constant throughout. Once the ideal impedance values were established, the corresponding trace widths were calculated to match the simulated impedance values.

Table 4.5 summarizes the calculated impedance and propagation delay values for the PCB pads where the thyristors and capacitors are mounted. The impedance values (Z) were estimated using FEMM simulations Meeker (2023), based on the actual geometric dimensions of the pads. These values serve as design approximations, since the simulations do not include the influence of the thyristors and capacitors that physically bridge the pad gaps. The delay values were calculated using the outer stripline propagation method following the approach presented in Bahl and Garg (1977).

The pad widths were adjusted to compensate for variations in the characteristic impedance of the transmission lines, ensuring smooth current continuity across the stages. For the initial stage, consisting of six parallel SiC MOSFETs, the impedance was calculated as $21/6 = 3.5 \Omega$, yielding a current of approximately

371 A at 1.3 kV. In the first Marx stage, the voltage doubles ($1.3 \text{ kV} + 1.3 \text{ kV} = 2.6 \text{ kV}$), requiring a corresponding doubling of the impedance to maintain the same current. This pattern continues in the second Marx stage, where the voltage again doubles to 5.2 kV, and in the third stage, where an additional 3.9 kV brings the total to 9.1 kV. To sustain current continuity at this level, an impedance of 24.5Ω is required. However, in practical measurements, losses such as voltage drops across thyristors and capacitors were observed, leading to output voltages slightly below the theoretical values. To compensate, the actual impedance was set approximately 5% lower than the calculated values at each stage.

Figure 4.25 shows the physical layout of the Marx generator stages, including the placement of capacitors C3_1 to C3_5, which are connected through D2PAK thyristors T3_1 to T3_9, as well as the charging resistors R3_1 to R3_9. The load resistor R3_10 is not depicted in the figure. The interconnecting traces between thyristors are designed with controlled impedance to ensure consistent signal propagation, based on the calculated values listed in Table 4.5.

4.6.3 Simulation-Based Validation and Analysis

To evaluate whether implementing impedance-controlled traces would reduce signal reflections in this design, an LTSpice simulation is performed comparing a non-controlled configuration with one featuring controlled transmission line impedances (Figure 4.26). The simulation assumes ideal closing switches for both the SiC MOSFETs and the thyristors, offering an approximate yet informative representation of the system's behavior. While not intended as an exact replication of the physical circuit, the model provides a valuable preliminary insight to support the design process (del Barrio Montañés et al. (2025)).

The simulation conditions closely reflect the circuit's actual operating environment, allowing us to observe the effects of impedance mismatches and signal reflections when using ideal switching elements. Transmission lines were modeled with both matched and unmatched impedances, using the values listed in Table 4.5, which also includes the calculated delay associated with each stage.

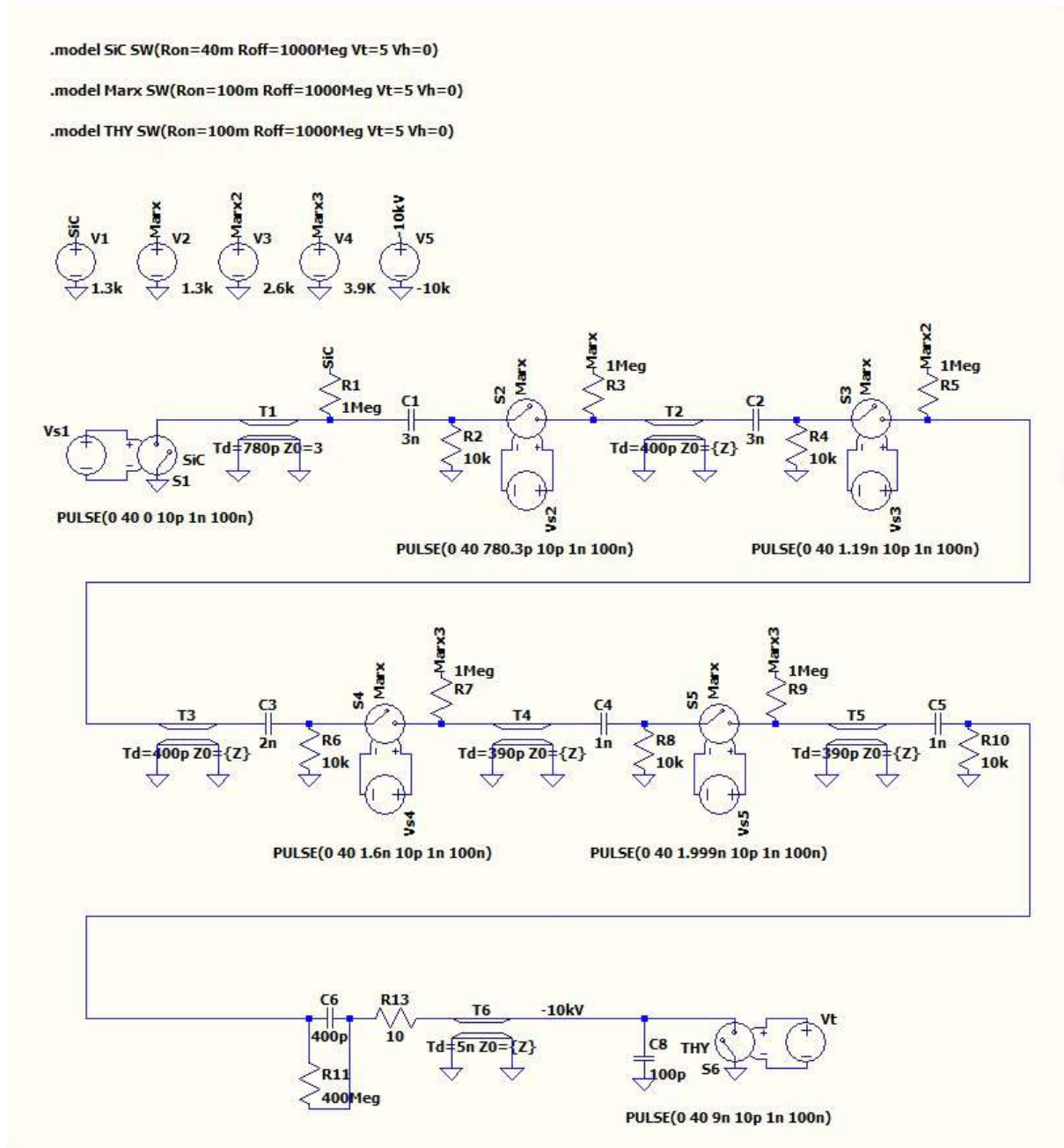


Figure 4.26: Simulation model of the Marx generator, following the schematic on Figure 4.24.

To evaluate the effect of transmission line impedance control on signal reflections, the current through the first switch, S_1 is monitored, representing the six parallel SiC MOSFETs. This point was chosen as a reference to compare two simulation cases: one with controlled impedance values for each stage and another with a uniform impedance of $20\ \Omega$ applied to all stages. The $20\ \Omega$ value reflects the

approximate impedance of the pads used for D2PAK thyristors, which corresponds to the minimum trace width feasible for this package in the PCB layout.

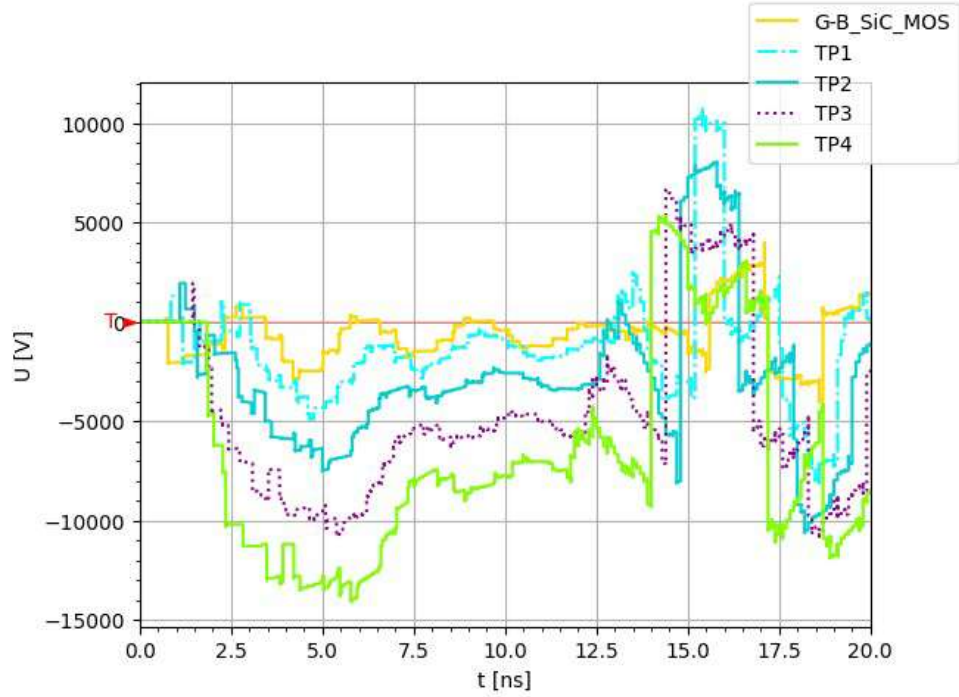


Figure 4.27: Simulated voltage reflections on the different stages (SiC MOSFETs and TP1 to 4) in the fixed ($20\ \Omega$) impedance case.

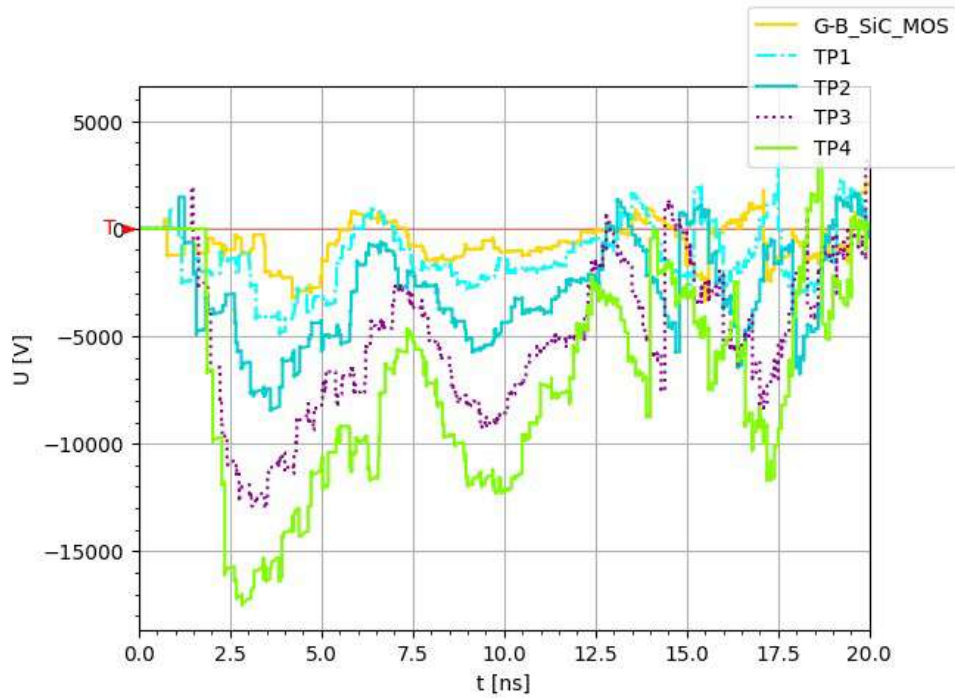


Figure 4.28: Simulated voltage reflections on the different stages (SiC MOSFETs and TP1 to 4) in the controlled impedance case.

The simulation results, shown in Figures 4.27 and 4.28, illustrate the voltage evolution across all stages, including the SiC MOSFETs ($U_{\text{SiC_MOS}}$) and the thyristors (U_{TP1} to U_{TP4}). These plots provide valuable insight into the dynamic behavior of the system. Although the simulation is a simplified representation, it demonstrates the progressive voltage amplification, stage-to-stage delay, and signal reflections with their attenuation over time.

A comparison between the two configurations reveals that the controlled impedance case (Figure 4.28, 17 kV maximal peak to peak amplitude) exhibits smaller voltage reflection amplitudes than the fixed $20\ \Omega$ configuration (Figure 4.27, 24 kV maximal peak to peak amplitude). This is further supported by the current analysis in Figure 4.29, which shows that the uniform $20\ \Omega$ impedance setup results in reflection peaks reaching up to 2 kA, whereas the controlled impedance configuration confines the reflections within the ± 1 kA range. However, a remaining peak at approximately 16 ns is still visible in both cases (del Barrio Montañés et al. (2025)). This corresponds to a reflection caused by the switched thyristor

stack, which lies beyond the impedance grading section and thus is not affected by the controlled impedance approach.

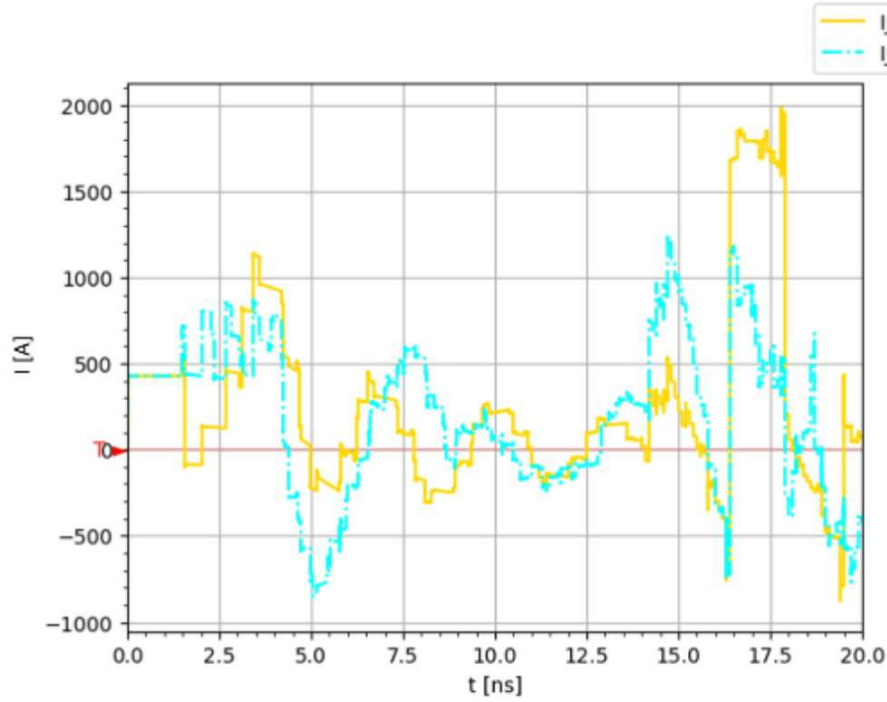


Figure 4.29: Simulated current reflections on the SiC MOSFETs in the fixed ($20\ \Omega$) impedance (continuous, yellow) and controlled impedance (dotted, blue) cases.

4.6.4 Stage-by-Stage Output Characterization

As shown by the measured waveforms in Fig. 4.30, the output signal exhibits the stepwise voltage addition from each Marx stage and a progressive increase in slew rate across the stages (first stage TP1, second TP2, etc.). This behaviour reflects the cumulative action of the cascaded Marx stages, each using a thyristor triggered in impact-ionization mode.

All voltage waveforms in Fig. 4.30 were captured with the PCB capacitive probe and integration method described in Section 3.

The output of the first Marx stage reaches a peak voltage of 4.4 kV with a 3.2 kV/ns slew rate (measured from 10% to 90%) when the thyristor bias voltage

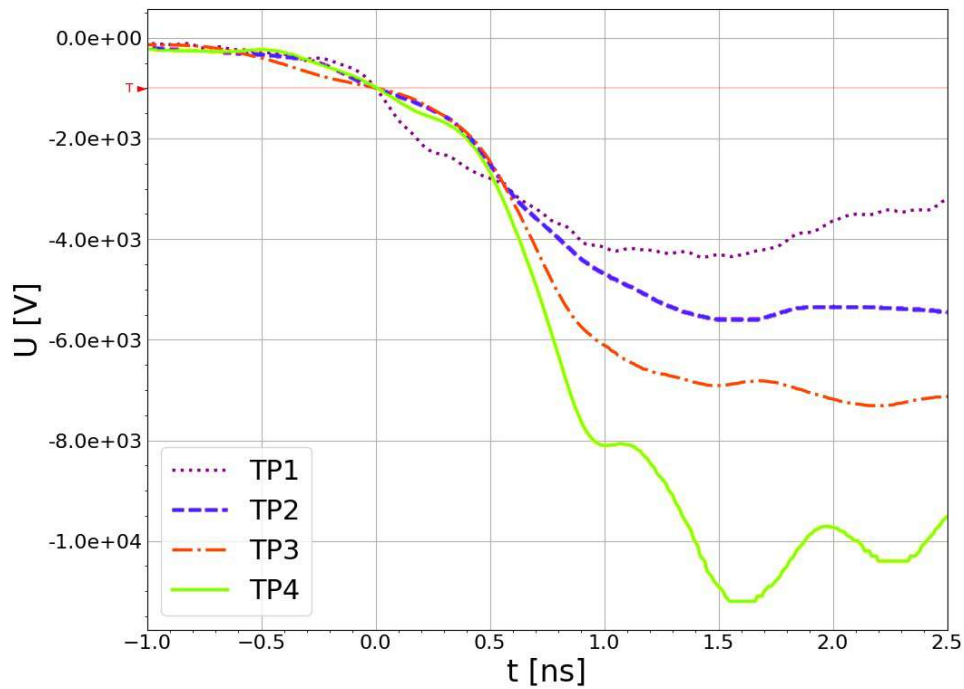


Figure 4.30: Comparison of the output voltage at each of the four Marx generator stages with the capacitive probe on a $50\ \Omega$ load.

is set to 1.3 kV. With each subsequent stage, the falling edge of the signal becomes sharper and the peak voltage increases, culminating in the fourth stage with a maximum amplitude of 11.2 kV and a 13.3 kV/ns slew rate (10% to 90%). A summary of these measurements is provided in Table 4.6 (del Barrio Montañés et al. (2025)).

Table 4.6: Comparison of maximum amplitude, fall time, and 10%–90% slew rate (dU/dt).

Test point	Maximum amplitude (kV)	Fall time (ns)	Slew rate (kV/ns)
TP1	4.4	1.1	3.2
TP2	5.6	0.7	6.6
TP3	7.3	0.7	8.2
TP4	11.2	0.7	13.3

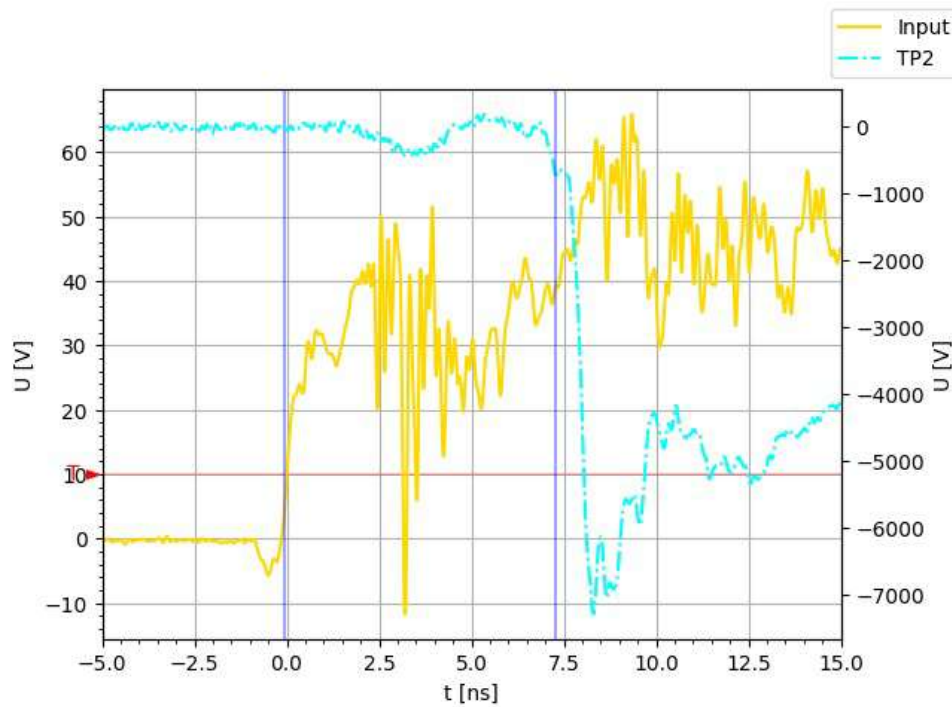


Figure 4.31: Measured delay between the input signal of the system and the second Marx stage output signal (TP2 in in Fig. 4.24).

4.6.4.1 Delay Measurements

While the system is optimized for delivering fast-falling edges, evaluating the delay between the input and output signals is crucial. To measure this propagation delay, one probe was positioned at the input—doubling as the oscilloscope trigger—while a second probe was placed at different test points across the PCB. This setup enabled a stage-by-stage assessment of the delay throughout the system.

Figure 4.31 displays the input signal (Input, Volts) alongside the output signal measured at test point 2 (TP2, Volts), as referenced in Figure 4.24. The vertical blue markers highlight the time interval between the two signals.

Table 4.7: Delay times for each stage of the system (as referred to in Figure 4.24).

Stage test point	Delay from reference (ns)
G–B SiC MOS out	5.4
TP1	6.2
TP2	7.3
TP3	8.3
TP4	9.3

The delay is defined as the time between the input signal reaching 10% of its maximum value and the output signal reaching 10% of its minimum (del Barrio Montañés et al. (2025)). Table 4.7 summarizes the measured delay values across the system. A consistent delay of 1 ns per Marx stage is observed, corresponding to the fixed physical path required to activate each subsequent stage. This measured value contrasts with the estimated 400 ps delay from Table 4.5, which assumes a continuous outer-layer stripline. The longer delay can be attributed to the segmented nature of the layout, where discrete component islands introduce parasitic capacitance and inductance, thereby slowing signal propagation.

5 Summary

5.1 Original Contributions and Advances over the State of the Art

Relative to thyatron plus PFN/PFL systems, the hereby proposed solid-state chain removes pre-ionization and conditioning overheads and avoids the turn-on delay and jitter of plasma switches. The measured trigger-to-edge latency is only a few nanoseconds, compared with the typical $\geq 100\text{--}500\text{ ns}$ preparation of opening-switch architectures. Maintainability and form factor also improve: instead of bulky, oil-cooled, hard-to-source gas devices, the chain is compact, COTS-based (SiC MOSFET stage plus D2PAK-thyristor Marx), straightforward to replicate, and offers deterministic timing for machine protection.

Compared with solid-state IGBT stacks and inductive adders, which excel at kA-class energy delivery and long flat-tops but face magnetic and stage-count limits for sub-10 ns edges and low latency, this work demonstrates 13.3 kV/ns falling edges at its output with sub-nanosecond edge formation and end-to-end latency of less than 10 ns. Target edge speed and amplitude are reached with a short, purely electronic chain rather than many transformer stages subject to core reset and saturation.

Against SiC-MOSFET Marx-only generators, the presented hybrid chain avoids per-stage gate drivers and timing by exploiting a propagating impact-ionization front: a super-boosted SiC stage launches a high- dU/dt , over-voltage edge into a compact thyristor-Marx, the load-side device turns first, and the conduction front then propagates stage-by-stage without dedicated triggers. This removes driver

replication and synchronization overhead while still delivering II-grade conditions at the output (up to 11.2 kV at 13.3 kV/ns). Reflection management is handled with graded-impedance staging: the strong initial reflection at the open thyristor is intentionally used to assist II initiation, after which impedances are tapered between stages to maintain current continuity and suppress ringing.

In contrast to SOS/DSRD and spiral/vector-inversion drivers, which either rely on bespoke opening switches with long pre-charge delays or retain gas gaps that complicate compact integration and scaling, the present chain is fully COTS, mechanically compact, and low-latency while still meeting II thresholds. Amplitude scaling follows stage count and impedance grading rather than rare opening-switch technologies.

At device level, the gate-boosting rule utilized links the series-capacitor value directly to the device's total gate charge at maximum gate bias $Q_g(V_{GS,\max})$, so a bounded, sub-nanosecond charge packet overdrives the gate only as long as needed for ultra-fast turn-on while controlling oxide stress. Sizing is tied transparently to datasheets with a clear rule.

On measurement methodology, a PCB-integrated capacitive probe in-situ calibration and integration captures kilovolt, sub-nanosecond pulses at the relevant test nodes without overstressing the $50\ \Omega$ chain. The probe factor can be discretely tuned (replaceable pad set), and waveforms can be cross-checked against a reference attenuator at the same test point. CST-extracted coupling for the actual geometry is used and documented.

Taken together, and to the best of the author's knowledge within accelerator-oriented literature, this is the first compact, COTS-only chain that combines charge-bounded gate boosting, graded-impedance Marx staging, and measured II-suitable waveforms (approximately 11.2 kV amplitude, 13.3 kV/ns falling edge, and few-nanosecond latency) aimed at industrial thyristors rather than custom fast SCRs, positioning the approach for fast-protection use while remaining reproducible and cost-effective.

5.2 Summary

This thesis develops a methodology for triggering industrial thyristors in high-voltage applications, with emphasis on accelerator use. The approach relies on boosted gate triggering to improve the switching behavior of SiC MOSFETs, increasing both dU/dt and dI/dt beyond conventional techniques and creating the field conditions required for impact-ionization triggering of thyristors. Because the MOSFET stage alone cannot reach the voltage needed for 2.4 kV devices, a compact Marx add-on using D2PAK thyristors is introduced to raise amplitude and sharpen the falling edge. The resulting chain achieves sub-nanosecond switching, output currents of about 400 A, and a falling-edge slew rate above 13 kV/ns at the final Marx output, suitable for II-mode triggering. To the best of the author's knowledge, this is the first demonstration within CERN's Pulsed Power Electronic Section of such a triggering strategy.

Summing up, this work contributes four elements that enable that result: charge-bounded gate boosting for sub-nanosecond edges, expressed as a practical sizing rule for the series coupling capacitor and injected gate charge and verified with measurements showing > 13 kV/ns edges and ~ 400 A pulses from a compact, COTS-based circuit; an ultra-fast trigger chain that minimizes latency from function generator to thyristor–Marx output to only a few nanoseconds—roughly two orders of magnitude shorter than opening-switch schemes—while remaining reproducible and low-cost; a graded-impedance Marx that first leverages the intentional reflection at the initially open thyristor to aid II initiation and then suppresses downstream ringing, with measured stepwise addition to 11.2 kV and 13.3 kV/ns at TP4; and a PCB-integrated high-voltage measurement method using a board-level capacitive probe with on-board bias-tee and in-situ calibration/integration to capture kilovolt, sub-nanosecond pulses without overstressing the $50\ \Omega$ chain. Overall, the design is cost-effective, reproducible, and scalable, and its few-nanosecond trigger-to-edge delay makes it well suited to fast machine-protection tasks such as accelerator beam-dump pre-triggering.

5.3 Outlook

This thesis has demonstrated the feasibility of replacing traditional thyatron-based systems with a compact, fast, and high-voltage pulse generator based on gate boosting and impact ionization principles. The successful triggering of thyristors using ultra-boosted SiC MOSFETs marks a significant step toward the development of reliable solid-state kicker systems.

Future work also includes reliability testing under operational conditions to confirm the suitability of this technology as a replacement for traditional thyatron-based systems. If proven, this approach has the potential to improve the performance, reliability, and maintainability of high-voltage switching systems in accelerator environments.

Looking forward, the next objective is to scale up the thyristor stack to increase output voltage and current, enabling practical deployment in accelerator environments such as CERN. Particular emphasis will be placed on optimizing thermal and electrical performance, ensuring long-term reliability, and simplifying system integration. As part of this effort, lifetime testing of the components under realistic operating conditions will be a key focus to validate their suitability for demanding pulsed power applications.

Further progress also depends on improving simulation tools. Extending existing models to account for impact ionization behavior under ultra-fast and high-voltage conditions will provide valuable insight for refining both the pulse generator and the thyristor stack.

Finally, this work opens the door to broader applications in high-voltage electronics beyond particle accelerators. The techniques and design strategies developed here may be applied to other fast-switching systems where compactness, precision, and robustness are critical. With continued development, this approach has the potential to redefine the standard for solid-state pulsed power systems in scientific and industrial contexts.

A Appendix

A.1 Designing a Thyristor Stack

As previously seen, the enhanced use of the components that we have achieved activates an ultra-fast Marx generator, boasting the capability to generate elevated levels of output voltage and current compared to the previously outlined design in del Barrio Montañés et al. (2023). The imminent application involves the triggering of a high-voltage, 5 cm diameter puck thyristor Multicomp Pro (2020). In order to trigger it, a thyristor stack composed of multiple thyristors connected in series is designed. The goal with this stack is to be able to progressively increase the amount of thyristors in series; and test the boundaries of maximum output voltage and current.

Said thyristor stack has been designed as per the schematic shown in Fig. A.1. The schematic begins with the Marx generator output presented in Section 4.6 (*Marx_gen_out*). Resistors $R4_1$, $R4_2$, $R4_3$, and $R4_4$ form a voltage divider network to balance the voltage across capacitors $C4_1$ and $C4_2$, which block the DC voltage and separate the different voltage levels at the output of the Marx generator and on the thyristor stack. Resistor $R4_5$ limits the current and protects the remaining circuit from surges. Its value is $10\ \Omega$. There is a potential low-pass filter effect formed by this resistor and the capacitance of the thyristor stack: the resistor in combination with the total capacitance (approximately 30 pF for a seven 2.4 kV thyristor stack) will influence the rise time, introducing an RC time constant of about 300 ps. The high-voltage (-HV) biasing voltage connects to resistor $R4_6$, which forms part of a low-pass filter towards the power supply, decoupling the power supply from the load circuit and helping to filter out

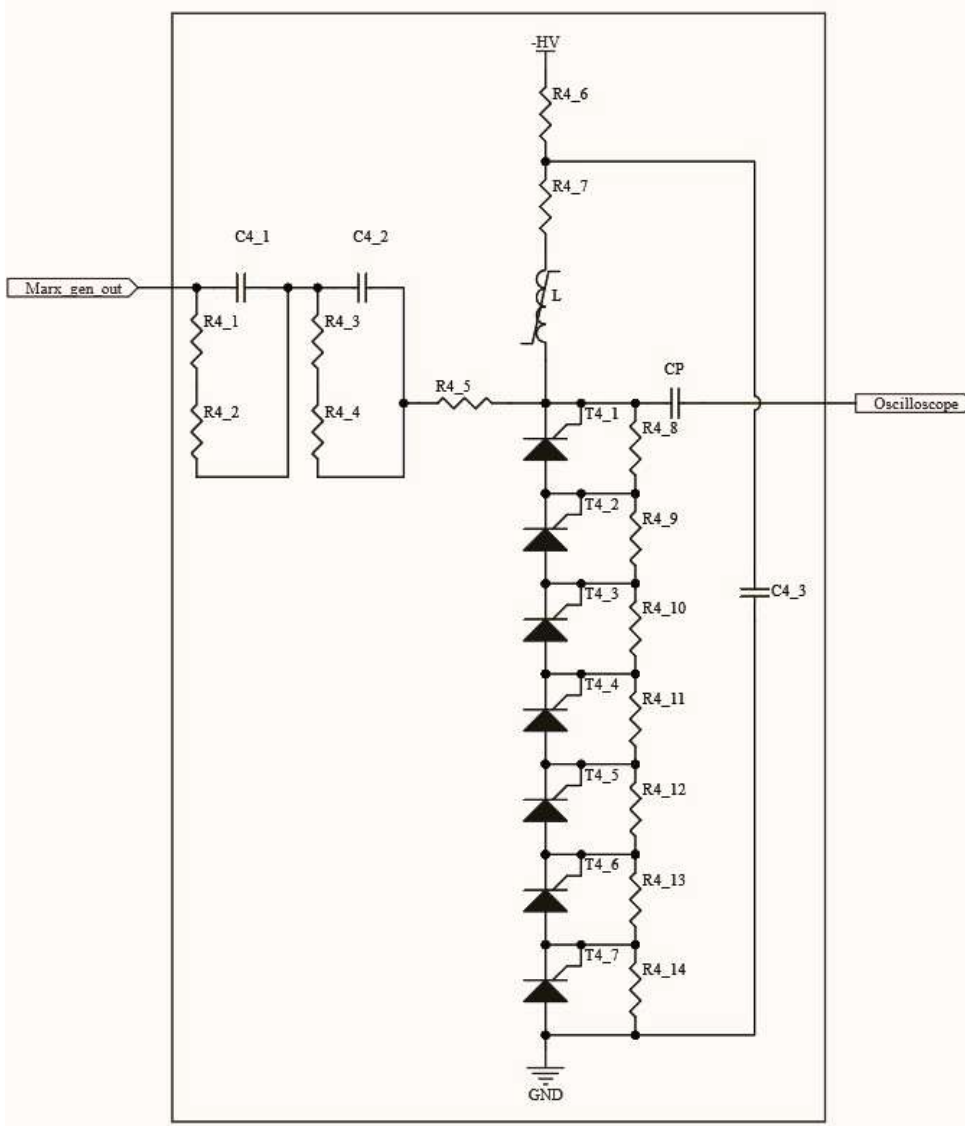


Figure A.1: Schematic of the planned 7-PUCK thyristor stack

transients. The inductor (L , 900 nH) is a saturable inductor serving to decouple the triggering pulse, which has a rise time in the kV/ns range, from the rest of the circuit. This decoupling prevents the fast transients generated during the triggering process from affecting other parts of the setup. The thyristor stack per se consists of thyristors $T4_1$ to $T4_7$. The pulse is delivered to a load resistor ($R4_7$). A capacitive probe (CP) is used to measure the output pulse, providing a non-invasive method to monitor the high-voltage pulses. Capacitor $C4_3$ (total desired capacitance for all parallel capacitors, as seen in blue in Fig. A.2, $\approx 10 \mu\text{F}$, 6.8 kV rated (ZEZ (2025))) functions as the primary energy storage element in the

circuit, designed to discharge through resistor $R4_7$. A ferrite ring, implemented as a saturable inductance (L in A.1), serves to inductively decouple the pulsing elements from the rest of the circuit. The overall design ensures controlled high-current pulses with proper voltage distribution, current limiting, and pulse shaping to protect the thyristors and deliver the desired pulse characteristics to the load.

The corresponding 3D render of the final device is shown in Fig. A.2, with the components labeled as they correspond to the schematic. Non-present are capacitors $C4_1$, $C4_2$ and resistors $R4_1$ to $R4_4$. This inductive decoupling reduces the load on the triggering signal, thereby enhancing its effectiveness during the commutation process. In addition, we include a Rogowski coil (CWTHF 150B/4/1000 Power Electronic Measurements (PEM) (2019)) intended to measure the current pulse through the stack. The thyristors and resistors are compressed in the stack to ensure proper connections, and they are submerged in oil for insulation.

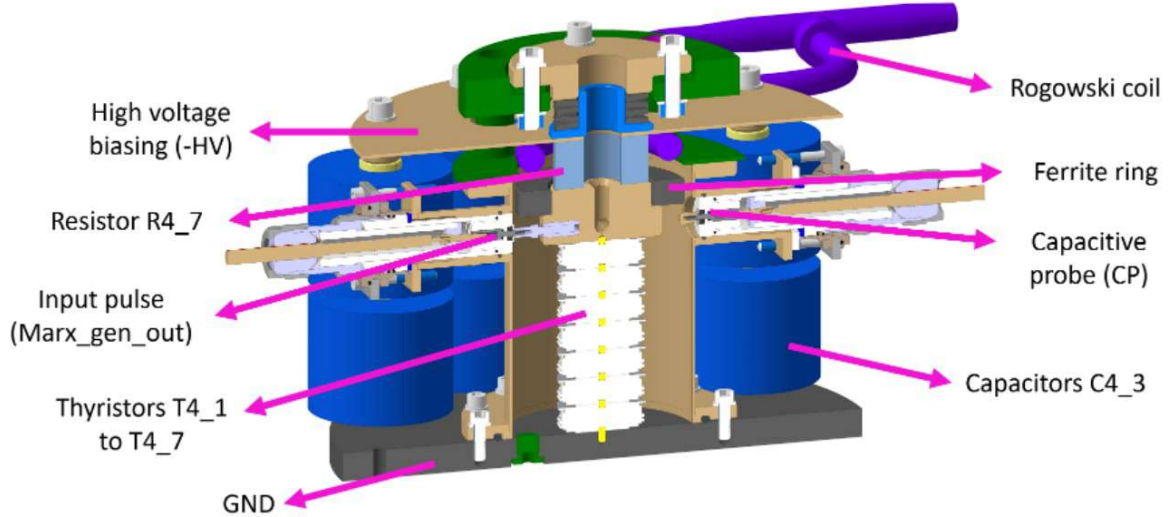


Figure A.2: Preview of the planned 7-PUCK thyristor stack

This final version of the stack accommodates up to seven puck thyristors. The present triggering circuit, however, cannot drive all seven 2.4 kV devices simultaneously because its available transient voltage is insufficient. Based on the

measured driver capability and the II-mode requirement (two thyristors each biased at 1.4 kV require a transient of about 6.8 kV to initiate impact ionization), the Marx setup is expected to trigger two 2.4 kV thyristors in series. This expectation derives from the validated output of the driver stages reported in Chapter 4 and from the II-mode thresholds discussed in Chapter 4.4; it is stated here as a design limit, not as a completed experiment.

To enable progressive testing while staying within present limits, the remaining positions in the stack are populated with metal dummy discs of identical form factor; the number of active thyristors can then be increased as the available triggering voltage is upgraded in future work.

The corresponding multi-device triggering experiment has not been included in this thesis for two practical reasons: (i) the current HV test bench imposes safety and component-rating constraints that limit repetitive operation above 7 kV transients, and (ii) the stack hardware in Fig. A.2 was finalized late in the work.

A.2 Leakage Current Measurements

Table A.1: Reverse-leakage measurements: VS-16TTS12S-M3, VS-25TTS08S, 2N6399.

	VS-16TTS12S-M3 (Vishay (2021))	VS-25TTS08S (Vis (2021))	2N6399 (Lit (2021a))
V_{RRM} (V)	1200	800	800
I_{RMS} (A)	16	25	12
I_{TSM} (A)	200	350	100
U (V)	I_{leak} (μ A)		
200	0.36	1.08	0.29
400	0.45	1.39	0.36
600	0.55	1.78	0.44
700	0.58	1.98	0.47
800	0.64	2.17	0.51
900	0.70	2.44	0.58
1000	0.76	2.77	0.65
1100	0.86	2.98	0.81
1200	0.95	3.23	1.24
1300	1.11	3.62	BD
1400	1.30	3.81	~
1500	1.73	4.59	~
1600	1.70	6.24	~
1700	BD	9.06	~

Note: VS-25TTS08S also showed breakdown at ~ 1.72 kV in a separate run.

Table A.2: Reverse-leakage measurements: BT258-800, BT145-800.127, BT151S-650.

BT258-800 (WeE (2022b)) BT145-800.127 (WeE (2022a)) BT151S-650 (WeE (2023a))			
V_{RRM} (V)	800	800	650
I_{RMS} (A)	8	16	12
I_{TSM} (A)	75	300	120
U (V)	I_{leak} (μA)		
200	0.04	0.04	0.04
400	0.05	0.05	0.06
600	0.07	0.09	0.08
700	0.08	0.11	0.09
800	0.08	0.12	0.11
900	0.09	0.14	0.13
1000	BD@960	BD@920	BD@910

Table A.3: Reverse-leakage measurements: BT152-800, 2N6509G, TYN1225RG.

BT152-800 (WeE (2023b)) 2N6509G (Lit (2021b)) TYN1225RG (STM (2014))			
V_{RRM} (V)	800	800	1200
I_{RMS} (A)	20	25	16
I_{TSM} (A)	200	250	300
U (V)	I_{leak} (μA)		
200	0.08	0.17	0.16
400	0.10	0.24	0.22
600	0.12	0.41	0.27
700	0.13	0.43	0.30
800	0.15	0.48	0.32
900	0.18	0.55	0.35
1000	BD	0.64	0.38
1100	~	0.81	0.45
1200	~	1.13	0.57
1300	~	BD@1320	0.84
1400	~	~	BD@1320
1500	~	~	~

Table A.4: Reverse-leakage measurements: MCR12DSMT4, MCR8DSNT4G, MCR12DCNT4G.

	MCR12DSMT4 (ons (2013))	MCR8DSNT4G (Lit (2023))	MCR12DCNT4G (Lit (2025))
V_{RRM} (V)	600	800	800
I_{RMS} (A)	12	8	12
I_{TSM} (A)	100	90	100
U (V)		I_{leak} (μA)	
200	0.07	0.08	0.11
400	0.08	0.10	0.17
600	0.10	0.12	0.22
700	0.11	0.13	0.27
800	0.12	0.14	0.35
900	0.14	0.16	BD@840
1000	0.18	0.17	~
1100	BD	0.22	~
1200	~	1.15–0.28	~
1300	~	1.17–0.40	~

Table A.5: Reverse-leakage measurements: S8016NARP (two samples) and S8012RTP.

	S8016NARP-A (Lit (2020))	S8016NARP-B (Lit (2020))	S8012RTP (Lit (2022))
V_{RRM} (V)	800	800	800
I_{RMS} (A)	16	16	12
I_{TSM} (A)	188	188	120
U (V)		I_{leak} (μA)	
200	0.31	0.33	0.22
400	0.39	0.38	0.27
600	0.46	0.46	0.33
700	0.50	0.51	0.36
800	0.52	0.55	0.39
900	0.58	0.60	0.43
1000	0.64	0.68	0.48
1100	0.71	0.79	0.54
1200	0.80	0.90	0.64
1300	0.94	1.11	BD@1260
1400	1.18	BD@1320	~
1500	1.76	~	~

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List of Publications

Journal articles

- A A del Barrio Montañés, V Senaj, T Kramer, Y Dutheil, and M Sack. Ultra-fast generator for impact ionization triggering. *Journal of Physics: Conference Series*, 2420(1):012085, jan 2023. doi: 10.1088/1742-6596/2420/1/012085. URL <https://dx.doi.org/10.1088/1742-6596/2420/1/012085>.
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