

Article

A Current Distribution Mechanism Study Between an SiC MOSFET Body Diode and a Paralleled SiC Schottky Barrier Diode During Freewheeling [†]

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[†] This paper is an extended version of our paper published in Zhang, H.; Steiner, F.; Demattio, H.; Blank, T. Temperature-Dependent Degradation of SiC Schottky Diode Inhibition Effect on SiC MOSFET Body Diode Reverse Recovery Current. In Proceedings of the 2024 Energy Conversion Congress & Expo Europe (ECCE Europe), Darmstadt, Germany, 2–6 September 2024.

Abstract

Paralleling an external SiC Schottky barrier diode (SBD) with an SiC MOSFET redistributes the reverse-conduction current and may reduce the reverse-recovery energy. However, the benefit depends on device selection and operating conditions, and an unsuitable SBD can increase the reverse-recovery energy. This paper presents simplified interval-specific models for turn-on, forward conduction, and turn-off and evaluates their qualitative trends using double-pulse tests. For the tested devices and operating conditions, the observed turn-on current distribution is qualitatively consistent with the combined influence of capacitive displacement currents and branch parasitic impedance. The forward-conduction waveforms exhibit case-temperature-dependent RL-type current redistribution. Compared with the configuration without an external SBD, the best-performing SBD group reduces the mean reverse-recovery energy E_{rr} by 19.8–54.5% at $T_c = 25\text{ °C}$ and by 70.0–81.4% at $T_c = 175\text{ °C}$ across four voltage–current operating points. Other SBD selections increase E_{rr} at low case temperature. Reducing the dead time from 3 μs to 500 ns increases the peak magnitude of the total reverse current by 36.8%. These results provide design considerations for the tested devices and operating range.

Keywords: freewheeling diode; SiC MOSFET; Schottky diode; case temperature; reverse recovery; parasitic inductance



Academic Editor: Krzysztof Górecki

Received: 8 August 2026

Revised: 14 September 2026

Accepted: 17 September 2026

Published: 22 September 2026

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1. Introduction

SiC MOSFETs are widely used in hard-switched converters because their fast switching can reduce switching loss. The same fast transitions increase sensitivity to circuit parasitics. In a half-bridge, dead time prevents shoot-through; during this interval, the inductive current flows through the reverse-conduction paths, and the subsequent commutation determines the reverse-current transient. The intrinsic body diode can exhibit temperature-dependent forward conduction and stored-charge recovery [1,2]. An external SiC Schottky barrier diode (SBD) can reduce minority-carrier injection, although its capacitive current remains relevant [3,4].

Improving the third-quadrant characteristic at chip level can affect the first-quadrant design because the intrinsic body diode shares the MOSFET drift and body regions. Integrated Schottky structures have been investigated [5], but an external SiC SBD remains a

practical option for commercial devices. Compared with the MOSFET body diode, an SiC SBD generally has a lower forward-voltage offset and negligible minority-carrier storage. Its measured reverse current is therefore mainly associated with junction capacitance and the applied voltage slew rate [3,4,6].

Connecting an external SiC SBD antiparallel to an SiC MOSFET is a common approach for diverting reverse current away from the intrinsic body diode. Device- and module-level studies have reported reductions in reverse recovery or switching loss when the external SBD carries a sufficient fraction of the freewheeling current [7–10]. Similar benefits have also been investigated at the converter level [11,12].

However, the external SBD does not block the intrinsic body diode, and its benefit is therefore conditional. Previous experiments have shown that the current sharing and switching performance depend on junction temperature, gate bias, operating current, and device configuration [3,6,10,13]. Dead time can further modify the initial diode current and the subsequent reverse recovery transient [14]. These studies mainly compare device configurations or aggregate switching performance, and the resulting comparisons do not directly provide a criterion that can be applied to a new MOSFET–SBD pair using only datasheet and layout data; the coupled current distribution during turn-on, forward conduction, and turn-off remains less explicitly resolved.

Our previous conference paper reported the case-temperature-sweep measurements re-analyzed in Section 5.3.1 [15]; the reuse is limited to those measured waveforms themselves. The interval-specific models, the branch-impedance, gate-bias, and dead-time sweeps, the four-operating-point E_{rr} characterization, and the waveform-processing pipeline are new in the present work. The main contribution is a framework that links measured branch current sharing during turn-on and forward conduction to the subsequent reverse-current transient and E_{rr} . Sections 2 and 3 develop the analytical description, Section 4 presents the DPT setup, Section 5 reports the measurements, and Sections 6 and 7 discuss the design implications and conclusions.

2. The Mechanism of a Diode's Freewheeling Behavior in Inductive Load Circuits

An ideal diode turns on and off synchronously with the complementary transistor and carries the load current during freewheeling. In practice, nonideal behavior occurs in each interval, including the turn-on current overshoot, current redistribution during forward conduction, and reverse recovery during turn-off. This section examines these processes using the double-pulse-test (DPT) circuit.

2.1. Overview of the DPT Circuit and Its Qualitative Waveforms

The freewheeling performance of the SiC MOSFET body diode with an external SiC SBD is characterized using the typical clamped inductive switching circuit shown in Figure 1.

The clamped inductive switching circuit consists of a DC voltage source, a half-bridge circuit, and a load inductor. On the DC side are one power supply V_{dc} and a set of bulk capacitors C_{dc} with equivalent series inductance L_{esl} . The bus bar impedance is represented by L_{stray1} and L_{stray2} . The half-bridge circuit contains two SiC MOSFETs Q_1 and Q_2 , and two SiC SBDs D_1 and D_2 (subscripts 1 and 2 denote the high side and the low side, respectively). The intrinsic body diodes D_{bd1} and D_{bd2} are drawn beside their MOSFET channels. Each SBD branch contains the junction capacitance C_j , the anode-side and cathode-side package inductances L_a and L_c , and the total resistance R_a of the package and the Printed Circuit Board (PCB) branch. Each MOSFET branch contains the gate–source, gate–drain, and drain–source capacitances C_{gs} , C_{gd} , and C_{ds} , the source-side and drain-side package inductances L_s and L_d , and the total resistance R_s of the package and the PCB branch.

and may become negative because of stored-charge recovery and capacitive displacement currents. The branch-current sum $I_{\text{tot}}(t) = I_{Q1}(t) + I_{D1}(t)$ becomes negative during the reverse-current interval, and $I_{Q2} \approx I_{\text{set}} - I_{\text{tot}}$.

2.2. Diode Forward Characteristics

The above analysis treats D_{bd1} and D_1 as a single diode. Their different forward characteristics, however, determine the current distribution between the two branches.

For the steady-state analysis, the forward characteristic of each diode branch is represented by the following piecewise-linear model:

$$I_k = \begin{cases} 0, & V_{\text{com}} < V_{F0,k}, \\ \frac{V_{\text{com}} - V_{F0,k}}{r_{F,k}}, & V_{\text{com}} \geq V_{F0,k}, \end{cases} \quad k \in \{D1, \text{bd1}\}, \quad (1)$$

where I_k is the current in diode branch k , and $r_{F,k}$ is the corresponding forward slope resistance. The parameter $V_{F0,k}$ is an operational low-current voltage offset defined as $V_{F0,k} = \hat{V}_{F,k}(0.01 I_{F,\text{rated},k})$, where $\hat{V}_{F,k}(I)$ is an exponential fit to the typical datasheet forward characteristic. The small reference current is neglected in the piecewise-linear screening model. Therefore, $V_{F0,k}$ is neither a V_F value at rated current nor a mathematical zero-current intercept. Both $V_{F0,k}$ and $r_{F,k}$ depend on junction temperature. For the MOSFET reverse-conduction branch, their effective values may also depend on gate bias when the channel participates in conduction.

As shown in Figure 2a, the forward-voltage offset $V_{F0,\text{bd1}}$ of the D_{bd1} branch is a few volts higher than $V_{F0,D1}$ of the external SBD D_1 . Because the two branches share the common forward voltage V_{com} , their currents are obtained from Equation (1) and added to give the total freewheeling current. As V_{com} increases, the steady-state conduction proceeds from neither branch conducting ($V_{\text{com}} < V_{F0,D1}$), to D_1 alone ($V_{F0,D1} \leq V_{\text{com}} < V_{F0,\text{bd1}}$), to both branches conducting ($V_{\text{com}} \geq V_{F0,\text{bd1}}$).

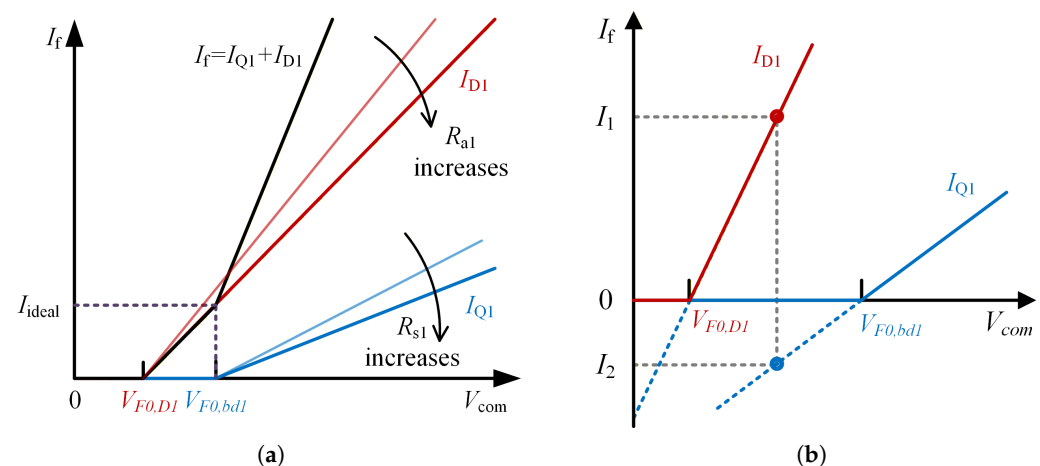


Figure 2. Piecewise-linear forward-characteristic analysis of the paralleled SiC MOSFET body diode and external SiC SBD: (a) individual and combined forward characteristics; (b) graphical construction of the virtual equilibrium associated with the extrapolated negative body diode current.

Within the simplified steady-state model, I_{ideal} is a reference current separating SBD-only conduction from shared conduction. It may be evaluated using measured branch characteristics or estimated from typical datasheet curves. It is therefore used as a screening indicator rather than a universal conduction threshold.

The steady-state screening model does not describe current commutation. During the transient intervals, branch parasitic impedances can produce voltage differences and ringing, so the measured MOSFET branch may conduct temporarily even when $I_{\text{set}} < I_{\text{ideal}}$. The following section therefore examines the interval-specific transient current distribution.

3. Transient-Behavior Models

3.1. Turn-On Transient

This section models the detailed current distribution of the SiC MOSFET and the SiC SBD during the freewheeling period between two pulses. When several diodes parallel together, the current distribution is more complex, because the conductivity of each diode highly depends on its own forward characteristics and the parasitic impedance of its loop. Analytical switching-loss models have also shown that the nonlinear device capacitances, the reverse-recovery effects, and the circuit parasitics must be considered together [16–18]. As Q_2 switches off at the end of the first pulse, the load current commutates to the high-side $D_{\text{bd}1}$ and D_1 . The turn-on process includes the blocking-voltage falling interval from t_1 to t_2 and the forward recovery interval from t_2 to t_3 . Then, the diodes enter the forward conduction. The corresponding qualitative waveforms are shown in Figure 3a, in which the gray curve is the high-side branch-current sum $I_{D1} + I_{Q1}$ and the green curve is the signed forward voltage $V_{\text{df}1}$ of the external SBD D_1 . The body diode forward voltage $V_{\text{sd}1}$ follows the same qualitative shape and is therefore not drawn separately. At t_1 , $V_{\text{df}1}$ starts to rise from its reverse-blocking value $-(V_{\text{dc}} - V_{\text{ds2,on}})$, in which $V_{\text{ds2,on}}$ is the on-state drain-source voltage of Q_2 . t_2 separates the capacitance-dominated stage from the conductive stage. At t_3 , the commutation ends, the branch-current sum reaches I_{set} , and $V_{\text{df}1}$ reaches its forward-recovery peak. At t_4 , $V_{\text{df}1}$ has settled at the steady-state forward voltage V_F of the paralleled branches at I_{set} ; its slow decay from t_3 to t_4 corresponds to the current redistribution transient analyzed in Section 3.2. Accordingly, $t_{\text{rise}} = t_3 - t_1$ denotes the current rise time and $t_{\text{on}} = t_4 - t_3$ the forward-conduction interval.

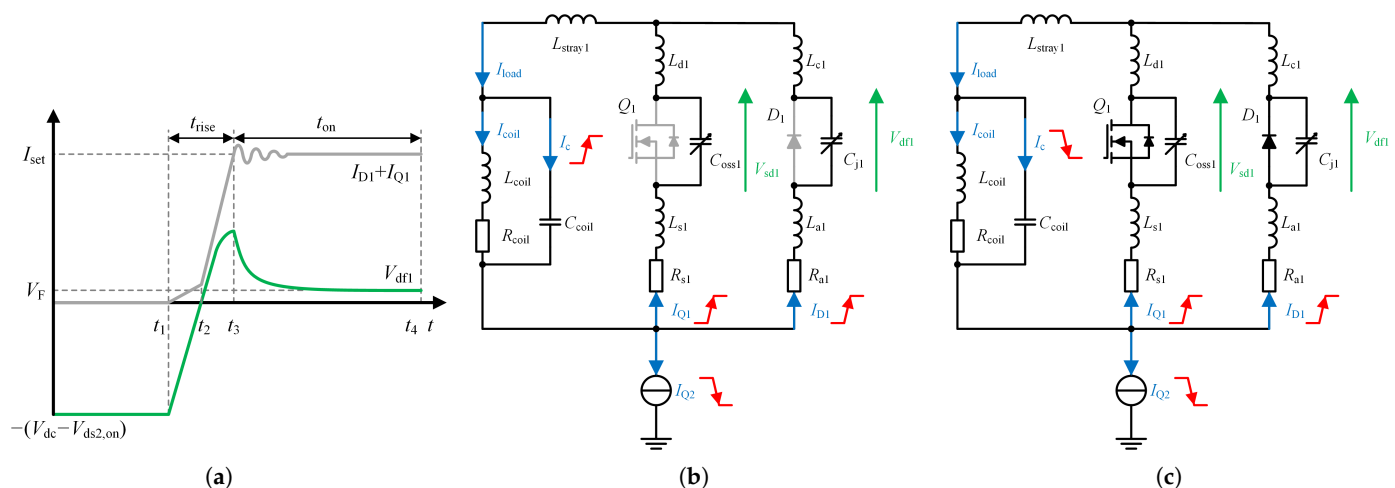


Figure 3. Turn-on transient of the paralleled Q_1 MOSFET branch and the external-SBD branch: (a) schematic waveforms of the high-side branch-current sum $I_{D1} + I_{Q1}$ (gray) and the external-SBD forward voltage $V_{\text{df}1}$ (green), drawn against a common qualitative axis and not to scale; (b) equivalent circuit during the interval from t_1 to t_2 ; (c) equivalent circuit during the interval from t_2 to t_3 . The red arrows indicate the qualitative trends of the branch currents.

In the interval models of this section, circuit components drawn in gray are assumed to conduct no current during the interval and are therefore omitted from the interval equations. In both equivalent circuits, the blue arrows are the branch currents and the green arrows are the branch voltages, with the positive reference directions defined the same as

in Figure 1, while the red symbols beside the branch currents indicate the qualitative trend of each current during the interval. During $t_1 \leq t < t_2$, the two semiconductor branches are capacitance dominated, and the corresponding equivalent circuit is shown in Figure 3b. Here, the Q_1 channel, the body diode D_{bd1} , and the external SBD D_1 are still blocking, and the high-side branch currents are carried by C_{oss1} and C_{j1} . The positive displacement currents are

$$\begin{cases} I_{Q1}(t) = C_{oss1}(V_{sd1}) \frac{dV_{sd1}(t)}{dt}, \\ I_{D1}(t) = C_{j1}(V_{df1}) \frac{dV_{df1}(t)}{dt}. \end{cases} \quad t_1 \leq t < t_2. \quad (2)$$

For ease of analysis, the equivalent output capacitance of the MOSFET branch is modeled as $C_{oss} = C_{ds} + C_{gd}$. Both C_{oss} and C_j are voltage-dependent and are represented by their time-related equivalent values from the datasheets [19–22]; the subscripts are hidden in the following analysis.

In general, the ratio of the two displacement currents in Equation (2) is

$$\frac{I_{D1}}{I_{Q1}} = \frac{C_{j1}}{C_{oss1}} \frac{dV_{df1}/dt}{dV_{sd1}/dt}. \quad (3)$$

Therefore, I_{D1}/I_{Q1} reduces to C_{j1}/C_{oss1} only when the two internal voltage slew rates are approximately equal. In the practical circuit, the branch parasitic inductances, resistances, and the load-coil capacitance also affect the voltage slew rates and the resulting current distribution.

For $t_1 \leq t < t_2$, the branch and load equations are

$$L_{coil} \frac{dI_{coil}}{dt} + L_{stray1} \frac{dI_{load}}{dt} + (L_{d1} + L_{s1}) \frac{dI_{Q1}}{dt} + R_{coil} I_{coil} + R_{s1} I_{Q1} + V_{sd1} = 0, \quad (4a)$$

$$L_{coil} \frac{dI_{coil}}{dt} + L_{stray1} \frac{dI_{load}}{dt} + (L_{c1} + L_{a1}) \frac{dI_{D1}}{dt} + R_{coil} I_{coil} + R_{a1} I_{D1} + V_{df1} = 0, \quad (4b)$$

$$V_c(t) = L_{coil} \frac{dI_{coil}}{dt} + R_{coil} I_{coil}, \quad I_c(t) = C_{coil} \frac{dV_c}{dt}, \quad (4c)$$

$$I_{load} = I_{Q1} + I_{Q2} + I_{D1} = I_{coil} + I_c. \quad (4d)$$

Immediately before commutation,

$$I_{Q1}(t_1) \approx I_{D1}(t_1) \approx I_c(t_1) \approx 0, \quad I_{Q2}(t_1) \approx I_{coil}(t_1) \approx I_{load}(t_1) \approx I_{set}.$$

The initial blocking voltages are retained as $V_{sd1}(t_1) \approx V_{df1}(t_1) \approx -V_{dc}$, while $V_c(t_1)$ is inherited from the first-pulse charging state. Small semiconductor and parasitic voltage drops are neglected in these approximate initial conditions.

Equation (4a) describes the Q_1 package branch, in which C_{oss1} carries the dominant current before the body diode junction becomes forward-biased. Equation (4b) describes the external-SBD branch and its junction capacitance. Equation (4c) is the internal voltage-current relation of the load inductor, and Equation (4d) is the node-current balance during commutation from the Q_2 channel to the two high-side branches.

In Figure 3b,c, the load coil is represented by the same lumped model as in Figure 1, that is, L_{coil} in series with R_{coil} and shunted by C_{coil} . In Equation (4a–d), $L_{coil} dI_{coil}/dt$ together with $R_{coil} I_{coil}$ sets V_c , which further affects the displacement current I_c through C_{coil} . I_{Q2} is the only current source in these equivalent circuits which represents the low-side commutation branch and defines the boundary conditions.

The current growth rate is relatively low during this interval. C_{coil} provides an additional displacement-current path. Because no parameterized simulation or independent capacitance sweep was performed, the contribution of C_{coil} is not quantified separately.

The instant t_2 marks the beginning of the conductive-stage approximation, in which the conductive components of both high-side branch currents dominate their displacement-current components. The small difference between the individual SBD and MOSFET branch conduction-onset instants is neglected in this interval model. The Q_1 channel is assumed to remain off. The equivalent circuit is shown in Figure 3c. The local differential resistances of the MOSFET body diode and SBD paths are denoted by r_{bd1} and r_{SBD1} , respectively. This model applies for $t_2 \leq t \leq t_3$, where t_3 denotes the end of commutation, defined by $I_{Q2}(t_3) = 0$ and $I_{Q1}(t_3) + I_{D1}(t_3) = I_{load}(t_3)$.

The model treats the Q_1 channel as off and therefore represents the conductive part of the MOSFET branch by D_{bd1} . In the measurements, however, I_{Q1} is the terminal current of the complete MOSFET branch and may include reverse-channel, body diode, and displacement-current components; experimental comparisons are therefore made at the branch level. Recent work has shown that C_{gs} and C_{gd} of SiC MOSFETs depend jointly on V_{gs} and V_{ds} and that their relative influence changes across the switching stages [18]. Because $C_{iss} = C_{gs} + C_{gd}$, this joint dependence also affects the dynamic input capacitance. The interval models resolve only the high-side branch-current distribution; the low-side Q_2/D_2 dynamics, including Q_2 gate charging and nonlinear capacitances, enter through the switching-node voltage and current boundary conditions and are not solved separately.

$$L_{coil} \frac{dI_{coil}}{dt} + L_{stray1} \frac{dI_{load}}{dt} + (L_{d1} + L_{s1}) \frac{dI_{Q1}}{dt} + R_{coil} I_{coil} + V_{F0,bd1} + (R_{s1} + r_{bd1}) I_{Q1} = 0, \quad (5a)$$

$$L_{coil} \frac{dI_{coil}}{dt} + L_{stray1} \frac{dI_{load}}{dt} + (L_{c1} + L_{a1}) \frac{dI_{D1}}{dt} + R_{coil} I_{coil} + V_{F0,D1} + (R_{a1} + r_{SBD1}) I_{D1} = 0. \quad (5b)$$

Equation (4c,d) remain unchanged in this interval. All inductor currents and capacitor voltages are continuous at t_2 . Therefore, the terminal states obtained from Equation (4a–d) are used as the initial conditions of Equation (5a,b).

Equation (5a,b) replace the capacitance-dominated branch descriptions in Equation (4a,b) with locally linearized conductive voltage drops. During this interval, $I_{Q1} + I_{D1}$ increases as Q_2 turns off and the current commutates to the high-side branches. The branch parasitic inductances produce voltage overshoot and current ringing. Therefore, the turn-on current distribution depends jointly on C_{coil} , the voltage-dependent device capacitances, and the commutation-loop impedance.

3.2. Forward Conduction

After the current commutation from Q_2 , the load current is redistributed between D_{bd1} and D_1 . The branch inductances and resistances produce an RL-type transient, while the forward characteristics determine the steady-state current sharing. Figure 4 shows this process from t_3 to t_4 .

Figure 4a,b represents two consecutive phases of this interval, with the arrow and color definitions the same as in Figure 3. In the first phase, C_{coil} , C_{oss1} , and C_{j1} still take part in the current redistribution and produce the voltage and current ringing. In the second phase, the ringing has decayed and these capacitive branches no longer take part; they are therefore drawn in gray and are omitted from the interval equations derived below. In Figure 4c,d, the axis I_f is the forward current, the gray curve is the branch-current sum $I_{D1} + I_{Q1}$, and the two blue curves are the individual branch currents I_{D1} and I_{Q1} . The dashed blue segments in the latter extrapolate the RL-type redistribution behavior beyond the instant at which D_{bd1} turns off; they correspond to the virtual equilibrium with a negative extrapolated body diode current constructed in Figure 2b and are not physically realized.

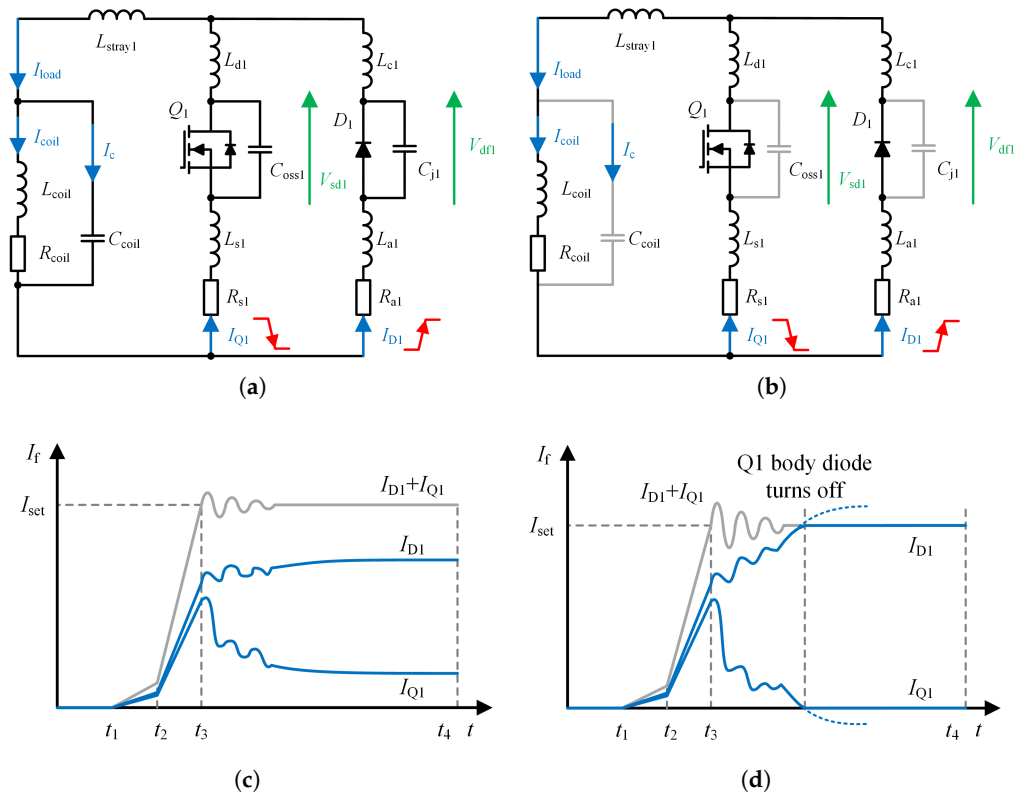


Figure 4. Current redistribution transient of the paralleled Q_1 MOSFET branch and the external-SBD branch from t_3 to t_4 interval: (a) equivalent circuit of the ringing phase that follows the end of commutation at t_3 ; (b) equivalent circuit after the ringing has decayed; (c) schematic current redistribution including the MOSFET branch current leakage when $I_{set} < I_{ideal}$; (d) schematic current redistribution when D_{bd1} eventually turns off. The red arrows indicate the qualitative trends of the branch currents. The dashed blue lines represent extrapolated current trajectories that are not physically realized.

During the t_3 to t_4 interval, Q_2 is off and the load current is shared by the MOSFET reverse-conduction branch and the external SBD branch. As discussed in Section 2, the load current is approximated as I_{set} .

For a compact model, define $L_Q = L_{d1} + L_{s1}$, $L_D = L_{c1} + L_{a1}$, $R_Q = R_{s1} + r_{F,bd1}$, and $R_D = R_{a1} + r_{F,D1}$. The two parallel branches have the same terminal voltage, and their currents sum to I_{set} . The common load-coil terms are shared by both branches and cancel out. Eliminating $I_{D1} = I_{set} - I_{Q1}$ from the branch voltage equality gives

$$(L_Q + L_D) \frac{dI_{Q1}}{dt} + (R_Q + R_D) I_{Q1} = R_D I_{set} + V_{F0,D1} - V_{F0,bd1}. \quad (6)$$

Figure 4 shows the two main effects during this interval. The branch inductances and capacitances cause ringing, while the forward characteristics drive the current redistribution.

The boundary current, steady-state MOSFET branch current, and redistribution time constant are defined as

$$\begin{aligned} I_{ideal} &= \frac{V_{F0,bd1} - V_{F0,D1}}{R_D}, \\ I_{Q1,v} &= \frac{R_D}{R_Q + R_D} (I_{set} - I_{ideal}), \\ \tau_d &= \frac{L_Q + L_D}{R_Q + R_D}. \end{aligned} \quad (7)$$

For the datasheet-based estimate used in this work, R_{a1} is neglected and $R_D \approx r_{F,D1}$; the resulting I_{ideal} is therefore an approximate, datasheet-based reference.

The unconstrained current predicted by the linear model is

$$\begin{aligned}\tilde{I}_{Q1}(t) &= I_{Q1,v} + [I_{Q1}(t_3) - I_{Q1,v}]e^{-(t-t_3)/\tau_d}, \\ I_{Q1}(t) &= \max[0, \tilde{I}_{Q1}(t)], \\ I_{D1}(t) &= I_{\text{set}} - I_{Q1}(t).\end{aligned}\quad (8)$$

Here, $I_{Q1}(t_3)$ is the initial MOSFET branch current at the end of the turn-on commutation.

When $I_{\text{set}} > I_{\text{ideal}}$, $I_{Q1,v} > 0$, and both branches conduct in the steady state. When $I_{\text{set}} = I_{\text{ideal}}$, $I_{Q1,v} = 0$. When $I_{\text{set}} < I_{\text{ideal}}$, $I_{Q1,v} < 0$, and the unconstrained current reaches zero during the redistribution; this virtual-equilibrium construction is illustrated graphically in Figure 2b. The actual MOSFET branch current is then clamped at zero, and the external SBD carries the complete load current. The small forward leakage current is neglected.

Depending on the device parameters and operating conditions, both branches may continue to conduct during part of the t_3 – t_4 interval. One representative case is shown in Figure 4d.

By the equations above, several factors affect the forward conduction current distribution. The major factors include:

- junction temperature T_j , which changes the forward characteristic of $D_{\text{bd}1}$ and D_1 ;
- the branch parasitic inductances $L_{s1} + L_{d1}$ and $L_{a1} + L_{c1}$;
- the gate-driver off-state voltage V_{EE} , which changes the effective forward characteristic of the MOSFET reverse-conduction branch.

3.3. Turn-Off and Reverse Recovery Transient

The turn-off and reverse-recovery waveform of a power diode during the DPT is shown in Figure 5. It contains three intervals from t_5 to t_8 . The interval definitions used in this section follow JEDEC JESD88E [23].

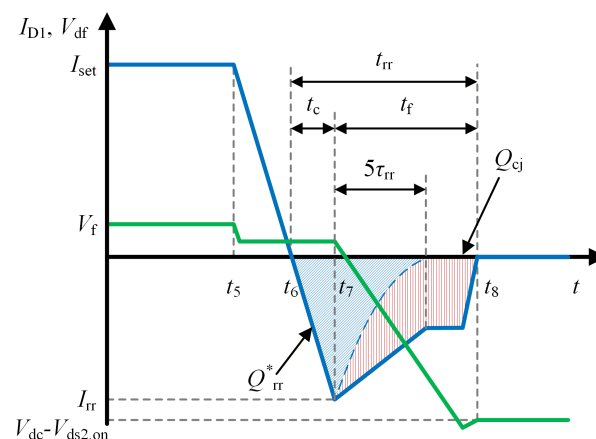


Figure 5. The definition of the reverse recovery performance of an arbitrary power diode. The shaded areas schematically distinguish the stored-carrier component Q_{rr}^* and the junction capacitance Q_{cj} . For an SiC SBD, $Q_{\text{rr}}^* \approx 0$ and the measured negative current is dominated by junction-capacitance charge Q_{cj} .

Before t_5 , the diode conducts the freewheeling current. At t_5 , Q_2 begins to turn on and commutates the load current from the diode. The diode current reaches zero at t_6 , and the reverse current reaches its peak magnitude I_{rr} at t_7 . From t_6 to t_7 , the reverse current of a bipolar diode is dominated by the extraction of stored carriers. After t_7 , the fast change of V_{df} towards the reverse-blocking value produces a capacitive displacement current, which

overlaps with the decaying carrier-related current. At t_8 , the diode completes its transition to the reverse-blocking state. In practice, t_8 is defined using a specified current threshold rather than by assuming that every internal charge component has become exactly zero. Therefore, the reverse charge illustrated in Figure 5 can be decomposed into the stored-carrier component Q_{rr}^* and the junction-capacitance component Q_{cj} . These components may overlap in time, and the shaded regions should be interpreted as a model-oriented decomposition rather than as two strictly separable physical intervals.

This distinction is particularly important when comparing the body diode D_{bd1} with the SiC SBD D_1 . Both stored-carrier and capacitive components may contribute to the reverse recovery of D_{bd1} . In contrast, D_1 is a majority-carrier device, and its negative transient current is predominantly associated with the charging of its junction capacitance.

Consequently, a measured negative current peak should not be interpreted solely as stored-carrier recovery. A capacitive displacement current can remain even when minority-carrier storage in a JBS or SBD is negligible [4]. Recovery charge and output-charge components may also affect switching energy differently [24].

For completeness, the charge-control formulation of Lauritzen and Ma is retained to show the origin of the two-component interpretation [25,26]:

$$\begin{cases} I_D(t) = \frac{q_E - q_M}{T_M}, \\ 0 = \frac{dq_M}{dt} + \frac{q_M}{\tau} - \frac{q_E - q_M}{T_M}, \\ q_E = I_s \tau \left[\exp\left(\frac{V_{df}}{nV_T}\right) - 1 \right]. \end{cases} \quad (9)$$

Here, q_E and q_M are the junction and stored-charge variables, T_M is the diffusion transit time, τ is the carrier lifetime, I_s is the saturation current, and n is the emission coefficient. $V_T = kT_j/q$ is the thermal voltage, where k is the Boltzmann constant, T_j is the absolute junction temperature, and q is the elementary charge. The recovery decay constant satisfies

$$\frac{1}{\tau_{rr}} = \frac{1}{\tau} + \frac{1}{T_M}. \quad (10)$$

For the signed current convention used in this paper,

$$Q_{rr} = \left| \int_{t_6}^{t_8} I_D(t) dt \right| = Q_{rr}^* + Q_{cj}. \quad (11)$$

The present work does not identify the internal parameters or experimentally separate Q_{rr}^* from Q_{cj} . Therefore, these equations are used only to interpret the overlap of stored-charge and capacitive current components.

Because SBDs do not rely on minority-carrier injection, their Q_{rr}^* is approximately zero, and their negative transient current is mainly capacitive.

When considering the parallel of D_{bd1} and D_1 , the total turn-off and reverse recovery current differs from a linear addition of their own reverse recovery current due to V_{df1} clamping the D_{bd1} . This clamping phenomenon is illustrated in Figure 6.

Figure 6 illustrates two limiting timing cases. In case 1, the body diode stored-carrier component decays before the combined capacitive current reaches its peak, so the total peak is mainly associated with the overlapping displacement currents. In case 2, the stored-carrier and capacitive components overlap and may increase the total reverse-current magnitude. The experiment measures only the complete Q_1 and D_1 branch currents; therefore, these internal components and their timing are qualitative interpretations rather than separately extracted quantities.

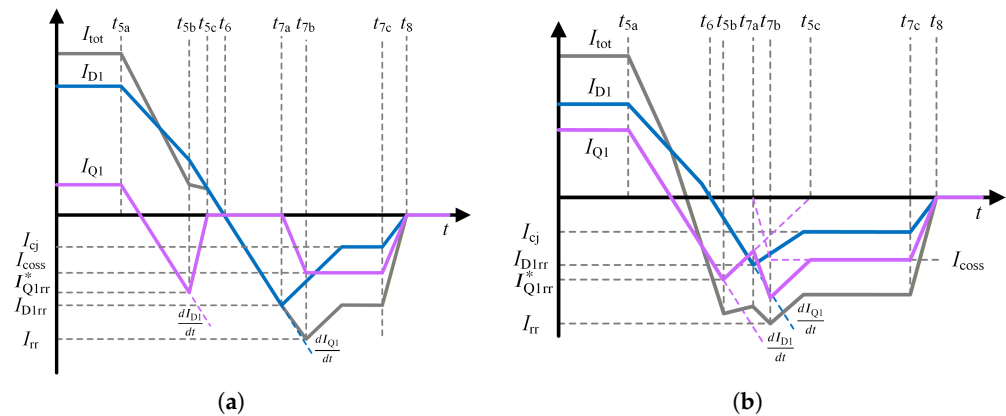


Figure 6. Qualitative reverse-current processes of D_1 and D_{bd1} : (a) case 1, where the body diode stored-carrier component decays before the capacitive-current peak; (b) case 2, where the stored-carrier and capacitive components overlap. Here, I_{Q1rr}^* denotes the schematic body diode stored-carrier component within the Q_1 branch. Blue: D_1 branch current; purple: Q_1 branch current; gray: high-side branch-current sum. The internal components are schematic and were not measured separately. The colored dashed lines indicate slope extrapolations and, in panel (b), the schematic decomposition of the MOSFET-branch reverse current into stored-carrier and capacitive components.

Based on the two-component interpretation and the qualitative analysis above, factors that can increase the measured reverse-current magnitude include:

- a larger MOSFET branch forward current at t_{5a} , which can increase the stored-carrier contribution;
- a higher voltage or current slew rate, which can increase the overlapping displacement currents through C_{oss1} and C_{j1} .

4. Experimental Setup

This section introduces the experimental setup and the device under test for the above-mentioned DPT.

4.1. DPT Setup

The DPT platform and devices under test are shown in Figure 7. Unless otherwise stated, the gate voltage of Q_1 was clamped at -4 V, and the gate-driver voltage of Q_2 was $+18/-4$ V. The gate resistances were $R_{g1} = R_{g2} = 10 \Omega$. Two PMK BumbleBee active differential voltage probes (± 2000 V, 400 MHz; PMK Mess- und Kommunikationstechnik GmbH, Bad Soden am Taunus, Germany) measured V_{sd1} and V_{df1} . Two PEM CWTUM/1/R Rogowski current probes (30 MHz; Power Electronic Measurements Ltd., Long Eaton, UK) measured I_{Q1} and I_{D1} . Waveforms were recorded using a 12-bit LeCroy HRO 66ZI oscilloscope (Teledyne LeCroy, Chestnut Ridge, NY, USA) at 2 GS/s, with 99,997 sample points per switching event, corresponding to a 0.5 ns sampling interval and an acquisition window of about 50 μ s. Before each measurement series, the probes were self-calibrated and zero-offset corrected with the manufacturer-provided functions. Channel deskew was performed by replacing the inductive load with a low-inductance resistor and adjusting the relative channel delays until the measured voltage and current rising edges coincided. The oscilloscope's default interpolation method was retained for waveform display, and no additional post-acquisition time alignment was performed. The gate-drive control and oscilloscope acquisition were synchronized using a common external trigger. The voltage and current channels used vertical scales of 100 V/div and 10 A/div, respectively.

The case temperature was controlled using a liquid-cooling system and Peltier elements attached to the heat sink. Five PT1000 sensors were distributed over the heat sink

and the external surfaces of the semiconductor packages. Before waveform acquisition, the temperature was considered stable only when all five sensor readings stayed within $\pm 1^\circ\text{C}$ of the target case temperature for at least 45 s, and the difference among the monitored packages stayed within the same window for the same duration. Because the PT1000 sensors were attached externally, the reported T_c denotes the stabilized package-surface case temperature before each DPT pulse and is not a direct junction-temperature measurement. An order-of-magnitude bound supports this usage: the energy deposited in the high-side devices per DPT event (freewheeling conduction plus reverse recovery) is on the order of 1 mJ or less, which, combined with the datasheet single-pulse transient thermal impedances at the microsecond scale [19–22], implies a per-event junction-temperature transition on the order of 1 K. With 200 ms between events, no accumulation is expected, so the case-temperature trends in Section 5, whose setpoints are separated by 25 K or more, are not affected by self-heating at the reported resolution.

To reduce the influence of the parasitic inductances $L_s + L_d$ and $L_c + L_a$, a symmetric hardware layout was used to balance the two branches. The branch impedances were characterized using a Bode 100 vector network analyzer before the DPT measurements, following the resonant-frequency-based method in the authors' previous work [27]. The extracted series inductance of each high-side branch was approximately 18 nH.

Each board carried three symmetrically arranged half-bridges, that is, the six device positions visible in Figure 7a. The middle half-bridge held the C3M0016120K devices used as Q_1 and Q_2 . In groups B, C, and D, the left half-bridge held the two SBDs used as D_1 and D_2 , and the two midpoints were joined by a copper bar with a central threaded hole so that the paralleled branches remained as symmetric as the layout allowed. The right half-bridge was a bypassed spare. It was populated with the same SBD type in groups B, C, and D and left unpopulated in group A. Its midpoint was left floating and it was not connected into the freewheeling loop. No SBD failure or measurable degradation occurred during the DPT, so the spare half-bridge was never used. The equivalent parallel capacitance of the load coil was also measured using the Bode 100 (OMICRON electronics GmbH, Klaus, Austria) and was approximately 130.5 pF at 1 MHz. The load inductor had a manufacturer-rated inductance of 90 μH . The first-pulse width was initially estimated from V_{dc} and the rated inductance and then adjusted in preliminary tests so that the measured steady freewheeling current differed from I_{set} by less than 3 A. Successive DPT events were separated by 200 ms.

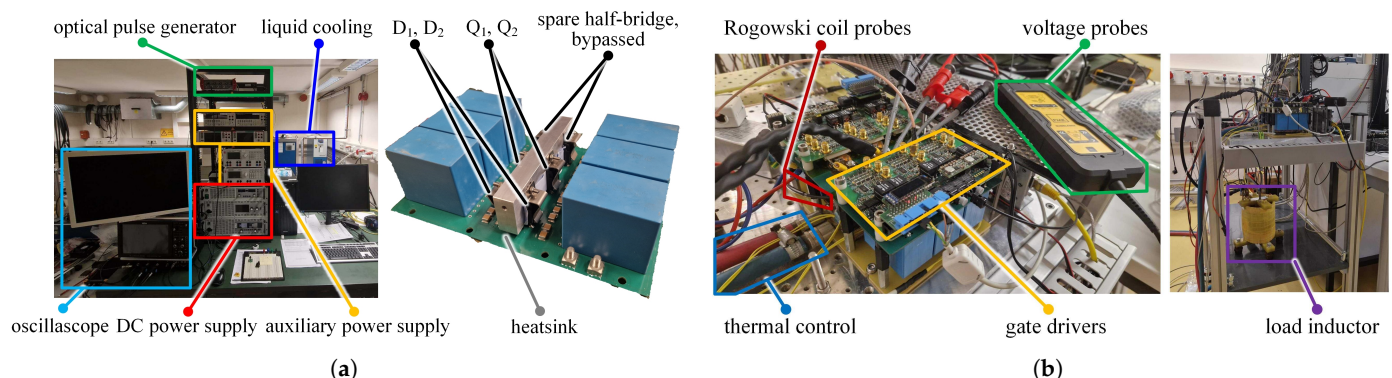


Figure 7. Experimental setup for the DPT: (a) instrument rack and the populated power board, with Q_1 and Q_2 on the middle half-bridge, D_1 and D_2 on the left half-bridge, and the spare half-bridge on the right; (b) assembled DPT platform with the load inductor.

The complete experimental matrix comprised four device groups, two DC-link voltages, two load-current levels, and nine case-temperature setpoints. The reverse recovery energy characterization was performed for groups A, B, C, and D at $V_{dc} \in \{400, 800\}$ V, $I_{set} \in \{25, 50\}$ A, and $T_c \in \{-30, 0, 25, 50, 75, 100, 125, 150, 175\}^\circ\text{C}$. The detailed turn-on,

forward-conduction, and reverse recovery waveform comparisons were performed at $V_{dc} = 800$ V and $I_{set} = 50$ A. The SBD-type and added-branch-inductance comparisons were performed at $T_c = 25$ °C for the applicable device groups. The case-temperature sweeps were performed for all four groups. The gate-driver off-state-voltage sweep was performed for group D over $V_{EE} = -2.0$ to -5.0 V, and the dead-time sweep was performed for group B at 350 ns, 500 ns, 1 μ s, 2 μ s, and 3 μ s. Unless otherwise stated, the nontemperature sweeps were performed at $T_c = 25$ °C.

Waveform Processing and Metric Extraction

Each operating point was measured in five consecutive DPT shots using the same devices and hardware assembly. The repeated measurements characterize shot-to-shot repeatability and suppress the influence of an individual anomalous switching event. The reported population standard deviations of I_{rr} and E_{rr} quantify only this five-shot dispersion; they do not include device-to-device variation or systematic probe uncertainty. Other retained summaries are identified as five-shot means or representative-waveform point estimates.

The same five-shot records were used to estimate the circuit-level voltage-transition time from the signed high-side MOSFET-branch voltage V_{sd1} . Under the dc-link constraint, this waveform provides an indirect indication of the half-bridge voltage transition associated with Q_2 switching while also including the voltage contributions of the branch parasitic inductances. For each turn-on and turn-off event, the transition time was measured between 10% and 90% of the corresponding rising or falling edge of the waveform.

Because V_{GS2} , V_{DS2} , and I_{Q2} were not acquired, this value is a phase-leg commutation metric rather than a direct measurement of the intrinsic switching time of Q_2 .

For the dead-time analysis, the electrical signal synchronized with the second optical gate pulse set the start of the search window. For each branch $k \in \{Q1, D1\}$, its value at the synchronized trigger instant, $I_{k,trig} = I_k(t_{trig})$, was used as the reference. This definition does not assume that the two-branch current redistribution has reached steady state before the second pulse. The onset of the branch-current decrease was the first post-trigger sample satisfying

$$t_{5a,k} = \min \{ t > t_{trig} : I_k(t) \leq I_{k,trig} - 1 \text{ A} \}. \quad (12)$$

The reported $I_{Q1}(t_{5a})$ uses the onset detected from the I_{Q1} trace, i.e., $t_{5a,Q1}$. All current metrics were extracted after applying the probe deskew described above.

For the reverse-recovery-energy calculation, the offsets of the four measured channels were removed using the median values in the first 5 μ s quiescent window W_0 . No switching event occurred in this window in any of the 720 records. Branch currents are positive during forward conduction, whereas V_{D1}^R and V_{Q1}^R are positive in the reverse-blocking direction. The total measured current is $I_{tot} = I_{D1} + I_{Q1}$. The integration starts at its downward zero crossing t_a . The subsequent minimum of I_{tot} defines the peak time t_p and $I_{rr} = -I_{tot}(t_p) > 0$. The end point t_b is the first post-peak crossing of $-0.1I_{rr}$ that remains above this level for at least 10 ns. Over the resulting window, the signed minima and positive total reverse-current magnitude are

$$\begin{aligned} I_{Q1,min} &= \min_{t \in [t_a, t_b]} I_{Q1}(t), \\ I_{tot,min} &= \min_{t \in [t_a, t_b]} I_{tot}(t), \\ I_{rr} &= -I_{tot,min} > 0. \end{aligned} \quad (13)$$

Thus, $I_{\text{tot}}(t_p) = I_{\text{tot,min}}$. The reverse-recovery energy is

$$E_{\text{rr}} = - \int_{t_a}^{t_b} [V_{\text{D1}}^{\text{R}}(t) I_{\text{D1}}(t) + V_{\text{Q1}}^{\text{R}}(t) I_{\text{Q1}}(t)] dt. \quad (14)$$

The unfiltered samples were integrated using the trapezoidal rule. Residual timing sensitivity was evaluated by shifting both voltage traces relative to the current traces by ± 1 and ± 2 ns while keeping the integration window unchanged. Figure 8 illustrates the calculation using one representative waveform.

The probe bandwidth sets an additional systematic bound. The reverse-recovery window of the representative event in Figure 8 is shorter than approximately 90 ns, so the dominant spectral content of the current lobes lies near 5–15 MHz. The approximately first-order 30 MHz response of the Rogowski probes attenuates this content by roughly 2–12%; the peak magnitude I_{rr} may therefore be underestimated by up to about 10%. Charge-type integrals are largely preserved by the unity low-frequency gain of the probe response, and the error in E_{rr} is bounded by the peak-amplitude error. The 400 MHz voltage channels add negligible attenuation. Because all compared configurations were measured with the same probes, the relative comparisons are affected far less than the absolute values.

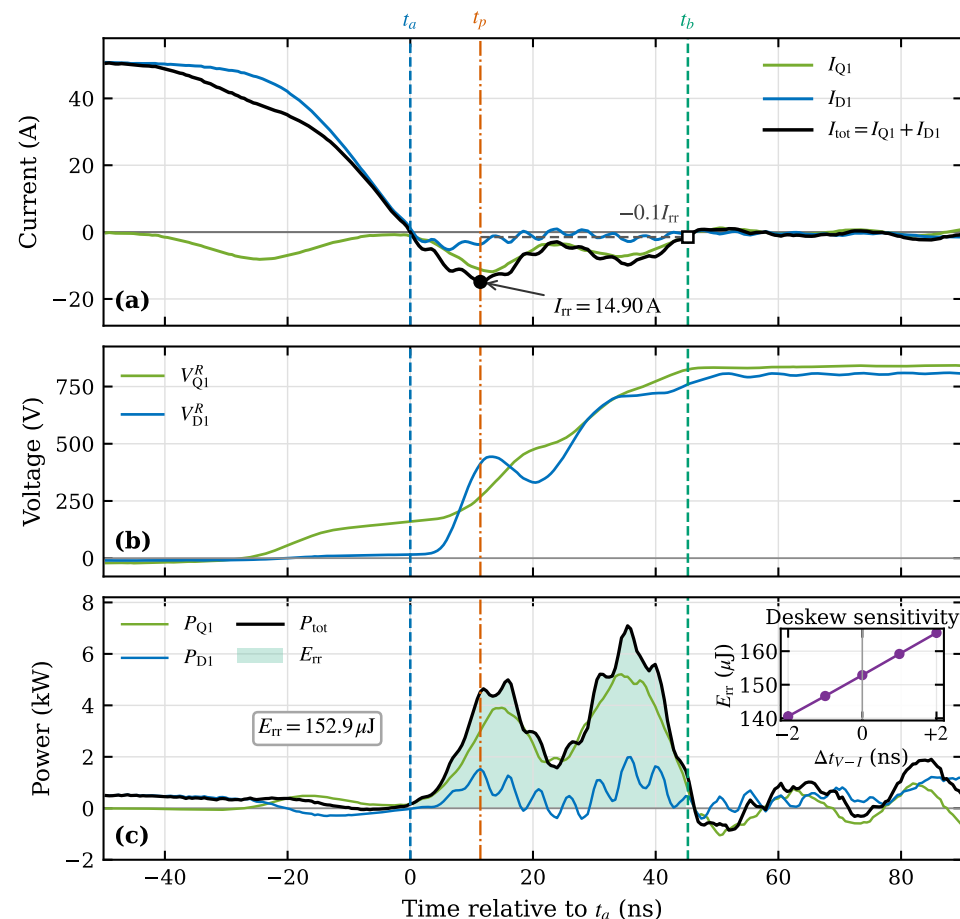


Figure 8. Representative reverse-recovery-energy calculation for group B at $V_{\text{dc}} = 800$ V, $I_{\text{set}} = 50$ A, $T_c = 25$ °C, and repetition 1. (a) Branch currents and their sum, with t_a , t_p , t_b , and I_{rr} marked. (b) Measured branch reverse-blocking voltages. (c) Branch and total powers; the shaded area from t_a to t_b represents E_{rr} . The inset shows the sensitivity of E_{rr} when both voltage traces are shifted together relative to the current traces.

4.2. Device Under Test

The device under test consists of one type of SiC MOSFET and three types of SiC SBD as in Table 1. The tabulated V_{F0} and r_F values were derived by the authors from the typical forward-characteristic curves in Figure 9. The V_{F0} values at 175 °C were obtained by applying the fitted temperature shift to the 25 °C values. The r_F values were evaluated over 1–35 A for the MOSFET reverse-conduction branch and over 15–45 A, or up to the end of the digitized range, for the SBDs. These ranges cover the branch currents at $I_{set} = 50$ A. The sensitivity to the linearization window is discussed in Section 6.1.

Table 1. Selected parameters of the 1.2 kV SiC MOSFET and SiC SBDs from the manufacturers' datasheets [19–22].

Part Number	Device Path	Forward Conduction				Recovery and Capacitance		
		V_{F0} (V)	r_F (m Ω)	V_{F0} (V)	r_F (m Ω)	Rated I_F (A)	Q_{rr} , Q_{cj} (nC)	C_{oss} , C_j (pF)
C3M0016120K	MOSFET body diode, TO-247-4	2.65 ^a	52.8 ^a	2.54 ^{a'}	39.2 ^{a'}	112 ^e	1238 ⁱ	230 ^m
IDWD15G120C5	SBD, TO-247-2	0.90 ^b	26.1 ^b	0.67 ^{b'}	55.6 ^{b'}	23 ^f	82 ^j	59 ⁿ
SCS220KG	SBD, TO-220	0.99 ^c	21.2 ^c	0.77 ^{c'}	54.3 ^{c'}	20 ^g	65 ^k	85 ⁿ
C4D20120A	SBD, TO-220	0.90 ^d	31.9 ^d	0.69 ^{d'}	74.8 ^{d'}	26 ^h	99 ^l	67 ^o

Unless otherwise specified, the datasheet values correspond to 25 °C. The manufacturers' original temperature symbols (T_j , T_{vj} , or T_c) are retained in the footnotes. The definitions of V_{F0} and r_F are given with Equation (1). In the last two columns, the MOSFET row gives Q_{rr} and C_{oss} , whereas the SBD rows give Q_{cj} and C_j . ^a $T_j = 25$ °C, $V_{GS} = -4$ V, $t_p < 200$ μ s; ^b $T_{vj} = 25$ °C, $t_p = 10$ μ s; ^c $T_{vj} = 25$ °C; ^d $T_j = 25$ °C; ^{a'} $T_j = 175$ °C, $V_{GS} = -4$ V, $t_p < 200$ μ s; ^{b'} $T_{vj} = 175$ °C, $t_p = 10$ μ s; ^{c'} $T_{vj} = 175$ °C; ^{d'} $T_j = 175$ °C; ^e $V_{GS} = -4$ V; ^f $T_c = 135$ °C, $D = 1$; ^g $T_c = 133$ °C, $D = 1$; ^h $T_j = 135$ °C, $D = 1$; ⁱ $T_j = 175$ °C, $V_{GS} = -4$ V, $I_{SD} = 75$ A, $V_R = 800$ V, $dI_{SD}/dt = 4$ kA/ μ s; ^j $T_{vj} = 25$ °C & 150 °C, $V_R = 800$ V; ^k $T_{vj} = 25$ °C, $V_R = 800$ V, $dI_{SD}/dt = 0.5$ kA/ μ s; ^l $T_j = 25$ °C, $V_R = 800$ V; ^m $V_{GS} = 0$ V, $V_{AC} = 25$ mV, $V_{DS} = 1000$ V, and $f = 1$ MHz; ⁿ $T_{vj} = 25$ °C, $V_R = 800$ V, and $f = 1$ MHz; ^o $V_R = 800$ V, and $f = 1$ MHz.

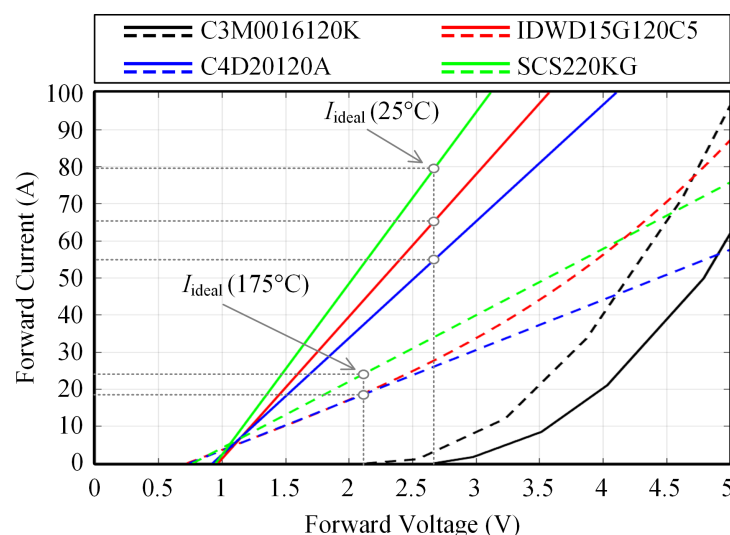


Figure 9. Forward characteristics of the devices under test, replotted from the manufacturers' datasheets [19–22].

None of the entries in Table 1 were independently characterized in this work: apart from the extracted V_{F0} and r_F values, they are datasheet ratings or reported parameters obtained under device-specific conditions. The table therefore provides nominal device

context only, and the quantitative conclusions of this work rest on the devices measured on the same DPT platform.

Four PCBs formed groups A–D, each with C3M0016120K (Wolfspeed, Inc., Durham, NC, USA) at both Q_1 and Q_2 . As a deliberate DPT constraint, D_1 and D_2 used the same SBD type to maintain phase-leg symmetry. Both SBD positions were empty in group A; groups B, C, and D used two IDWD15G120C5 (Infineon Technologies AG, Munich, Germany), SCS220KG (ROHM Co., Ltd., Kyoto, Japan), and C4D20120A (Wolfspeed, Inc., Durham, NC, USA) devices, respectively. Thus, the comparisons refer to matched phase-leg configurations rather than isolated substitutions of D_1 .

The datasheet forward characteristics of the body diode and the SBDs are illustrated in Figure 9. Together with the model in Section 3, these typical curves indicate that I_{ideal} decreases substantially as temperature increases. Its approximate position changes from above the tested current range at $T_j = 25^\circ\text{C}$ to near or below the lower test current at $T_j = 175^\circ\text{C}$. This trend motivated the selected test currents of 25 and 50 A.

5. Experimental Results

In this section, the current distribution in each interval is investigated according to different factors. As discussed in Section 3, the factors associated with the measured current distribution are highlighted. Unless otherwise stated, the waveform measurements in this section were performed at $V_{dc} = 800\text{ V}$, $I_{set} = 50\text{ A}$, and $T_c = 25^\circ\text{C}$.

5.1. Turn-On Transient Measurement Results

The initial t_1 – t_2 interval is dominated by capacitive displacement currents. During t_2 – t_3 , conductive branch currents become important as the load current commutates from Q_2 to the high-side branches.

5.1.1. Junction Capacitance

The investigation of the influence of junction capacitance is implemented by using different SBDs, which have different C_j . This comparison examines whether the measured turn-on current distribution follows the ordering expected from the device capacitance data. The current waveforms of the four experimental groups are illustrated in Figure 10.

Figure 10 shows representative turn-on current waveforms from a single DPT. The oscilloscope was triggered by an electrical signal synchronized with the optical gate-drive command. Within the following 200 ns window, the branch peaks were independently extracted as $I_{D1,pk} = \max I_{D1}(t)$ and $I_{Q1,pk} = \max I_{Q1}(t)$. Their ratio is used only as a peak-amplitude indicator because the two maxima need not occur at the same instant. Table 2 reports the five-shot mean.

Table 2. Turn-on peak-amplitude ratios and forward-conduction ringing metrics without and with the extra SBD-branch impedance. The peak-amplitude ratios are five-shot means; the ringing peak-to-peak values and $5\tau_d$ are representative-waveform point estimates. The with-cable inductance ratio is nominal, i.e., the standalone cable self-inductance added to the measured base branch inductance.

Group	C_{j1}/C_{oss1}	$\frac{L_s+L_d}{L_c+L_a}$ Nominal, with Cable	$\frac{I_{D1,pk}}{I_{Q1,pk}}$, No Cable	$\frac{I_{D1,pk}}{I_{Q1,pk}}$, with Cable	Ringing pk–pk (A), No/with	$5\tau_d$ (μs), No/with
B	0.26	0.36	0.85	0.35	15.44/3.38	1.18/2.20
C	0.37	0.37	1.09	0.60	15.80/11.20	1.17/1.33
D	0.29	0.38	0.94	0.75	16.80/14.40	1.18/1.26

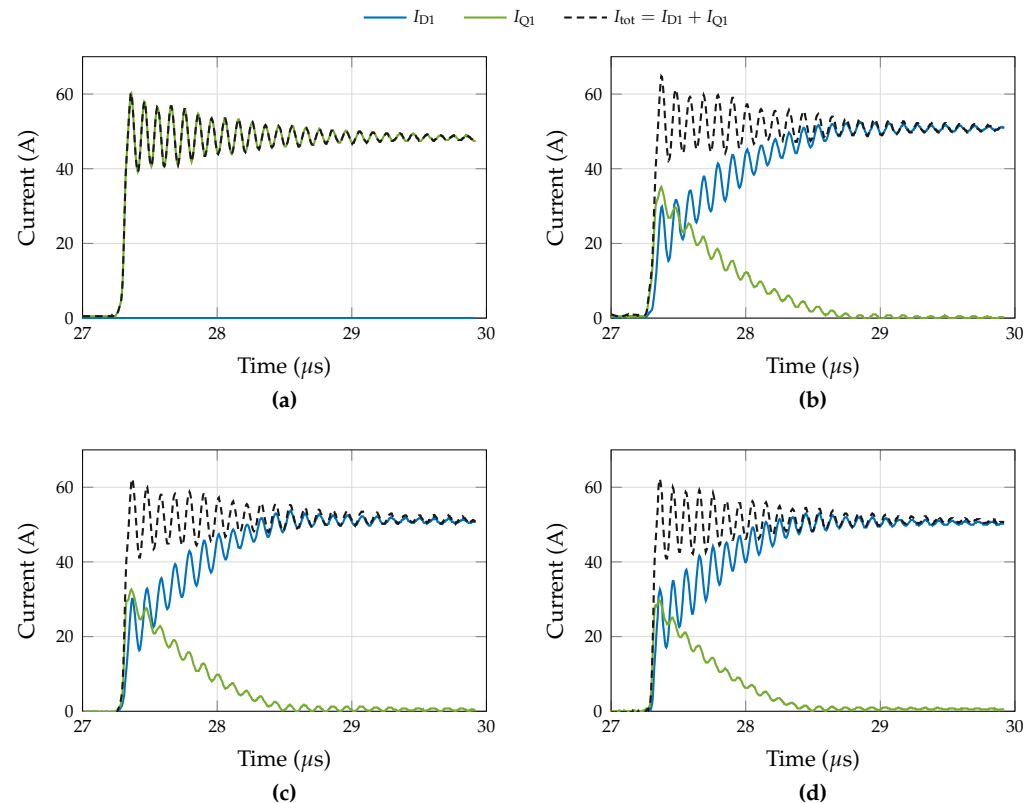


Figure 10. Experimental measured turn-on current waveforms at $V_{dc} = 800$ V, $I_{set} = 50$ A, and $T_c = 25$ °C: (a) group A; (b) group B; (c) group C; (d) group D. Blue: measured SBD-branch current I_{D1} ; green: measured MOSFET branch current I_{Q1} ; dashed black: calculated branch-current sum $I_{tot} = I_{D1} + I_{Q1}$.

The ordering of the measured peak-amplitude ratios, $B < D < C$, agrees with the ordering of the datasheet capacitance indicator C_{j1}/C_{oss1} values. This result is qualitatively consistent with the capacitive displacement current mechanism. However, the three SBDs have different packages, forward characteristics, and parasitic impedances. Therefore, the present comparison does not establish a universal linear proportionality between $I_{D1,pk}/I_{Q1,pk}$ and C_{j1}/C_{oss1} .

5.1.2. Added SBD-Branch Impedance

To examine the sensitivity of the turn-on current distribution to an increase in the SBD-branch impedance, a 45 mm, 16 AWG copper cable was inserted in series with L_a . The cable introduced a measured standalone self-inductance of 30.9 nH and a DC resistance of 2.9 mΩ. In the assembled circuit, the cable couples magnetically with the adjacent return path, so the standalone value is an upper bound for the effective increase of the redistribution-loop inductance; within the RL model of Section 3.2, the 6.8–13.7% increase of the measured redistribution time constants of groups C and D (Table 2) corresponds to an effective loop-inductance increase of approximately 3–6 nH. Group B is excluded from this estimate because its settling is dominated by the nonlinear diode resistance rather than by a linear RL decay (Section 5.2.2).

The same independent 200 ns peak-extraction method was applied to Figure 11. Table 2 reports the five-shot mean of $I_{D1,pk}/I_{Q1,pk}$ with the extra impedance, together with the forward-conduction ringing metrics discussed in Section 5.2.2.

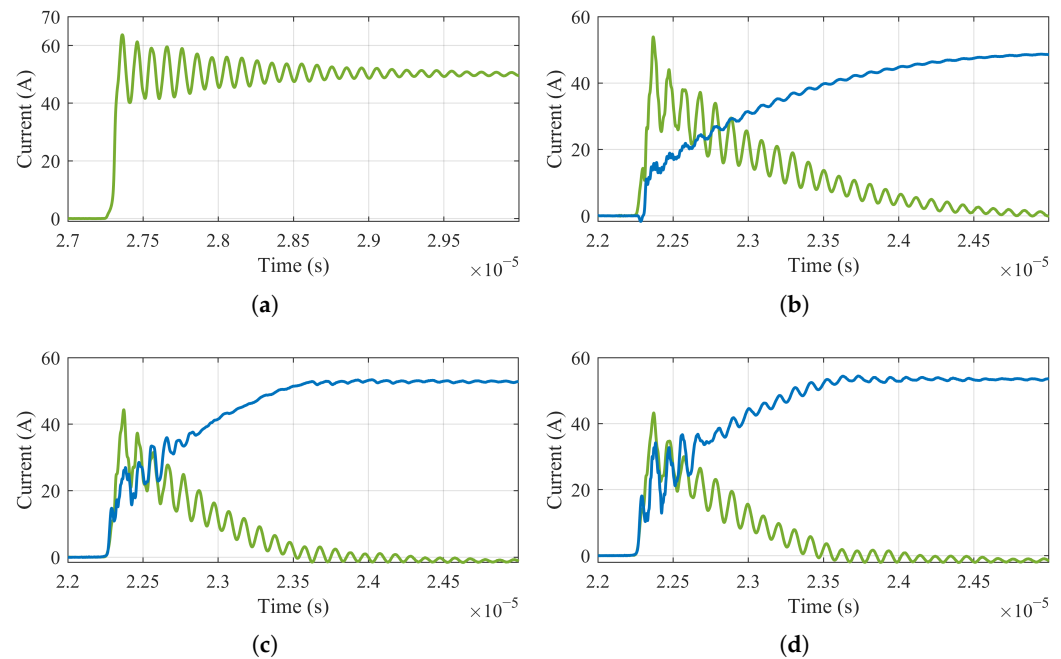


Figure 11. Turn-on transient current distribution with an extra inductance on L_a : (a) group A; (b) group B; (c) group C; (d) group D. Blue: measured SBD-branch current I_{D1} ; green: measured MOSFET-branch current I_{Q1} .

With the additional cable, the measured $I_{D1,pk}$ was lower for groups B–D, as expected from the increased SBD-branch impedance limiting the branch-current growth rate. The measured change cannot be attributed exclusively to $L_c + L_a$ because the cable also modified the branch resistance and geometry.

5.2. Forward Conduction Measurement Results

The current redistribution during the t_3 – t_4 interval is examined with respect to case temperature T_c , branch inductance, and V_{EE} .

5.2.1. Effect of Case Temperature on Current Redistribution

Changing T_c changes the measured current redistribution because the device forward characteristics vary with temperature. The waveforms are shown in Figure 12.

As shown in Figure 12a, increasing T_c was associated with a longer turn-on delay, while the settled current amplitude remained similar. For groups B–D, the settled MOSFET branch current increased with T_c . At $T_c = 25^\circ\text{C}$, $I_{Q1}(t_4)$ was approximately 0 A, whereas at $T_c = 175^\circ\text{C}$ it reached 14.25 A, 9.88 A, and 8.57 A for groups B, C, and D, respectively. This trend is qualitatively consistent with the expected temperature-induced shift of I_{ideal} .

As a worked screening example, I_{ideal} is obtained from Figure 9 by reading the SBD forward current at the common voltage $V_{F0,bd1}$ of the MOSFET reverse-conduction branch, which is 2.65 V at $T_j = 25^\circ\text{C}$ and 2.54 V at 175°C (Table 1). The construction yields $I_{ideal} \approx 55, 65$, and 80 A for groups D, B, and C at 25°C , and approximately 25, 26, and 32 A for the same groups at 175°C . The screening thus predicts SBD-only steady-state conduction at $T_c = 25^\circ\text{C}$ and shared conduction at 175°C , in agreement with the measured settled currents. Within the shared-conduction region, however, the measured share ordering does not follow I_{ideal} alone: groups B and D have similar $I_{ideal}(175^\circ\text{C})$ yet differ in settled current by a factor of 1.7. I_{ideal} therefore serves as a go/no-go screen, while the share magnitude requires the full branch model of Equation (7).

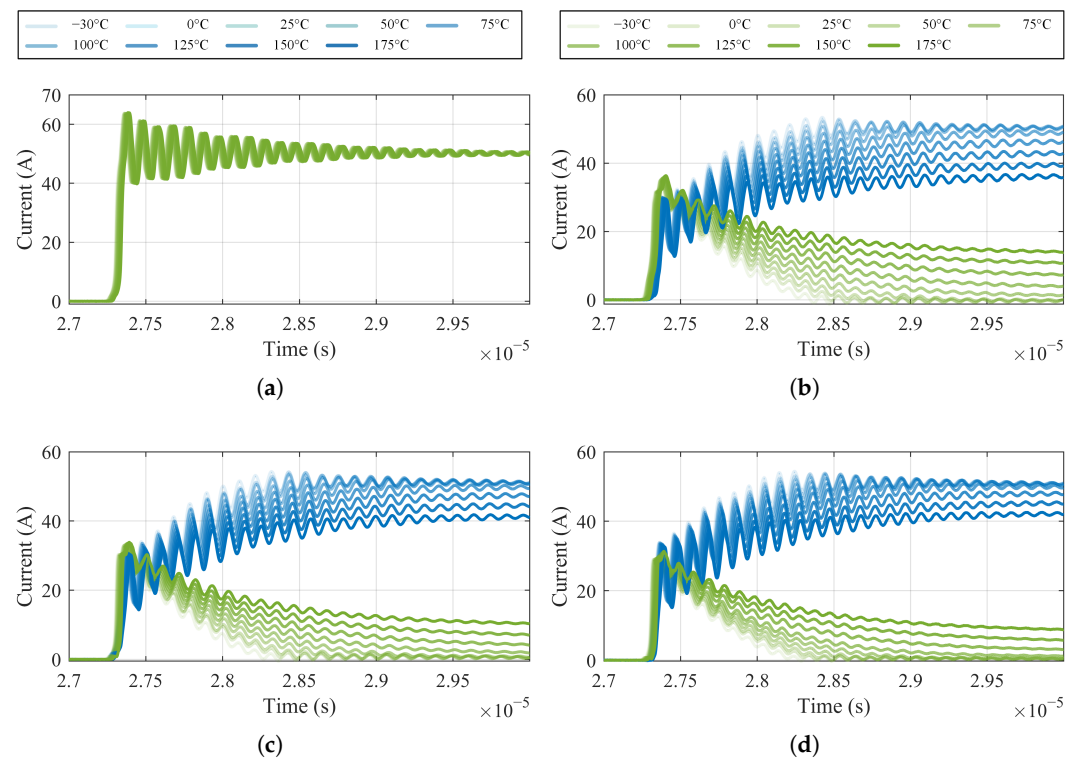


Figure 12. Current redistribution during forward conduction at case temperatures from $-30\text{ }^{\circ}\text{C}$ to $175\text{ }^{\circ}\text{C}$: (a) group A; (b) group B; (c) group C; and (d) group D. The color-opacity legends indicate T_c for the SBD current I_{D1} and the SiC MOSFET branch current I_{Q1} .

5.2.2. Branch Inductance

The added branch impedance changed the observed ringing and the reported redistribution time constant. No resolvable change in the settled current was observed within the five-shot repeatability. The peak-to-peak I_{D1} ringing over the t_3 – t_4 interval and the corresponding $5\tau_d$ values were extracted from the representative waveforms in Figures 10 and 11 and are listed in Table 2. They are representative-waveform point estimates rather than five-shot statistics.

In these representative waveforms, the peak-to-peak value of the I_{D1} ringing is reduced by 78.1%, 29.1%, and 14.3% for groups B, C, and D, respectively. The corresponding τ_d value is increased by 86.4%, 13.7%, and 6.8%, respectively. The large increase in group B should not be read as a linear-RL time constant. In group B, the MOSFET branch current settles at about 1.6 A instead of zero, so the redistribution ends near the knee of the body-diode forward characteristic, where the differential resistance changes strongly with the current. The long settling time of group B therefore reflects this nonlinear resistance, and the linear-RL interpretation of τ_d is applied only to groups C and D.

With the measured branch inductances ($L_Q + L_D \approx 36\text{ nH}$), the extracted $\tau_d \approx 236\text{ ns}$ implies $R_Q + R_D \approx 0.15\text{ }\Omega$. The datasheet differential resistances read from Figure 9 along the actual redistribution trajectory—the body diode decaying below $\sim 20\text{ A}$ (≈ 60 – $100\text{ m}\Omega$) and the SBD conducting at 30 – 55 A ($\approx 25\text{ m}\Omega$)—sum to ≈ 0.09 – $0.13\text{ }\Omega$, the same order of magnitude, with the remainder attributable to the package and PCB resistances and the piecewise-linear approximation.

5.2.3. Gate Driver Off-State Voltage

The datasheet reverse-conduction curves indicate that the fitted low-current voltage offset of the complete MOSFET reverse-conduction branch depends on gate bias. This effective parameter is denoted by $V_{F0,Q1}^{\text{eff}}(V_{EE})$. Its gate-bias dependence motivates the V_{EE}

sweep because it can change the steady-state current sharing between the MOSFET and SBD branches.

The off-state gate voltage was swept from $V_{EE} = -2.0$ to -5.0 V. The current waveforms for group D are shown in Figure 13.

The sweep produces a gate-bias-dependent redistribution between the measured SBD-branch current I_{D1} and MOSFET branch current I_{Q1} . The trend is consistent with increased gate-controlled reverse-channel conduction at less-negative V_{EE} . Because the channel and intrinsic body diode currents were not measured separately, the result should not be interpreted as a direct change in the intrinsic body diode characteristic.

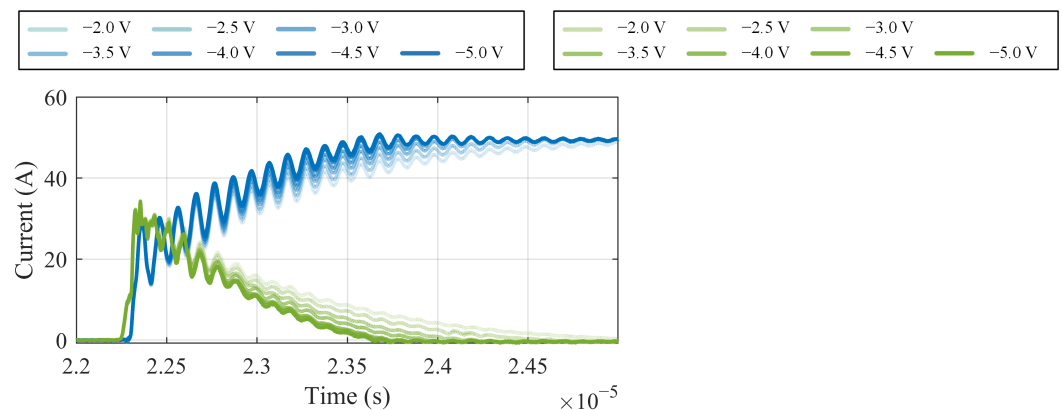


Figure 13. Current distribution in group D when V_{EE} is swept from -2.0 to -5.0 V. The color-opacity legend strips map trace shade to V_{EE} (blue: measured SBD-branch current I_{D1} ; green: measured MOSFET branch current I_{Q1}).

5.3. Turn-Off and Reverse Recovery Transient Measurement Results

The total reverse recovery current is the sum of I_{D1} and I_{Q1} . Apart from the factors that affect the single diode reverse recovery performance, there are different effects that change the total reverse recovery performance.

5.3.1. Effect of Case Temperature on Reverse Recovery

The framework in Section 3 suggests that a larger MOSFET branch current before commutation and a temperature-dependent stored-carrier contribution can modify the temporal overlap of the MOSFET- and SBD-branch reverse-current components. The case-temperature-sweep measurements previously reported in [15] are reanalyzed here to examine whether the measured waveforms are consistent with this mechanism. The dataset covers $T_c = -30$ °C to 175 °C. The waveforms of the four experimental groups are shown in Figure 14.

As shown in Figure 14, the measured MOSFET branch reverse-current magnitude in group A increased by 153.2% as T_c increased from -30 °C to 175 °C. Over the same range, the total reverse-current magnitude increased by 50.1%, 33.5%, and 15.7% for groups B, C, and D, respectively. The relative timing of the MOSFET branch and SBD-branch current features is qualitatively consistent with the clamping and temporal-overlap mechanism proposed in Section 3. In group B, a later decay of the measured MOSFET branch reverse-current feature coincided with a larger total reverse-current peak. This observation is consistent with, but does not independently isolate, a stored-carrier contribution within the MOSFET branch.

The case-temperature dependence of the measured reverse-current peak magnitude is summarized in Figure 15.

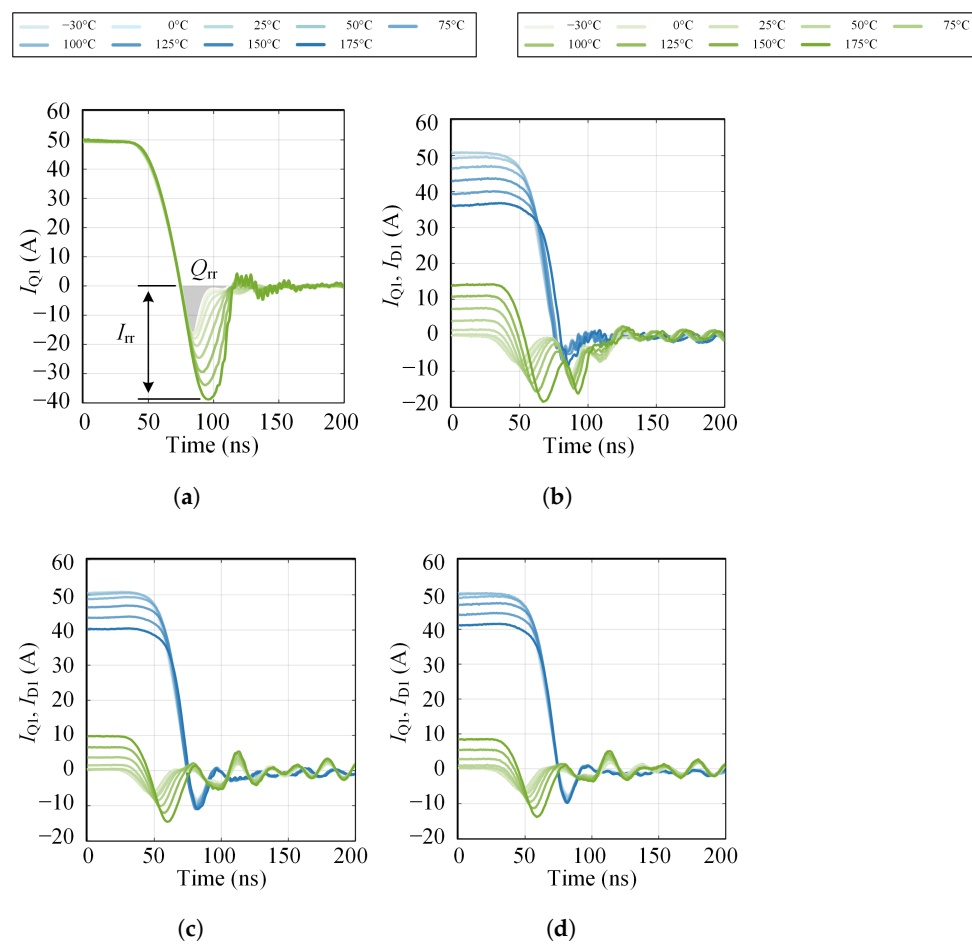


Figure 14. The turn-off and reverse recovery current distribution results: (a) group A; (b) group B; (c) group C; (d) group D. The color-opacity legend strips map trace shade to T_c , with the same encoding as Figure 12: blue denotes the measured SBD-branch current I_{D1} , and green denotes the measured MOSFET branch current I_{Q1} . Replotted using data from the authors' previous work [15].

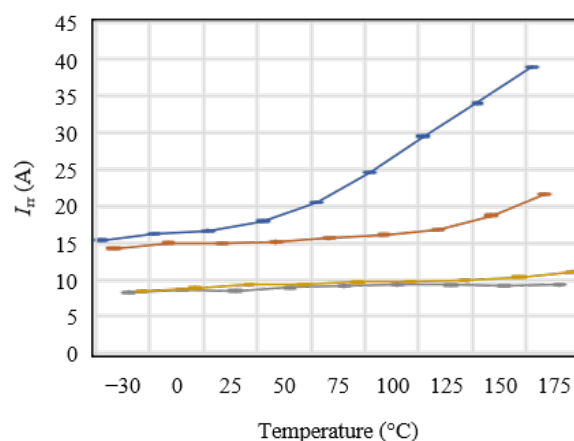


Figure 15. Case-temperature dependence of the reverse-current peak magnitude at $V_{dc} = 800$ V and $I_{set} = 50$ A. Blue: group A (no SBD); orange: group B (IDWD15G120C5); yellow: group C (SCS220KG); gray: group D (C4D20120A). The box-and-whisker elements summarize five shots at each condition using the exclusive-quartile convention, and the superimposed curves connect the five-shot means. Across all 36 plotted conditions, the population standard deviation did not exceed 0.100 A; the median and maximum coefficients of variation were 0.41% and 0.87%, respectively. The small dispersion makes most boxes and whiskers difficult to distinguish at the plotted scale. Replotted using data from the authors' previous work [15].

Figure 16 shows that the transition associated with Q_2 turn-on became shorter as case temperature increased for all four configurations. From $T_c = -30^\circ\text{C}$ to 175°C , the measured time decreased by 39.5–45.6%. Despite this change in absolute transition time, groups B and C remained longer than group A at every temperature setpoint, whereas group D closely followed group A. At $T_c = 175^\circ\text{C}$, the group B and group C values were 57.6% and 78.4% longer than that of group A, respectively, whereas the group D value was only 1.7% longer.

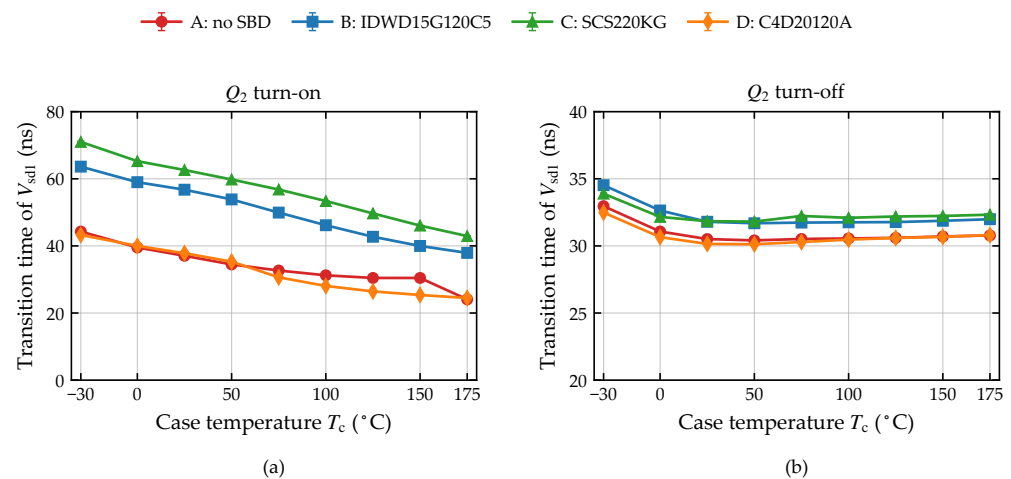


Figure 16. Case-temperature dependence of the circuit-level voltage-transition time measured from V_{sd1} at $V_{dc} = 800\text{ V}$ and $I_{set} = 50\text{ A}$: (a) the transition associated with Q_2 turn-on; (b) the transition associated with Q_2 turn-off. Markers indicate five-shot means, and error bars denote the population standard deviation. Across all 72 plotted points, the population standard deviation did not exceed 0.267 ns and the coefficient of variation did not exceed 0.76%. Consequently, most error bars are smaller than and obscured by the plotted markers. Reprocessed using data from the authors' previous work [15].

The turn-off-associated transition showed a much weaker temperature dependence. It decreased between -30°C and approximately 25°C and then remained nearly constant. At 175°C , the group B and group C values were 3.9% and 5.0% longer than the group A value, respectively, and the group D value differed from group A by only 0.1%. Therefore, the measured commutation-speed effect of an external SBD was device-dependent rather than universal.

5.3.2. Reverse Recovery Energy

Peak current alone does not determine the reverse-recovery energy. The reported E_{rr} was calculated for all 720 records using Equation (14) and the waveform-processing procedure described in Section Waveform Processing and Metric Extraction and illustrated in Figure 8.

The dataset contains nine case-temperature setpoints and four operating points: 800 V/50 A, 800 V/25 A, 400 V/50 A, and 400 V/25 A. Each point in Figure 17 is the mean of five measurements, and the error bars denote the population standard deviation.

The measured effect of the matched external-SBD configuration depends on the selected device and operating point. Relative to group A, group D reduces the mean E_{rr} at $T_c = 25^\circ\text{C}$ by 50.8%, 54.5%, 19.8%, and 43.1% for the four operating points in Figure 17. At $T_c = 175^\circ\text{C}$, the corresponding reductions are 70.7%, 70.0%, 76.1%, and 81.4%. In contrast, group B increases E_{rr} at $T_c = 25^\circ\text{C}$ by 172.7%, 185.2%, 109.6%, and 126.0%. Group D also exceeds group A at 400 V/50 A by 48.5% at $T_c = -30^\circ\text{C}$ and by 32.0% at $T_c = 0^\circ\text{C}$. These crossovers are consistent with the combined influence of current sharing, device

capacitance, and MOSFET branch conduction. The reported E_{rr} applies only to the reverse recovery event and is not a measurement of total converter switching loss or efficiency.

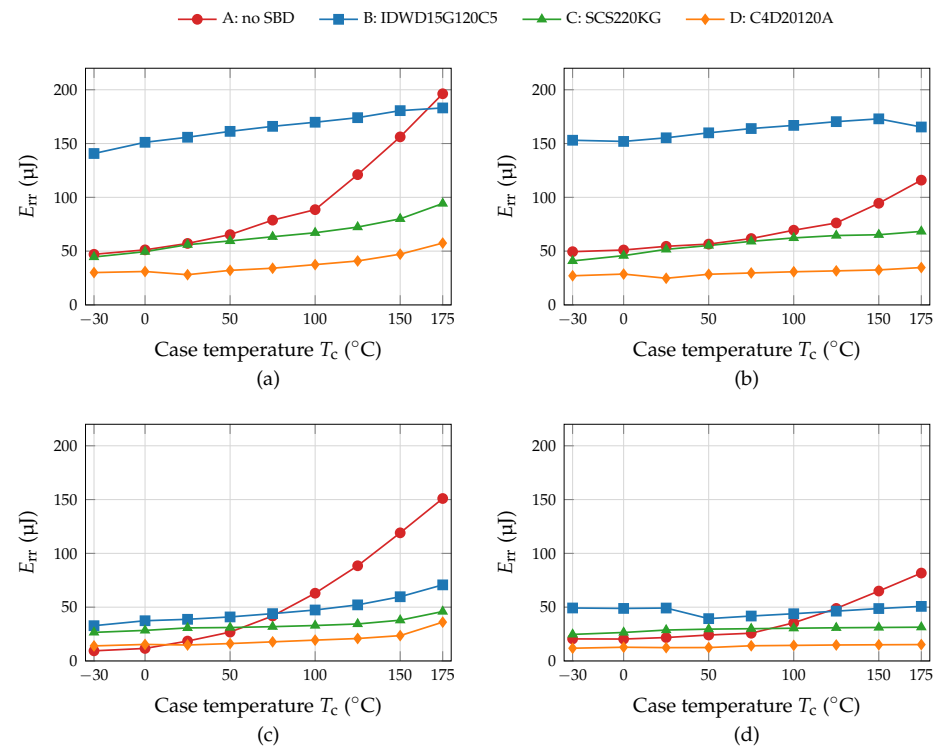


Figure 17. Reverse recovery energy E_{rr} for groups A–D. Group A has no external SBD; groups B, C, and D use IDWD15G120C5, SCS220KG, and C4D20120A, respectively. Panels (a–d) show 800 V/50 A, 800 V/25 A, 400 V/50 A, and 400 V/25 A. Markers show five-shot means. Across all 144 plotted conditions, the standard deviation did not exceed 1.93 μJ and the coefficient of variation did not exceed 2.53%.

5.3.3. Dead Time Duration

The dead time determines the duration available for current redistribution between t_3 and t_4 . Figure 18 shows the measured branch-current distribution for group B over 350 ns to 3 μs . Figure 19 summarizes the dependence of $I_{Q1}(t_{5a})$, $|I_{Q1,\min}|$, and I_{rr} on dead time.

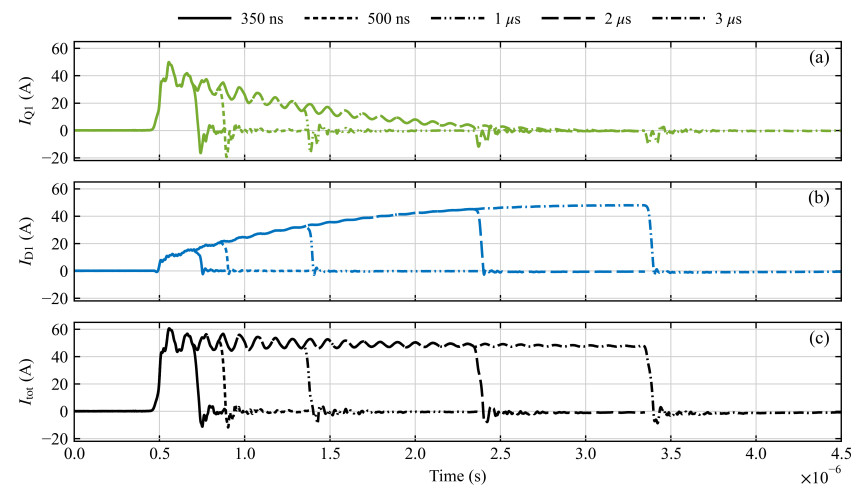


Figure 18. Current distribution for group B at dead times of 350 ns, 500 ns, 1 μs , 2 μs , and 3 μs : (a) measured MOSFET-branch current I_{Q1} (green); (b) measured SBD-branch current I_{D1} (blue); (c) calculated branch-current sum $I_{tot} = I_{D1} + I_{Q1}$ (black). In all three panels, solid, short-dashed, dash-dot-dot, long-dashed, and dash-dotted lines correspond to the listed dead times, respectively.

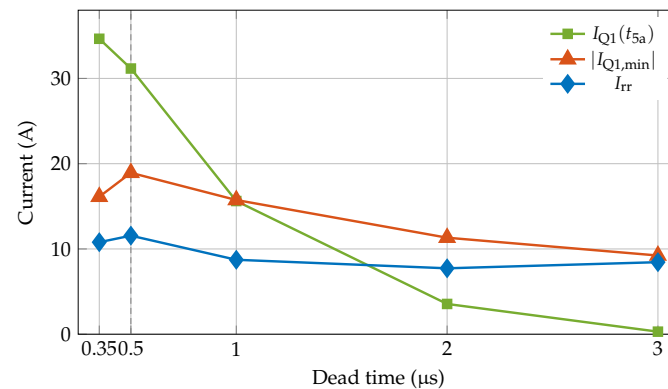


Figure 19. Dead-time dependence for group B at $V_{dc} = 400$ V and $I_{set} = 50$ A. Green squares: $I_{Q1}(t_{5a})$; orange dashed triangles: $|I_{Q1,min}|$; blue dash-dotted diamonds: I_{rr} . The vertical line indicates the largest measured I_{rr} , at 500 ns.

A shorter dead time leaves less time for forward-current redistribution before the second pulse and therefore changes $I_{Q1}(t_{5a})$. The measured reverse-current magnitudes $|I_{Q1,min}|$ and I_{rr} depend nonmonotonically on dead time and reach their largest values at 500 ns. Table 3 lists the corresponding signed current minima.

Table 3. Signed reverse-current metrics as a function of dead time for group B. Negative values retain the measured current direction. The entries are processed point estimates.

Dead Time (μ s)	$I_{Q1}(t_{5a})$ (A)	$I_{Q1,min}$ (A)	$I_{D1,min}$ (A)	$I_{tot,min}$ (A)
0.35	34.65	−16.12	−2.49	−10.79
0.5	31.16	−18.93	−2.48	−11.56
1	15.62	−15.74	−2.97	−8.73
2	3.55	−11.32	−2.87	−7.73
3	0.30	−9.23	−3.27	−8.45

In Table 3, each signed minimum is the global minimum of the corresponding trace, $I_{Q1,min} = \min_t I_{Q1}(t)$, $I_{D1,min} = \min_t I_{D1}(t)$, and $I_{tot,min} = \min_t I_{tot}(t)$, and is not restricted to the reverse interval $[t_a, t_b]$ used in Equation (13). Each minimum falls within the reverse-recovery interval from t_5 to t_8 defined in Figure 5, and for I_{tot} the two windows give the same value because the peak time t_p lies in $[t_a, t_b]$ by construction. The three minima are extracted independently and need not occur at the same instant; $|I_{D1,min}|$ gives the SBD reverse-current peak magnitude.

Relative to the 3 μ s dead time, the largest I_{rr} , reached at 500 ns, is 36.8% larger.

6. Discussion

In the tested matched phase-leg configurations, the external SBD did not unconditionally reduce the measured high-side reverse-recovery energy. Its effectiveness depended in part on how much forward current it carried before commutation. This interpretation is consistent with previous phase-leg and high-voltage device comparisons in which body diode participation remained possible despite the parallel SBD [10,13].

Groups B and C slowed down the Q_2 turn-on-associated V_{sd1} transition relative to group A throughout the temperature sweep, whereas group D remained close to group A. The Q_2 turn-off-associated transition differences were much smaller. The external SBD remains involved in the commutation through its junction capacitance, even when it is not conducting current. During Q_2 turn-on, this capacitance is charged as the SBD changes from forward conduction to reverse blocking; during Q_2 turn-off, it is discharged

as the switching-node voltage rises. The additional junction charge increases the charge exchanged and therefore tends to reduce the half-bridge voltage slew rate under the same operating and gate-drive conditions. This device-dependent behavior is consistent with the combined influence of nonlinear device capacitances, branch parasitic impedance, and transient current redistribution.

The current at the boundary of each freewheeling interval sets the initial condition for the next interval, so the interval-specific models in Section 3 are coupled rather than independent. The experimental sweeps in Section 5 examine how the tested interventions are associated with the measured current distribution. Table 4 summarizes the directly observed metrics and indicates where an effect was not resolved, isolated, or tested.

Table 4. Measured influence of each factor on the branch-current distribution in each interval. Entries give the observed change of the dominant metric of that interval over the tested sweep. “Not resolved”: no effect distinguishable from shot-to-shot variation; “not tested”: no independent sweep performed; “not isolated”: the effect could not be separated from the other device properties that changed at the same time. The entries summarize point estimates or ranges reported in the preceding figures and tables.

Factor (Tested Intervention)	Turn-On	Forward Conduction	Turn-Off and Reverse Recovery
Added SBD-branch impedance (+30.9 nH standalone, effective $\approx 3\text{--}6$ nH; +2.9 m Ω)	The I_{D1} spike is lower in groups B–D.	The ringing peak-to-peak value decreases by 14.3–78.1%. $5\tau_d$ increases by 6.8–13.7% in groups C and D, and by 86.4% in group B, where the settling is nonlinear.	Not tested.
Gate-driver off-state voltage	Not resolved.	The MOSFET branch share increases at a less negative V_{EE} .	Not resolved.
SBD selection (three devices; capacitance not independently varied)	The $I_{D1,pk}/I_{Q1,pk}$ ratio is 0.85–1.09. Relative to group A, the turn-on-associated V_{sd1} transition is longer in groups B and C and similar in group D.	Not isolated.	The turn-off-associated V_{sd1} differences are small. The reverse-current contributions are not isolated.
Case temperature ($T_c = -30\text{--}175$ °C)	The turn-on-associated V_{sd1} transition becomes shorter by 39.5–45.6%.	The settled I_{Q1} increases from 0 to 8.57–14.25 A.	The turn-off-associated transition depends weakly on temperature. I_{rr} increases by 15.7–50.1% in groups B–D and by 153.2% in group A.
Dead time (350 ns–3 μ s, group B)	Not resolved.	$I_{Q1}(t_{5a})$ increases from 0.30 to 34.65 A.	I_{rr} peaks at 500 ns, which is 36.8% higher than at 3 μ s.

The observations summarized in Table 4 are discussed below. The added cable raises the standalone $L_c + L_a$ nominally by about 177%, whereas the effective redistribution-loop increase inferred from the measured time constants of groups C and D is approximately 3–6 nH, i.e., roughly 10–20% of the standalone value (Table 2). The larger settling-time increase in group B is attributed to its nonlinear end point rather than to the added inductance (Section 5.2.2). It limits the current growth rate of the SBD branch during turn-on, damps the ringing, and slows down the redistribution during forward conduction. This sensitivity to branch impedance is qualitatively consistent with analytical switching-cell models that include nonlinear capacitances and loop parasitics [16,17].

A higher case temperature was associated with a larger measured MOSFET branch current share and a changed total reverse current, possibly involving a larger stored-carrier contribution. The observed redistribution is consistent with earlier reports that the external-

SBD current share decreases when the MOSFET reverse-conduction path becomes more favorable [3,10,15]. A less-negative V_{EE} acts in the same direction through a lower $V_{F0,Q1}^{eff}$.

A shorter dead time interrupts the current redistribution during forward conduction and leaves a larger MOSFET branch current before commutation. The nonmonotonic reverse-current response is qualitatively consistent with the previously reported sensitivity of SiC diode recovery to dead time [14]. However, the different voltage class, device structure, and test conditions preclude a direct quantitative comparison.

6.1. Accuracy of the Interval Models

The interval models in Section 3 are screening and assessment tools rather than predictive circuit models. Their accuracy depends on the quantity considered. Table 5 summarizes the comparison between model predictions and measurements for each evaluated quantity.

The two turn-on comparisons in Table 5 are consistent with the joint influence of device capacitances and branch impedances described in Section 3.1. Neither comparison isolates a single parameter: the SBDs also differ in package and forward characteristics, and the added cable changed both the branch resistance and the geometry. The current-ratio relation in Section 3.1 applies to simultaneous displacement currents during t_1 – t_2 ; it reduces to C_{j1}/C_{oss1} when the two internal voltage slew rates are approximately equal. The independently extracted branch peaks need not occur at the same instant or within this capacitance-dominated interval, so their ratio does not directly test that relation; without the added branch impedance, the measured peak ratios are approximately three times the corresponding C_{j1}/C_{oss1} values in all three groups. For the high-side MOSFET Q_1 , the capacitance-dominated model uses $C_{oss1} = C_{ds} + C_{gd}$ and does not resolve the gate-loop dynamics associated with $C_{iss} = C_{gs} + C_{gd}$ and its joint V_{gs} – V_{ds} dependence [18] or the partition of the C_{gd} displacement current within the gate network. C_{j1}/C_{oss1} is therefore used as a datasheet indicator for the qualitative comparison and device selection, not to calculate the branch peak currents.

Table 5. Accuracy of the interval models of Section 3 against the measurements of Section 5.

Predicted Quantity	Model Result	Measured Result	Agreement
Turn-on branch peak ratio $I_{D1,pk}/I_{Q1,pk}$	Current distribution depends jointly on device capacitances and branch impedances (Section 3.1)	0.85, 1.09, 0.94 without the added impedance; 0.35, 0.60, 0.75 with the added SBD-branch impedance (Table 2)	Qualitative agreement: the baseline ordering follows C_{j1}/C_{oss1} , and adding SBD-branch impedance lowers the ratio in every group. Peak-ratio magnitudes are not predicted.
Conduction state, SBD only or shared	I_{ideal} screen, Equation (7)	three groups at 25 and 175 °C	All six cases are classified correctly.
Settled MOSFET branch current at 175 °C	14.3, 10.5, 16.7 A	14.25, 9.88, 8.57 A	The errors are +0.4%, +6%, and +95% for groups B, C, and D.
Redistribution time	$5\tau_d = 1.2 \mu s$	2–3 μs , group B dead-time sweep	The model underestimates the required time, so $5\tau_d$ is used as a lower bound only.
Turn-off charge split into Q_{rr}^* and Q_{cj}	Equation (11)	Not available	This quantity is not evaluated. The branch parameters were not identified, and the two charges were not separated experimentally.

The conduction screen correctly classified all six evaluated cases. The predicted settled MOSFET branch currents of groups B and C also agreed with the measurements within 0.4% and 6%, respectively. The model therefore captured both the conduction state and the current-sharing magnitude for these groups. Group D was the exception: its predicted current was 16.7 A, compared with the measured value of 8.57 A, giving an error of 95%.

One possible source of this deviation is the representation of a curved reverse-conduction characteristic by a single slope resistance. Changing the linearization window produced MOSFET r_F values from 14 to 39 m Ω and changed the predicted currents by up to 36%. This sensitivity may explain part of the numerical deviation, but it did not remove the group D mismatch. In addition, the model parameters were derived from typical datasheet curves rather than from the individual device characterization. The group D result could be explained if the SBD slope resistance were assumed to be 30% below its datasheet typical value. Because the repeated measurements for each configuration were obtained from the same DUT assembly rather than from a population of devices, this comparison provides only an indicative assessment of the interval model accuracy and does not quantify device-to-device variation.

6.2. Device Selection Procedure

The interval models of Section 3 and the experimental results of Section 5 can be combined into a screening procedure for choosing a suitable external SiC SBD for a given SiC MOSFET. The procedure uses only datasheet forward characteristics, datasheet capacitances, and layout-level branch parasitics, and it is intended to narrow the candidate list before any DPT characterization.

1. **SBD forward conduction screen.** Evaluate I_{ideal} from Equation (7) at the highest expected junction temperature $T_{j,max}$ and require $I_{ideal}(T_{j,max}) > I_{op,max}$, where $I_{op,max}$ is the largest freewheeling current of the application. A suitable SBD is one whose $V_{F0,D1}$ lies well below the $V_{F0,bd1}$ of the MOSFET reverse-conduction branch and whose R_D is low. The worked example in Section 5.2.1 illustrates the temperature dependence of this screen. Within the shared-conduction region, quantitative prediction of the current share requires the complete branch model in Equation (7).
2. **Timing screen.** Evaluate $\tau_d = (L_Q + L_D)/(R_Q + R_D)$ from Equation (7) and require the dead time t_{dead} of the half-bridge gate driver to satisfy $t_{dead} \gtrsim 5\tau_d$. A shorter dead time may interrupt redistribution, leaving a nonnegligible MOSFET branch current before commutation. As shown in Table 5, $5\tau_d$ underestimated the dead time required in the group B sweep. It is therefore a lower-bound timing criterion rather than a sufficient condition for complete current redistribution.
3. **Capacitance penalty.** Among the candidates that pass the first two screens, select the one with the smallest junction capacitance and stored charge. The first and the third requirements oppose each other. Raising I_{ideal} usually requires a smaller R_D and therefore a larger die area. The negative transient current of an SiC SBD, however, is dominated by the junction-capacitance charge Q_{cj} of Equation (11), which grows with die area.
4. **Layout and gate bias.** Keep the SBD branch inductance $L_c + L_a$ comparable to the MOSFET branch inductance $L_s + L_d$ rather than minimizing it independently, and reduce the commutation-loop stray inductance. The turn-on distribution follows the branch impedance ratio. When the conduction screen is only narrowly satisfied, the most negative permissible V_{EE} increases $V_{F0,Q1}^{eff}$ and therefore raises I_{ideal} . This extends the operating range in which the SBD remains the dominant freewheeling path without requiring modifications to the power stage.

The four screens also clarify where the external SBD may provide a practical benefit. The added hardware includes one SBD device and the associated board area per switch position inside the commutation loop. In the tested configurations, an external SBD could reduce E_{rr} at high case temperatures, whereas some configurations increased it at low case temperatures. Because τ_d scales with the branch L/R , this benefit is more readily realized in high-temperature, low-inductance designs with sufficient dead time but may be

limited in designs optimized for the shortest possible dead time. Whether the resulting loss reduction justifies the additional device and board area is application specific and was not evaluated here.

This study covers one MOSFET type, three SBD types, and one DPT layout. The reported trends and thresholds are therefore limited to the tested devices and operating range.

7. Conclusions

This paper investigates current sharing between the reverse-conduction path of an SiC MOSFET and a paralleled SiC SBD during freewheeling. Simplified interval-specific models are presented for turn-on, forward conduction, and turn-off. The proposed I_{ideal} is a datasheet-based screening metric rather than a universal conduction threshold.

The DPT results qualitatively support the proposed branch-level interpretation within the tested conditions. The measured current distribution was associated with device capacitance and branch impedance during turn-on and showed case-temperature-dependent RL-type redistribution during forward conduction, with the MOSFET branch conducting an increasing share of the freewheeling current at elevated case temperature.

At $V_{dc} = 800$ V and $I_{set} = 50$ A, the turn-on-associated V_{sd1} transition time decreased by 39.5–45.6% as T_c increased from -30 °C to 175 °C. The influence of the external SBD was device-dependent and was much smaller during turn-off.

The effect of the external SBD depended on the tested phase-leg configuration and operating point. Relative to group A, group D reduced the mean E_{rr} by up to 81.4% at $T_c = 175$ °C, whereas some configurations increased E_{rr} at low case temperature. In the group B dead-time sweep, the total reverse-current magnitude was 36.8% larger at 500 ns than at 3 μ s; these numerical trends are specific to the investigated devices and operating range.

Author Contributions: Conceptualization, H.Z. and T.B.; data curation, H.Z. and F.S.; formal analysis, H.Z.; investigation, H.Z.; methodology, H.Z. and T.B.; software, H.Z.; validation, H.Z.; resources, T.B.; writing—original draft preparation, H.Z.; writing—review and editing, F.S. and T.B.; visualization, H.Z.; supervision, T.B.; project administration, T.B.; funding acquisition, H.Z. and T.B. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by the China Scholarship Council, grant No. 202006120019.

Data Availability Statement: The processed data supporting the findings of this study are available from the corresponding author upon reasonable request.

Acknowledgments: During the preparation of this manuscript, the authors used Claude Code (Anthropic) to help refine the measurement-data extraction algorithm and the plotting code for the figures of the authors' cited conference paper [15] so that the redrawn figures match the color style of the other figures in this work. The authors have reviewed and edited the output and take full responsibility for the content of this publication.

Conflicts of Interest: The authors declare no conflicts of interest.

Abbreviations

The following abbreviations are used in this manuscript:

DPT	Double-pulse test
JBS	Junction barrier Schottky (diode)
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
PCB	Printed circuit board
SBD	Schottky barrier diode

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