

RESEARCH ARTICLE | SEPTEMBER 28 2026

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Appl. Phys. Lett. 129, 132601 (2026)

<https://doi.org/10.1063/5.0349777>



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Cite as: Appl. Phys. Lett. **129**, 132601 (2026); doi: [10.1063/5.0349777](https://doi.org/10.1063/5.0349777)

Submitted: 25 June 2026 · Accepted: 7 September 2026 ·

Published Online: 28 September 2026



View Online



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ABSTRACT

We have developed a fabrication technique for Josephson junctions that employs a three-dimensional patterned, low-loss substrate instead of commonly used organic resists. The technique enables the fabrication of high-quality trilayer junctions from a wide range of geometries and materials, including high-melting-point superconductors such as tantalum or niobium. The junction electrodes are free from intentionally introduced oxides and organic materials, which are known sources of decoherence. We fabricate and characterize underdamped Nb/AlO_x/Nb junctions of different sizes in several geometries.

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Superconducting quantum circuits critically depend on the quality of their Josephson junctions (JJs), most commonly implemented as Al/AlO_x/Al trilayers. There are two main reasons for this approach: AlO_x's exceptional quality as a tunnel barrier¹ and the technologically relevant low melting point of aluminum. The latter allows a wide range of fabrication possibilities, such as the use of organic resist liftoff masks and angle-dependent patterning.^{2–4} Despite these advantages, the relatively low superconducting gap energy of aluminum limits the operating temperature to ≤ 300 mK and circuit frequencies to ≤ 40 GHz.

Josephson junctions with a higher superconducting gap can overcome these limitations and allow operation of, e.g., SQUIDs or qubits at much higher temperatures^{5,6} and frequencies. Unfortunately, many well-established thin-film superconductors with an energy gap higher than Al (e.g., Ta, TiN, Nb, and NbTi) also have significantly higher melting points and therefore require higher deposition temperatures when the materials are thermally evaporated. Protecting organic resists from burning becomes challenging, and the junction quality is reduced.^{7,8} Although other deposition techniques, such as magnetron sputter deposition, can produce high-quality Nb/AlO_x/Nb JJs,⁵ this technique requires the addition of a lossy dielectric in the immediate vicinity of the JJs, which introduces excess noise.^{9–18} Recent developments have eliminated the presence of these dielectrics through a wet etching post-processing step⁶ or via a flip chip technique.¹⁹

To avoid aggressive oxide etching near the delicate junction, we propose²⁰ an alternative approach to junction-electrode isolation based on profiling the substrate material. A step profile electrically disconnects the metal films deposited below and above the step. We use this geometric feature to shape and insulate the JJ barrier and electrodes. No additional lossy dielectric material is deposited, nor do organic resist residues contaminate the junction vicinity, because our method allows thorough acid cleaning of the wafer immediately before deposition of the junction metals. The only dielectric seen by the JJ is the low-loss substrate crystal, typically a high resistivity Si or sapphire.²¹ We envisage Josephson junctions that are largely independent of the superconductor, tunneling barrier, deposition techniques, or cleaning methods used. We discuss several implementation possibilities below. An overview of the studied junction types is given in Table I.

The step profile consists of an overhang²³ of height α and an undercut of height β and depth γ [Fig. 1(a)]. In the following stage, the M1/TB1/M2 trilayer is deposited *in situ* on S1 and S2 simultaneously, where M1 (M2) is the top (bottom) junction metal of thickness δ (ϵ), TB1 is the tunnel barrier of negligible thickness, and S1 (S2) is the lower (upper) floor of the patterned substrate. The overhang sidewall is generally also coated with M1, creating a thin parasitic sidewall film (SWF) that may short the junction. The effect is less

TABLE I. An overview of the Josephson junction types investigated.

Junction type (abbrev.)	Exp. Stud.	Typ. Feat. Lim
Step edge insulated (SEI)	✓ ^a	$\geq 1 \mu\text{m}^2$
Cross-step edge insulated ^b (cSEI)	✓ ^c	...
Manhattan trench (MT)	✓ ^a	$\leq 1 \mu\text{m}^2$
Cross trench (cT)	✓ ^a	...
Bridge trench (BT)	... ^d	$\leq 1 \mu\text{m}^2$

^aFabrication and cryogenic characterization.^bThe planarized cross-step edge insulated junction (p-cSEI) is a fabrication variant of the cSEI junction.^cFabrication and room temperature characterization.^dConceptual.

pronounced with anisotropic deposition methods, such as e-beam evaporation or laser ablation, applied at an appropriate deposition angle; however, it is still non-negligible. The purpose of the undercut in the substrate step is to prevent this short by setting $\epsilon < \beta$ and $\gamma > 0.5\epsilon$. TB1 can be formed by deposition of a dielectric or, often, by oxidation of the bottom electrode (BE). M2 can generally be formed by a different technique than M1, e.g., isotropic atomic layer deposition (ALD) or sputtering, provided the vacuum is not broken, to ensure clean interfaces across the junction. If M2 is deposited with an anisotropic method, we find it feasible to deposit at an angle facing the overhang to avoid growth boundaries between the bottom and top M2.

The bottom electrode (BE) and the top electrode (TE) are located on S1 and S2, respectively, and are laterally defined by two consecutive lithography steps with organic or hard masks and dry or wet etching. The junction size is determined by the TE lithography resolution and alignment precision (Fig. 1).

The *cross step edge insulated* (cSEI) junction removes the SEI junction alignment accuracy limitation using a second step edge, parallel to the first step, to define a BE confining trench. TE is lithographically patterned in a direction perpendicular to the trench, with a large alignment margin. The junction lateral dimension is defined by the intersection of the trench and the TE line, and is only limited by the lithography resolution. The fabrication sequence is similar to the SEI junction (Fig. 2). In the case of consecutive layer deposition, M2 fully protects M1 and TB1 from potential shorts and aggressive etching or cleaning steps. Deposition onto S1 at the bottom of a narrow, deep trench requires a deposition angle close to normal incidence, potentially causing enhanced SWF formation and irregularities at the boundary where M2 grown on S1 meets M2 grown on S2.

A planarized variation of the cSEI junction (*p-cSEI* junction) resolves the latter problem by adding a planarization step^{34,25} [e.g., chemical-mechanical polishing (CMP)] after the trilayer deposition, followed by ion-mill cleaning and an additional M2b deposition [Fig. 2(a), steps I-II-IIIb-IVb-Vb]. After planarization, subsequent steps, e.g., to form interconnects, are simpler because there are no large height differences to consider.

The *Manhattan Trench* (MT) junction³ is formed entirely on S1 at the intersection of two perpendicular trenches. First, M1 is deposited at a steep angle (30° – 60°), which exposes S1 of the first trench

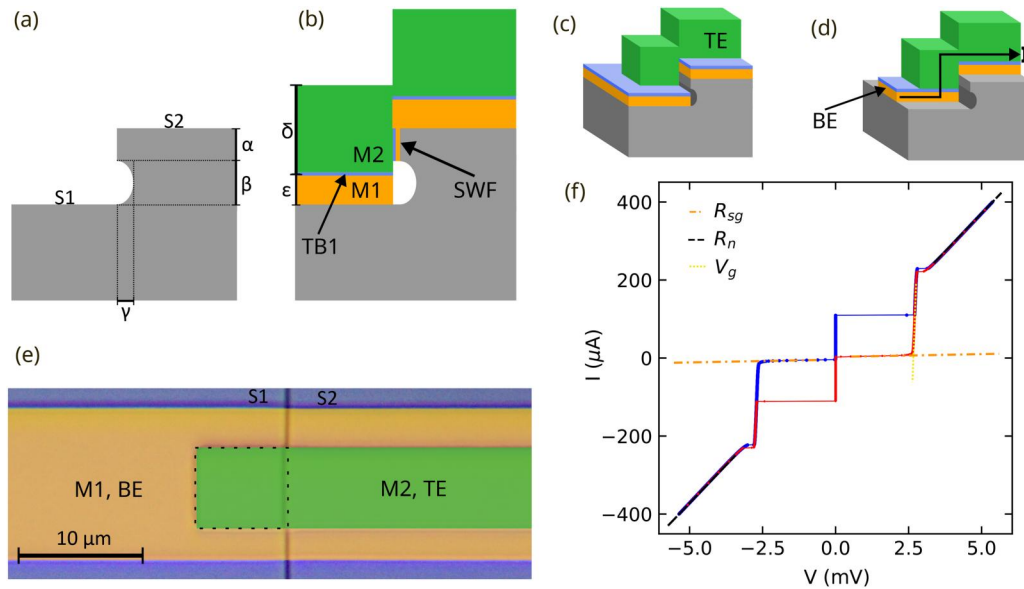


FIG. 1. Step edge insulated tunnel junction. (a) Substrate cross section after forming the step with an undercut. (b) Trilayer deposition. To ensure M2 continuity across the step, we require $\delta > \alpha + \beta - \epsilon$. (c) The top electrode (TE) is formed by lithography. (d) The bottom electrode (BE) is formed by lithography. The current direction is shown by the black arrow. (e) False-color optical image of an Nb/AlO_x/Nb SEI junction. The junction area is enclosed by the dashed-line rectangle. (f) A typical I–V characterization of a junction with nominal area $A = 100 \mu\text{m}^2$ at 4.2 K indicates an underdamped junction with a linear dissipative branch for bias current above $I_c = 110 \mu\text{A}$. The return path shows a pronounced hysteresis with a low retrapping current I_r . A gap voltage of $V_g = 2\Delta/e = 2.78 \text{ mV}$ was extracted at the interpolation of the yellow dotted line with the x-axis.²² The line is a linear fit between the 10-th and 50-th percentile of current in the $[2.3, 5]$ mV window. Normal (subgap) resistance of $R_n = 12.7 \pm 0.1 \Omega$ ($R_{sg} \approx 700 \Omega$) was extracted by fitting the black (orange) dashed (dashed dotted) line above 3.5 mV (between 0.9 and 2.2 mV) and measuring the inverse slope $(I(2 \text{ mV})/2 \text{ mV})$. The knee adjacent to the normal resistance branch is associated with the proximity effect of Nb on the not fully oxidized Al.²²

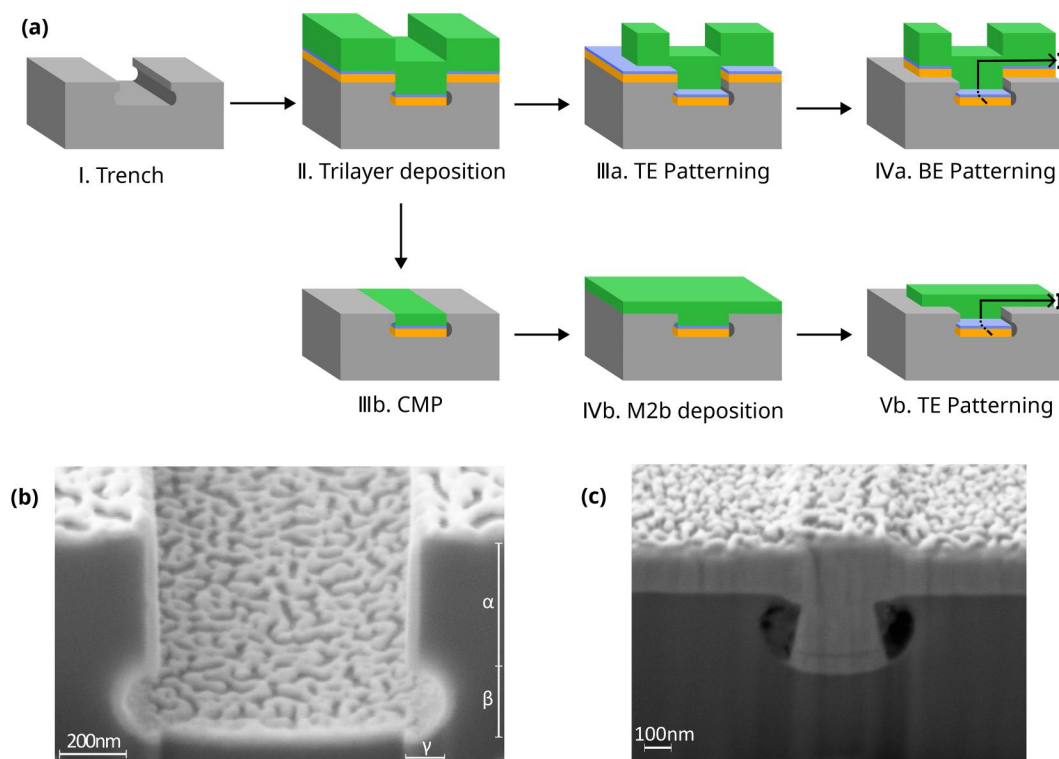


FIG. 2. (a) cSEI (steps I-II-IIIa-IVa) and p-cSEI (steps I-II-IIIb-IVb-Vb) junctions. (b) Cross-sectional scanning electron microscope (SEM) image of a trench, taken at 55° tilt after a 4 nm Au sputter and a focused ion beam (FIB) cut. The 800 nm wide trench is etched into a silicon substrate using the Bosch undercut process. The undercut dimensions are in good agreement with the design parameters of $\alpha = 450$ nm, $\beta = 250$ nm, and $\gamma = 100$ nm. (c) p-cSEI Nb/AIO_x/Nb/Nb junction cross-sectional SEM image.

(T1) but keeps S1 of the second trench (T2) in the shade of the T2 steps, forming the BE in T1. Before M2 deposition, the sample azimuth is rotated by 90° so that S1 of the second trench is exposed while the BE is shaded by the T1 steps; the TE is formed in T2. The junction does not touch any walls on which SWF could form ($\delta + \epsilon < \beta$, Fig. 3). The trenches can be deeper than in the SEI and the cSEI junctions because the TE does not climb from S1 to S2. An optional planarization step removes the excess trilayer from S2. Outside the trenches, the trilayer on S1 acts as an effective single superconducting layer due to unavoidable pinholes in TB1 that electrically short M1 and M2. As a result, typical single-layer microwave and DC readout and control circuitry can be defined by the same lithography step that formed the junction trenches. In a generalized junction geometry, the S1/M1/TB1/M2 patch is wider than the BE and TE trenches that lead to it, allowing arbitrarily large junctions.²⁶

We propose an additional closely related junction geometry, the *bridge trench*, where a single trench is interrupted by a short break. The undercuts of the two segments join, creating an S1 tunnel under an S2 bridge, similar to the Dolan-bridge.⁴ Adjusting the bridge shadow between M1 and M2 depositions allows the formation of a junction on S1, while all material on S2 is sacrificial and may be removed in an optional planarization step. The effective junction dimensions depend on the deposition angles.

In the *cross-trench* (cT) junction, the wafer is planarized down below S2 after M1 deposition (Fig. 4). Exposing M1 to an aggressive treatment stands in stark contrast to the other trilayer deposition

methods described above and may affect the junction quality. Yet, the simplicity of trench formation without an undercut and of all subsequent fabrication steps may outweigh this disadvantage. The junction size is limited only by lithography resolution. Unlike the traditional cross-junctions,^{27,28} the BE trench walls leave only the top BE surface exposed, allowing non-isotropic TB1 and M2 deposition. M1 and M2 can be conveniently deposited in separate tools.

Quantum circuits require low-microwave-loss wafers, typically sapphire or high-resistance silicon.²¹ The step-with-undercut profile required for our junctions could possibly be realized in the former using wet etching.²⁹ We instead use the Bosch process on silicon^{30,31} to pattern the latter with high precision and reproducibility [Fig. 2(b)].

We measured the surface roughness of S1 and S2 using an atomic force microscope. For a 250 nm-deep trench, the average S1 surface roughness is $S_a \approx 1.2$ nm, compared with $S_a \approx 0.8$ nm for S2. Although higher, this value is still acceptable for typical thin films of 20–200 nm thickness. Further surface treatment, e.g., wet chemical etching, may reduce the roughness if required. To determine the influence of Si surface roughness on the superconducting film quality, we deposited 75 nm Nb in a home-built DC magnetron sputtering system with a base pressure of $\sim 1 \times 10^{-8}$ mbar. Cryogenic measurements showed a critical temperature $T_c = 9.0$ K for films on S1, similar to the T_c measured for films deposited on pristine substrates.

To investigate the microwave properties of superconducting quantum circuits realized with the CMP technique, we measured

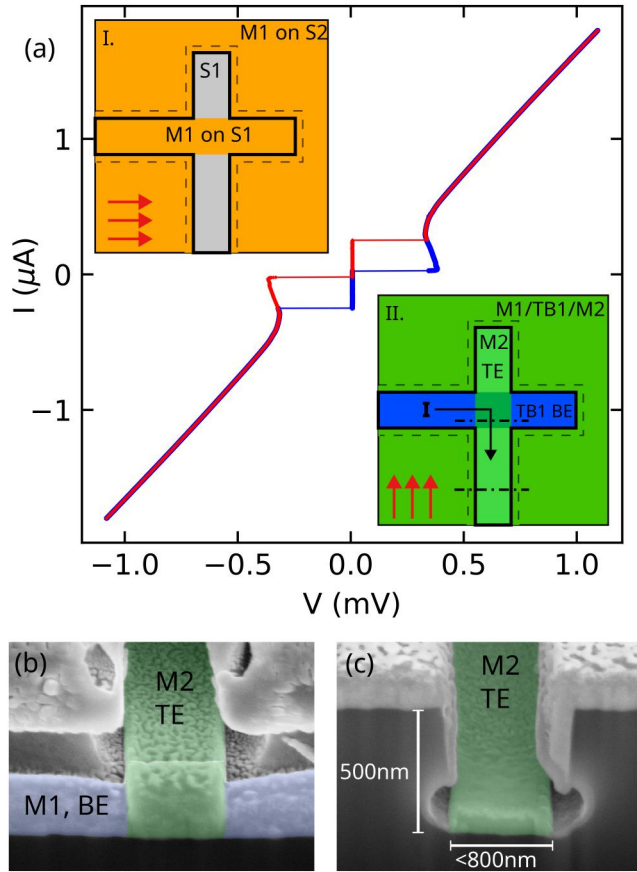


FIG. 3. (a) I-V characterization of an Al/AIO_x/Al planarized Manhattan Trench junction with area $A = 0.25 \mu\text{m}^2$ at 15 mK. Inset I. Top-view schematic after etching two perpendicular trenches in the substrate and depositing M1 along the red arrows. The cross shape of the trenches' top (in the S2 plane) is depicted with a solid black line. Around it, the dashed gray line depicts the undercut (in the S1 plane). The walls of the north-south trench cast a shadow on the S1 floor of the trench and protect it from deposition. Inset II. TB1 deposition followed by M2 deposition along the red arrows. Now, the east-west trench floor is in the shade. The junction is formed in the overlap of the two trenches. The black arrow illustrates the electrical current direction. (b) and (c) False-color SEM image of the FIB-cut Nb/AIO_x/Nb cross-sectional view before planarization. The location is indicated by the top (bottom) dash-dotted line in (a) II.

niobium $\lambda/4$ coplanar waveguide (CPW) resonators at millikelvin temperatures. The measured resonance frequency was approximately 7 GHz, and the internal quality factor exceeded 3×10^5 . The most likely sources of loss are the native niobium oxide layer of M1 and the roughness of the argon-milled S1. To test the M1-M2 interface, we introduce a gap in the BE trench, fill both segments with M1, planarize, and bridge the gap with M2 (Fig. 5). The surface of the first niobium film is ion milled *in situ* before the second film is deposited. The two-layer resonators show no degradation in quality factor compared with the single-layer resonators.

A set of SEI junctions of various sizes with different oxidation parameters but a common 3D geometry $(\alpha, \beta, \gamma) = (100, 150, 50)$ nm were characterized at room and cryogenic temperatures [data taken at 4.2 K for chips from wafer I and at ~ 2.5 K for chips from wafer II

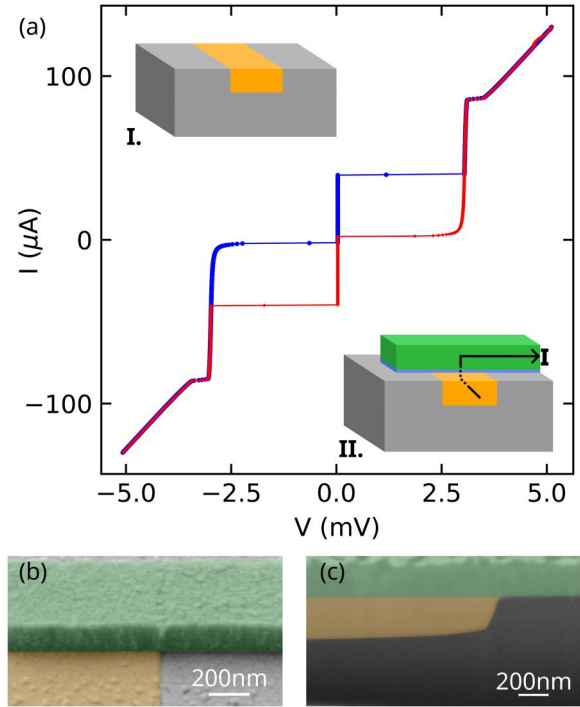


FIG. 4. (a) I-V characteristic of an Nb cT junction with $A = 16 \mu\text{m}^2$ at 50 mK. Inset I. Sample state after (1) no-undercut trench etch ($\gamma \leq 0$), (2) M1 deposition ($\epsilon > \alpha + \beta$), and (3) planarization. BE is formed in the trench. Inset II Sample state after (4) hydrofluoric acid dip and ion-mill cleaning to remove the native oxide, (5) TB1 and M2 deposition, (6) TE patterning, and (7) TB1 patterning (optional, possibly with the same mask as the previous step). (b) False-color SEM image of Nb cT junction. (c) Cross-sectional SEM image of Nb cT junction.

and III, as depicted in Fig. 1(f)). The junctions are nominally square with an area of L_{design}^2 . The critical current was extracted with the help of the Ambegaokar-Baratoff formula³⁵ $I_c = R_n^{-1} (\pi V_g / 4) \tanh(V_g e / 4 k_B T)$. We model the critical current density J_c of a junction as

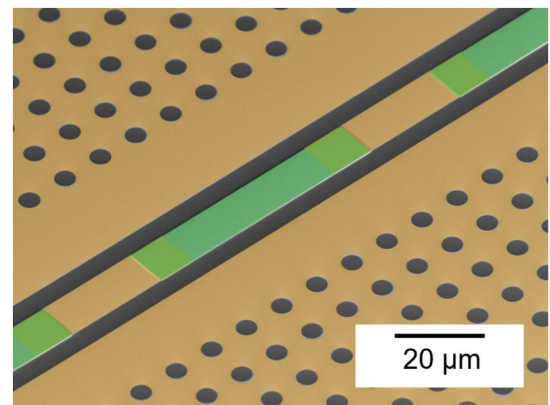


FIG. 5. False-color SEM image of a two-layer niobium CPW resonator structure. Niobium embedded in the substrate is shown in orange, and the second niobium layer in green.

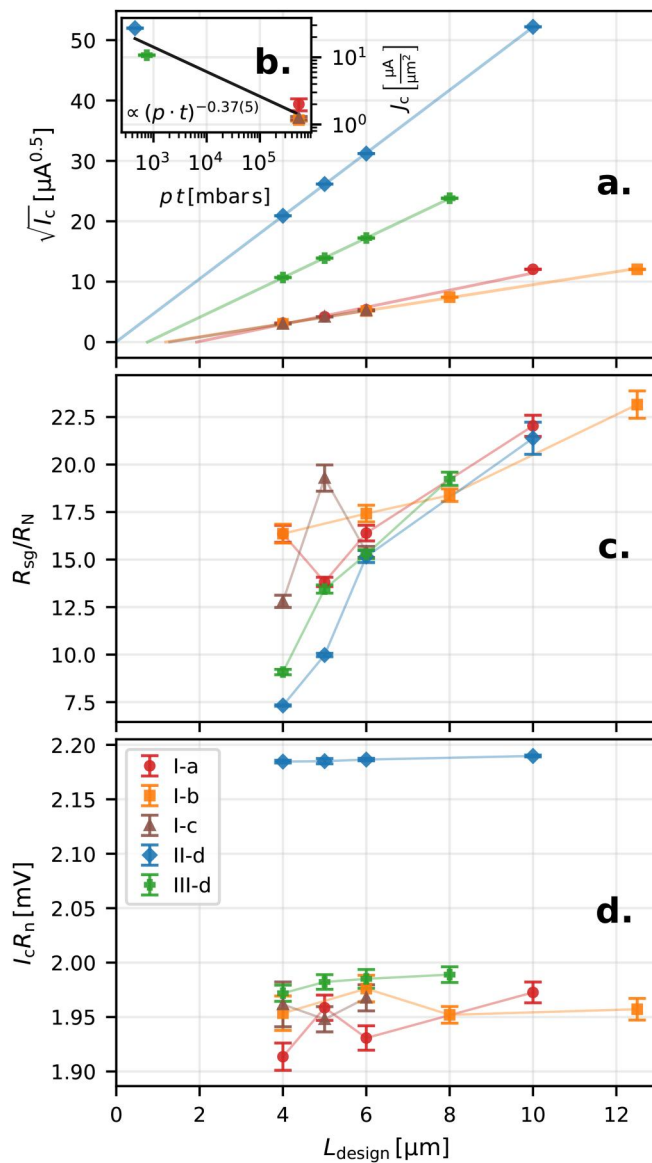


FIG. 6. (a) Roman numerals I–III indicate different wafers, while letters a–d indicate the test-chip position on the wafer. I_c modeled by Eq. (1) using the fit parameters u and J_c . For readability, the vertical axis shows $\sqrt{I_{\text{sw}}}$ (instead of I_{sw}): The square-root scaling compresses the dynamic range so large-current junctions do not dominate the plot. Chip II-d, with the highest J_c , presented a self-heating signature—negative slope near V_g . For this chip, only V_g was taken as the maximum voltage in the $[0, 100]$ μA window. (b) The dependence of the critical current density on the product of oxygen partial pressure p and oxidation time t^{32} is fitted by a power law. (c) The leakage ratio R_{sg}/R_n is improved with junction size. (d) The characteristic voltage $I_c R_n$. Values are on par with other Nb/AlO_x/Nb junctions.^{6,12,33,34}

$$J_c = I_c / L_{\text{eff}}^2, \quad (1)$$

where $L_{\text{eff}} = L_{\text{design}} - 2u$ is the effective length and u is the undercut parameter. A linear fit of $\sqrt{I_c}(L_{\text{design}})$ hence allows to identify $\sqrt{J_c}$ as the inclination of the line, and $2u$ as the interception with the x-axis (Fig. 6).

Two size-independent junction figures of merit are the characteristic voltage $V_c \equiv I_c R_n$ and the leakage ratio R_{sg}/R_n . High V_c indicates that the junction approaches the Ambegaokar–Baratoff tunneling limit, whereas barrier defects/excess conductance typically reduce it. Likewise, large R_{sg}/R_n implies suppressed subgap quasiparticle transport (lower intrinsic dissipation).³⁶ In our case, R_{sg}/R_n increased with junction size, suggesting that junction edges primarily contribute to the leakage.

In conclusion, we have established a substrate-profiling technique to fabricate oxide-free and resist-residue-free underdamped Josephson junctions of various sizes and geometries. The current–voltage characteristics show pronounced hysteresis, indicating a high junction quality. The technique enables the fabrication of quantum circuits across a wide range of materials and deposition conditions.

See the [supplementary material](#) for additional information, including magnetic field-dependent (Fraunhofer pattern) and temperature-dependent measurements, fabrication details, and an evaluation of junction critical currents.

We thank Silvia Diewald and Patrice Brenner for their help with lithography and FIB imaging. This work was supported by funding from the European Research Council (ERC) under the European Union’s Horizon 2020 research and innovation program (project Milli-Q, Grant Agreement No. 101054327). This research was also supported by the Fraunhofer QNC space project CohereMP and the German Federal Ministry of Education and Research under the Research Program Quantum Systems, through the projects GeQCoS (No. FZK13N15691), qBriqs (No. FZK13N15950), and Qrious (No. FZK13N17125).

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

U. Strobel: Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Validation (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **L. Radtke:** Conceptualization (equal); Investigation (equal); Methodology (equal); Writing – review & editing (equal). **L. Kamps:** Conceptualization (equal); Investigation (equal); Methodology (equal). **J. N. Voss:** Conceptualization (equal); Investigation (equal); Methodology (equal); Supervision (equal); Writing – review & editing (equal). **J. Lisenfeld:** Conceptualization (equal); Formal analysis (equal); Funding acquisition (equal); Investigation (equal); Methodology (equal); Project administration (equal); Supervision (equal); Writing – review & editing (equal). **J. Lenschen:** Data curation (equal); Investigation (equal); Validation (equal). **J. N. Kämmerer:** Data curation (equal); Investigation (equal); Validation (equal). **J. Luo-Hoffman:** Investigation (equal); Methodology (equal); Supervision (equal); Writing – review & editing (equal). **D. Reuter:** Investigation (equal); Methodology (equal); Supervision (equal); Writing – review & editing (equal). **S. Masis:** Data curation (equal); Formal analysis (equal); Methodology (equal); Project administration

(equal); Supervision (equal); Writing – original draft (equal); Writing – review & editing (equal). **A. V. Ustinov:** Conceptualization (equal); Funding acquisition (equal); Project administration (equal); Supervision (equal); Writing – review & editing (equal). **H. Rotzinger:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Funding acquisition (equal); Investigation (equal); Methodology (equal); Project administration (equal); Supervision (equal); Validation (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding authors upon reasonable request.

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