

Lightweight Single-Phase Dynamic Load Model for Real-Time Simulation

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ABSTRACT The real-time simulation of large-scale power grids with dynamic loads can be challenging due to the presence of computationally heavy blocks such as Root-Mean-Square (RMS), variable frequency mean, Phase-Locked-Loop (PLL), synchronous frame transformation ($abc - dq0$), and conversion blocks (polar-to-complex). This paper proposes an alternative method to implement an equivalent computationally efficient single-phase dynamic load model based on the concept of instantaneous p-q theory to simulate large-scale unbalanced power grids and enhance real-time performance. A single-phase instantaneous p-q theory-based load (PQL) model has been developed as an alternative to the existing single-phase Simulink dynamic load (SDL) model in MATLAB/Simulink to demonstrate the accuracy and computational efficiency of the proposed approach. The two dynamic loads have been compared in terms of their behavior during steady-state and transient simulations and the computational demand in a real-time environment on the standard test feeders.

INDEX TERMS Dynamic load, instantaneous p-q theory, load modeling, real-time simulation.

I. INTRODUCTION

In a digital real-time simulation environment, accurate, fast, scalable, and flexible models are required to understand the power system dynamics for Hardware-in-the-Loop (HIL) and Power Hardware-in-the-Loop (PHIL) studies. These testing techniques have attracted considerable attention in the last years, both at power electronics and power system level [1], [2], [3], [4]. In a real-time simulation, the equations of power networks should be solved within a fixed time-step to avoid overruns. The presence of overruns in a real-time simulation will cause a decline in real-time capabilities since it can be solved only by either increasing the fixed time-step or simplifying the models [5].

However, increasing the time-step means that the simulation may not be able to capture fast system dynamics accurately [6], making the choice of time-step challenging [7]. Indeed, the ideal solution for real-time simulations for HIL and PHIL studies is to find the optimal trade-off between the model complexity and fixed time-step size so that all system

dynamics can be captured. Therefore, the best way to solve the equations without overruns in a fixed time-step is to reduce the computational complexity of the system models without losing accuracy and without varying the behaviour of the modelled system.

This paper focuses on reducing the complexity of an electrical grid model for real-time simulation by reducing the computational burden of the load models, which play a vital role in the dynamics of electrical systems. This paper addresses the issue of making the single-phase dynamic load models computationally efficient, targeting a reduction of the computation time. Particular attention needs to be given to the systems' response during disturbances (e.g., during transients) as it may lead to inaccurate prediction of system stability [8], [9], [10].

The existing methodologies used for load modeling are component-based and measurement-based approaches. Most of the software available for power system simulation uses a measurement-based approach [11], whereas the exponential

dynamic model or induction motor is used to represent the dynamics of the load [12]. These models have been tested and are accepted worldwide for performing power system transient studies. Furthermore, these dynamic load models play a vital role in emulating the behaviour of distributed active resources [13] and complex power system grids [14] in a real-time simulation for HIL and PHIL testing.

Among various simulation software available in the market to perform power system studies, MATLAB gives the possibility to extend its application from offline to real-time simulations. The single-phase SDL model developed in the library of MATLAB/Simulink is an exponential dynamic load model that can mimic the behaviour of a power component by tracking a time-varying power profile.

The main drawback of using the SDL model is the continuous access to the computer local memory, for example the variable frequency mean block, which requires an array of data to compute the mean value. In addition, the model employs iterative non-linear loops in the Phase-Locked-Loop (PLL) and polar-to-complex conversion blocks. These calculations and memory access significantly affect computation time during the real-time simulation, causing overruns and limiting the extent and complexity of the real-time simulation at a specific fixed time-step.

To overcome the computational burden problem and the limitation in the prior work of the authors [15], this paper proposes a novel single-phase dynamic load model for digital real-time simulations of power systems, based on instantaneous p-q theory. This work identifies and eliminates the compute-intensive blocks present in the SDL model by substituting them with lighter algebraic equations. The goal is to develop a single-phase dynamic load model that is computationally lighter and provides large-scale power grid simulation capabilities without losing accuracy with respect to the SDL model. By connecting multiple single-phase PQL models, its application can also be extended to model balanced and unbalanced three-phase loads. In this work, the single-phase PQL model is modelled and validated for both steady-state and transient-state analysis.

The contribution of this work on load modeling can be summarized as follows:

- Introduction and mathematical explanation of the proposed single-phase PQL model and its implementation with frequency support capability in digital real-time simulation
- Comparison of the accuracy of the PQL model with the SDL model by performing steady-state and transient-state analysis
- Computational comparison of the PQL load model against the Simulink static load (SSL), consisting of a static impedance, and SDL blocks

The paper is organized as follows. Section II deals with the current state of the art and describes the single-phase SDL and its implementation. Section III introduces the concept of instantaneous p-q theory, single-phase PQL model implementation, and provides a comparison in terms of computational

complexity with the SDL model. In Section IV, the proposed PQL model is validated using the standard IEEE test feeders under different scenarios, and the results are compared against the SDL model. Section V assesses and compares the computational performance of the PQL model with SSL and SDL model in a real-time environment. Finally, Section VI concludes the paper.

II. STATE OF THE ART

Load modeling is performed using component-based and measurement-based approaches, and they are further classified into static and dynamic load models. The relevant information about the load behavior, such as the active and reactive power demand response to variations in voltage or system frequency, is contained in the load model. The main difference between the static loads and the dynamic loads is their transient behaviour capability. The static loads respond instantaneously to voltage or frequency variations and are time-independent, whereas the dynamic loads are characterized by a time-dependent response to voltage or frequency deviations. The second-order polynomial, exponential, and linear loads are frequently used among the existing static loads. The induction motor and dynamic exponential load models are the most commonly used dynamic loads. Sometimes, composite load models, such as ZIP-motor model, are used for modeling aggregate load models [16].

To develop and simulate these loads, there are many power system software platforms, commercially available, like PSCAD, PSSe, EMTP-RV, DigSILENT, Modelica, MATLAB/Simulink, PowerFactory, etc., which allow the implementation of mathematical models of dynamic loads and perform simulations for power system studies. However, only a few platforms provide integration with real-time simulators. Without losing in generality, this work will assume the use of MATLAB/Simulink and OPAL-RT as development platform and digital real-time simulator, respectively. However, the proposed PQL model can be applied to any simulation platform, showing similar performances to the one demonstrated in this work.

An exponential single-phase dynamic load model, which is mathematically a special case of generalized polynomial single-term generalized polynomial form (single-term ZIP load), is derived from the three-phase dynamic load model implemented in the MATLAB/Simulink library and can be used to perform power system studies and real-time simulations. As can be seen in Fig. 1, the SDL model is characterized by a few computational burden blocks such as PLL, RMS, mean, and conversion blocks. Analogously to the three-phase dynamic load model, the power consumption of the single-phase exponential dynamic load model also depends on voltage, as mentioned in (1).

$$\begin{aligned} P &= P_0 \left(\frac{V}{V_0} \right)^{n_p} \left(\frac{1 + T_{p1}}{1 + T_{p2}} \right) \\ Q &= Q_0 \left(\frac{V}{V_0} \right)^{n_q} \left(\frac{1 + T_{q1}}{1 + T_{q2}} \right) \end{aligned} \quad (1)$$

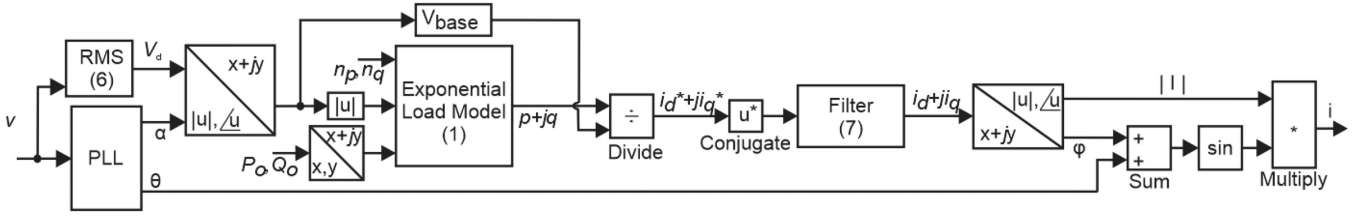


FIGURE 1. Simulink dynamic load.

The active power (P) and reactive power (Q) are dependent on the positive sequence of the measured voltage (V), and the exponential values n_p and n_q control the nature of the load (i.e. exponents 0, 1, and 2 represent the characteristics of constant power, constant current, and constant impedance loads, respectively). The nominal active and reactive power at the positive sequence reference voltage V_0 are given by P_0 and Q_0 . The dynamics of the active power are controlled by the time constants $[T_{p1} \ T_{p2}]$ and the dynamics of the reactive power are controlled by the time constant $[T_{q1} \ T_{q2}]$.

A. IMPLEMENTATION OF SINGLE-PHASE SDL MODEL

In this section, the algorithm implementation of the SDL model (Fig. 1) to generate the reference currents as exponential load model is explained in detail. In the SDL model, the phase voltage is measured in per unit (pu) at the load connection point. For representation simplicity, the time dependency of electric variables has not been represented in the equation notation. The measured phase voltage v is given by (2), where V_m is peak amplitude of the input signal, ω is the angular frequency in rad , and ϕ is the phase angle of the input signal in rad . The measured signal is fed to a RMS block to obtain the magnitude of the signal and a PLL block to generate the phase angle (α) and angular position (θ) in rad .

$$v = V_m \sin(\omega t + \phi) \quad (2)$$

The PLL has no Clarke's transformation block to convert the voltage signal into an $abc - dq0$ frame due to the single-phase system and hence, v is treated as v_d . Internally, the PLL uses an adaptive filter and an adaptive mean block to obtain the phase angle (α). The adaptive frequency block is used to filter out the harmonics of the input signal. The output of the adaptive filter v_f is given by the (3), where, v is the measured phase voltage, $\omega_n = 2 * \omega$ is the angular frequency corresponding to the input frequency, ζ is the damping factor, and x is the output of the adaptive filter.

$$v_f = \frac{d^2x}{dt^2} = v\omega_n^2 - 2\zeta\omega_n \frac{dx}{dt} - \omega_n^2 x \quad (3)$$

The filter output is fed through an integrator before feeding as an input to the adaptive mean block. The integrated filter output is fed as an input to generate the angular position θ and also to the adaptive mean block. The angular position θ is obtained by adding the integrated filtered generated output with the integrated angular frequency to get the corrected

angular position θ .

$$\theta = \int_0^t \omega dt + \int_0^t v_f dt \quad (4)$$

The adaptive mean block is used to obtain the smooth and reliable average value of the input signal by calculating the average value of the input signal over a frequency-dependent average window. The average period is determined by the natural frequency provided with a small constant 10^{-6} to prevent division by zero. The output of the adaptive mean block α is given by the (5), where v_f is the input signal to the adaptive mean block, f is the frequency input in Hz , $f_\epsilon = f(t) + 10^{-6}$ is the modified frequency used to avoid division by zero, $T_a = \frac{1}{f_\epsilon}$ is the adaptive average period, and phase angle (α) is the output of the adaptive mean block.

$$\alpha = f_\epsilon \int_{t-T_a}^t v_f dt \quad (5)$$

The measured voltage is passed through an RMS block to get the voltage magnitude V_d using (6), where f is the fundamental frequency, T is time period of the signal given by the reciprocal of fundamental of frequency ($\frac{1}{f}$), and v is the measured phase voltage.

$$V_d = RMS(v) = \sqrt{\frac{1}{T} \int_{t-T}^t v^2 dt} \quad (6)$$

The generated output V_d from the RMS block, and the angle α obtained from the PLL is fed to a polar-to-complex conversion block to generate the voltage signal in the complex form. The magnitude of the complex voltage signal is used in the exponential load model block to mimic the load behaviour, as mentioned in (1). The active and reactive power generated is used in calculating the current $i_d^* + j i_q^*$. The conjugated current is passed through a first-order low-pass filter given by (7) to break the algebraic loop and initialize, where $u(t)$ and $x(t)$ are the current input and output respectively, $\frac{dx(t)}{dt}$ is the rate of change of the output, and τ represents the time constant.

$$\frac{dx(t)}{dt} = \frac{1}{\tau} [u(t) - x(t)] \quad (7)$$

A complex-to-polar conversion block provides magnitude $|I|$ and angle ϕ of the current. The angle ϕ is added with the angular position θ obtained from PLL for synchronization to generate the actual current i given by (8) and fed to a controlled current source to have the characteristics of the load

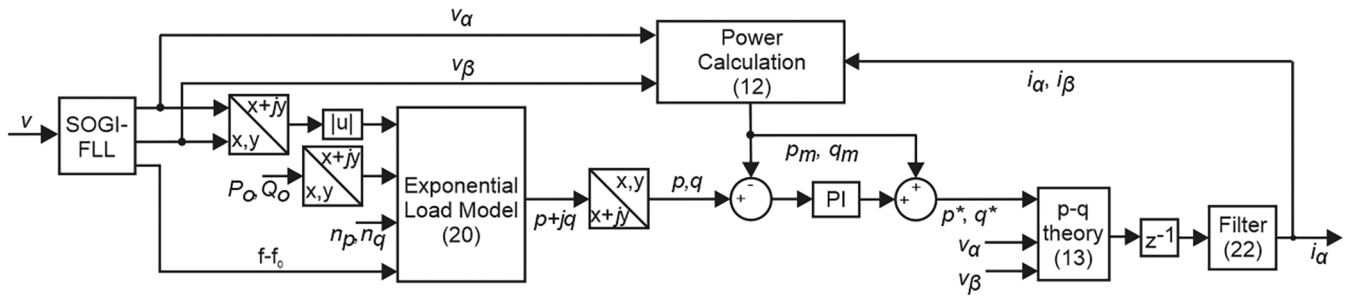


FIGURE 2. p-q theory-based Load.

as shown in Fig. 1.

$$i = I \sin(\theta + \phi) \quad (8)$$

Compiling and simulating the SDL model in a real-time environment leads to high CPU usage due to compute-intensive blocks such as Mean, PLL, and polar-to-complex conversion. Calculating trigonometric functions, managing variable transport delays, and applying transformations can significantly increase CPU usage. This is due to the approximation methods utilized by fixed-time or digital solvers, such as the Taylor series algorithm (9), CORDIC (Coordinate Rotation Digital Computer), or lookup tables [17], [18], [19]. These methods often require more iterations to produce accurate results. Increasing the number of iterations to achieve more accurate results may lead to increased computation and latency [20].

$$\begin{aligned} \sin x &= x - \frac{x^3}{3!} + \frac{x^5}{5!} - \frac{x^7}{7!} + \dots; -\infty < x < \infty \\ \cos x &= 1 - \frac{x^2}{2!} + \frac{x^4}{4!} - \frac{x^6}{6!} + \dots; -\infty < x < \infty \end{aligned} \quad (9)$$

As previously remarked, in a digital real-time environment, the increase in latency and computation leads to overruns and limits the extent of real-time simulations. To overcome these issues on computational burden and allow the simulation of large and complex networks, an instantaneous p-q theory-based approach is proposed and illustrated in the next Section.

III. LOAD MODELING BASED ON INSTANTANEOUS P-Q THEORY

This section explains the mathematical approach behind the proposed single-phase PQL model. The p-q theory is defined as a set of instantaneous power equations expressed in the time domain [21], [22], [23] and was initially developed for three-phase systems and subsequently extended to single-phase ones.

Unlike in three-phase systems, the natural quadrature signals ($\alpha\beta$ coordinates) generated directly using Clarke's transformation, the single-phase p-q theory adopts a pseudo two-phase system concept to ensure that the overall system can be represented in $\alpha\beta$ coordinates (Fig. 2). Here, the single-phase p-q theory initially uses a Second-Order Generalized Integrator - Frequency Locked Loop (SOGI-FLL) with gain normalization to transform the voltage and current in

$\alpha\beta$ coordinates, through which the instantaneous powers are defined. For representation simplicity, the time dependency of electric variables such as current, voltage, frequency, and power has not been represented in the equation notation. The instantaneous voltage and current vectors can be expressed in terms of $\alpha\beta$ axes as (10),

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = V \begin{bmatrix} \sin(\omega t + \phi) \\ -\cos(\omega t + \phi) \end{bmatrix} \quad (10)$$

Hence, the product of voltage vector v and the conjugate of current vector i^* is defined as complex power s , and is valid both during steady-state and transient states:

$$\begin{aligned} s &= v_{\alpha\beta} \cdot i_{\alpha\beta}^* = (v_\alpha + jv_\beta)(i_\alpha - ji_\beta) \\ &= (v_\alpha i_\alpha + v_\beta i_\beta) + j(v_\beta i_\alpha - v_\alpha i_\beta) \end{aligned} \quad (11)$$

Therefore, the instantaneous active power p_m and reactive power q_m are expressed as:

$$\begin{aligned} p_m &= v_\alpha i_\alpha + v_\beta i_\beta \\ q_m &= v_\beta i_\alpha - v_\alpha i_\beta \end{aligned} \quad (12)$$

Using (12), the $\alpha\beta$ currents can be derived as a function of p_m and q_m :

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \frac{1}{v_\alpha^2 + v_\beta^2} \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} p_m \\ q_m \end{bmatrix} \quad (13)$$

By expanding the right-hand part of the (12), we get,

$$\begin{aligned} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} &= \frac{1}{v_\alpha^2 + v_\beta^2} \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} p_m \\ 0 \end{bmatrix} \\ &+ \frac{1}{v_\alpha^2 + v_\beta^2} \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} 0 \\ q_m \end{bmatrix} \\ &= \begin{bmatrix} i_{\alpha p} \\ i_{\beta p} \end{bmatrix} + \begin{bmatrix} i_{\alpha q} \\ i_{\beta q} \end{bmatrix} \end{aligned} \quad (14)$$

The active and reactive components of the instantaneous current on α -axis can be derived from (14) and expressed as:

$$i_{\alpha p} = \frac{v_\alpha}{v_\alpha^2 + v_\beta^2} p_m \quad (15)$$

$$i_{\alpha q} = \frac{v_\beta}{v_\alpha^2 + v_\beta^2} q_m \quad (16)$$

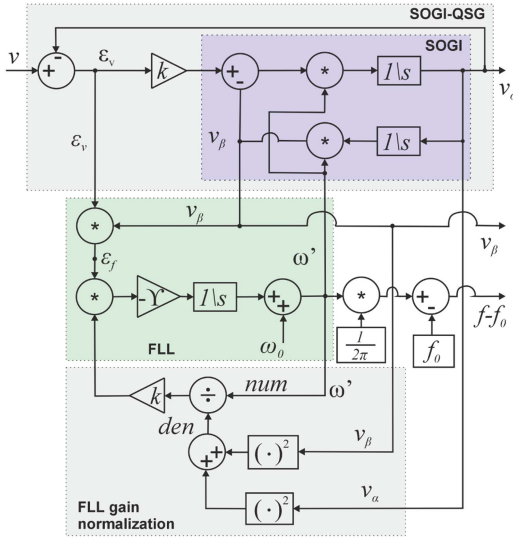


FIGURE 3. Second-Order Generalized Integrator - Frequency Locked Loop (SOGI-FLL) with gain normalization.

Similarly, the active and the reactive component of the instantaneous current on β -axis can be expressed as:

$$i_{\beta p} = \frac{v_{\beta}}{v_{\alpha}^2 + v_{\beta}^2} p_m \quad (17)$$

$$i_{\beta q} = \frac{-v_{\alpha}}{v_{\alpha}^2 + v_{\beta}^2} q_m \quad (18)$$

Unlike using inverse Clarke's transformation in three-phase p-q theory to achieve the actual currents, i_{α} is considered as the actual reference current signal, while i_{β} is a phase-shifted quantity only used for power calculation. So, the generated i_{α} reference current is fed through a current source to reproduce the desired power demand. Similarly, in case of an unbalanced three-phase load, the current on other phases can be generated in similar way and fed to a controlled current source for each phase.

A. IMPLEMENTATION OF SINGLE-PHASE PQL MODEL

The proposed PQL model is structured based on the scheme shown in Fig. 2. Its main functional blocks include the SOGI-FLL, the exponential load model, power calculation, PI controller, and the $p-q$ theory block. The detailed explanation of the PQL scheme is provided in the subsequent description.

The measured voltage v is fed through a SOGI-FLL with gain normalization as shown in Fig. 3, which consists of a SOGI Quadrature Signal Generator (SOGI-QSG), and a FLL with gain normalization to provide grid synchronization. The SOGI-QSG generates the in-quadrature signals v_{α} and v_{β} of equal amplitudes with the center frequency equal to the frequency of the input signal v . The FLL is used to adapt the center frequency of the SOGI-QSG. The behaviour of the FLL can be determined based on the analysis of the error signal ε_v and v_{β} . The frequency error variable ε_f allows a direct FLL

loop to be designed with an integral controller of negative gain $-\gamma$ to make the DC component of ε_f zero by shifting the center frequency ω' of the SOGI-QSG, until it matches the input signal frequency ω .

The nominal value of the grid frequency ω_c is added as a feed-forward to the FLL output to accelerate the initial synchronization process. A feedback-based normalization is done to adjust the FLL gain in runtime by feeding back the estimated grid operating conditions, which ensures constant settle time in grid frequency estimation independent of the characteristics of the input signal. The state-space equations of the SOGI-FLL are expressed as (19), where $x = [x_1 \ x_2]^T$ in (19a) and $y = [v_{\alpha} \ v_{\beta}]^T$ in (19b) are the SOGI-QSG states and output vectors respectively, and (19c) describes the behaviour of the FLL. The complete analysis is discussed in [24], [25]. Even though the measured voltage can be treated as v_{α} , the SOGI-FLL is used to obtain the fictitious value of v_{β} , which is used for power calculation. The SOGI-QSG gain k is set to $\sqrt{2}$, which provides an optimal trade-off between overshooting, settle time, and harmonic rejection. An integral controller with a negative gain of $-\gamma = -46$ [25] can drive the dc component of the frequency error to zero by continuously shifting the SOGI resonance frequency ω' until it matches the input frequency ω [26]. The values of k and γ are also chosen in such a way to have a frequency adaptation settling time of 100 ms and provide a trade-off between the dynamic immunity and responsiveness of the input signal.

$$\dot{x} = \begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} -k\omega' & -\omega'^2 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} k\omega' \\ 0 \end{bmatrix} v \quad (19a)$$

$$y = \begin{bmatrix} v_{\alpha} \\ v_{\beta} \end{bmatrix} = Cx = \begin{bmatrix} 1 & 0 \\ 0 & \omega' \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} \quad (19b)$$

$$\dot{\omega}' = -\gamma x_2 \omega' (v - x_1) \quad (19c)$$

The quadrature signals v_{α} and v_{β} generated by the SOGI-FLL are converted, as shown in Fig. 2, into complex form and fed to the exponential load model block along with the difference in center frequency (f) and nominal frequency (f_0) to have the load characteristics. The exponential load model is similar to the one mentioned in the SDL model but adds a frequency-dependent term, as in (20), where K_{pf} and K_{qf} are the frequency-sensitive gains of active and reactive power, respectively. The frequency-sensitive gain of active power (K_{pf}) and reactive power (K_{qf}) ranges from -6 to 6 [27], [28].

$$P = P_0 \left(\frac{V}{V_0} \right)^{n_p} (1 + K_{pf} \Delta f) \left(\frac{1 + T_{p1}}{1 + T_{p2}} \right)$$

$$Q = Q_0 \left(\frac{V}{V_0} \right)^{n_q} (1 + K_{qf} \Delta f) \left(\frac{1 + T_{q1}}{1 + T_{q2}} \right) \quad (20)$$

The active and reactive powers obtained from the exponential load model are compared with the measured powers (p_m and q_m) (12). The error signals generated after comparison are fed through a PI controller to match the reference powers. The measured powers are added to the PI controller output

TABLE 1 Characteristics Comparison of Different Load Models

Features Load model	Dynamic Model	Constant Power	Constant Current	Constant Impedance	External Power Control	No Need for Synchronization	Frequency Support	Low Computational Burden
SSL	✗	✗	✗	✓	✗	✓	✗	✓
SDL	✓	✓	✓	✓	✓	✗	✗	✗
PQL	✓	✓	✓	✓	✓	✓	✓	✓

SSL - Simulink static load; SDL - Simulink dynamic load; PQL - $p-q$ theory-based load

as a feed-forward variable to accelerate the system response. The corrected active power (p^*), reactive power (q^*), and the generated v_α and v_β are used in the $p-q$ theory block to generate the quadrature currents i_α and i_β using (13). It is also ensured that the term $(v_\alpha^2 + v_\beta^2)$ is minimal given by (21) during near zero denominator conditions to avoid numerical instability, which is validated under short-circuit in [29].

$$if \left(v_\alpha^2 + v_\beta^2 \right) < 10^{-6}, \quad v_\alpha^2 + v_\beta^2 = 10^{-6} \quad (21)$$

The generated quadrature currents are fed through a first-order Butterworth filter ((22)), to have smooth response and reduce discontinuities. The coefficients $b(1)$ and $b(2)$ maintain a DC gain equal to one with a smooth response, $a(1)$ is the normalization constant equal to one, and $a(2)$ represents a cut-off frequency (w_c). The cut-off frequency of 400 Hz is chosen for our studies. The equations to calculate the coefficients $a(2)$, $b(1)$, and $b(2)$ are given by (23).

$$H(z) = \frac{B(z)}{A(z)} = \frac{b(1) + b(2)z^{-1}}{a(1) + a(2)z^{-1}} \quad (22)$$

where,

$$b_1 = b_2 = \frac{1 + a_2}{2} \quad a_2 = -\frac{1 - \frac{w_c T_s}{2}}{1 + \frac{w_c T_s}{2}} \quad (23)$$

The filtered i_α current represents the actual single-phase current i , whereas i_β is fictitious and used only in calculations. The generated phase current i is then fed to a controlled current source to mimic the single-phase load behaviour.

In brief, the operation of the model can be outlined as follows:

- Input acquisition: the instantaneous voltages are processed by the SOGI-FLL to obtain the $\alpha\beta$ components and estimate the frequency deviation ($f - f_0$).
- Load behavior calculation: according to the exponential load (20), the active and reactive power references (P and Q) are evaluated to represent the load characteristics.
- Power estimation: the instantaneous active and reactive powers (p_m , q_m) are computed from $v_{\alpha\beta}$ and $i_{\alpha\beta}^*$ (obtained by the $p-q$ theory block).
- Reference tracking and correction: the measured powers (p_m , q_m) are compared with the reference values. The resulting errors are processed by PI controllers and the corrective actions are added to the measured values to obtain the updated values of active and reactive powers (p^* , q^*).

TABLE 2 Mathematical Operations Required by the Dynamic Load Models

Operations	Simulink dynamic load (SDL)	p-q theory-based load (PQL)
Multiplication	52	55
Integration	6	5
Unit Delay	3	2
Discrete variable transport Delay	2	0
Switch	4	4
Summation/Subtraction	11	16
Trigonometric Calculations	2	0
Polar - Complex conversion	1	0
Complex - Polar conversion	1	0
Complex - Real-Img conversion	3	0
Real-Img to Complex conversion	4	1

- Current calculation: The updated power references p^* , q^* together with the quadrature voltages $v_{\alpha\beta}$ are used in the $p-q$ theory (13) to obtain $i_{\alpha\beta}^*$.
- Output Filtering: the output current components are filtered (22) to smooth their dynamic response before being applied.

All these steps occur simultaneously at each simulation step, ensuring accurate real-time emulation of load behaviour.

The features supported using different load models (SSL, SDL, and PQL) are shown in Table 1. The PQL model has the ability to follow the external active and reactive power profiles, which can represent either a load or generation. The characteristics validation and computational performance of the SSL, SDL, and PQL models are performed using a standard test feeder and are discussed in the upcoming section.

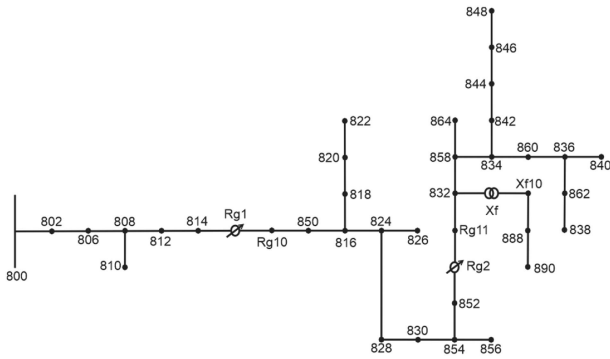
B. COMPARISON OF COMPUTATIONAL COMPLEXITY

In order to investigate the calculation complexity, Table 2 compares the number of mathematical operations required by each of the dynamic load models previously discussed. It can be observed that the SDL model entails more complex mathematical calculations than the PQL model. The SDL model requires multiplications, delays, integrations, discrete variable transport delays, trigonometric calculations, and conversion blocks. Table 3 shows that the PLL alone requires the most complicated operations, making the computation relatively heavy for the SDL model. The Mean and RMS block further increases the overall computational burden of the SDL model.

On the other hand, the PQL model does not require any trigonometric calculation, discrete variable transport delay, nor polar/complex conversion blocks, but it consists mostly of sums, subtractions, multiplications, and unit delays. The

TABLE 3 Mathematical Operations Required by Compute-Intensive Blocks in the Simulink Dynamic Load

Operations	Modules	Phase-Locked-Loop (PLL)	Mean (Variable frequency)	Root Mean Square (RMS)
Multiplication		19	3	4
Integration		4	1	1
Unit Delay		2	0	1
Variable Transport Delay		1	1	1
Switch		0	0	2
Summation/Subtraction		5	2	1
Trigonometric Calculations		1	0	0


FIGURE 4. IEEE-34 node distribution feeder.

reduced number of complex calculations helps lighten the PQL model's computational burden, making it more suitable for digital real-time simulations.

IV. TEST FEEDERS

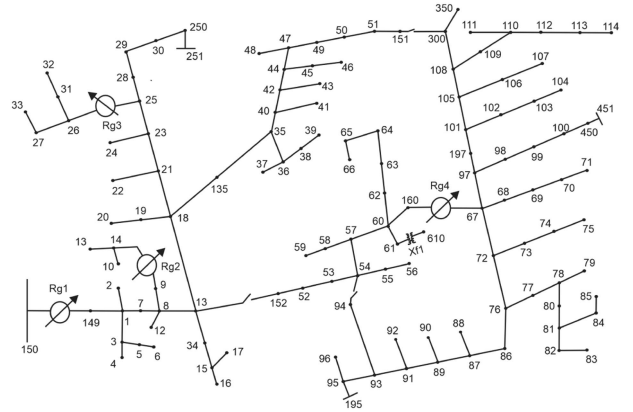
In order to validate the performance of the proposed p-q theory-based model, two standard IEEE benchmark models have been used in this work: the IEEE-34 node test feeder and the IEEE-123 node test feeder. These two networks have been chosen considering the topological features, wide variety of components, size, and complexity as the optimal benchmark for large grids performance and computational analysis. The OPAL-RT ARTEMiS toolbox is used for decoupling the models for real-time testing, considering both accuracy and computational effort of the model.

A. IEEE-34 NODE TEST FEEDER

The IEEE-34 bus network [30], [31] represents a typical rural distribution network with single-phase and three-phase laterals and long feeders which resembles a distribution network. The one-line diagram is as shown in Fig. 4. This distribution network is operated at 24.9 kV and has two voltage regulators, an in-line transformer to step-down the voltage to 4.16 kV, and two shunt capacitor banks. Loads are modelled as three-phase (balanced or unbalanced), single-phase spot or distributed loads.

B. IEEE-123 NODE TEST FEEDER

The IEEE-123 node test feeder [32], [33] is an unbalanced radial distribution system operated at 4.16 kV. The one-line diagram of the distribution network is as shown in Fig. 5.


FIGURE 5. IEEE-123 node distribution feeder.

This distribution network is equipped with four voltage regulators and four shunt capacitor banks. The network also comprises 85 loads, including 80 single-phase loads and 5 three-phase loads. Among the single-phase loads, 56 are modeled as constant power, 13 as constant impedance, and 11 as constant current. One of the single-phase loads is connected across phases *a* and *b*, while the remaining loads are phase-to-neutral connected. The three-phase loads include three wye-connected loads, one for each load model (constant power, constant impedance, and constant current), and two delta-connected loads, modeled as constant-impedance and constant-current, respectively.

V. MODEL VALIDATION

To test the proposed p-q theory-based load model approach, the IEEE-34 node and the IEEE-123 node test feeders have been used. These models have been modelled and simulated in a MATLAB/Simulink v2021b development platform. The model is decoupled using OPAL-RT's ARTEMiS stubline and SSN (State-Space-Nodal) interface modules [34], [35], compiled and executed in real-time with RT-Lab software (RT-LAB v2022.1). The behaviour of the system has been analyzed by modeling the loads with SDL and PQL models.

In the PQL model, the PI controller gains were set to 25 (proportional) and 6000 (integral) for the IEEE-34 node test feeder while 0.15 (proportional) and 250 (integral) for the IEEE-123 node test feeder. Although the detailed tuning procedure is omitted for brevity, the model has proven stable across a wide range of gain values. The selection of suitable parameters was made by simple testing, aiming to achieve a specific load dynamic bandwidth that reflects typical power system response times. This ensures that the PQL model responds quickly enough to track changes in system conditions while avoiding excessive sensitivity to fast transients, thereby providing realistic dynamic behaviour for both steady-state and transient studies. The real-time simulation of the network has been carried out adopting a time-step of 50μs and ARTEMiS SSN solver to ensure deterministic, fixed steps, optimizes for stiffness, enhances numerical stability, and supports parallel computation.

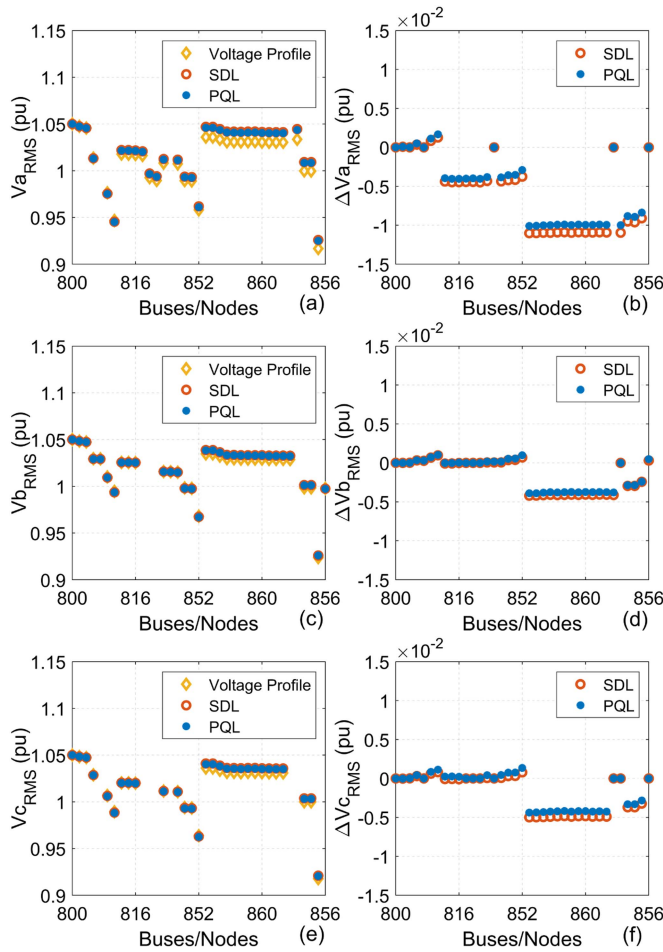


FIGURE 6. RMS voltages (left) and its deviations with respect to IEEE-34 node test feeder voltage profile (right).

A. STEADY-STATE ANALYSIS

1) STEADY-STATE ANALYSIS OF IEEE-34 NODE TEST FEEDER

The PQL model has been tested for steady-state analysis by choosing a nominal voltage and power of 4.16 kV and 500 kVA for the nodes at the secondary of the inline transformer ($Xf10$), 888 and 890. A nominal voltage of 24.9 kV and a nominal power of 5 MVA is used at other nodes. In this test, the model has been tested to achieve the voltage profile results of the IEEE-34 node test feeder [31].

Tests have been performed modeling each load with the PQL and then with the SDL model. The RMS voltages and currents measured at each phase of every node have been collected and compared. In Fig. 6 RMS voltages are compared with the existing load flow results of the IEEE-34 node distribution network. As shown in Fig. 6, the RMS voltage deviations observed for each phase and node have minimal mismatch in both PQL and SDL tests. The deviation of RMS voltages, with respect to the theoretical load flow solution, barely exceeds 1 %, and it is, in general, negligible.

Similarly, the RMS currents of each phase in the network have been compared and Fig. 7(a) shows the comparison of

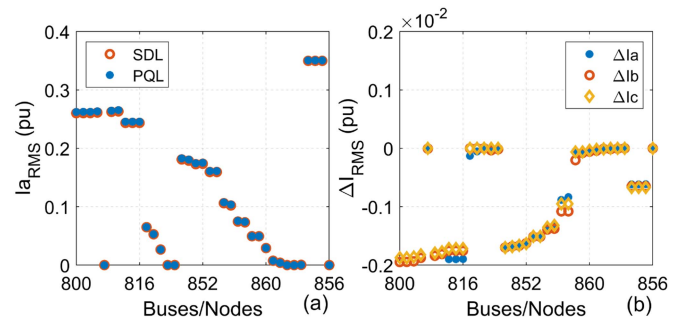


FIGURE 7. Phase-A (a) RMS currents and (b) deviation of currents in each phase with respect to Simulink dynamic load on IEEE-34 node test feeder.

TABLE 4 Mean Absolute Error (MAE) and Root Mean Square Error (RMSE) of the Steady-State RMS Voltages and Compared to the Reference Values (p.u.) on IEEE-34 Node Test Feeder

		V_a	V_b	V_c	$\times 10^{-3}$
MAE	SDL	5.96	1.79	1.97	
	PQL	5.43	1.70	1.82	
RMSE	SDL	7.41	2.58	2.98	
	PQL	6.75	2.39	2.62	

TABLE 5 Mean Absolute Error (MAE) and Root-Mean-Square Error (RMSE) of the Steady-State RMS Current Adopting PQL Model Compared to SDL Model (p.u.) on IEEE-34 Node Test Feeder

		I_a	I_b	I_c	$\times 10^{-3}$
MAE		0.94	0.91	0.88	
RMSE		1.27	1.21	1.18	

Phase-A RMS currents at different nodes. Similarly to the voltage profiles, the RMS currents with the PQL model show no deviation from the SDL model behaviour. The deviation of RMS currents with respect to the theoretical solution, shown in Fig. 7(b), is negligible since it is always below 0.2 %.

In order to provide a more in-depth comparison between the PQL and SDL models, the MAE and RMSE error indices were calculated considering the steady-state RMS voltages and currents at the various nodes of the network under test.

For the voltages, the MAE and RMSE indices were computed with respect to the RMS reference values of each network node. For the currents, since no reference values were available, the indices were calculated as the deviation between the values obtained using the proposed PQL model and those from the SDL model. From the results reported in Tables 4 and 5, both models produce extremely accurate results, in the order of thousandths of p.u. However, even if only by a small margin, the steady-state RMS voltages obtained with the proposed PQL model deviate less from the reference values than those obtained with the SDL model, demonstrating a higher level of accuracy.

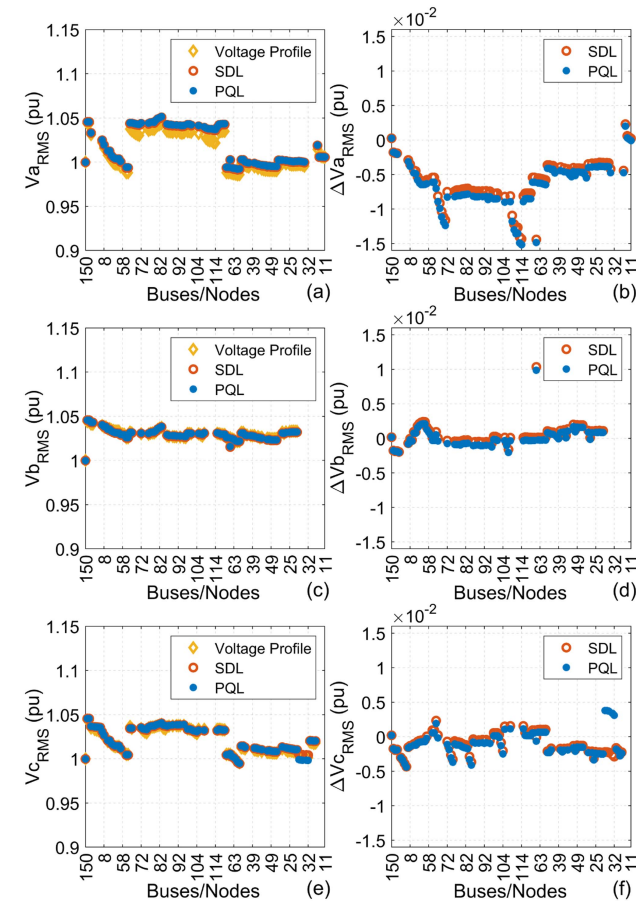


FIGURE 8. RMS voltages (left) and its deviations with respect to IEEE-123 node test feeder voltage profile (right).

2) STEADY-STATE ANALYSIS OF IEEE-123 NODE TEST FEEDER

As in the previous case study, even the IEEE-123 node test feeder was modeled using both the proposed PQL model and the SDL model.

Fig. 8 compares the steady-state RMS voltages obtained with the PQL and SDL models against the reference load flow solution of the IEEE 123-node test feeder. Both the PQL and SDL models exhibit excellent agreement with the reference values, with only minor discrepancies observed across the network. The RMS voltage deviations generally remain below 2 %, indicating negligible errors. The largest deviations are observed in Phase A, reaching a maximum of 15×10^{-3} p.u., whereas the deviations in Phase-B and Phase-C remain below 5×10^{-3} p.u., except at Bus 610 (located downstream of transformer XF1) in Phase-B, where the deviation reaches 10×10^{-3} p.u. Since no load is connected at this node, this discrepancy is likely related to the modeling of transformer XF1, which results in a slightly different voltage profile with respect to the reference solution. A noticeable difference between the SDL and PQL voltage profiles in Phase-C is observed at the buses downstream of voltage regulator RG3, which is attributed to the different tap positions selected by the automatic voltage regulator.

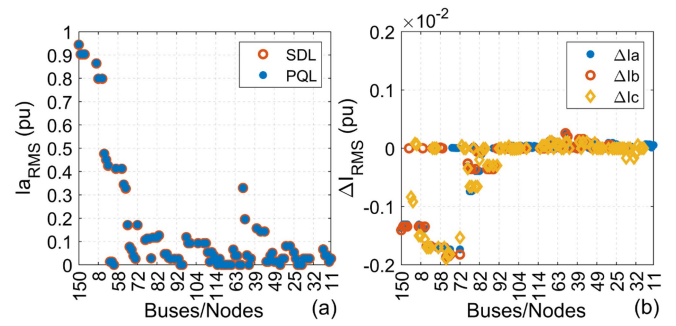


FIGURE 9. Phase-A (a) RMS currents and (b) deviation of currents in each phase with respect to Simulink dynamic load on IEEE-123 node test feeder.

TABLE 6 Mean Absolute Error (MAE) and Root Mean Square Error (RMSE) of the Steady-State RMS Voltages Compared With the Reference Values (p.u.) on IEEE-123 Node Test Feeder

		V_a	V_b	V_c	$\times 10^{-3}$
MAE	SDL	4.44	0.59	1.06	
	PQL	4.88	0.61	1.18	
RMSE	SDL	5.76	1.24	1.47	
	PQL	6.29	1.18	1.66	

TABLE 7 Mean Absolute Error (MAE) and Root-Mean-Square Error (RMSE) of the Steady-State RMS Current Adopting PQL Model Compared to SDL Model (p.u.) on IEEE-123 Node Test Feeder

		I_a	I_b	I_c	$\times 10^{-3}$
MAE		0.24	0.23	0.29	
RMSE		0.57	0.57	0.68	

A similar comparison has been carried out for the steady-state RMS currents. Fig. 9(a) reports the Phase-A RMS currents obtained with the proposed models and the reference solution. As observed for the voltage profiles, the RMS currents obtained with the PQL model closely match those of the SDL model. The current deviations between the load models, reported in Fig. 9(b), are consistently below 0.2 %.

For this test case, the MAE and RMSE error indices were also evaluated, and the corresponding results are reported in Tables 6 and 7, respectively. As in the previous case study, both models exhibit excellent accuracy, with error indices on the order of thousandths of p.u. Unlike the previous test case, the SDL model yields slightly lower MAE and RMSE values than the proposed PQL model even if the difference is negligible.

B. TRANSIENT ANALYSIS

The performance of the PQL model has been validated by performing a transient analysis, considering voltage, frequency, and active/reactive power changes in the IEEE-34 node distribution feeder. The transient study on the IEEE-34 node distribution network has been performed considering

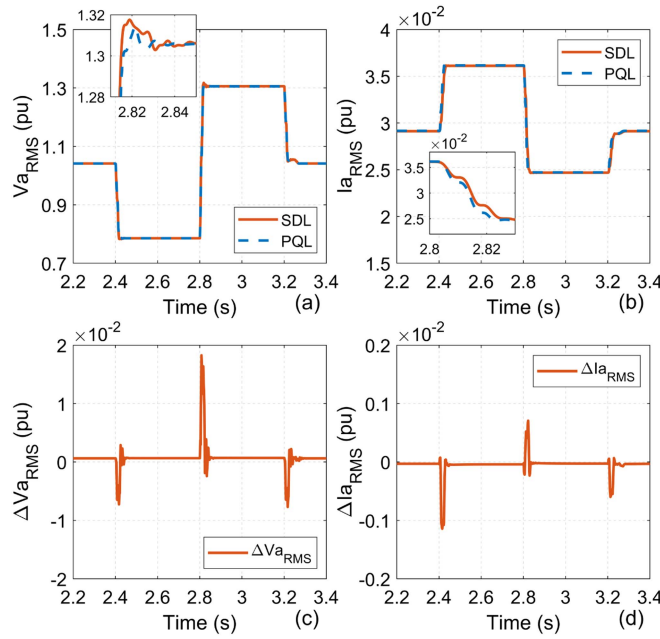


FIGURE 10. Phase-A RMS voltage, RMS current, and its deviation with respect to SDL model at Node 860 due to variation in supply voltage.

the network in steady-state conditions and then applying the following disturbances:

- 1) a series of step-changes in supply voltage following the sequence [1.0, 0.8, 1.2, 1.0] pu at the time intervals [0, 2.4, 2.8, 3.2] s, respectively;
- 2) an over/under-frequency step change of ± 0.5 Hz applied at $t = 2$ s and followed by the return to nominal frequency after 300 ms;
- 3) a series of step changes applied to the active and reactive power of the load connected at node 860, following the sequence [1.0 1.1 0.9 1.0] pu at the time intervals [0, 2.4, 2.8, 3.2] s, respectively.

1) VOLTAGE VARIATION

The response of the PQL model has been studied by imposing a sequence of step variations in the supply voltage of the IEEE-34 node distribution network, and comparing it with the behaviour of the commonly employed SDL model. The node 860, which is relatively far from the system slack bus, has been chosen as an observatory point for this study.

In Fig. 10(a), the transient behaviour of the Phase-A RMS voltage trajectory at node 860 has been shown for the two load models. The voltage behaviour of the PQL model closely follows the voltage behaviour of the SDL model, with negligible steady-state error. The maximum deviation of RMS voltages between the SDL and the PQL models has been observed to be approximately 2 %, and the deviation of phase-A voltage at node 860 is as shown in Fig. 10.

In Fig. 10(b), the Phase-A RMS current trajectories at node 860 have been plotted. In Fig. 10(b), it can be observed that the current dynamics of the PQL model match those of the SDL model. It can also be observed that the PQL model reaches

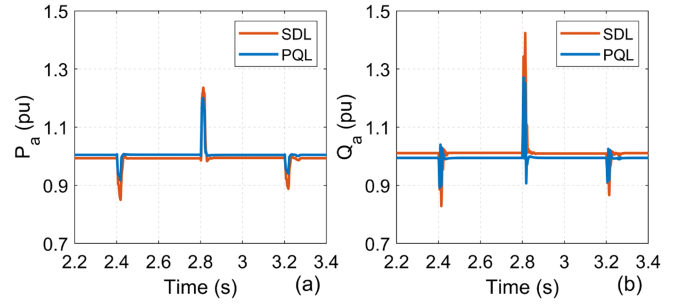


FIGURE 11. Phase-A Active and Reactive powers at Node-860 due to variation in supply voltage.

the steady-state faster than the SDL model. This means that the PQL model provides a better response with respect to the SDL model in the transient state. This is also confirmed by the plot in Fig. 10(d), where it shows that the maximum current deviation between the PQL and SDL model is below 0.2 %.

Similarly, in Fig. 11, the comparison plots of active and reactive powers are shown. The PQL model is able to follow the SDL model power behaviour with a minimum error and a relatively lower overshoot compared to the SDL model. Moreover, the SDL model has a slower response in reaching the steady-state power values due to the presence of delays introduced by the blocks such as PLL, moving average blocks, and RMS. The maximum peak deviation of active power between the SDL and the PQL models was approximately observed to be 8 % and that of reactive power was approximately 18 %. The other nodes of the grid, not shown for the sake of brevity, follow the same trends as Node 860, with negligible differences in the steady-state values, of the same order as those shown in Section V-A.

2) FREQUENCY VARIATION

In this test, the supply frequency of the IEEE-34 bus network under test was varied to study the dependency and response of the load power on over- and under-frequency variations. The test is composed of two different simulations, performed by imposing a step change of ± 0.5 Hz, followed by the return to nominal frequency after 300 ms. The PQL model at node 844 was subjected to study the frequency support response of the load and is compared against the SDL model. A frequency sensitivity gain of 0.5 for active power and -0.5 for reactive power is chosen for this test.

In Fig. 12, the behaviour of Phase-B active and reactive power at node 844 under an over-frequency scenario has been shown for both the models. Fig. 12(a) and (b) show that the active power (P) and reactive power (Q) of the PQL model follow the reference powers (obtained from (20)) with a slight deviation and ensure frequency support during a period of over-frequency deviation. On the other hand, the SDL model is not capable to react to the over-frequency deviation and does not follow the reference values as it does not have the frequency dependency term in its implementation. The maximum deviation of the active and reactive powers of the PQL

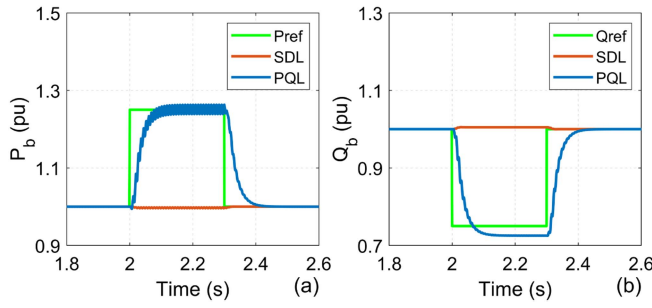


FIGURE 12. Phase-B Active and Reactive powers at Node-844 due to over frequency.

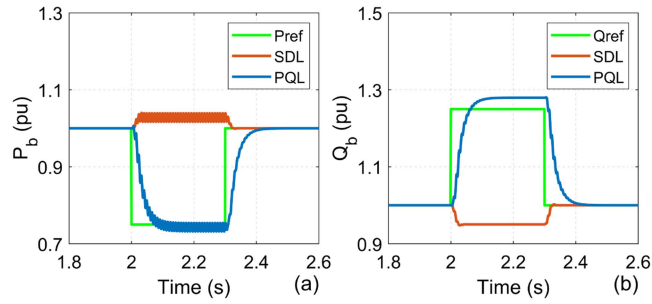


FIGURE 13. Phase-B Active and Reactive powers at Node-844 due to under frequency.

model concerning reference values during over-frequency deviation is around 1 % and 2.5 %, respectively.

Similarly, Fig. 13 shows the response of the active and reactive powers at node 844 due to the under-frequency scenario of both load models. The PQL model tries to follow the reference power during frequency changes, while the SDL model does not react to the under-frequency variation, as shown in Fig. 13(a) and (b). The active and reactive powers at node 844 of the PQL model have a maximum deviation of 1.3 % and 3 % to the reference value. The SDL model experiences a maximum deviation due to the non-implementation of the frequency dependency characteristics. The other nodes of the grid, not shown for the sake of brevity, follow the same trends as Node 844.

3) POWER VARIATION

In this test, a step change in reference power was performed to study the behaviour of the PQL model. A constant power load ($n_p = 0$, $n_q = 0$) at node 860 was subjected to a change of 10 % in active and reactive power compared to its previous steady-state value. The PQL and SDL models follow the reference values with similar dynamics on each phase.

As an example, Fig. 14 shows the power trajectory and its deviation in phase-C of the spot load in node 860 with respect to the reference power. The maximum deviation between the PQL and the SDL models concerning reference power is about 0.5 – 0.7 %, making their mismatch negligible.

To enable a more concrete comparison between the two models, the MAE and RMSE indices were calculated over the time window in which the active and reactive power set-point

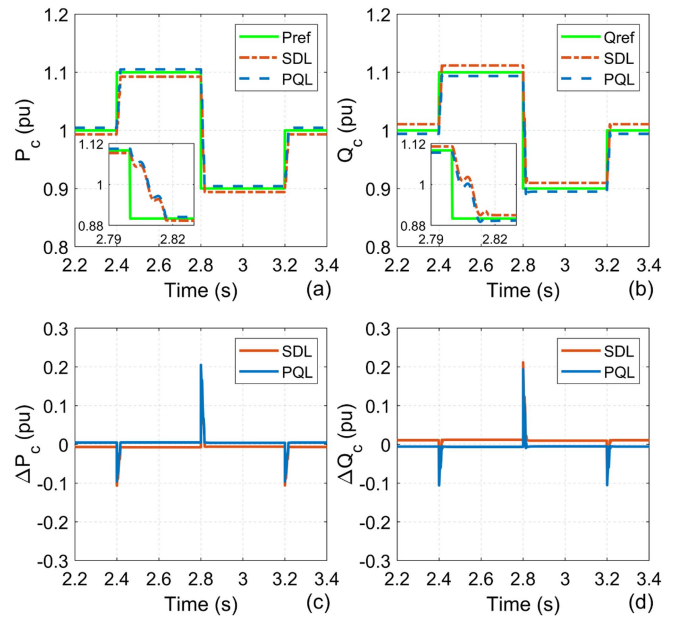


FIGURE 14. Phase-C Active power variation, Reactive power variation, and its deviation with respect to reference power of spot load 860.

TABLE 8 Mean Absolute Error (MAE) and Root Mean Square Error (RMSE) of the Active and Reactive Powers During the Transient in Fig. 14 (p.u.)

		P_a	Q_a	P_b	Q_b	P_c	Q_c	$\times 10^{-3}$
MAE	SDL	9.86	10.75	8.97	10.55	9.65	9.90	
	PQL	7.64	7.28	6.68	7.14	7.25	6.27	
RMSE	SDL	20.19	17.59	16.31	17.03	18.73	14.18	
	PQL	19.63	15.75	15.49	15.40	17.83	11.99	

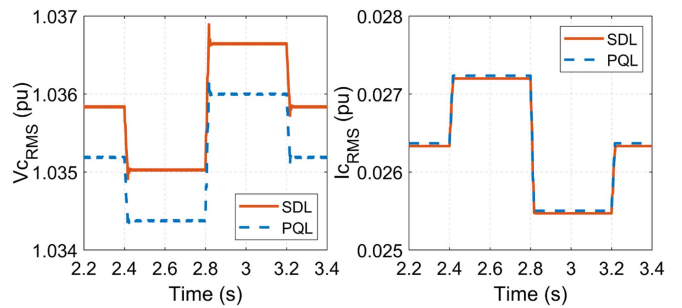


FIGURE 15. RMS voltage (a) and current (b) at Node 860 due to active and reactive power changes.

variations occur. The index values for each phase are reported in Table 8. Even though both the load models exhibit a strong ability to track the reference signals, the proposed PQL model demonstrates a slightly higher level of accuracy.

The change in active and reactive power references leads to voltage and current profile changes to meet the power demand. Fig. 15 shows the phase-C RMS voltage and current profiles during power variation. Similar characteristics can be observed in each phase's RMS voltage and current profiles. The maximum deviation of RMS voltage and current between

the PQL and the SDL models are approximately 0.035 % and 0.003 %, which is negligible.

C. VALIDATION OF PQL MODEL UNDER HARMONICS AND DC OFFSET

The performance of the PQL model was evaluated under harmonic distortion and DC offset. The input voltage with a THD of 10 % and 20 %, the output of the SOGI-FLL with FLL gain normalization, the THD of v_α increased from 3.84 % to 8 % and the THD of v_β increased from 1.23 % to 2.60 %. The THD of the output current i_α increased from 2.09 % to 3.63 %, respectively. In both cases, the estimated frequency exhibited oscillations around the nominal value, with peak deviations of $\pm 0.3\text{Hz}$ to $\pm 0.5\text{Hz}$. These results demonstrate that the normalized SOGI-FLL substantially attenuates the input harmonic distortion. However, the residual harmonic components remain in the orthogonal signals and propagate to the generated phase current i_α . In contrast, the SDL model with an input voltage of THD 10 % and 20 %, the output current had a THD of 8 % and 15 % respectively, showcasing a higher current distortion during harmonics.

When the input signal had a DC offset of 2 %, 5 %, and 10 %, the corresponding frequency oscillations were approximately ± 0.2 , ± 0.5 , and $\pm 1\text{Hz}$, respectively. There is no significant DC offset effect observed in v_α , whereas the DC offset effect is observed predominantly in v_β . This behaviour indicates that the FLL gain normalization does not inherently provide DC offset rejection. It is also observed that the reference current exhibits higher distortion when the input signal exhibits both harmonics and a DC offset simultaneously. On the other hand, the SDL model exhibits smaller frequency oscillations during DC offset conditions.

Furthermore, increasing the value of the normalized gain γ enables faster response to frequency variations; reducing the settling time and increasing the sensitivity of the estimated frequency to distortion, DC offset, and measurement noise, resulting in larger estimation ripple. In contrast, a low value of normalized gain γ provides a better harmonic attenuation and smoother frequency estimate; increasing the frequency tracking time. Hence, the value of the normalized gain γ has to be selected in such a way to obtain a trade-off between the fast dynamic response and attenuate harmonics considerably.

Overall, the robustness to input voltage magnitude variations and harmonic attenuation is improved by FLL gain normalization, but it doesn't eliminate harmonics or DC offset completely. When harmonic distortion and DC offset occur simultaneously in the input voltage, residual frequency and phase estimation oscillation may affect the quality of the generated current.

VI. EXECUTION TIME REQUIREMENTS

As a final point for the comparison of these two models, the computational burden of the PQL and the SDL models have been assessed and compared. The study investigated the maximum number of loads that can be simulated adopting a $50\text{ }\mu\text{s}$ time-step on a single core before experiencing overruns.

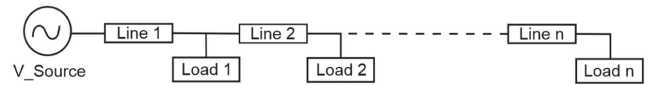


FIGURE 16. Simple test feeder for calculating the maximum number of simulated loads per core.

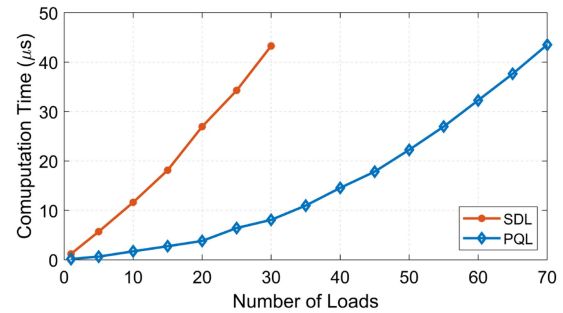


FIGURE 17. Computational analysis of single-phase dynamic load block on a single CPU core.

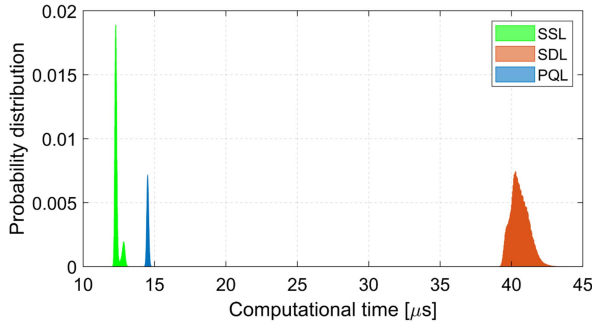
As a realistic test case, the assessment of the computational time of the IEEE-34 node test feeder mentioned in Section IV using the PQL and the Simulink load models (SSL and SDL) has been made.

An OPAL-RT's OP5700 real-time simulator is used for performing the computational study, but similar trends are expected on lower-end real-time platforms with increased absolute step sizes due to lower clock frequency and core counts. Although the FPGA-based solvers show much smaller time-steps and greater determinism, its performance depends more on logic utilization than on complexity of the algorithms, which restricts the aim of simulating large power networks. The real-time simulator is configured with Red Hat Enterprise Linux Server release 5.2 OS version and 2.6.29.6-opalrt-6.2.1 Kernel version. The RT-LAB version used is the v2022.1, and the models are programmed to run in software-synchronized mode to check the overall computation time without any overruns.

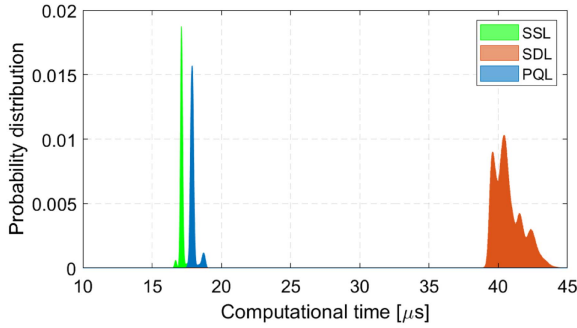
To assess the maximum number of loads that can be simulated on a single core (without any decoupling element) at $50\text{ }\mu\text{s}$, a simple single-phase test feeder with just a voltage source, transmission lines (PI lines), and constant power loads has been considered, as shown in Fig. 16.

It is observed that the PQL model had low computational time and could simulate up to 70 loads within the limit of $50\text{ }\mu\text{s}$ time-step. When loads are modelled with the SDL model, this number drops down to 30. This is the maximum number of loads which can be simulated under the previous assumptions using the dynamic load model found in the common libraries. As shown in Fig. 17, which shows how the computational time progresses with the insertion of additional loads, it is clear that the PQL model offers much better computational performance than the SDL model, showing a 130 % additional simulation capability.

Similarly, the computational study of the IEEE-34 node test feeder and the IEEE-123 node test feeder was also



(a) Probability distribution of computational time of IEEE-34 node distribution feeder



(b) Probability distribution of computational time of IEEE-123 node distribution feeder

FIGURE 18. Probability distribution of computational time of the IEEE-34 node and the IEEE-123 node test feeders.

investigated by assuming the loads to be constant impedance and simulating it in the real-time environment for more than 15 hours to verify that no overruns are experienced. The models are simulated with a minimum time-step value of $50 \mu s$ using PQL and Simulink load models (SSL and SDL). In the occurrence of overruns, the time-step has been increased in multiples of $50 \mu s$, and the test feeder has been tested again for no overruns in the entire time window. In this test, multiple active cores are used to simulate the test feeder and the models are decoupled using OPAL-RT's ARTEMiS stubline and the SSN NIBs (Nodal Interface Blocks) in the OPAL-RT's ARTEMiS library.

The minimum simulation time required to simulate the IEEE-34 node test feeder without any overruns in a real-time environment using 1 to 4 cores of the real-time simulator and that for the IEEE-123-node test feeder using 1 to 5 cores, is shown in Table 9. The minimum time-step ensures that the models experience zero overruns during the simulation. The average computational time is calculated over a simulation time of 5 minutes, and the increase in computational time is calculated over the SSL model as a reference.

The probability distribution in Fig. 18 shows that the computation time of the SDL model experiences significant deviations around the mean value, which may lead to random overruns during real-time simulation. In the case of IEEE-34 node test feeder, compared to the static SSL model, the SDL

TABLE 9 Overall Computation Time Comparison of Test Feeders With Different Load Models

(a) Overall computation time comparison of IEEE-34 node test feeder with different load models

Dynamic Load Model used	Min. Ts required [μs]	Comp. time required [μs]	Comp. time increase [%]
<i>1 core</i>			
SSL	50	36.96	0%
SDL	250	197.8	435.2%
PQL	100	58.32	57.79%
<i>2 core</i>			
SSL	50	19.56	0%
SDL	150	104.2	432.7%
PQL	50	26.54	35.68%
<i>3 core</i>			
SSL	50	12.54	0%
SDL	100	65.59	423.04%
PQL	50	19.04	51.83%
<i>4 core</i>			
SSL	50	12.26	0%
SDL	50	40.32	228.87%
PQL	50	14.52	18.43%

(b) Overall computation time comparison of IEEE-123 node test feeder with different load models

Dynamic Load Model used	Min. Ts required [μs]	Comp. time required [μs]	Comp. time increase [%]
<i>1 core</i>			
SSL	150	95.24	0%
SDL	350	289.21	203.66%
PQL	150	111.12	16.67%
<i>2 core</i>			
SSL	100	45.12	0%
SDL	150	130.82	189.93%
PQL	100	49.52	9.75%
<i>3 core</i>			
SSL	50	32.21	0%
SDL	100	85.25	164.66%
PQL	50	37.93	17.75%
<i>4 core</i>			
SSL	50	23.66	0%
SDL	100	61.50	159.93%
PQL	50	27.84	17.75%
<i>5 core</i>			
SSL	50	17.12	0%
SDL	50	40.82	138.43%
PQL	50	18.65	8.9%

model has an average computational time of around +229 % when implemented on four cores at $50 \mu s$. This increase is even worse when implemented on a single core at $250 \mu s$ (+435.2 %). On the other hand, the PQL model shows a significant reduction in the computational time compared to the SDL model. It is observed that the PQL model has an average computational time of 18.43 % on four cores at $50 \mu s$ compared to the SSL model and a maximum of 57.79 % on a single core at $100 \mu s$ without any overruns.

Similarly, in case of IEEE-123 node test feeder, the SDL model has a computational time of around +139 % compared to SSL model when implemented on 5 cores at $50 \mu s$. When implemented on single core at $350 \mu s$ (290 %), the SDL model shows significant computational burden. In contrast, the PQL model provides a significant reduction in the computational time compared to the SDL model. The PQL model shows an

average computational time of around 9 % on five cores at 50 μ s compared to the SDL model, while on a single core, it shows a maximum of 17 % at 150 μ s without any overruns.

The adoption of the PQL model allows the IEEE-34 node test feeder to be simulated at 50 μ s with just two cores, whereas the SDL model requires around four cores with the same time-step. Similarly, the adoption of the PQL model in IEEE-123 node test feeder requires three cores to be simulated at 50 μ s, whereas the SDL model requires five cores with the same time-step. Reducing the computational time helps to simulate larger networks without any additional active cores. The availability of idle cores is of fundamental importance because it allows to simulate more complex systems which can integrate detailed models of power electronics-based interfaces, controls, communication protocols, and hardware-synchronized equipment.

VII. CONCLUSION

The proposed PQL model has been adopted to implement a lightweight alternative to the single-phase SDL model in the MATLAB/Simulink simulation environment. Indeed, the presence of computationally intensive blocks in the SDL model increases the computational burden and, consequently, the overall computation of the simulated system. Compared to the SDL model, the proposed PQL model demonstrated significant reductions in computational burden by eliminating the compute-intensive blocks such as PLL, RMS, variable frequency mean, and conversion blocks, making it more suitable for real-time simulation. Furthermore, dynamic performance was enhanced by incorporating algebraic frequency dependency features into its modeling.

The PQL model is compared with the SDL model to reproduce the behaviour of load and validate the accuracy of the developed model while keeping a lower computational burden. Although there are minor differences in voltage, current, and power responses, the overall deviations remain small and negligible. Therefore, the objective of the PQL model is to maintain accuracy and achieve a comparable lower computational burden while simulating the model.

The validation and computational testing results using an IEEE-34 node and IEEE-123 node distribution feeder show that:

- The single-phase PQL model can have a faster steady-state response compared to the SDL model, achieving almost accurate results as the voltage profile data
- The single-phase PQL model significantly proves its efficiency by requiring less computation time without compromising accuracy, a clear advantage over the well-accepted SDL model
- The number of cores required to simulate in real-time the IEEE-34 node and IEEE-123 node distribution feeder with a single-phase PQL model is less when compared to using a single-phase SDL model at a specified time-step;
- The computational time required by the proposed PQL model is characterized by significantly smaller deviations around the mean value, leading to better stability

of the real-time simulation and a lower probability of random overruns.

Concluding, the instantaneous p-q theory-based load modeling approach helps to reduce the cost of simulating complex networks and also provides the option of having a lower time-step for HIL and PHIL testing, increasing the interface stability. Moreover, the proposed modeling approach is sufficiently general to be applicable to various types of energy resources, making it an efficient solution for HIL and PHIL testing.

Future work includes focusing on generalizing the mathematical formulation of the PQL to any unbalanced three-phase load and experimental validation. Also, comparing the PQL model with other load models and extending the PQL framework to a data-driven and reduced-order grey-box model, aiming to enhance its ability to adapt under various operating conditions.

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