

Cost-efficient Inductor Sizing in Solid-state DC Breakers Based on Semiconductor Fault-current Conduction Capability

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Abstract—Solid-State Circuit Breakers (SSCBs) are taking on a vital role in DC power system protection due to their ultra-fast fault interruption capability. DC faults are characterized by a drastic rise in current and continuous arc formation, which impose severe electrical and thermal stress on semiconductor switches. The rate of rise of the fault current (di/dt) directly affects the maximum fault current, the resulting over-voltage stress, and the associated power dissipation. While the di/dt is naturally determined by the fault-loop inductance, it can still be limited through integrated fault current limiters. Since the average breaking time of different semiconductor technologies lies within a relatively narrow range, limiting the fault di/dt reduces the maximum breaking current, allowing smaller semiconductor and varistor sizes at the cost of a larger fault-limiting inductor. This paper investigates the optimal trade-off between the required semiconductor fault-current breaking capability and the size of the fault-current-limiting inductor. The analysis demonstrates that this optimum is strongly dependent on the ratio of maximum non-repetitive surge current to nominal current for different semiconductor technologies. These findings are substantiated through detailed analytical evaluation, providing guidance for cost-effective design of the SSCB across a broad range of semiconductor technologies.

Index Terms—DC microgrid, Fault Current Limiter (FCL), protection, Solid-State Circuit Breakers (SSCB)

I. INTRODUCTION

Since the early 20th century, electricity has served as the foundation of industrial and technological advancement, with Alternating Current (AC) established as the dominant standard due to its efficient long-distance power transmission capability. However, increasing environmental concerns and the depletion of fossil fuel resources have accelerated the transition toward cleaner and more decentralized energy systems. Under these evolving conditions, the limitations of traditional AC microgrids have become increasingly apparent, particularly in the integration of renewable energy sources and modern DC-based technologies [1]. Renewable energy resources and storage systems such as photovoltaic arrays, fuel cells, and battery units inherently generate Direct Current (DC). Modern loads including mobile transportation systems such as electric cars, and ships, light-emitting diode (LED) lighting, and data centers also operate on DC power [2]. Since renewable sources

and many loads operate on DC, AC architectures must rely on additional power conversion stages to ensure compatibility, leading to increased energy losses, higher system complexity and synchronization issues, and elevated operational costs [3], [4]. In contrast, DC microgrids address these challenges by enabling the direct integration of distributed energy resources and loads through a common DC bus. This configuration reduces conversion stages, enhances overall system efficiency, minimizes thermal stress and cable losses, and eliminates synchronization requirements. Consequently, DC microgrids are increasingly recognized as a practical and technically efficient solution for renewable-based energy systems [5].

Despite their efficiency and flexibility, DC microgrids face operational challenges including immaturity, lack of standardization, and most critically, protection [6]. Unlike AC systems, the absence of natural current zero-crossing points prevents arc extinction, allowing fault currents to rise rapidly, further intensified by capacitive discharge from DC-link and load capacitors, necessitating ultra-fast and coordinated protection strategies.

Conventional protection devices exhibit significant limitations in DC microgrids. Fuses are simple and low cost but are single-use, lack reclosure capability, and provide limited selectivity. Mechanical circuit breakers also provide high conduction efficiency but operate in a few hundreds of milliseconds, allowing substantial fault energy to accumulate, limiting fast and automated protection. Hybrid breakers offer faster response by combining mechanical and semiconductor elements, but remain slower than fully solid-state solutions, and are less efficient than mechanical breakers under normal operation [6]. These limitations emphasize the need for high-speed, fully controllable protection solutions that can actively limit fault currents while enabling reliable and automated system operation [7].

In contrast, SSCBs represent a promising solution for DC microgrid protection due to their ultra-fast fault interruption capability, typically operating in the microsecond range. SSCBs employ fully controllable semiconductor devices such as IGBTs, MOSFETs, or Thyristors to interrupt fault currents

electronically, eliminating mechanical arcing phenomena and enabling precise control over fault clearing and system recovery. Their rapid response significantly reduces fault energy and improves coordination in converter-dominated DC systems [8]. However, semiconductor switches inherently possess limited overcurrent withstand capability, as surge currents can only be tolerated for very short durations within the safe operating area. In addition, continuous conduction losses caused by the finite on-state voltage drop generate thermal stress during normal operation and require appropriate thermal management [9]. Since the maximum interruptible current of semiconductor devices is typically only a few multiples of their nominal current, the rate of rise of fault current plays a decisive role in SSCB design, as excessive di/dt may rapidly drive the device beyond its safe operating limits. Therefore, controlling the fault current slope becomes a fundamental requirement to ensure reliable and safe SSCB operation.

To limit the fault current rise, SSCBs commonly incorporate a series fault current limiter in the form of an inductor. By increasing the fault loop inductance, the inductor limits di/dt and reduces the peak fault current, thereby keeping the semiconductor within its permissible surge current capacity. However, the sizing of this inductor introduces a critical trade-off. A larger inductance effectively reduces peak current and semiconductor device stress but increases the inductor size, and weight. Conversely, a smaller inductance results in higher current slopes, requiring semiconductors with greater surge capability and MOVs with higher energy absorption ratings to manage the associated overvoltage stress. This interdependence between inductor size, semiconductor rating, and surge protection requirements directly impacts the total cost and physical dimensions of the SSCB.

Although numerous studies have addressed SSCB topologies, switching performance, and protection coordination in DC microgrids, limited attention has been given to the systematic and cost-oriented optimization of the fault current limiting inductor based on semiconductor fault current conduction capability. Existing approaches often assume predefined device ratings or fixed inductance values without analytically linking the permissible surge current ratio of the semiconductor to the optimal di/dt and corresponding inductance. As a result, the interaction between semiconductor surge capability, current slope limitation, and overall system cost remains insufficiently explored in the literature. To address this gap, this paper proposes a cost-efficient analytical methodology for optimizing the fault current slope and corresponding series inductance in SSCBs for DC microgrids. The method is based on the semiconductor key characteristics, including nominal current, non-repetitive surge current, and nominal voltage. Using these parameters, the optimal di/dt and inductance are derived to ensure that the peak fault current remains within the safe operating limits of the semiconductor device. The proposed approach balances the trade-off between inductor size and device rating, and is validated across different semiconductor technologies, including IGBTs, MOSFETs, and thyristors, demonstrating its scalability and device-independent applica-

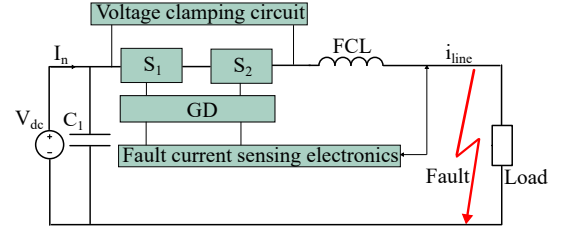


Fig. 1. Bidirectional Solid state circuit Breakers

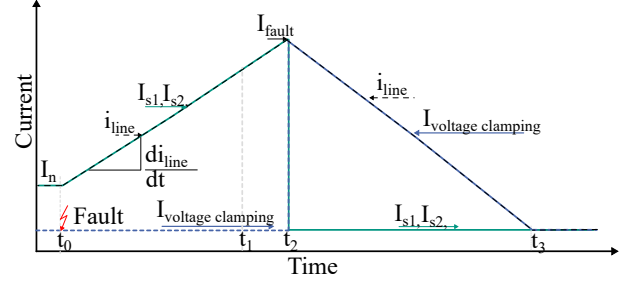


Fig. 2. Transient response of the solid-state circuit breaker during a fault

bility for cost-effective SSCB design.

II. MODELING AND INDUCTOR SIZING OF SOLID-STATE CIRCUIT BREAKERS

A generalized configuration of the bidirectional SSCB is illustrated in Fig. 1. The topology consists of two controllable semiconductor switching units (S_1 and S_2), a series fault current limiting inductor (FCL), an input capacitor C_1 , signal conditioning circuit, and a voltage clamping circuit for overvoltage protection. The semiconductor switches are driven by dedicated gate drivers (GD), while the system operates at a nominal DC voltage V_{dc} and rated current I_n .

A. SSCB Configuration and Operating Principle

Under normal operating conditions, the semiconductor switches conduct the load current in the ON state with minimal conduction losses. When a fault occurs, the protection circuitry initiates the interruption sequence. The combination of the series FCL and the voltage clamping branch controls the transient current rise and suppresses overvoltage stress, ensuring that the semiconductor devices operate within their safe limits. The transient response of the solid-state circuit breaker during a fault is illustrated in Fig. 2. At the instant the fault occurs, t_0 , the line current, initially equal to the nominal current I_n , begins to rise at a rate determined by the ratio of the nominal DC-bus voltage V_{dc} to the inductance L of the fault loop. The initial rate of rise of the fault current is determined by

$$\frac{di_{line}}{dt} = \frac{V_{dc}}{L} \quad (1)$$

which indicates that the series inductance directly determines the slope of the fault current, which in turn sets the peak current before semiconductor turn-off and limits device stress.

Between t_0 and t_1 , the fault current increases approximately linearly while the switch remains in the on state. At t_1 , the breaker detects the fault. However, due to the delay of the drivers and switches, the current continues to rise until the switch is fully turned off at t_2 . The maximum fault current reached during this interval can be approximated as

$$I_{f,max} = I_n + \frac{di_{line}}{dt} \cdot t_s \quad (2)$$

where $t_{s,max} = t_2 - t_0$ is the total fault breaking time. This highlights the combined effect of system voltage, series inductance, and breaker reaction time on the maximum fault current. At t_2 the current commutates to the voltage clamping branch. The clamping circuit absorbs the energy stored in the fault inductor, allowing the line current to decay to zero and completing fault interruption at t_3 .

B. Analytical Determination of Optimal Current Slope and Inductance

To ensure safe operation of SSCB, the maximum fault current must remain within the safe operating limits of the semiconductor devices. Each device has a nominal current rating ($I_{nom,semi}$), and a non-repetitive fault current capacity ($I_{max,semi}$). The surge ratio α can be defined accordingly as:

$$\alpha = \frac{I_{max,semi}}{I_{nom,semi}} \quad (3)$$

In practical designs, multiple devices are connected in parallel to meet the system nominal current I_n and provide sufficient margin for thermal reliability and current sharing. The aggregate nominal current of the parallel connected switches can be expressed as:

$$I_{nom,agg} = N * I_{nom,semi} \quad (4)$$

where N is the number of devices selected to meet both steady-state and fault requirements. The relationship between the aggregate device rating and the system nominal current can be represented by a scaling factor k is defined as:

$$k = \frac{I_{nom,agg}}{I_n} \quad (5)$$

Using this factor, the maximum fault current that the SSCB can safely interrupt is given by:

$$I_{max} = \alpha * I_{nom,agg} = \alpha * k * I_n \quad (6)$$

This formulation directly incorporates both the surge handling capability of the devices and the parallel configuration into a system-level fault current limit. The cost-optimal configuration is achieved when the number of parallel semiconductor devices required for steady-state current conduction equals the number necessary to ensure adequate surge current capability for interrupting the maximum fault current. Among configurations with an identical optimal semiconductor count, the one employing a smaller fault-limiting inductance results in the minimum total

TABLE I
DC MICROGRID AND SEMICONDUCTOR PARAMETERS FOR SSCB DESIGN

Parameter	Notation	Value
System DC voltage	V_{dc}	1500 V
System nominal current	I_n	100 A
Breaker maximum breaking time	$t_{s,max}$	10 μ s
Semiconductor nominal current	$I_{nom,semi}$	50 A
Maximum fault current ratio	α_{max}	3

cost. The optimal slope of the fault current, $(di/dt)_{opt}$, can then be derived by putting Eq. (2) and Eq. (6) are equal.

$$\left(\frac{di_{line}}{dt}\right)_{opt} = \frac{I_{max} - I_n}{t_{s,max}} = \frac{\alpha * k * I_n - I_n}{t_{s,max}} \quad (7)$$

$$\left(\frac{di_{line}}{dt}\right)_{opt} = \frac{(\alpha * k - 1)I_n}{t_{s,max}} \quad (8)$$

where $t_{s,max}$ is the breaker maximum breaking time. When $I_{nom,agg} = I_n$

$$\left(\frac{di_{line}}{dt}\right)_{opt} = \frac{(\alpha - 1) * I_n}{t_{s,max}} \quad (9)$$

then the optimum inductance can be

$$L_{opt} = \frac{V_{dc}}{\left(\frac{di_{line}}{dt}\right)_{opt}} \quad (10)$$

It should be noted that L_{opt} in Eq. (10) represents the total fault-loop inductance, including parasitic contributions from cabling and interconnections.

C. Numerical analysis

An analytical approach is therefore adopted to calculate the optimal fault current slope and the corresponding inductor value based on the system parameters summarized in Table I.

The numerical analysis is conducted based on the following assumptions and procedural steps.

- (1) The breaker maximum breaking time $t_{s,max}$ is assumed constant, as listed in Table I.
- (2) Under a bolted fault condition, the fault current slope is solely determined by the DC bus voltage and the series inductance L .
- (3) The maximum fault current per device is determined from the allowable fault current ratio α

$$I_{max,device} = \alpha * I_{nom,semi} = 3 * 50 = 150 \text{ A} \quad (11)$$

From Table II, it can be seen that increasing the fault current slope $\frac{di_{line}}{dt}$ directly increases the peak fault current I_{max} calculated using Eq. (2).

- (4) The required number of parallel semiconductor devices is determined by the more restrictive of the steady-state and fault current requirements. Accordingly, the number of devices required under normal operating conditions is defined as:

$$N_{nom} = \frac{I_n}{I_{nom,semi}} \quad (12)$$

TABLE II
IMPACT OF FAULT CURRENT SLOPE ON INDUCTANCE AND PARALLEL SWITCH REQUIREMENT

$\frac{di_{line}}{dt}$ (A/ μ s)	I_{max} (A)	N_{nom}	N_{fault}	$N_{required}$	L (μ H)
1	110	2	1	2	1500
5	150	2	1	2	300
10	200	2	2	2	150
15	250	2	2	2	100
20	300	2	2	2	75
25	350	2	3	3	60

Similarly, the number of devices required to withstand the maximum fault current is given by

$$N_{fault} = \frac{I_{max}}{I_{max,device}} \quad (13)$$

therefore, the total number of parallel switches is selected as

$$N_{required} = \max(N_{nom}, N_{fault}) \quad (14)$$

Using the system parameters listed in Table I, the fault current is calculated according to Eq. (2). The resulting semiconductor switch selection based on the fault current is summarized in Table II.

- (5) When $I_{nom,agg} = I_n$, optimum rate of current rise, $\frac{di_{line}}{dt}$, is first calculated using Eq. (9) and then used to determine the corresponding optimum inductance, L_{opt} , from Eq. (10). This inductance directly affects the physical size and cost of the SSCB, ensuring the inductor is properly selected for both performance and economic considerations.

$$\left(\frac{di_{line}}{dt}\right) = \frac{(\alpha - 1) * I_{nom}}{t_{s,max}} = \frac{(3 - 1) * 100}{10} = 20 \frac{A}{\mu s} \quad (15)$$

$$L_{opt} = \frac{1500}{20} = 75 \mu H \quad (16)$$

III. CASE STUDY FOR VALIDATION OF THE PROPOSED SYSTEM SIZING METHODOLOGY

To validate the proposed cost-efficient SSCB sizing methodology, a representative case study is conducted for a 1.5 kV, 100 A DC system based on Scenario 1, with device parameters summarized in Table III. The maximum junction temperature is assumed to be 110 °C, and both nominal and non-repetitive current ratings are considered at this temperature. The semiconductor switch is selected based on the system voltage and current requirements. For Scenario 1, the IXBH42N250 IGBT is employed, providing a blocking capability of 2.5 kV, which ensures reliable operation under the nominal 1.5 kV DC bus voltage as well as the transient overvoltages generated during fault interruption. The set voltage rating provides sufficient margin to maintain the clamped transient voltage within the device SOA. To suppress the overvoltage during current interruption, a MOV (V881BA60) is employed. Its clamping voltage is selected to remain below the IGBT blocking capability, thereby preventing excessive voltage stress across the

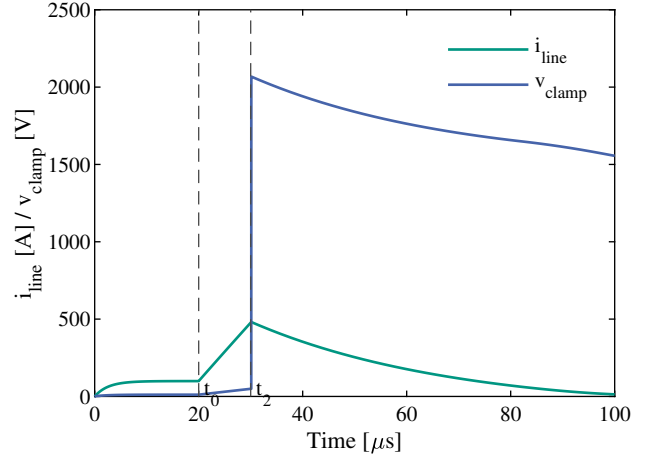


Fig. 3. Simulated fault current and MOV clamping voltage for Scenario 1

semiconductor device. The system rated current is 100 A, while each semiconductor device is rated for 42 A continuous operation at 110 °C, with a non-repetitive current capability of 161.53 A at the same temperature. The coefficient α is calculated as:

$$\alpha = \frac{161.53}{42} = 3.83 \quad (17)$$

As the fault current slope (di/dt) increases, the peak fault current is calculated and summarized in Table IV. Based on the nominal and non-repetitive current ratings, the required number of parallel switches to safely interrupt the fault current is determined and also listed in Table IV. For the considered system, connecting three devices in parallel provides an aggregate nominal current of 126 A, ensuring steady-state design margin and reliable current sharing. The scaling factor can be calculated as

$$k = \frac{126}{100} = 1.26 \quad (18)$$

The respective optimal fault current slope and the corresponding fault current limiting inductance were calculated using Eq. (8) and Eq. (10), respectively.

$$\left(\frac{di_{line}}{dt}\right)_{opt} = \frac{(3.83 * 1.26 - 1)100}{10} = 38.258 \text{ A}/\mu s \quad (19)$$

$$L_{opt} = \frac{1500}{38.258} = 39.20 \mu H \quad (20)$$

To validate the linear current ramp assumption of Eq. (2), a circuit-level simulation was conducted in MATLAB Simulink for Scenario 1 as shown in Fig. 3, comprising three parallel anti-series IGBT pairs with freewheeling diodes, a series inductance of 39.20 μ H, and a V881BA60 MOV. The fault current rises linearly to a peak of 482 A within the 10 μ s breaking time, confirming Eq. (2), while the MOV clamping voltage remains within the device blocking capability, confirming safe interruption within the SOA.

The cost of components is estimated based on the market prices available to consumers as of January 2026. The IGBT price is 28 USD per unit, while the inductors are considered

TABLE III
SYSTEM, SEMICONDUCTOR, AND OPTIMAL DESIGN PARAMETERS USED FOR INDUCTOR SIZING

Scenario	System Parameters		Semiconductor Parameters							Optimal Design	
	V_{dc} (V)	I_n (A)	Semiconductor Type	Switch Name	$V_{rated,semi}$ (V)	$I_{nom,semi}$ (A @ 110°C)	$I_{max,semi}$ (A @ 110°C)	α	$t_{s,max}$ (μ s)	$(di/dt)_{opt}$ (A/ μ s)	L_{opt} (μ H)
1	1500	100	IGBT ₁	IXBH42N250	2500	42	161.53	3.83	10	38.258	39.20
2	1500	100	IGBT ₂	IXYX25N250CV1	2500	25	61.84	2.4	10	18.56	101.78
3	800	50	SiC MOSFET	G3R30MT12K	1200	45	129.57	2.8	3	69.04	11.58
4	800	50	Thyristor	CLA50E1200HB	1200	54.35	343.95	6.32	1000	0.633	1262.737

TABLE IV
IMPACT OF FAULT CURRENT SLOPE ON INDUCTANCE AND PARALLEL SWITCH REQUIREMENT FOR SCENARIO 1

$\frac{di_{line}}{dt}$ (A/ μ s)	I_{max} (A)	I_C (A)	N_{nom}	$I_{cm}@25^\circ C$ (A)	$I_{cm}@110^\circ C$ (A)	N_{fault}	N_{req}	$N_{req,cost}$ (USD)	L (μ H)	L_{cost} (USD)	Total Cost (USD)
1	110	42	3	400	161.53	1	3	84	1500	985.25	1069.25
5	150	42	3	400	161.53	1	3	84	300	364.75	448.75
10	200	42	3	400	161.53	2	3	84	150	257.42	341.42
15	250	42	3	400	161.53	2	3	84	100	216.14	300.15
20	300	42	3	400	161.53	2	3	84	75	193.60	277.60
25	350	42	3	400	161.53	3	3	84	60	179.18	263.17
30	400	42	3	400	161.53	3	3	84	50	169.06	253.06
35	450	42	3	400	161.53	3	3	84	42.85	161.52	245.52
40	500	42	3	400	161.53	4	4	112	37.5	155.65	267.65
45	550	42	3	400	161.53	4	4	112	33.33	150.95	262.95
50	600	42	3	400	161.53	4	4	112	30	147.08	259.08
55	650	42	3	400	161.53	5	5	140	27.27	143.83	283.83
60	700	42	3	400	161.53	5	5	140	25	141.06	281.06
65	750	42	3	400	161.53	5	5	140	23.07	138.67	278.67
70	800	42	3	400	161.53	5	5	140	21.42	136.58	276.58
75	850	42	3	400	161.53	6	6	168	20.19	134.73	302.73
80	900	42	3	400	161.53	6	6	168	18.70	133.09	301.09
85	950	42	3	400	161.53	6	6	168	17.65	131.62	299.62
90	1000	42	3	400	161.53	7	7	196	16.67	130.29	326.29

as air-core inductors wound with copper conductors, capable of continuously carrying 100 A, with a material cost of 10 USD/kg. In addition, an average labor cost of 15 % of the material cost is included. The resulting component costs are summarized in Table IV.

The variation of inductor cost and semiconductor cost with respect to the fault current slope is illustrated in Fig. 4. As the fault current slope increases, the maximum fault current rises, which consequently increases the required number of semiconductor switches and their associated cost. In contrast, a higher fault current slope necessitates the use of a smaller fault current limiting inductance, resulting in a reduction in the inductor cost. This behavior highlights the inherent design trade-off between the semiconductor rating and the inductance value in the SSCB configuration. Since a single MOV component is retained across all operating points, the MOV procurement cost remains constant and does not influence the cost optimization presented in this work.

The cost analysis of the SSCB in this study is based primarily on the power semiconductors and the FCL, as these components largely determine the overall system cost. Consequently, the sizing of the inductor and the selection of semiconductors play a central role in both performance and economic optimization. The total system cost, obtained by summing the semiconductor and inductor costs, is presented in Fig. 5. The results indicate that the total cost initially decreases

with increasing fault current slope due to the significant reduction in the required inductance. However, beyond a certain point, the need for additional semiconductor switches causes the overall system cost to rise. The minimum total cost occurs at approximately 35 A/ μ s, corresponding to an inductance of about 42.85 μ H and a total system cost of approximately 245.52 USD, representing the optimal operating point for the proposed SSCB sizing methodology. The true optimum values of the inductance and fault current slope are 38.258 μ H and 39.20 A/ μ s, as listed in Table III; the value of 35 A/ μ s appears in Fig. 5 because a stepwise fault current slope was used for illustration. Notably, the proposed cost-efficient inductor sizing approach is applicable across different semiconductor technologies and system ratings and is not restricted to a specific configuration. The proposed analytical framework can also be extended to alternative switching technologies, including power MOSFETs and thyristor-based devices, across different DC bus voltages, rated currents, and short-circuit conditions, as summarized in Table III. From Table III, it is evident that SiC-MOSFETs exhibit the highest rate of change of current (di/dt) capability, indicating that they can safely handle faster increases in current during transient or fault conditions compared to IGBTs and thyristors. IGBTs offer moderate di/dt capability, while thyristors provide the lowest, resulting in a significantly larger optimal inductance of approximately 1262 μ H, confirming their limited suitability

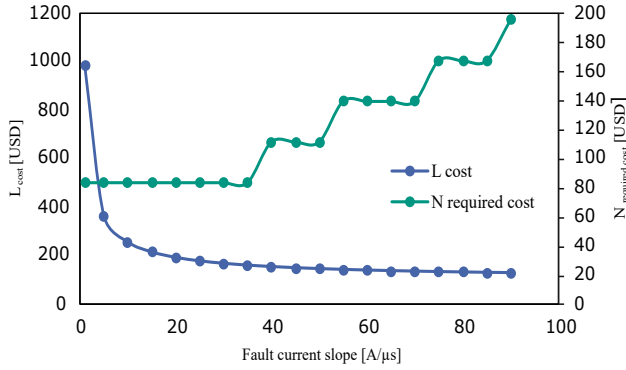


Fig. 4. The variation of inductor cost and semiconductor cost with respect to the fault current slope

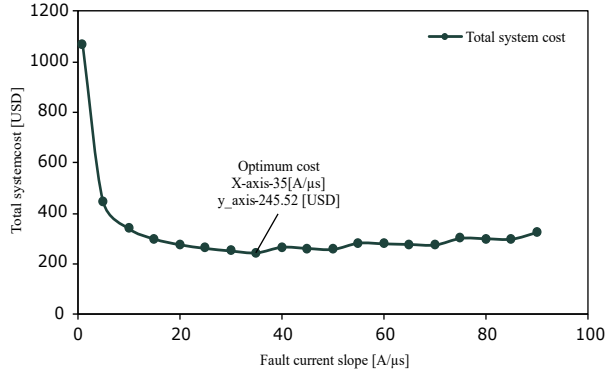


Fig. 5. The total system cost with respect to the fault current slope

for fast DC protection. Consequently, engineers should select the semiconductor device based on both the system's current rating and the expected rate of current change: MOSFETs are preferred for fast-switching, low-to-moderate current applications, whereas IGBTs or thyristors may be more appropriate for higher current levels or slower dynamic conditions. At elevated current ratings, MOSFET availability may be limited, which could require increasing the number of devices or adjusting the fault current limiter to maintain performance. By incorporating the respective device rated voltage, nominal current, non-repetitive surge current capability, and effective interruption time into the governing equations, the same optimal current-slope formulation remains applicable. These results demonstrate that the proposed methodology is fully scalable with respect to DC-link voltage, feeder current rating, and overall protection system requirements in DC microgrid architectures, enabling designers to achieve an optimal balance of cost, performance, and reliability.

IV. CONCLUSION

In SSCBs for DC microgrids, the FCL is essential for limiting short-circuit currents and protecting system components. A suboptimally designed FCL can result in excessive energy absorption, higher MOV and semiconductor ratings,

and a larger, more costly SSCB. In this work, the FCL is optimized by considering key semiconductor characteristics, including nominal current, non-repetitive surge current, and the maximum permissible surge ratio (α). These parameters are used to analytically determine the optimal current slope, which in turn defines the series inductance required for effective fault current limitation. The methodology is validated for multiple semiconductor technologies, including MOSFETs, IGBTs, and thyristors. The study also shows that MOSFETs can accommodate relatively higher current slopes than IGBTs, while thyristors are limited to lower slopes. Although MOSFETs are generally better suited for higher di/dt applications, the optimal choice of semiconductor depends on specific design details and practical constraints, including the device's surge current capability. This demonstrates that the proposed approach is device-independent and scalable, enabling optimization of series inductance, MOV rating, and semiconductor selection to minimize SSCB size and cost while ensuring robust protection. Overall, the framework provides a systematic and practical tool for cost-effective SSCB design across diverse DC microgrid configurations and can be extended to incorporate future advancements in semiconductor technology and microgrid architectures.

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