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Declaration

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I hereby declare under oath that I have written the present thesis independently and have used only the sources, internet sources, and aids specified. All passages taken literally or in spirit from other works or from the internet have been clearly identified as such and properly cited.

Eggenstein-Leopoldshafen, November 3, 2026

Palak Gupta

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Abstract

The development of emerging transistor technologies has enabled new electronic applications requiring mechanical flexibility, low-temperature processing, large-area fabrication, and low-voltage operation. However translating these technologies from individual device demonstrations into practical integrated circuits remains challenging due to the limited availability of Electronic Design Automation (EDA) infrastructure, device models, Process Design Kits (PDKs), and circuit methodologies. This thesis addresses these challenges by investigating complementary levels of integrated-circuit enablement, ranging from design infrastructure and circuit methodology to industrial technology implementations.

First, a Fully Hybrid Organic Process Design Kit (FH-OPDK) is developed for printed Organic Field Effect Transistor (OFET) technology. Electrical characterization is performed to extract compact transistor models based on the Variable Range Hopping Theory (VRHT) mechanism and device variability is incorporated to enable realistic circuit simulations. The developed Flexible Hybrid Organic Process Design Kit (FH-OPDK) integrates technology files, compact models, design rules, and verification utilities within a commercial EDA environment, enabling schematic capture, layout generation, physical verification, and circuit simulation. Using this framework, a standard-cell library comprising logic gates, ring oscillators, decoders, and a hardware demonstrator for a pressure sensor readout platform is successfully implemented. To evaluate device reliability and performance, low-frequency noise characteristics of OFETs are experimentally investigated. The measured noise behavior is analyzed using Mc-Whorter carrier number fluctuation and Hooge mobility fluctuation models, providing insight into the dominant physical noise mechanisms and establishing guidelines for future compact noise modelling of printed transistors.

Second, circuit-level enablement of emerging transistor technologies is investigates using Electrolyte Gated Transistors (EGTs). Since unipolar transistor technologies cannot directly employ conventional Complementary Metal Oxide Semiconductor (CMOS) logic, pass-gate logic is explored as an alternative circuit methodology. AND, OR and XNOR logic gates are designed and experimentally validated. Based on the logic gates, a full-adder circuit architecture design is proposed as outlook.

Finally, the methodology is extended to an industrial silicon platform through the implementation os digital and mixed-signal building blocks using a commercial 16 nm Fin Field-Effect Transistor (FinFET) PDK. Ring oscillators, voltage-controlled oscillators, and a phase-locked loop is designed, fabricated, and experimentally characterized following a complete industrial design and tape-out flow.

Together, these contributions demonstrate a design-enablement pathway connecting emerging printed transistor technologies with established silicon integrated-circuit methodologies. The work provides a foundation for developing future flexible and hybrid electronic systems that combine the application-specific advantage of emerging

devices with the performance and integration capabilities of mature semiconductor technologies.

Zusammenfassung der Arbeit

Die Entwicklung neuartiger Transistortechnologien hat neue elektronische Anwendungen ermöglicht, die mechanische Flexibilität, Niedertemperaturverarbeitung, großflächige Fertigung und einen Niederspannungsbetrieb erfordern. Die Überführung dieser Technologien von einzelnen Bauelementdemonstratoren hin zu praktischen integrierten Schaltungen stellt jedoch aufgrund der begrenzten Verfügbarkeit von EDA-Infrastrukturen, Bauelementemodellen, PDKs und Schaltungsmethoden eine Herausforderung dar. Diese Arbeit adressiert diese Herausforderungen durch die Untersuchung verschiedener Ebenen der Befähigung zur Entwicklung integrierter Schaltungen, die von Designinfrastrukturen und Schaltungsmethoden bis hin zu industriellen Technologieimplementierungen reichen.

Zunächst wird ein Fully Hybrid Organic Process Design Kit (FH-OPDK) für die gedruckte OFET-Technologie entwickelt. Durch elektrische Charakterisierung werden kompakte Transistormodelle auf Grundlage des VRHT-Mechanismus extrahiert und die Bauelementvariabilität wird integriert, um realitätsnahe Schaltungssimulationen zu ermöglichen. Das entwickelte FH-OPDK integriert Technologiedateien, kompakte Modelle, Designregeln und Verifikationswerkzeuge in eine kommerzielle EDA-Umgebung und ermöglicht damit die Schaltplanerstellung, Layoutgenerierung, physikalische Verifikation und Schaltungssimulation. Auf Grundlage dieses Frameworks wird erfolgreich eine Standardzellenbibliothek bestehend aus Logikgattern, Ringoszillatoren und Decodern sowie ein Hardware-Demonstrator für eine Drucksensor-Ausleseplattform implementiert.

Zur Bewertung der Zuverlässigkeit und Leistungsfähigkeit der Bauelemente werden die Niederfrequenzrauscheigenschaften von OFETs experimentell untersucht. Das gemessene Rauschverhalten wird mithilfe der Mc-Whorter-Modelle für Trägerzahlfluktuationen und der Hooge-Modelle für Mobilitätsfluktuationen analysiert. Dadurch werden Erkenntnisse über die dominierenden physikalischen Rauschmechanismen gewonnen und Richtlinien für die zukünftige kompakte Rauschmodellierung gedruckter Transistoren abgeleitet.

Zweitens wird die Schaltungsebene zur Befähigung neuartiger Transistortechnologien anhand von EGTs untersucht. Da unipolare Transistortechnologien konventionelle CMOS-Logik nicht direkt einsetzen können, wird Pass-Gate-Logik als alternative Schaltungsmethode untersucht. AND-, OR- und XNOR-Logikgatter werden entworfen und experimentell validiert. Auf Grundlage dieser Logikgatter wird als Ausblick eine Architektur für eine Volladdiererschaltung vorgeschlagen.

Schließlich wird die Methodik auf eine industrielle Siliziumplattform erweitert, indem digitale und Mixed-Signal-Schaltungsblöcke unter Verwendung eines kommerziellen 16 nm FinFET-PDK implementiert werden. Ringoszillatoren, spannungsgesteuerte Oszillatoren und eine Phasenregelschleife werden entworfen, gefertigt und experimentell charakterisiert, wobei ein vollständiger industrieller Design- und Tape-out-Prozess durchlaufen wird.

Zusammenfassend demonstrieren diese Beiträge einen Design-Enablement-Pfad, der neuartige gedruckte Transistortechnologien mit etablierten Methoden zur Entwicklung von Silizium-integrierten Schaltungen verbindet. Die Arbeit schafft damit eine Grundlage für die Entwicklung zukünftiger flexibler und hybrider elektronischer Systeme, die die anwendungsspezifischen Vorteile neuartiger Bauelemente mit den Leistungs- und Integrationsmöglichkeiten etablierter Halbleitertechnologien kombinieren.

List of Publications

Journal Publications

- **P. Gupta**, J. Lukosiunas, G. C. Marques, S. Raths, S. Stehlin, S. Schlisske, K. Exner, K.-P. Strunk, C. Melzer, P. Erk, J. Mittermaier, A. Klotz and J. Aghassi-Hagmann, "Active Matrix-Based Pressure Sensor System with a 4×16 Printed OFET Array and Integrated Hardware Readout Platform," *Flexible and Printed Electronics*, vol. 9, no. 1, Art. 015006, 2024.

- **P. Gupta**, et al., "Low frequency noise analysis in printed p-type organic field-effect transistors," Manuscript in submission [FPE-101523]

Conference Publications

- G. M. Cheragh, **P. Gupta**, G. C. Marques, G. Matei and J. Aghassi-Hagmann, "Pass Logic-Gates Based on Electrolyte-Gated Field-Effect Transistors with Metal Oxide Channels," *Proceedings of the 2024 IEEE International Flexible Electronics Technology Conference (IFETC)*, Bologna, Italy, pp. 1–4, 2024.

- **P. Gupta**, "Circuit Design and Optimization using Organic Process Design Kit based on Industrial EDA Tools," Oral Presentation, *LOPEC Conference*, Munich, Germany, Mar. 2022.

- **P. Gupta**, et al., "Sensor Design and Circuit Implementation using Organic Process Design Kit based on Industrial EDA Tools," Conference Presentation, *MRS Spring Meeting & Exhibit*, Honolulu, HI, USA, 2022.

- **P. Gupta**, J. Lukosiunas and S. Stehlin, "Basic OPDK Usage and Design of Standard Cells for Printed Electronics," Tutorial Presentation, *Design, Automation and Test in Europe (DATE)*, Antwerp, Belgium, 2022.

FH-OPDK Resources

- **P. Gupta**, J. Lukosiunas, G. C. Marques, S. Raths, S. Stehlin, S. Schlisske, K. Exner, K.-P. Strunk, C. Melzer, P. Erk, J. Mittermaier, A. Klotz, and J. Aghassi-Hagmann, "Flexible Hybrid Organic Process Design Kit (FH-OPDK)," Karlsruhe Institute of Technology (KIT). Available at: FH-OPDK Download Files [1].

- **P. Gupta**, J. Lukosiunas, G. C. Marques, S. Raths, S. Stehlin, S. Schlisske, K. Exner, K.-P. Strunk, C. Melzer, P. Erk, J. Mittermaier, A. Klotz, and J. Aghassi-Hagmann, "Organic Printed Electronics PDK Education Kit," Cadence Academic Network. Available at: FH-OPDK Education Kit [2].

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Abbreviations

FET Field Effect Transistor

MOSFET Metal Oxide Semicondutor Field Effect Transistor

OFET Organic Field Effect Transistor

FinFET Fin Field-Effect Transistor

CMOS Complementary Metal Oxide Semiconductor

EGT Electrolyte Gated Transistor

GAA Gate All Around

OECT Organic Electrochemical Transistor

CNT Carbon Nanotube based transistor

PDK Process Design Kit

EDA Electronic Design Automation

PLL Phased Look Loop

LFN Low Frequency Noise

PVT Process Voltage Temperature

FH-OPDK Flexible Hybrid Organic Process Design Kit

SPICE Simulation Program with Integrated Circuit Emphasis

VCO Voltage Controlled Oscillator

DRC Design Rule Check

LVS Layout versus Schematic

LPF Low Pass Filter

RTL Resistor transistor logic

TTL Transistor transistor logic

GR Generation-Recombination

PMOS P-Channel MOSFET

NMOS N-Channel MOSFET

DC Direct Current

TDC Time-to-Digital Converter

PCB Printed Circuit Board

ESD Electro Static Discharge

PVD Physical vapor deposition

PSD Power Spectral Density

FFT Fast Fourier Transform

PGL Pass Gate Logic

EDL Electronic Double Layer

VRHT Variable Range Hopping Theory

PET Polyethylene Terephthalate

PMMA Poly(methyl methacrylate)

PVP Poly(4-vinylphenol)

IC Integrated Circuit

PVS Physical Verification System

DRD Design Rule Driven

2T 2-Transistor

4T 4-Transistor

NTC Negative Temperature Coefficient

1. Introduction

Silicon CMOS technology has been the foundation of modern electronics for more than five decades. Continuous advances in CMOS technology have enabled the realization of highly integrated circuits, driving remarkable progress in computing, communication, consumer electronics, and numerous other application domains. Supported by mature fabrication processes and comprehensive electronic design methodologies, silicon CMOS has become the dominant platform for integrated-circuit implementation [3–5].

As electronic systems have diversified, semiconductor technology has evolved to address distinct technological requirements [3]. Innovations in silicon device architecture, including FinFET and Gate All Around (GAA) transistors, have enabled continued improvements in high-performance integrated circuits while maintaining compatibility with the mature silicon ecosystems [6–8].

Another significant research direction is motivated by the emergence of application domains that extend beyond the capabilities of conventional silicon electronics. Applications such as flexible electronics, wearable healthcare systems, electronic skins, smart packaging, robotics, and large-area sensing require characteristics including mechanical flexibility, lightweight form factors, low-temperature processing, additive manufacturing, and compatibility with large-area substrates [9–12]. These requirements have stimulated the development of alternative semiconductor materials and fabrication technologies, giving rise to emerging transistor platforms such as Carbon Nanotube based transistors (CNTs), Organic Electrochemical Transistor s (OECTs), OFETs, and EGTs [10,12,13]. Rather than replacing silicon technology, these emerging devices complement conventional CMOS by enabling functionalities tailored to application-specific electronic systems. The evolution of semiconductor technologies is illustrated in Fig. 1.1.

Although these emerging technologies have demonstrated promising device performance and enabled new application domains, the successful demonstration of an individual transistor represents only the first step toward realizing practical electronic systems. The implementation of integrated circuits requires not only functional devices but also a comprehensive design ecosystem that enables reliable circuit design, simulation, verification, and fabrication [3,4]. Modern integrated-circuit design relies

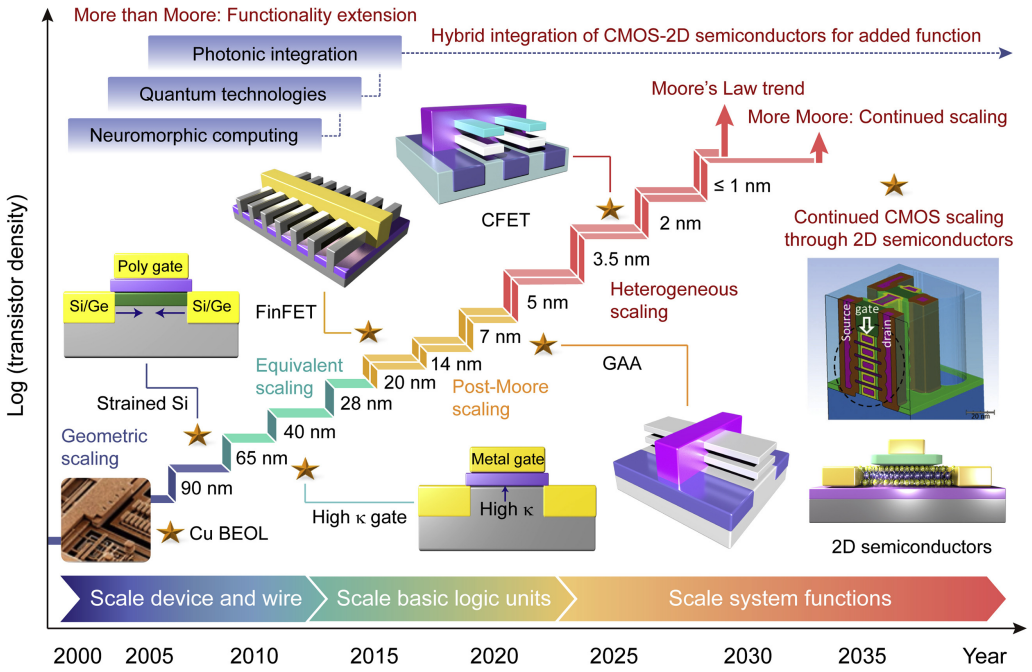


Figure 1.1: Evolution of semiconductor technologies toward high-performance and application-specific electronics [14]. Licensed under CC BY-NC-ND 4.0 [15].

on accurate compact device models, PDKs, design rules, simulation environments, verification methodologies, standard-cell libraries, and reusable design flows that collectively enable designers to predict circuit behavior prior to fabrication. Many emerging transistor technologies continue to lack standardized design methodologies and supporting infrastructure, limiting their transition from laboratory-scale device demonstrations to practical integrated-circuit technologies. Consequently, the development of comparable design ecosystems is essential for enabling emerging transistor technologies to evolve into reliable and scalable electronic platforms [16].

At design level, the absence of standardized PDKs, validated compact device models, reusable circuit libraries, and comprehensive EDA support limits the ability to design, simulate, and verify complex circuits within a unified workflow. At circuit level, many emerging transistor technologies exhibit device-specific constraints, such as unipolar operation, which prevent the direct adoption of conventional complementary CMOS design methodologies and instead require alternative logic families and circuit topologies. Furthermore, at system level, future electronic systems are expected to combine mature silicon technologies with emerging printed electronics through heterogeneous integration, requiring unified design methodologies capable of supporting hybrid electronic platforms. Therefore, advancing these technologies from laboratory-scale demonstration to practical integrated-circuit platforms requires progress in design infrastructure, circuit methodologies, and system-level integration.

To address these challenges, this thesis investigates three complementary aspects of integrated-circuit enablement for emerging transistor technologies. The first aspect focuses on establishing a comprehensive design infrastructure through the development of a Flexible Hybrid Organic Process Design Kit (FH-OPDK) for hybrid printed OFET technology. Device characterization is performed to extract compact transistor models, which are integrated into a commercial EDA environment to-

gether with technology files, design rules, and verification utilities. This framework enables schematic capture, circuit simulation, physical verification, and layout generation, providing a complete workflow for circuit implementation. The design flow enabled exploration of alternative circuit topologies because only unipolar transistors are available. Using the developed design environment, digital standard cells, decoder architectures, ring oscillators, and an OFET-based hardware demonstrator were designed and evaluated, demonstrating the front-to-back-end flow and the feasibility of constructing complex circuits [16].

The second aspect addresses circuit-design methodologies compatible with the constraints of emerging transistor technologies. Unlike conventional CMOS technologies, many emerging transistor platforms are unipolar and therefore cannot directly employ complementary logic styles. Consequently, alternative circuit topologies become necessary for implementing digital functionality [11, 12]. In this work, a pass-gate-logic topology is investigated using EGT, enabling the realization of compact and low-voltage digital circuits, including fundamental logic gates, with an outlook toward a full-adder circuit [17].

The third aspect investigates integrated-circuit implementation using a commercial 16 nm FinFET PDK. By following a complete industrial design flow from schematic capture to tape-out and experimental characterization, this work places the proposed methodology within the context of established semiconductor design practice. Together with the design infrastructure developed for printed OFETs and the circuit methodologies demonstrated using EGTs, it supports the broader vision of future hybrid electronic systems that combine mature silicon technologies with emerging printed electronics.

Here, enabling practical integrated-circuit technologies requires considerably more than the development of novel transistors. By addressing challenges in design infrastructure, circuit methodology, and technology integration, this work establishes a unified framework for translating emerging transistor technologies from laboratory-scale device demonstrations to practical integrated-circuit platforms. This work contributes to the realization of practical hybrid electronic systems that combine the strengths of mature silicon technologies with the unique capabilities of emerging printed electronics [8].

1.1 Structure of the thesis

Fig. 1.2 illustrates the overall organization and workflow of the thesis. The study begins with the theoretical background and progresses through the development of the FH-OPDK framework, EGT based pass-gate logic implementation, and industrial FinFET circuit design. Finally, the thesis concludes with a summary of the major contributions and future research directions.

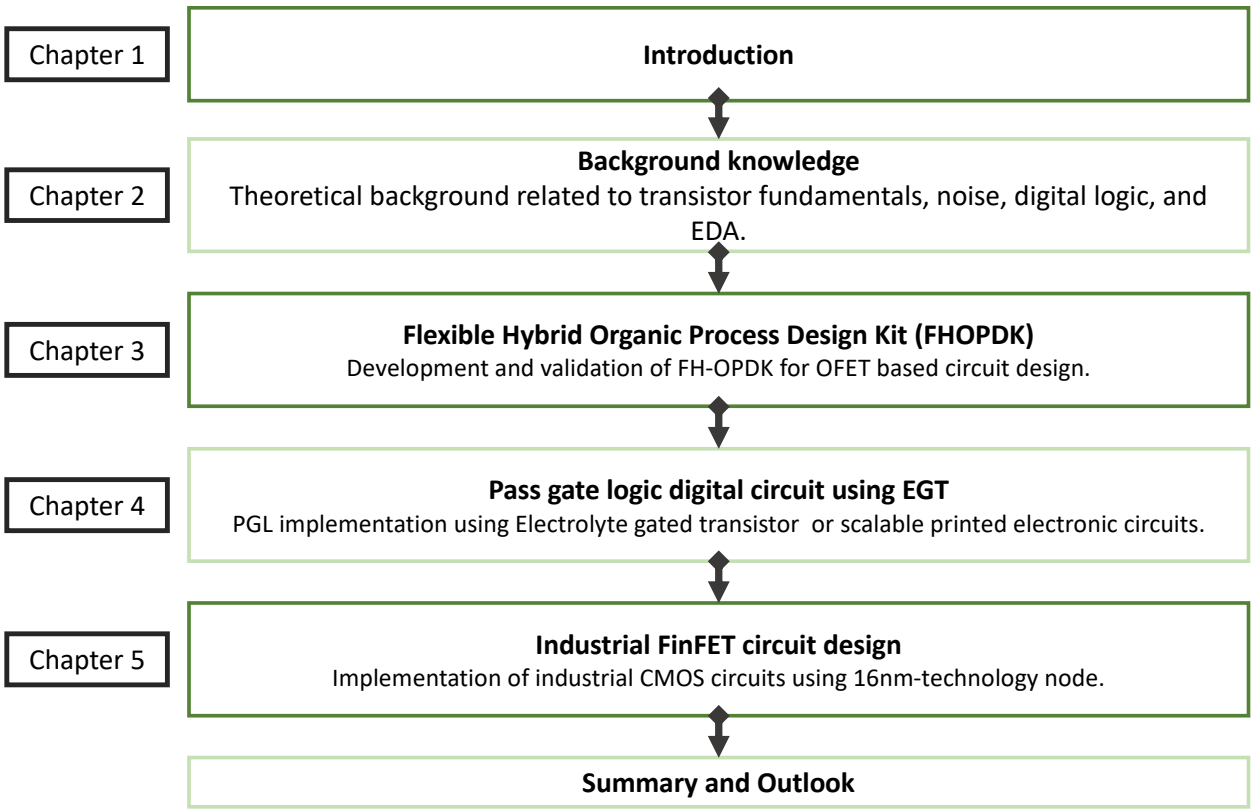


Figure 1.2: Organization and workflow of the thesis, showing the progression from background knowledge to the development of the FH-OPDK, EGT-based circuit methodologies, industrial FinFET integrated circuit implementation, and the concluding summary.

2. Background information

2.1 Transistor fundamentals

Transistors are fundamental active devices used in modern electronic circuits to control and amplify electrical signals [18]. In digital electronics, transistors primarily operate as electrically controlled switches that enable the implementation of logic functions and signal processing. The operation of most contemporary integrated circuits is based on Field Effect Transistors (FETs), in which the current flow between two terminals is controlled through an electric field applied at a third terminal [3,4].

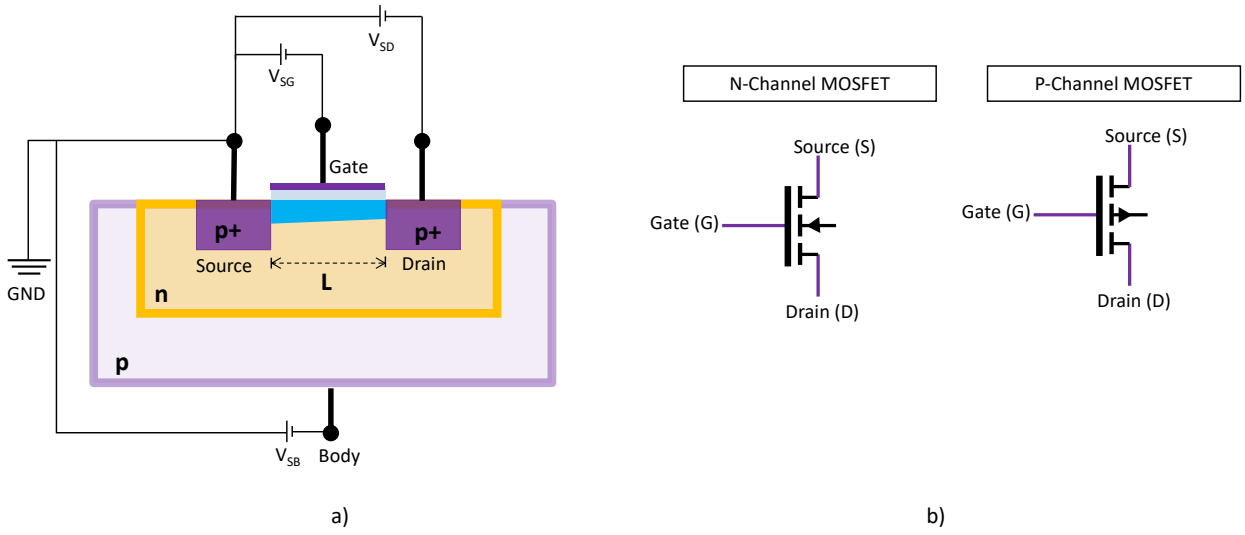


Figure 2.1: a) Cross-sectional structure of a Metal Oxide Semicondutor Field Effect Transistor (MOSFET) showing source, drain, gate, and body terminals with applied bias voltages, b) Standard circuit symbols of n-channel and p-channel MOSFETs.

A FET typically consists of three terminals referred to as source, drain, and gate, as shown in Fig. 2.1. The source and drain terminals define the conduction path through the semiconductor channel, while the gate electrode controls the conductivity of this channel through an electric field applied across the gate terminal. This

modulates the carrier concentration within the semiconductor channel beneath the gate. As a result, the conductivity of the channel between the source and drain terminals can be controlled by the applied gate voltage [18].

The formation of a conductive channel is governed by the threshold voltage, which represents the minimum gate voltage required to create a conductive channel and allow current flow between the drain and source terminals. When the applied gate voltage exceeds this threshold value, charge carriers accumulate near the semiconductor–dielectric interface, forming a conductive path between the source and drain terminals. Once this channel is formed, a drain-to-source voltage can drive a current through the device, which is commonly referred to as the drain–source current [18].

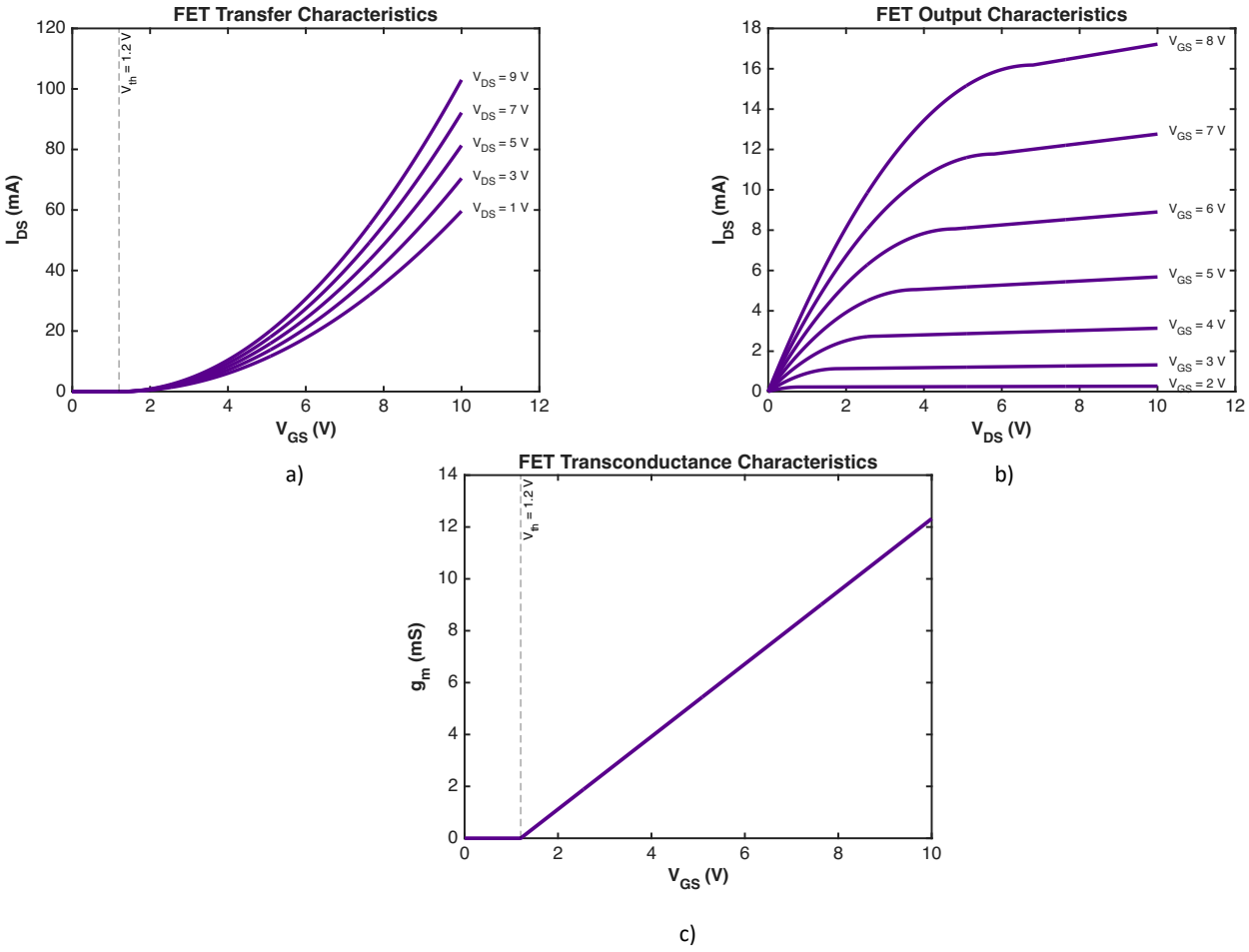


Figure 2.2: Simulated (a) transfer, (b) output, and (c) transconductance characteristics of the FET, showing the variation of drain current (I_{DS}) with drain-to-source voltage (V_{DS}) and gate-to-source voltage (V_{GS}), along with the corresponding transconductance (g_m) response. The threshold voltage (V_{TH}) is indicated by the dashed vertical line.

The electrical behavior of a FET can be described using the long-channel model equation [19]:

$$I_D = \frac{\mu_n C_{ox} W}{2L} (V_{GS} - V_T)^2 \tag{2.1}$$

where I_D represents the drain current, μ_n denotes the charge-carrier mobility, C_{ox} is the gate-oxide capacitance per unit area, W/L is the channel width-to-length ratio, V_{GS} is the gate-to-source voltage, and V_{TH} is the threshold voltage.

The electrical characteristics of a FET are commonly described using transfer and output characteristics. The transfer characteristics represent the relationship between the drain current and gate voltage, as plotted in Fig. 2.2(a), while the output characteristics describe the variation of drain current with drain-to-source voltage for different gate-bias conditions, as shown in Fig. 2.2(b). The transconductance is shown in Fig. 2.2(c). These characteristics provide important insight into the switching behavior, current-drive capability, and overall performance of the transistor [4].

Although the fundamental operating principle of FET remains similar across different technologies, the specific device structure, materials, and fabrication process can vary significantly. Different transistor structures employ alternative semiconductor materials, dielectrics, layers, and electrode materials, as well as fabrication processes that extend beyond conventional silicon-based transistors [5, 11].

2.2 Noise mechanisms in transistors

Noise in semiconductor devices refers to fluctuations in current or voltage generated by the random behavior of charge carriers [20]. This noise is not due to external sources, such as contacts or signal interference; rather, it is inherent to the device. The magnitude of noise depends on the device type, manufacturing process, and trap density. The inherent noise of semiconductor devices is an important parameter for assessing device quality and reliability, and it is often used when evaluating new devices. Noise sources can originate from fundamental physical mechanisms associated with charge transport and influenced by operating conditions and material imperfections [21], as illustrated for thermal and flicker noise in Fig. 2.3. The different noise types are explained below.

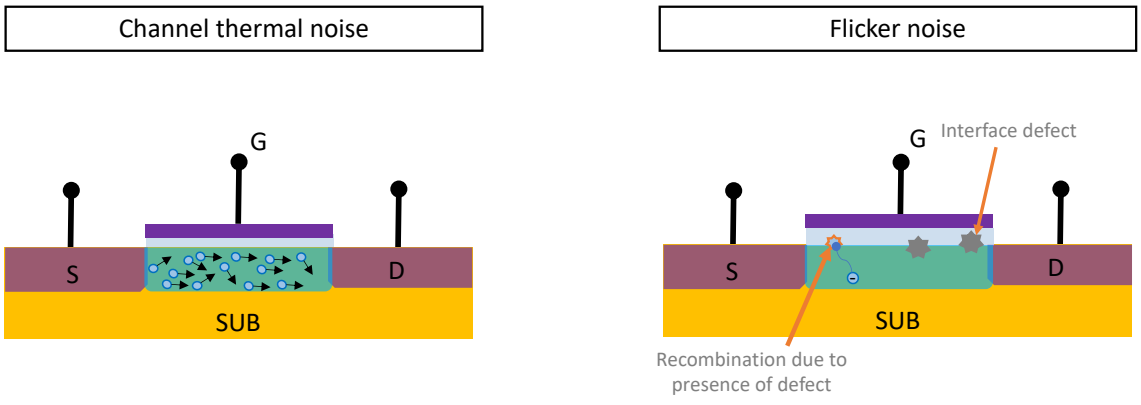


Figure 2.3: Illustration of channel thermal noise and flicker-noise mechanisms in a FET, highlighting carrier fluctuations in the channel and defect-assisted carrier trapping/de-trapping at the semiconductor–oxide interface.

2.2.1 Types of noise

Thermal noise.

Thermal noise arises from the random motion of charge carriers caused by thermal excitation, as shown in Fig. 2.3 [22]. The thermal motion of carriers alters terminal voltages and currents and is influenced by temperature and the resistance of the conducting element. The thermal-noise voltage is described by the Nyquist equation:

$$\overline{V_n^2} = 4kTR\Delta f \tag{2.2}$$

where k is the Boltzmann constant, T is the absolute temperature, R is the resistance, and Δf is the measurement bandwidth. Thermal noise, also known as Johnson–Nyquist noise, exhibits a white-noise spectrum, meaning that the power spectral density remains constant over frequency [22]. The voltage-noise power spectral density $S_V(f)$ is given by:

$$S_V(f) = 4kTR \tag{2.3}$$

Shot noise.

Shot noise in semiconductor devices arises from individual charge carriers crossing a potential barrier in a random and statistically independent manner. The noise is most prominent in devices with p–n junctions and is commonly modeled as white noise, i.e., with approximately constant power spectral density over a wide frequency range [23]. The shot-noise current power spectral density is expressed as [21]:

$$S_I(f) = 2qI \tag{2.4}$$

where q is the elementary charge.

Generation-Recombination (GR) noise.

GR noise originates from fluctuations in the number of carriers due to generation–recombination centers. Changes in the carrier number modulate the device conductance. GR noise depends on temperature and biasing conditions. The power spectral density of GR noise is described as [21]:

$$S(f) = \frac{4\langle \Delta N^2 \rangle \tau}{1 + (2\pi f \tau)^2} \tag{2.5}$$

where $\langle \Delta N^2 \rangle$ is the variance of the carrier-number fluctuations and τ is the carrier lifetime. Since different generation–recombination centers possess different lifetimes, the total GR-noise spectrum can be approximated as the superposition of multiple Lorentzian spectra.

Flicker noise.

Flicker noise originates from defects and material imperfections in semiconductor devices. A notable property of flicker noise is that it dominates at low frequencies; therefore, it is also referred to as Low Frequency Noise (LFN), while white noise

is typically observed at higher frequencies. Flicker noise is influenced by the operating point and is often referred to as $1/f$ noise because the noise spectrum varies approximately as $1/f^{\gamma}$, where γ is close to unity [24].

$$S(f) \propto \frac{1}{f^{\gamma}} \tag{2.6}$$

where the exponent γ is typically close to unity.

In addition to semiconductor devices, flicker noise has also been observed in liquid metals, Josephson junctions, and electrolyte solutions. Therefore, the physical origin of flicker noise depends strongly on the material system and device structure [24].

The power spectral density of flicker noise is generally expressed as [25]:

$$S_I(f) = \frac{K I_{DC}^{\alpha}}{f^{\gamma}} \tag{2.7}$$

where K, α, and γ are empirical constants that depend on the device and fabrication process, f is the frequency, and I_{DC} is the direct current through the device.

For a well-designed system, flicker noise is often observed in the frequency range from 1 Hz to 10 kHz. The $1/f$ characteristic indicates that the noise power increases as $f \to 0$. The flicker-noise corner frequency f_c is the boundary frequency between the flicker-noise-dominated and white-noise-dominated regions.

Flicker noise is commonly described using two competing theories: McWhorter's number-fluctuation theory and Hooge's mobility-fluctuation theory. Experimental evidence has supported both models, and the dominant mechanism depends on the material and device structure.

McWhorter Number Fluctuation Theory The model was developed by A. L. McWhorter at MIT Lincoln Laboratory in 1957 [26]. It proposes that flicker noise is a surface effect [24]. McWhorter's theory states that noise is generated by fluctuations in the charge carrier number caused by charge trapping in surface states. These traps communicate with the channel through tunneling processes, causing fluctuations in the carrier concentration. The resulting variations in channel conductivity manifest as drain-current noise. The traps are spatially distributed within the oxide and have a time constant associated with the carrier capture and emission processes. Since the distribution of trap time constants is broad, the superposition of various trap-related emission processes leads to the characteristic $1/f$ frequency dependence of the noise power spectral density. The spectral density of the drain current with bias dependence is described as [26]:

$$\frac{S_{I_D}}{I_D^2} = \frac{q^2 kT\lambda N_{ST}}{WLC_{ox}^2 f^{\gamma}} \left(\frac{g_m}{I_D}\right)^2 \tag{2.8}$$

where λ is the tunneling attenuation distance, N_{ST} is the surface trap density, and g_m is the transconductance. The effective mobility is voltage dependent and can be described as:

$$\mu_{\text{eff}} = \frac{\mu_0}{1 + \theta(V_{GS} - V_{TH})} \tag{2.9}$$

where μ_0 is the low-field mobility and θ is the mobility attenuation factor [27].

Hooge Mobility Fluctuation Theory F. N. Hooge described $1/f$ noise as a bulk phenomenon within metallic films [24]. The empirical relation for $1/f$ noise in terms of resistance fluctuations is expressed as:

$$\frac{S_R}{R^2} = \frac{\alpha_H}{Nf} \tag{2.10}$$

where N is the number of free carriers in the bulk, and α_H is Hooge's constant.

Hooge's empirical relation attributes the origin of noise primarily to mobility fluctuations of charge carriers within the conducting medium. The theory is based on the observation that the normalized noise power spectral density is inversely proportional to the number of free carriers and frequency. The dimensionless constant, known as Hooge's parameter (α_H), is material dependent and serves as a useful metric to compare the intrinsic noise properties of different materials and devices [24]. Vandamme further adapted Hooge's theory for MOSFETs and described the drain current noise as [28]:

$$\frac{S_{I_D}}{I_D^2} = \frac{\alpha_H q \mu_{\text{eff}} V_{DS}}{f W L I_D} \tag{2.11}$$

Popcorn Noise

Popcorn noise, also known as burst noise or random telegraph signal (RTS) noise, is caused by the capture and emission of charge carriers within the transistor channel. It appears as sudden discrete fluctuations between two or more current or voltage levels [29]. The noise has a significant influence at lower frequencies and is affected by temperature, mechanical stress, and radiation-induced defects. It is commonly observed in MOSFETs and bipolar junction transistors containing crystal defects or trap states.

Power Spectral Density

For noise analysis, the noise is commonly represented using power spectral density (PSD), which describes the distribution of noise power with respect to frequency. The effect and spectral characteristics of each noise mechanism can be observed over different frequency ranges as displayed in Fig. 2.4.

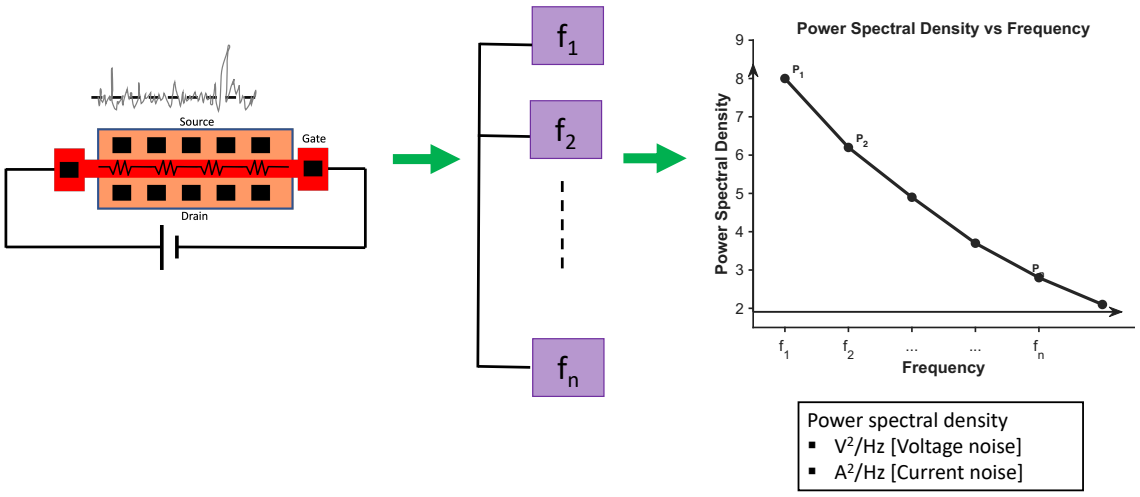


Figure 2.4: Extraction of frequency dependent power spectral density from measured device noise signals. Adapted from: Vikram Sekar, 2024 [30].

For transistors, thermal and shot noise are generally frequency independent and therefore exhibit a white-noise spectrum. In contrast, flicker noise shows an inverse dependence on frequency and dominates at lower frequencies. At higher frequencies, additional effects such as parasitic capacitance and carrier transport limitations can influence the signal performance [21].

The analysis of transistor noise in the frequency domain provides important insights for designing circuits optimized for specific frequency ranges.

2.3 Process design kit and EDA design flow

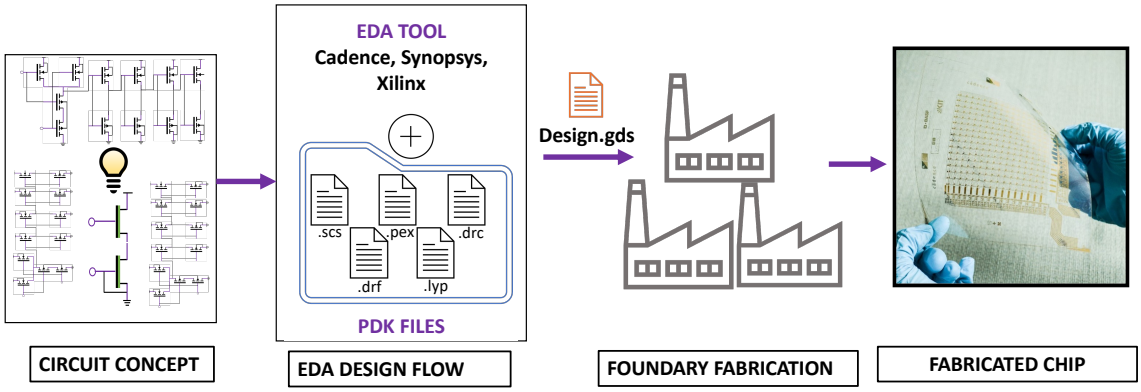


Figure 2.5: Semiconductor design-to-fabrication workflow from circuit conception to fabricated-chip realization [31].

The design and simulation of integrated circuits rely on a set of tools and models collectively known as the EDA environment. These tools allow circuit designers to create schematics, simulate device behavior, and verify the performance of digital and analog circuits prior to manufacturing. A key component enabling this workflow is the PDK, which provides the device models, design rules, and technology parameters required for circuit design within a specific fabrication process.

For emerging device technologies such as OFETs and EGTs, the development of accurate PDK models is particularly important because it can reduce optimization time and cost. In contrast to mature silicon technologies, where extensive device libraries already exist, novel transistor technologies require the creation of custom compact models and simulation frameworks. EDA tools use these models to perform circuit simulation based on Simulation Program with Integrated Circuit Emphasis (SPICE) and other numerical techniques. An overview of the EDA/PDK-based design flow is shown in Fig. 2.5.

In this work, FH-OPDK-based device models are used within the EDA environment to simulate the behavior of the investigated transistor technologies. The simulation framework allows the performance of digital standard cells and larger circuit blocks to be analyzed, providing insights into the feasibility of implementing complex digital systems using the proposed device technologies.

2.4 Standard-cell design methodology

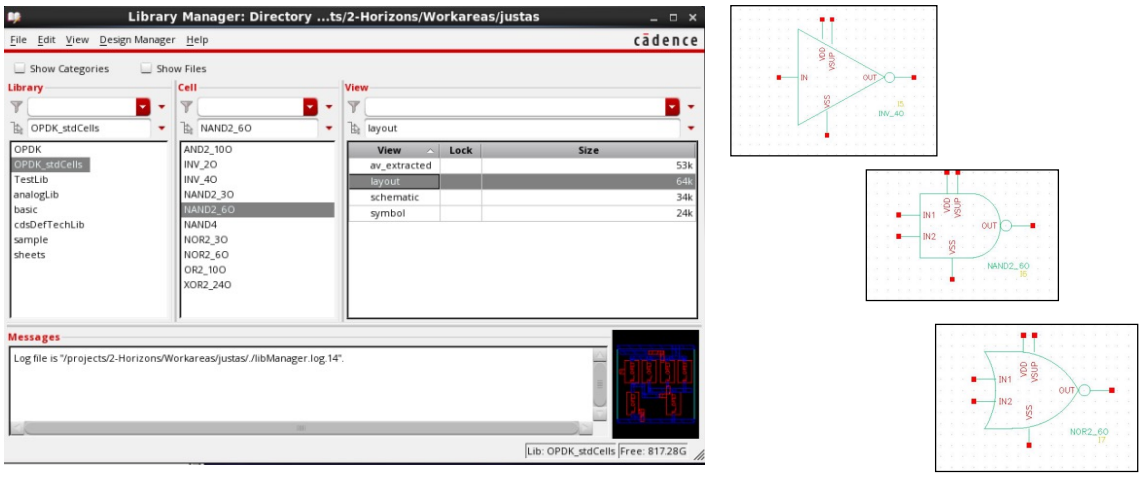


Figure 2.6: Custom standard-cell library development and implementation within the EDA design environment [31].

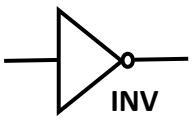
Standard-cell design is a widely used methodology in digital integrated-circuit development in which complex digital systems are constructed using a library of predefined logic gates. Each standard cell implements a specific logic function, such as an inverter, NAND, or NOR gate, and is characterized by well-defined electrical behavior and timing characteristics. By combining these reusable circuit blocks, larger digital systems can be designed in a modular and scalable manner.

In this thesis, standard cells were designed using the device models provided through the developed FH-OPDK and simulated within an EDA environment, as shown in Fig. 2.6. Circuit schematics were constructed using transistor-level implementations based on the investigated logic topologies, and transient simulations were performed to analyze the dynamic switching behavior of the circuits. From the simulated waveform responses, key timing parameters such as propagation delay were extracted. This methodology enables a systematic evaluation of transistor technologies at the circuit level. By analyzing the switching behavior of the implemented standard cells, the suitability of the devices for digital logic applications can be assessed before integrating the circuits into larger functional blocks.

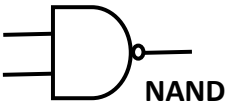
2.5 Digital circuitry

2.5.1 Fundamentals of digital logic circuits

Digital logic circuits are the basis of modern electronic systems by enabling the processing of binary information using discrete voltage levels that represent logic states. In digital implementations, signals are interpreted as two logic levels: logic 0, which usually corresponds to a low voltage (ground), and logic 1, which corresponds to a high voltage (supply voltage). Logic operations on these signals are performed using elementary logic gates such as inverters, NAND, and NOR gates, which implement Boolean functions and serve as the fundamental building blocks of digital systems [18]. An overview of standard logic gates and their truth tables is illustrated in Fig. 2.7.



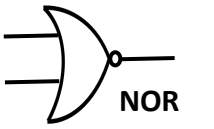
A	Out
0	1
1	0



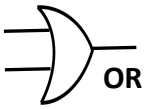
A	B	Out
0	0	1
0	1	1
1	0	1
1	0	0



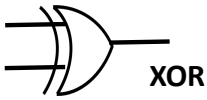
A	B	Out
0	0	0
0	1	0
1	0	0
1	0	1



A	B	Out
0	0	1
0	1	0
1	0	0
1	0	0



A	B	Out
0	0	0
0	1	1
1	0	1
1	0	1



A	B	Out
0	0	0
0	1	1
1	0	1
1	0	0

Figure 2.7: Logic symbol and truth tables of fundamental digital standard-cell gates [31].

In integrated circuit development, these logic gates are typically realized as standard cells, which are reusable circuit blocks that provide well-defined functionality and electrical characteristics. Standard cell fabrication plays a crucial role when evaluating and benchmarking emerging device technologies. Implementing a set of basic logic gates allow the fundamental switching behavior of the underlying devices to be assessed in a circuit-level context. Because these cells represent the smallest functional units of digital logic, they provide an effective platform for verifying whether a new technology can reliably perform digital operations [4]. Among the standard-cell library element INV, NAND, and NOR gates play a critical role due to their functional completeness, enabling the realization of arbitrary combinational logic circuits. Fabricating and characterizing these gates enable the evaluation of key performance parameters such as switching behavior, timing characteristics, and propagation delay. These parameters determine how quickly logic transitions propagate through a circuit and therefore directly influence the achievable operating speed of digital systems [18]. The propagation delay describes the time required for a transistor at the input of logic gate to produce the corresponding transition at the output. Analyzing the delay characteristics of standard cells provides insight into the dynamic response of circuit and allows different circuit topologies to be compared under identical conditions [18]. Consequently, the implementation and characterization of basic logic gate serve as an important benchmark for validating new device technologies. By analyzing the switching behavior and timing characteristics of these standard cells, it is possible to assess the suitability of the technology

for constructing more complex digital systems [4]. While digital circuits are defined by Boolean logic operation, their physical implementation depends on the underlying circuit topology used to realize the logic function. A logic topology describes how active devices are arranged to implement pull-up and pull-down networks that generate the desired output voltage levels. Different topologies can realize the same Boolean function while exhibiting different switching characteristics, timing behavior, and implementation complexity [18]. The following subsections introduce the most relevant logic gate topologies considered in digital circuit design, including standard CMOS logic, Transistor transistor logic (TTL), pseudo-CMOS logic, and pass gate logic.

2.5.2 Circuit Topologies

2.5.2.1 Standard CMOS topology

CMOS logic is the dominant topology used in modern digital integrated circuits due to its low static power consumption, high noise immunity, and excellent scalability [4]. It employs complementary pairs of p-type and n-type transistor arranged in pull-up and pull-down network, as shown Fig. 2.8. The pull up network connects the output node to the positive supply voltage (V_{DD}), while the pull-down network connects the output to the ground. Depending on the input conditions, only one of these networks conducts in the steady state, ensuring that the output is actively driven to either logic high or logic low with negligible static power dissipation [18].

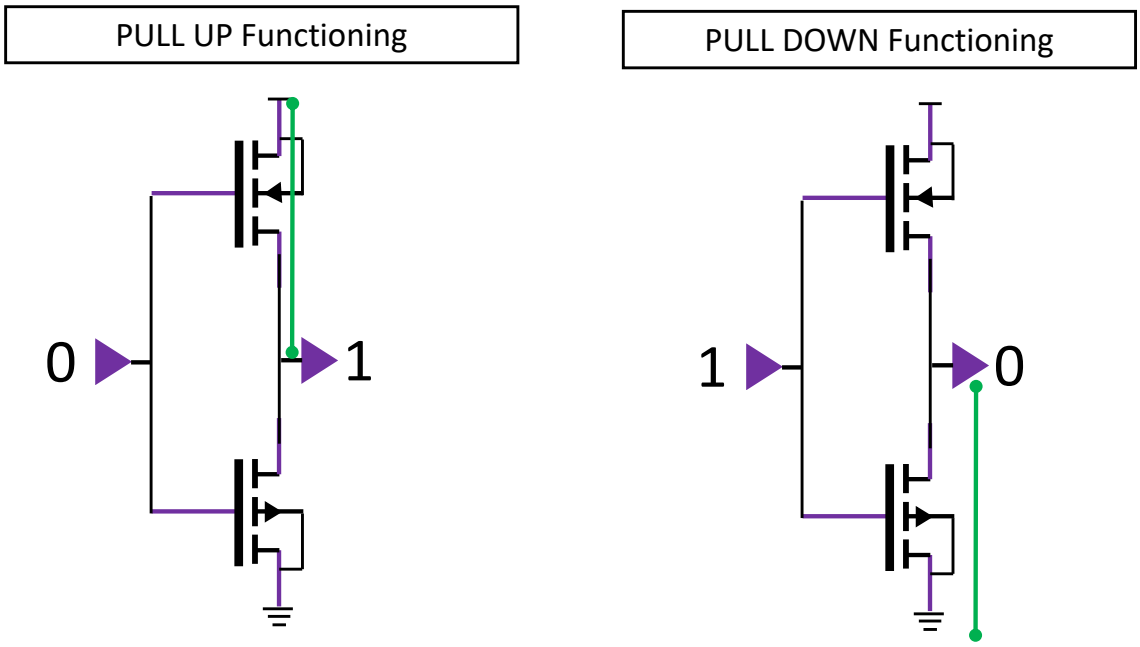


Figure 2.8: Operating principle of CMOS inverter through complementary pull-up and pull-down networks. [31]

As shown in Fig 2.8, CMOS logic employs a complementary structure consisting of a P-Channel MOSFET (PMOS)-based pull up network and an N-Channel MOSFET (NMOS)-based pull-down network. In stable operating states, one network conducts while the other remains non-conductive, thereby connecting the output node either to V_{DD} or to ground. This complementary operation provides high noise margins, low

static power dissipation, and robust switching characteristics. Through appropriate series and parallel interconnections of the pull-up and pull-down transistors, CMOS circuits can implement arbitrary Boolean functions, with NAND and NOR gates serving as fundamental building blocks for digital logic design. Due to its robust switching characteristics, scalability, and compatibility with modern semiconductor fabrication processed, CMOS has become the standard implementation style for digital logic in contemporary integrated circuits.

2.5.2.2 RTL Topology

In emerging transistor technologies, digital logic circuits are often implemented using load-basic logic structures due to limitation in device polarity and fabrication processes. For instance, many organic semiconductor technologies, predominantly provide reliable p-type transistors as stable complementary n-type devices are rare difficult [32,33]. As a result, fully complementary circuit architecture such as CMOS cannot always be implemented. Instead, digital logic is frequently realized using unipolar logic structure, where a single transistor type performs the switching operation and a load element defines the output voltage level.

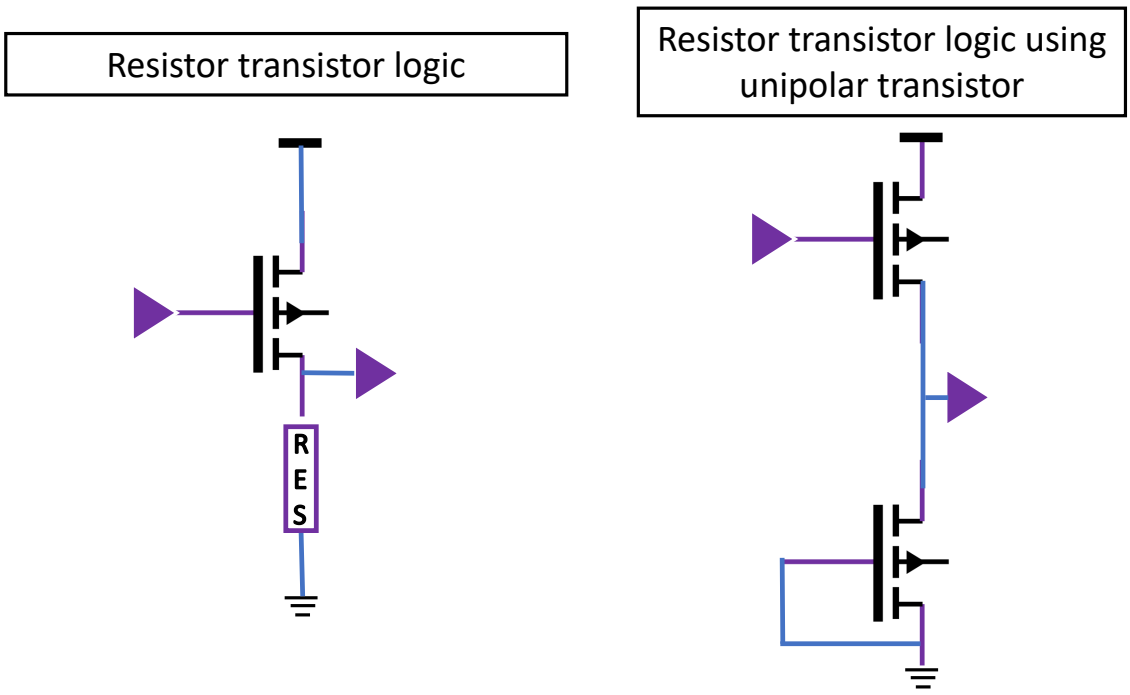


Figure 2.9: Schematic representation of resistor-transistor logic and unipolar transistor logic inverter architectures.

In the circuit investigated in this work, the load element is implemented using a p-type transistor biased with a fixed gate voltage, rather than a passive resistor as in Fig. 2.9. By applying a constant Direct Current (DC) bias to the gate terminal, the transistor operates in a region that provides a controlled conduction path between the output node and the supply voltage, thereby behaving as an effective resistive load. This approach simplifies fabrication since it avoids the need for dedicated passive resistor structures and allows the entire circuit to be implemented using the same transistor technology. Such transistor-load configurations are commonly used

in organic electronics and other unipolar device technologies to realize digital logic gates and to circuit level switching behavior and timing characteristics. [34], [35].

2.5.2.3 Pseudo-CMOS topology

Pseudo-CMOS logic represented a simplified variation of complementary CMOS logic that can be adapted for unipolar transistor technologies. Since only one transistor polarity is available, complementary pull-up and pull-down transistor network cannot be implemented as in conventional CMOS circuits. In this configuration, the pull-up path is controlled by the input signal through a switching p-type transistor, which connects the output node to the supply voltage when activated, The pull-down path is realized by a transistor that is biased with a fixed gate voltage, causing it to operate as a continuously conducting load element that connects the output node towards ground as in Fig. 2.10. The output voltage is therefore determined by the interaction between the switching pull-up transistor and the biased pull-down device [35].

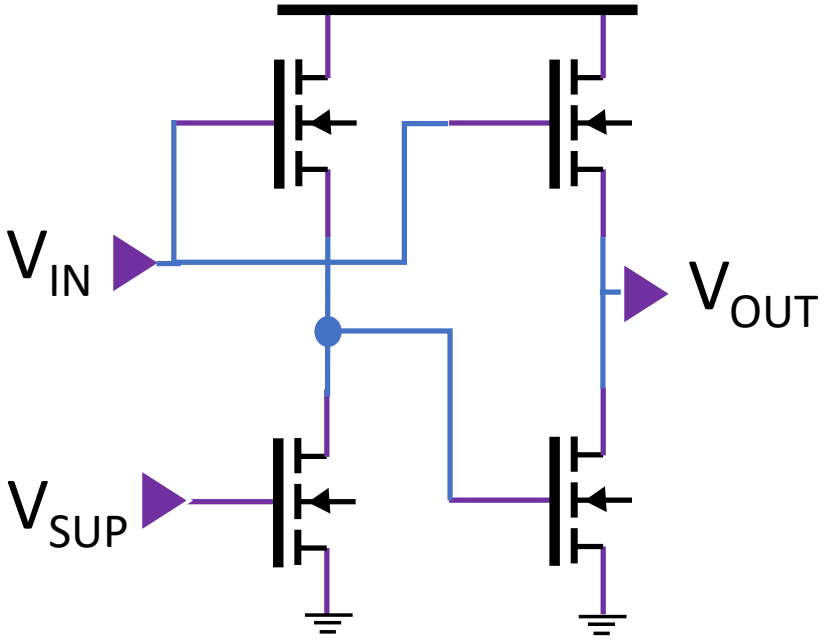


Figure 2.10: Schematic representation of an inverter designed using pseudo-CMOS transistor.

This approach is particularly advantageous in organic electronics, where achieving stable complementary transistor pairs can be challenging [34]. In addition, the presence of a permanently biased transistor in the pull-down network modifies the switching dynamics compared to fully complementary CMOS circuits. The output voltage depends on the relative conduction strengths of the switching transistor and the load transistor, which influences the charging and discharging behavior of the output node and therefore affects timing characteristics such as propagation delay [18].

2.5.2.4 Pass-gate logic

Conventional digital logic families, such as CMOS, Resistor transistor logic (RTL), and pseudo-CMOS, realize Boolean functions through dedicated pull-up and pull-

down networks. While these approaches provide reliable logic operation, they generally require a relatively large number of transistors. When transistor technologies are predominantly unipolar, implementing compact digital circuits using these conventional logic styles becomes challenging. Consequently, alternative circuit topologies that efficiently utilize a single transistor polarity are required.

Pass-gate logic addresses this challenge by using transistors as electrically controlled switches that directly transfer logic signals between circuit nodes rather than generating output levels through complementary networks. When the control signal activates the transistor, a conductive channel is formed, allowing the input signal to propagate to the output; when the control signal is inactive, the transistor switches off, interrupting the conduction path. Compared with conventional logic families, pass-gate logic reduces transistor count and circuit complexity, making it particularly attractive for emerging transistor technologies. Although signal degradation due to the threshold voltage must be considered, pass-gate logic remains an efficient solution for implementing compact digital circuits using unipolar devices [18].

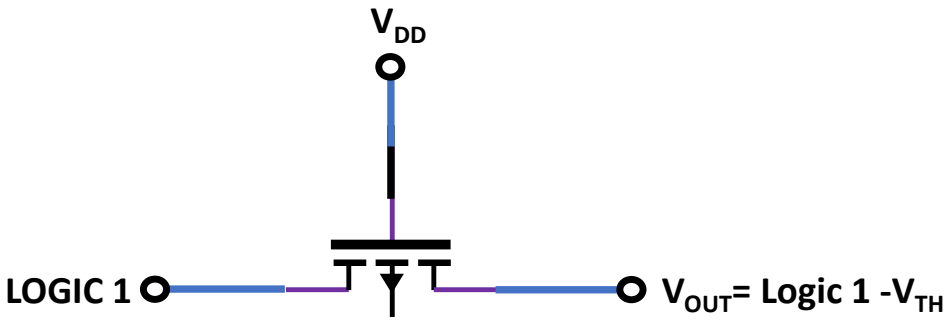


Figure 2.11: Schematic representation of a single-transistor pass gate.

In conventional CMOS implementations, pass gates are realized using transmission gates, which require n-type and p-type transistors connected in parallel. In emerging technologies, Pass Gate Logic (PGL) circuits can instead be realized using a unipolar transistor, as shown in Fig. 2.11. The single transistor acts as the switching element that controls signal propagation between circuit nodes.

In summary, digital logic circuits rely on the implementation of Boolean operations through physical circuit topologies that determine switching behavior and timing performance. Standard CMOS topologies remain dominant for modern integrated circuits due to scalability and reliable logic-level restoration. However, in many emerging device technologies complementary transistor structures are not available; therefore, alternative circuit topologies based on unipolar devices and load-based logic structures are required. Topologies such as RTL, pseudo-CMOS, and PGL provide practical solutions for realizing digital functionality in these technologies.

2.5.3 Power-performance assessment

Evaluating the performance of a digital circuit requires analyzing how quickly logic signals propagate through the circuit during switching events. An important metric used for this purpose is the propagation delay, which provides a direct measure of the dynamic response of a logic gate.

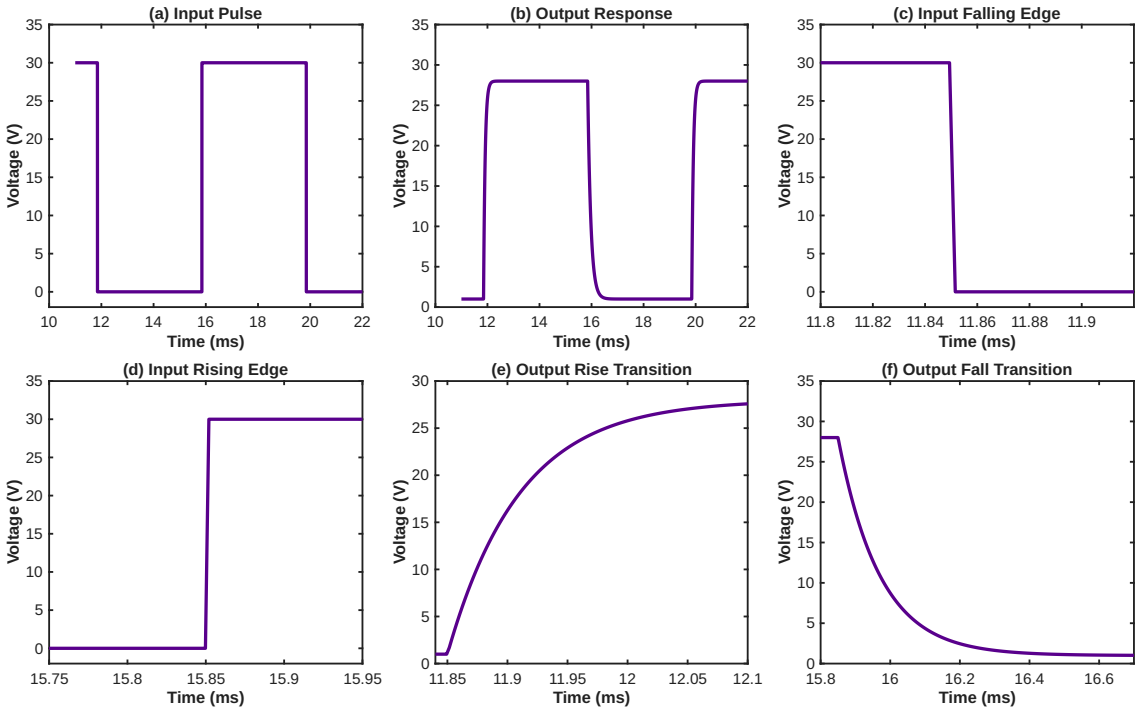


Figure 2.12: Transient response of an inverter showing input–output switching characteristics and transition dynamics.

Propagation delay is defined as the time interval between an input transition and the corresponding output transition of a logic gate. In digital circuits, two delay components are typically considered: the low-to-high transition delay and the high-to-low transition delay, as shown in Fig. 2.12 [18]. The propagation delay is commonly defined as:

$$t_{pd} = \frac{t_{PLH} + t_{PHL}}{2} \tag{2.12}$$

where t_{pd} is the propagation delay, t_{PLH} is the propagation delay for a low-to-high output transition, and t_{PHL} is the propagation delay for a high-to-low output transition.

In practice, propagation delay is commonly determined by measuring the time difference between the 50% transition point of the input signal and the 50% transition point of the output signal. This method provides a consistent reference for comparing switching performance across different circuit topologies and device implementations. The observed delay is largely determined by the charging and discharging of the capacitive load connected to the output node [18].

In this work, propagation delay is used as the primary metric for assessing the switching performance of the implemented logic gates. By examining the timing characteristics of inverter, NAND, and NOR standard cells, the dynamic behavior of the investigated circuit topologies can be compared and evaluated.

2.5.3.1 Propagation-delay extraction using a ring oscillator

Although the propagation delay of individual logic gates provides a direct measure of their switching performance, evaluating each gate separately does not fully represent the dynamic behavior of larger digital circuits. A commonly used benchmark for

assessing the overall speed of a digital technology is the ring oscillator. Since the oscillation frequency is directly determined by the propagation delay of the individual inverter stages, ring oscillators provide a simple and effective method for evaluating the dynamic performance of a standard-cell library and comparing different device technologies [18].

A ring oscillator exploits the finite propagation delay of cascaded inverters to generate a periodic output signal without requiring an external clock source. When an odd number of inverters are connected in a closed feedback loop, the inversion introduced by each stage prevents the circuit from reaching a stable logic state [3]. Instead, the logic transition continuously propagates around the loop, producing a self-sustained oscillation. Since the oscillation frequency is determined by the cumulative propagation delay of all inverter stages, ring oscillators provide a convenient and widely adopted method for evaluating the switching speed of digital technologies and standard-cell libraries.

A ring oscillator consists of an odd number (N) of cascaded inverter stages connected in a feedback loop, resulting in a periodic output waveform, as shown in Fig. 2.13. The oscillation period (T) is measured directly from the output waveform by determining the time interval between two successive peaks or zero crossings.

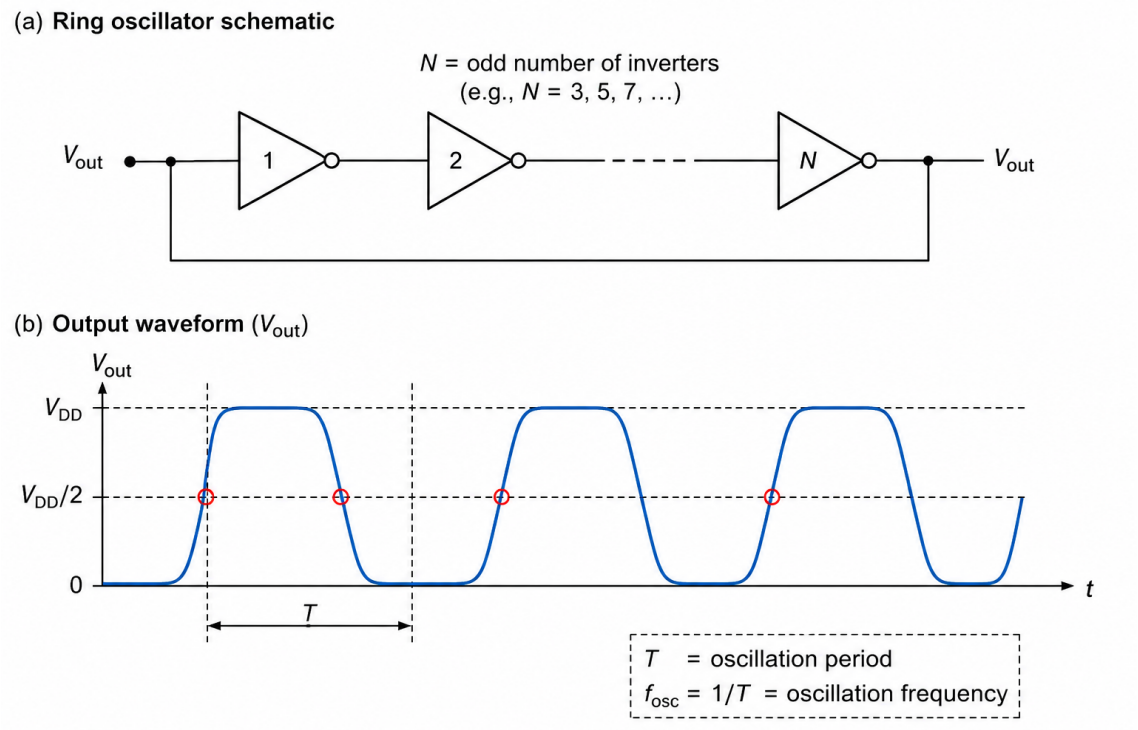


Figure 2.13: Ring oscillator architecture and corresponding output waveform. Adapted from:Generated using OpenAI image-generation tools based on the author's prompt.

The oscillation frequency (f) is given by

$$f = \frac{1}{T}, \tag{2.13}$$

Since each oscillation cycle corresponds to two signal transitions through all N inverter stages, the oscillation period can be expressed as

$$T = 2N\tau, \tag{2.14}$$

where τ represents the propagation delay of a single inverter stage. Therefore, the stage delay can be calculated as

$$\tau = \frac{1}{2Nf}, \tag{2.15}$$

This approach enables the extraction of the average inverter delay within the ring oscillator, providing a complementary method to direct transient measurements. It is particularly useful for validating the dynamic performance of the developed standard cell library under realistic operating conditions.

2.6 Selected technologies used in this thesis

The performance of field effect transistor strongly depends on the materials used for the semiconductor channel, gate dielectric, and electrode contacts, as well as processed used to assemble the device structure [5]. In organic field effect transistors, the semiconductor layer consists of conjugates organic molecules or polymers that support charge transport through overlapping π -orbitals. These materials can be deposited using solution-based techniques such as spin coating, printing or evaporation, enabling low-temperature fabrication on flexible substrates. Due to this reason, acpOFET are widely investigated for applications including flexible electronics, sensors and-large area electronics systems [10, 34]. EGT utilize an ionic electrolyte as the gate insulator. When voltage is applied to the gate electrode, mobile ions within the electrolyte migrates toward the semiconductor interface, forming electric double layers that strongly modulate the carrier density in the channel [13]. This mechanism enables high gate capacitance and allows transistor operation at relatively low voltages. EGT structures are therefore attractive for application requiring low-power operation and compatibility with solution-processed materials [36]. FinFET, on the other hand, are fabricated using advanced semiconductor processing techniques based on silicon technology. In these devices, the channel is patterned into a narrow fin structure using lithography and etching processes. The gate electrode is subsequently deposited so that it surrounds the fin on multiple sides, improving electrostatic control over the channel. This three-dimensional geometry has become widely adopted in modern integrated circuits due to its ability to support strong gate control as device dimension continues to scale [6].

3. Flexible hybrid organic process design kit

This chapter describes the hybrid organic printed transistor technology developed as part of the project "2-Horizon" (collaborators: KIT, Heidelberg University, InnovationLab, and Cadence GmbH). The chapter begins with the materials and processes used to fabricate the OFET [16]. This is followed by characterization of the transistor devices and the extraction of key device parameters, including threshold voltage, operating voltage, and carrier mobility. Additionally, a variation analysis is performed to account for technology variability. Finally, the device behavior is modeled and a FH-OPDK is created [16], representing a step forward in design automation for complex large-area circuits [37].

3.1 Introduction

An OFET refers to a transistor that contains an organic semiconductor as its channel. It can be fabricated via solution processing, mechanical transfer, vacuum evaporation, and inkjet printing. OFETs enable low-cost production and large-area electronics [34]. Compared to inorganic thin-film transistors, OFETs offer the advantage of mechanical flexibility, but typically require higher operating voltages [38]. Due to these characteristics, OFETs are widely used in biomedical applications [13, 39] as well as sensing applications [40], as shown in Fig. 3.1.



Figure 3.1: Application of OFET-based flexible electronics in wearable healthcare monitoring and sensing systems: (a) a skin-conformal biosensing patch and (b) an ultra-thin electronic-skin device [41].

OFETs were first demonstrated in 1986 by H. Koezuka, A. Tsumura, and T. Ando [42]. The concept of a field-effect transistor dates back to the 1930s [43], and OFETs have since emerged as a promising device class for low-cost, flexible electronics [34]. While OFETs do not yet match the performance of silicon MOSFETs, their compatibility with flexible substrates and low-cost fabrication processes makes them attractive for emerging applications such as wearable, printed, and large-area electronics [10].

Materials used to fabricate OFETs are typically based on aromatic or conjugated π-electron systems [44]. The semiconductor materials can be small molecules such as pentacene and rubrene or conjugated polymers such as P3HT and PBTTT [45]. OFETs are predominantly p-channel; however, in recent years improvements have been made toward n-type options [45]. Device performance depends on molecular packing, crystallinity, purity, side-chain engineering, and interface treatments that reduce traps and contact resistance [46]. The electrodes are usually gold, silver, or copper, or transparent conductors such as ITO, graphene, or PEDOT:PSS [34]. The gate dielectric is commonly a polymer film such as Poly(methyl methacrylate) (PMMA), Poly(4-vinylphenol) (PVP), or Cytop [46]. Fabrication can involve vacuum deposition for small molecules and solution processing or printing for polymers on flexible substrates such as Polyethylene Terephthalate (PET), paper, and textiles [34].

Despite considerable progress in organic semiconductor materials and fabrication processes, several challenges continue to hinder the widespread adoption of OFET technology. One of the primary limitations is the high density of trap states present within the semiconductor and at the semiconductor–dielectric interface. These trap states capture and release charge carriers, resulting in reduced mobility, threshold-voltage shifts, hysteresis, and increased device-to-device variability [47]. Furthermore, organic semiconductors are often susceptible to degradation caused by exposure to oxygen, moisture, and ambient environmental conditions, leading to reduced operational stability and shortened device lifetime [39, 47]. Variations in printing and deposition processes can also introduce significant parameter spread, making it difficult to achieve predictable and reproducible circuit performance. In addition, imperfections at the semiconductor–dielectric interface can increase charge trapping, degrade switching characteristics, and limit overall device reliability [34].

Even with these challenges, OFETs offer several unique advantages, including low-temperature processing, mechanical flexibility, lightweight construction, and compatibility with large-area manufacturing techniques. These characteristics make OFET technology particularly attractive for applications such as flexible displays, wearable sensors, RFID tags, electronic skin, and bioelectronic systems [39].

To translate advances in materials and fabrication technologies into practical electronic systems, a comprehensive circuit-design infrastructure is required in addition to high-performance materials and reliable printing technologies [47]. The development of accurate device models, circuit primitives, standard-cell libraries, and hardware-validated macrocells is essential for the design of complex printed electronic systems [48]. Accurate compact models capture electrical behavior, process variability, and non-ideal characteristics of OFET devices, enabling reliable circuit simulation and performance prediction. Furthermore, a PDK provides technology-specific information required for circuit implementation, including device models, layer definitions, fabrication constraints, and design rules. By integrating these components into EDA tools, the PDK supports schematic capture, simulation, layout implementation, and physical verification, thereby reducing design effort, shortening development cycles, and improving design reliability [49].

Within this context, a FH-OPDK is developed based on p-type OFET technology [48, 49]. The OFETs are fabricated using a solution-compatible process and subsequently characterized to obtain relevant electrical parameters. The capability of the FH-OPDK is demonstrated through the implementation of printed sensor systems and associated peripheral circuitry using the integrated design flow [40].

3.2 Technology, fabrication, and process

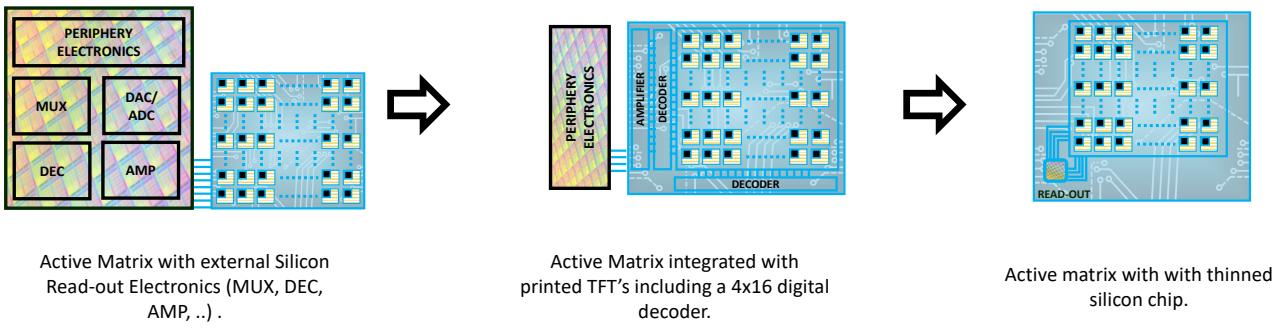


Figure 3.2: Progressive integration of active-matrix systems incorporating digital decoding and chip miniaturization [16], licensed under CC BY-NC-ND 4.0.

As discussed in Chapter 2, OFETs have emerged as a promising technology within the field of printed electronics due to their potential for low-cost, large-area, and flexible electronic systems. Beyond their traditional use in sensing and medical applications [13], OFETs are increasingly explored for digital and peripheral circuitry, enabling more complex functionalities in printed electronic systems [40]. Achieving high-performance OFET devices requires careful optimization of material systems and fabrication processes, as device characteristics are strongly influenced by semiconductor properties, dielectric interfaces, and electrode contacts [50]. Significant

research has therefore been directed toward developing material combinations and processing techniques that enable reliable and scalable transistor fabrication.

In this work, the investigated OFET technology is realized through the integration of multiple fabrication techniques and material layers to form a top-gate bottom-contact transistor structure. The process combines conventional microfabrication methods with solution-based deposition techniques to form the source/drain electrodes, organic semiconductor channel, dielectric layer, and gate electrode. The following section describes the device architecture, materials, and fabrication process used to realize the OFET devices investigated in this thesis.

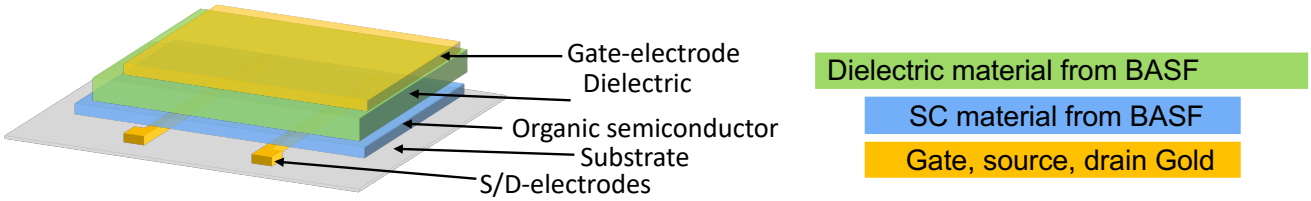


Figure 3.3: Layer diagram of the top-gate bottom-contact p-channel OFET [16], licensed under CC BY-NC-ND 4.0.

The fabrication of the OFET was carried out through a sequential process designed to form the source/drain contacts, organic semiconductor layer, dielectric layer, and gate electrode. First, the source and drain electrodes were patterned using photolithography. In this process, a photoresist layer is deposited and selectively exposed to ultraviolet light through a photomask, enabling the formation of well-defined electrode geometries after development and metal patterning. Gold was used as the electrode material due to its high work function and chemical stability [34]. Photolithography remains one of the most widely adopted techniques for precisely defining electrode structures in thin-film transistor fabrication due to its high resolution and reproducibility [34].

Following the formation of the source and drain contacts, the organic semiconductor layer was deposited using inkjet printing. The semiconductor material used in this thesis is a proprietary BASF organic semiconductor (XPRD01B06) that can be formulated for solution-processable organic electronics. Inkjet printing enables precise deposition of the semiconductor material directly into the transistor channel region while minimizing material waste and enabling compatibility with flexible substrates and large-area electronics. Solution-based deposition techniques such as inkjet printing are commonly employed in OFET fabrication due to their scalability and ability to form patterned semiconductor layers without additional lithographic steps [44].

After semiconductor deposition, a dielectric layer (a proprietary BASF material, XDRD41L01) was applied using spin coating. Spin coating enables the formation of uniform thin dielectric films by dispensing a liquid dielectric solution onto the substrate and rotating it at high speed, causing the liquid to spread evenly through centrifugal force. The resulting dielectric layer provides electrical insulation between the semiconductor channel and the gate electrode while enabling capacitive coupling that modulates charge accumulation in the channel. The quality and uniformity of

the dielectric layer are critical parameters that influence threshold voltage, leakage current, and overall device stability in OFETs [46].

Finally, the gate electrode was deposited on top of the dielectric layer using gold Physical vapor deposition (PVD). In PVD, metal atoms are vaporized in a vacuum environment and subsequently condensed onto the substrate surface to form a thin metallic film. Gold was selected for the gate electrode due to its excellent conductivity. The resulting layered structure forms the complete OFET device, where the gate electrode modulates charge transport in the organic semiconductor channel through the dielectric layer [34].

Figure 3.3 shows a cross-sectional schematic of the OFET.

3.3 Electrical characteristics

The electrical performance of the fabricated OFETs was evaluated through standard current–voltage characterization. Both transfer and output characteristics were measured to analyze charge-transport behavior, switching performance, and key device parameters such as field-effect mobility μ and threshold voltage V_{TH}. These measurements provide insight into conductive-channel formation, carrier injection at the source and drain contacts, and modulation of the drain current by the gate electrode.

3.3.1 Transfer characteristics

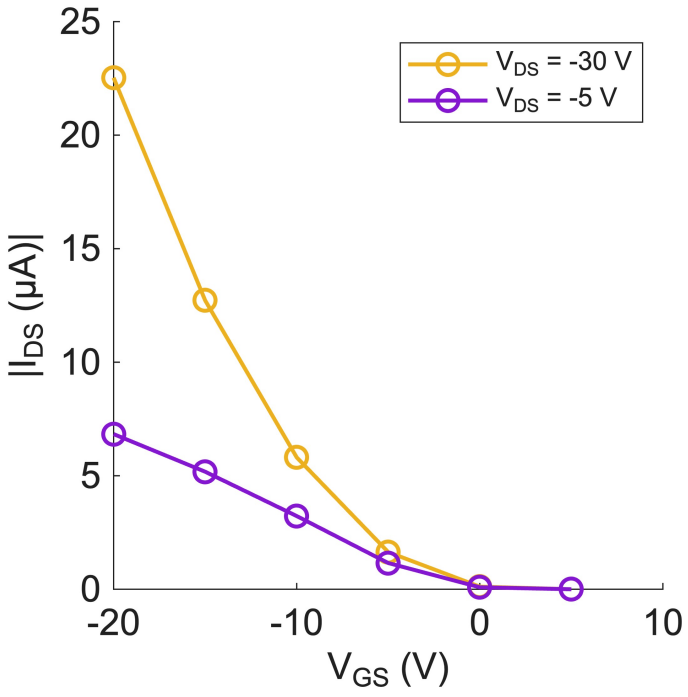


Figure 3.4: Measured transfer characteristics of the OFET at $V_{DS} = -5$ V and $V_{DS} = -30$ V [16], licensed under CC BY-NC-ND 4.0.

Transfer characteristics were measured by sweeping the gate voltage V_{GS} while maintaining a constant drain voltage V_{DS}. The absolute value of the drain current $|I_D|$ was recorded as a function of V_{GS} to evaluate the switching behavior of the device.

The measured transfer curves are shown in Fig. 3.4. As the gate voltage becomes more negative, the drain current increases significantly, indicating hole accumulation at the semiconductor–dielectric interface and the formation of a conductive channel between the source and drain electrodes. This behavior confirms p-type operation of the OFET.

At gate voltages close to zero (or positive values), the drain current is strongly suppressed, indicating off-state operation. As the gate voltage becomes more negative than the threshold voltage, the device transitions into the on state, where the channel conductivity increases rapidly. The logarithmic representation of the drain current highlights the wide dynamic range between the on and off states of the OFET. Such switching behavior is characteristic of OFET operation and reflects effective gate modulation of charge carriers at the semiconductor–dielectric interface [11].

3.3.2 Output characteristics

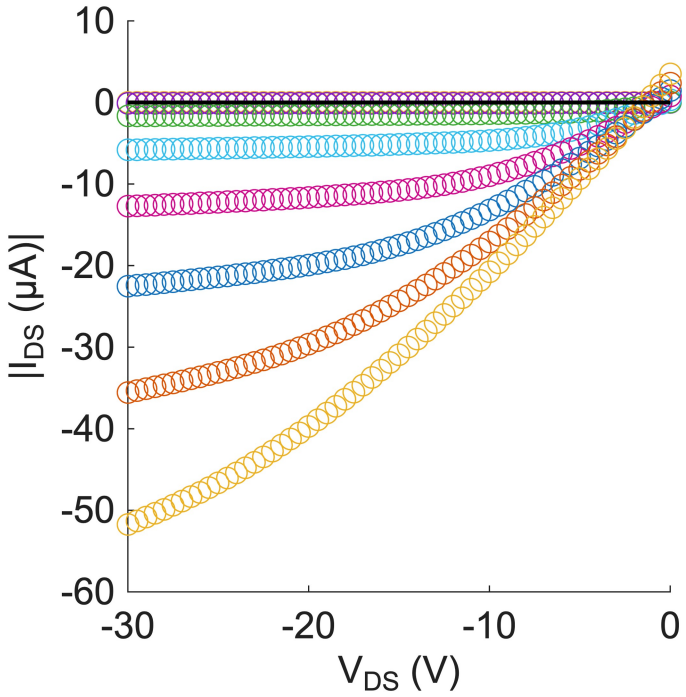


Figure 3.5: Measured output characteristics of the OFET for gate voltages V_{GS} from 0 to −30 V [16], licensed under CC BY-NC-ND 4.0.

The output characteristics of the OFETs were obtained by measuring I_D as a function of the drain voltage V_{DS} for different gate voltages. The measured output curves are presented in Fig. 3.5. At small drain voltages, the drain current increases approximately linearly with V_{DS}, indicating that the device operates in the linear regime, where the channel behaves as a voltage-controlled resistor. This region reflects efficient charge injection from the source electrode into the organic semiconductor channel.

As the drain voltage further increases, the device transitions into the saturation regime, where the current begins to level off due to the formation of a pinch-off region near the drain electrode. In this regime, the channel is partially depleted

near the drain, and the current becomes primarily controlled by the gate voltage. The observed output characteristics show smooth transitions from the linear to the saturation regime, indicating stable transistor operation and effective charge transport within the channel.

The gradual increase in drain current for increasingly negative gate voltages further confirms the accumulation-mode operation of the OFET. The absence of abrupt discontinuities in the output curves suggests reasonably good electrical contact between the gold electrodes and the organic semiconductor layer. Efficient charge injection at the metal–semiconductor interface is critical for achieving reliable OFET performance and minimizing contact-limited transport effects [46]. Overall, the measured

Table 3.1: Device performance summary

Parameter	**Value**
Mobility	0.35 $\mathrm{cm}^2/(\mathrm{V}\cdot\mathrm{s})$
Threshold voltage	-1 ± 0.7 V
Channel length	10–50 μm
Channel width	100–6500 μm
Dielectric thickness	780 nm

electrical characteristics demonstrate typical OFET behavior with clearly distinguishable linear and saturation regimes, as well as strong gate modulation of the drain current. The observed p-type conduction, negative threshold voltage, and moderate mobility values are consistent with previously reported results for solution-processed organic semiconductor devices [34], [44]. The measured average mobility of approximately $0.35\,\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$ indicates efficient charge transport within the printed semiconductor channel and is consistent with reported values for solution-processed OFETs, while the threshold voltage near -1 V suggests relatively low gate voltage requirements for channel formation. The device performance parameters were extracted from the measured transfer characteristics using the gradual channel approximation in the saturation regime, where the drain current is expressed as

$$I_{DS,\mathrm{sat}} = \frac{W}{2L}\mu C_{\mathrm{ox}}\left(V_{GS} - V_{TH}\right)^2 . \tag{3.1}$$

The field-effect mobility (μ) was determined from the slope of a linear fit to $\sqrt{I_{DS}}$ as a function of V_{GS}, while the threshold voltage (V_{TH}) was obtained by extrapolating the fitted line to the gate-voltage axis. The extracted device-performance parameters are summarized in Table 3.1.

To investigate the influence of transistor geometry on device performance, a systematic variation study was performed. OFETs were fabricated and characterized across a wide range of channel widths (100–6500 μm) and channel lengths (10–50 μm) to observe trends in mobility (μ) and threshold voltage (V_{TH}). For OFETs, electrical performance is often influenced by intrinsic semiconductor properties, geometry scaling, contact effects, and interfacial trapping phenomena [11].

3.3.3 Parameter variation

As shown in Fig. 3.6, the V_{TH} variation is plotted as a function of transistor channel width and length. The results indicate a broad distribution of V_{TH} values across

the investigated device dimensions, suggesting only a weak dependence of threshold voltage on channel geometry. The extracted threshold voltage exhibits a mean value of approximately −1 V with a standard deviation of 0.7 V. An inverse dependence of threshold voltage on channel length can be observed in Fig. 3.6(b). Literature reports that this channel-length dependence is associated with contact resistance and injection barriers at the source and drain electrodes [11].

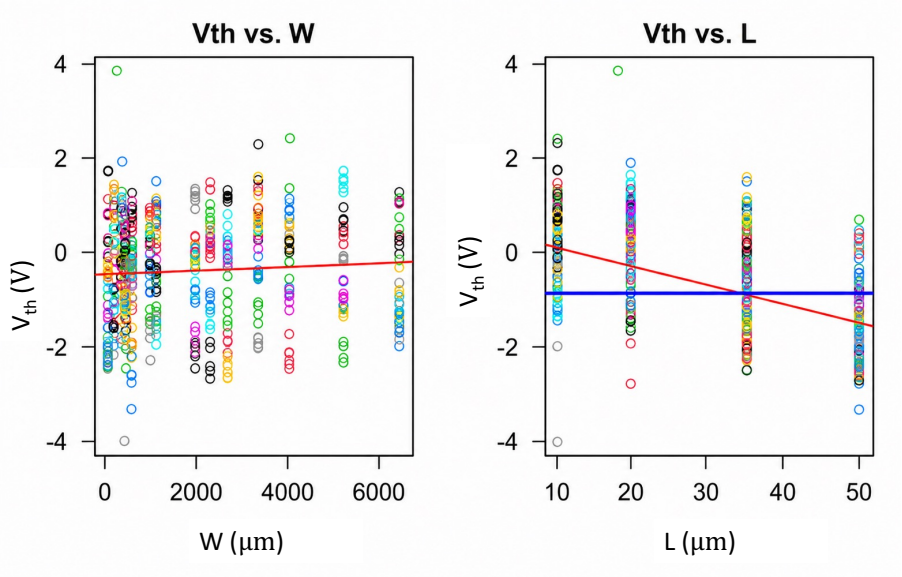


Figure 3.6: Threshold voltage variation as a function of transistor channel width (W) and channel length (L).

In Fig. 3.7, the mobility as a function of the geometric factor W/L is plotted. The mobility increases with increasing W/L ratio, although notable scatter is present across the devices. Ideally, the carrier mobility should be an intrinsic property of the semiconductor material; however, experimental studies often show a geometry dependence [11]. The extracted mobility of the evaluated OFETs can vary with channel dimensions due to parasitic resistances, contact effects, and trapping phenomena [11].

The extracted mobility is lower for smaller W/L ratios, where the influence of contact resistance becomes more pronounced relative to the intrinsic channel resistance. Consequently, the extracted mobility increasingly reflects contact-limited transport rather than the intrinsic transport properties of the organic semiconductor. Similar behavior has been reported by Bittle et al. [51], who attributed the geometry dependence of the extracted mobility to contact resistance and carrier injection barriers that distort the transfer characteristics.

3.4 Mathematical modeling of transistor data

The development of a reliable compact model is a crucial step for enabling circuit simulation and design using organic based technologies [52]. In contrast to conventional silicon-based devices, OFETs exhibit transport mechanisms dominated by localized states, energetic disorder and hopping conduction. As a result, traditional MOSFET models cannot directly capture the electrical behavior of OFETs, particularly in the subthreshold regime and under strong accumulation conditions [44]. To

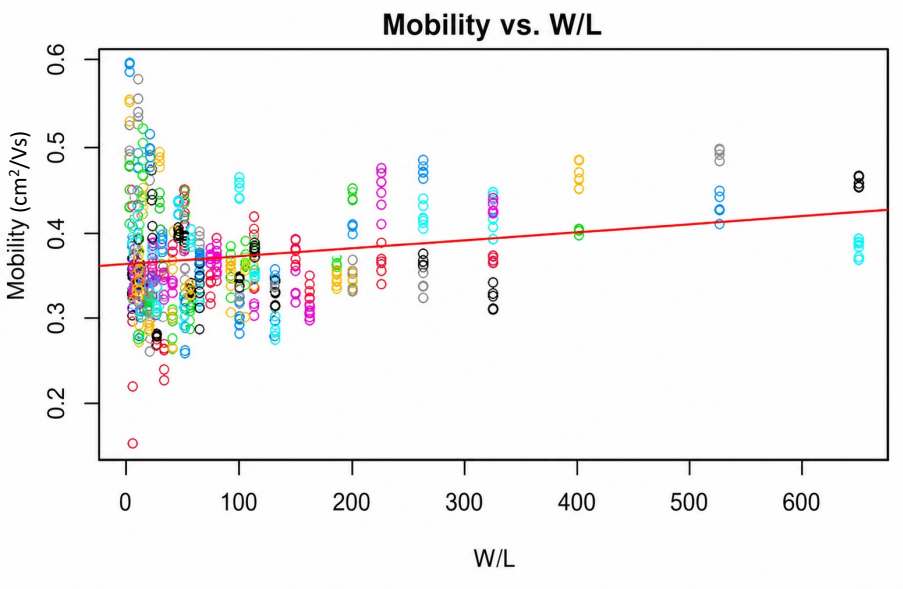


Figure 3.7: Variation of charge carrier mobility on transistor width-to-length ratio.

address these challenges, a compact modeling framework based on variable range hopping transport formulation is adopted. The modeling approach combines a physics-inspired current formulation with parameter extraction, statistical variability modeling, and capacitance modeling suitable for circuit simulation.

3.4.1 Variable range hopping model

Charge transport in organic semiconductors typically occurs via thermally activated hopping between localized states. This mechanism differs significantly from band transport in crystalline semiconductors and is often described using the VRHT. A flow chart explaining the VRHT is described in Fig. 3.8.

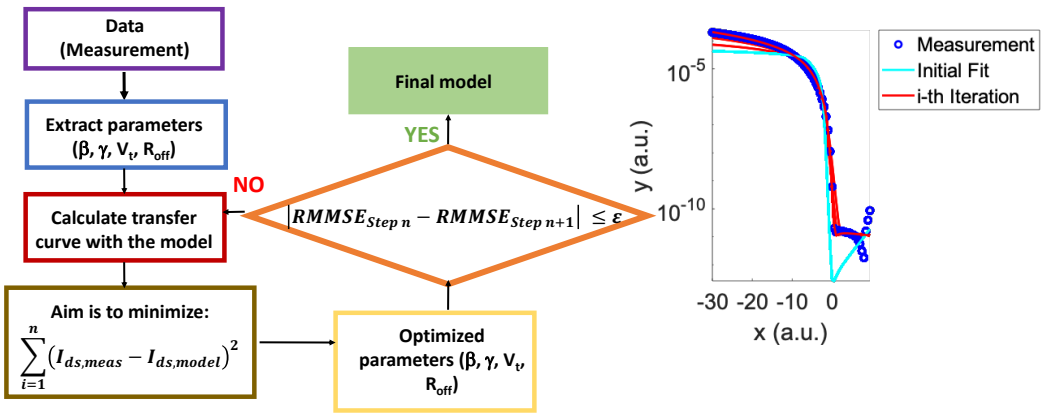


Figure 3.8: Flowchart of the iterative parameter-extraction and optimization procedure for OFET modelling [16], licensed under CC BY-NC-ND 4.0.

In OFETs, this transport mechanism strongly influences the transfer characteristics, particularly in the subthreshold and moderate accumulation regions. To capture

this behavior in a compact model suitable for circuit simulation, the drain current is introduced using an adaptation of the variable range hopping formulation [16]. The drain current is expressed as

$$I_{DS} = -\frac{\beta}{2}\left[F(V_{\mathrm{TH}} - V_{GS}, S)^{2+\gamma} - F(V_{\mathrm{TH}} - V_{GD}, S)^{2+\gamma}\right] + I_{\mathrm{off}}. \tag{3.2}$$

The function $F(x, S)$ is defined as

$$F(x, S) = S \ln\left(1 + e^{x/S}\right), \tag{3.3}$$

This function provides a smooth transition between the subthreshold and accumulation regimes and ensures numerical stability during circuit simulation [16]. The parameter S represents the subthreshold slope and determines the transition steepness between weak and strong accumulation regions.

The scaling factor β is given by

$$\beta = \frac{W}{L} C_G \mu_{\mathrm{eff}}, \tag{3.4}$$

Where W and L denote the channel width and length, respectively, C_G is the gate capacitance per unit area, and μ_{eff} represents effective mobility. This formulation captures the geometric scaling behavior of the device and allows the model to be applied to different transistor dimension.

I_{off} represents the off-state leakage current, which is particularly important in OFET devices due to trap-assisted transport and imperfect gate control. In the implemented model, the off current is parameterized as

$$I_{\mathrm{off}} = 10^{\left(V_{GS} C_{\mathrm{off},1} + C_{\mathrm{off},2}\right)}, \tag{3.5}$$

Which allows the off-state current to be fitted accurately across several orders of magnitude.

The parameter γ introduces a power-law dependence that captures deviations from the ideal quadratic current behavior typically assumed in MOSFET models. This parameter effectively accounts for the disorder-induced transport characteristics observed in organic semiconductors [53].

A resulting compact model provides a continuous and differentiable current formulation that accurately reproduces the transfer characteristics of OFET devices over several decades of current.

3.4.2 Parameter extraction and model optimization

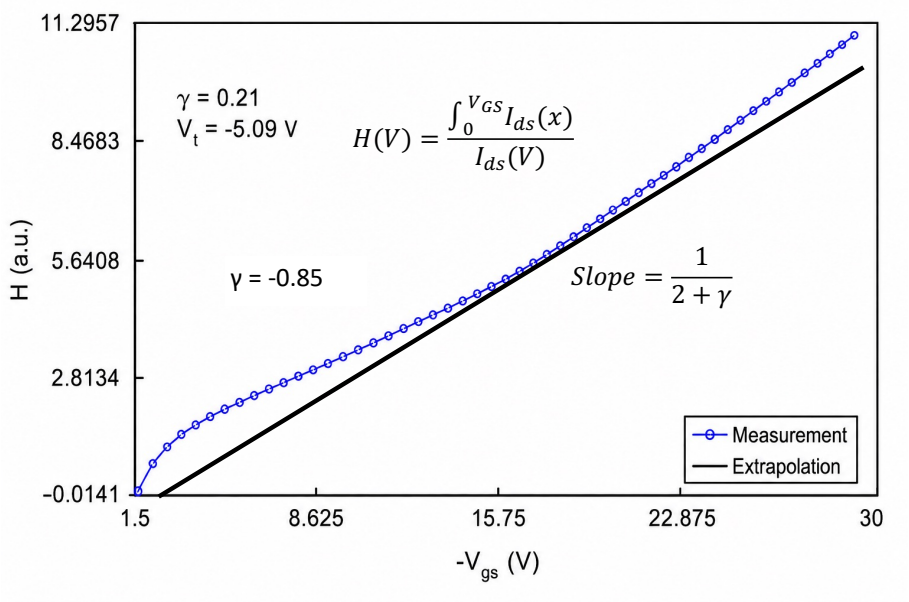


Figure 3.9: H-integral function derived from the transfer characteristics at V_{DS} = -30 V, used to extract the threshold voltage and power law parameter. DATE 2022 tutorial presented by P. Gupta, J. Lukosiunas, and S. Stehlin [54].

To accurately reproduce the measured device characteristics, a systematic parameter extraction and optimization procedure is implemented. Parameter extraction plays a critical role in compact modeling, as the accuracy of the resulting model strongly depends on the quality of extracted parameters [53]. The process begins with electrical measurements of the OFET transfer characteristics, providing the drain current IDS as a function of the gate voltage V_{GS} under a fixed drain bias condition. From the measured data, an initial set of model parameters is extracted, including the current scaling parameter β, the power law exponent γ, the threshold voltage V_{TH}, and the off-state resistance R_{off} [16, 54]. These parameters serve as starting values for the optimization algorithm. The accuracy between measured and simulated currents is quantified using the least-squared error function as shown in Fig. 3.9.

3.4.3 Variation modelling

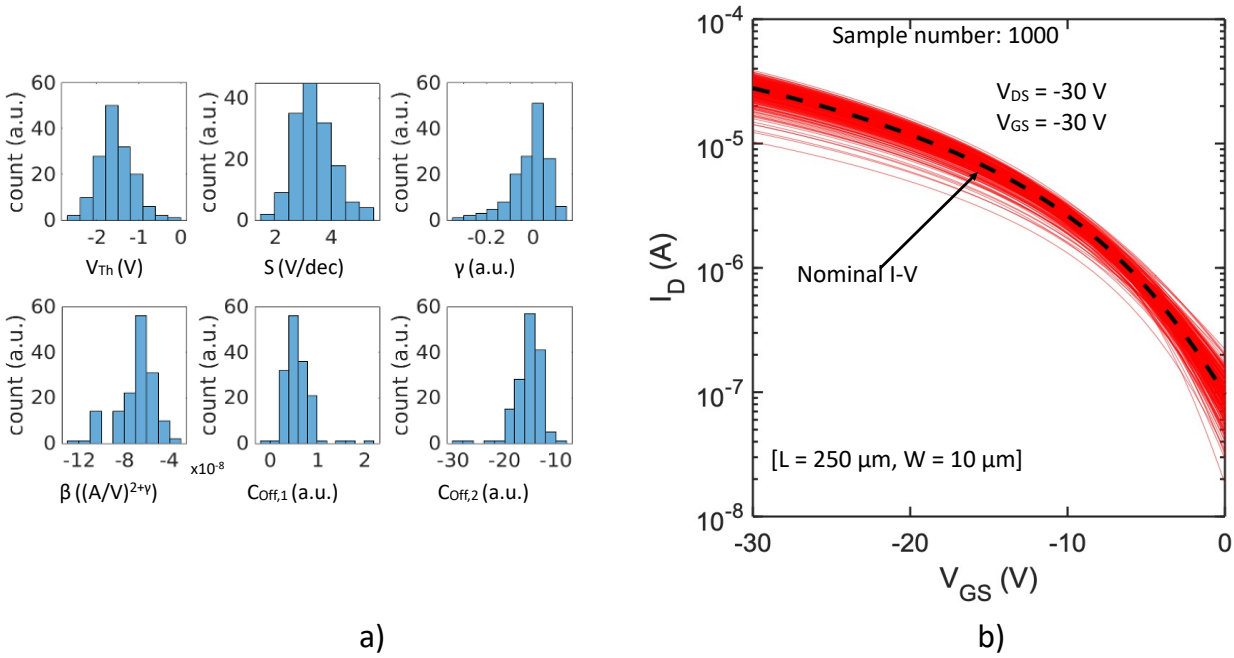


Figure 3.10: a)Measured parameter distributions of threshold voltage, subthreshold swing, power-law parameter, and fitting coefficients, b) simulated transfer characteristics illustrating device to device variability relative to nominal IV curve [16], licensed under CC BY-NC-ND 4.0.

Device variability is an important challenge in organic electronics technologies. Due to structural disorder in organic semiconductor films and variation in fabrication processes, OFET devices often show significant parameter fluctuations [11]. To characterize this variability, electrical measurements are performed on 151 OFETs. For each device, the compact model parameters were extracted using the optimization procedure described previously. The resulting parameters are used to construct statistical distributions for the most relevant parameters, including the threshold voltage V_{TH}, subthreshold slope S, power-law parameter *gamma*, current scaling factor β, and off-current coefficients $C_{off,1}$ and $C_{off,2}$, presented in Fig. 3.10. The extracted parameter distributions are incorporated into the compact device model to represent the measured device to device variations. During Monte-Carlo simulations, parameter values are randomly sampled from these statistical distributions for each transistor instance, enabling the variability observed int he measured devices to be propagated to the circuit level.

3.4.4 Capacitance modeling

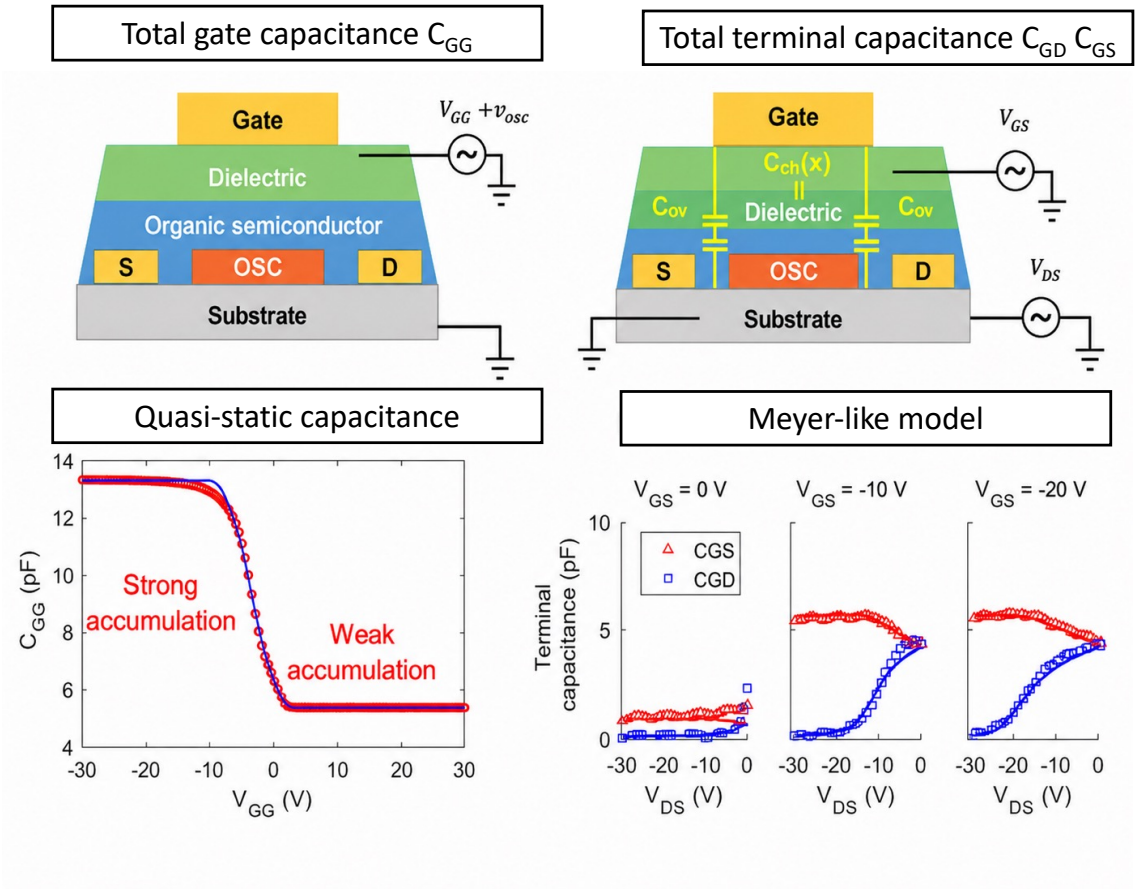


Figure 3.11: Extracted total and terminal capacitances of the OFET using quasi-static and Meyer like capacitance models [55, 56], licensed under CC BY-NC-ND 4.0.

Accurate modeling of intrinsic device capacitance is required for dynamic circuit simulations in addition to the static current–voltage characteristics. In OFET devices, the gate capacitance is strongly bias dependent due to the formation of the charge accumulation layer at the semiconductor–dielectric interface [56]. The total gate capacitance, C_{GG}, was experimentally characterized using quasi-static capacitance measurements, which reveal two operating regimes corresponding to weak and strong accumulation. In strong accumulation, channel formation increases the effective gate capacitance, whereas in weak accumulation the capacitance decreases due to reduced channel charge density.

To capture this behavior, a Meyer-like capacitance model was adopted [56], where the intrinsic gate capacitance is partitioned into the terminal capacitance C_{GS} and C_{GD} also illustrated in Fig. 3.11. These are expressed as

$$C_{GS} = \frac{2}{3} C_{GG,\text{int}} K_S \left(1 - \left(\frac{V_{GTe} - V_{DSe}}{2V_{GTe} - V_{DSe}}\right)^2\right), \tag{3.6}$$

$$C_{GD} = \frac{2}{3} C_{GG,\text{int}} K_D \left(1 - \left(\frac{V_{GTe}}{2V_{GTe} - V_{DSe}}\right)^2\right), \tag{3.7}$$

where $C_{GG,\text{int}}$ denotes the intrinsic gate capacitance, while K_S and K_D are fitting parameters controlling the charge partitioning between the source and drain terminals. This approach ensures smooth transitions between the operating regions and preserves charge conservation, which is essential for accurate transient circuit simulation [56].

3.5 Design environment and implementation

This section describes the EDA workflow and the implementation of a PDK tailored for printed OFETs named as FH-OPDK. It outlines the schematic, simulation, and layout tools employed, details the structure and function of key PDK components (mathematical model, Design Rule Check (DRC), and Layout versus Schematic (LVS) files), and examines how their implementation affects circuit design accuracy and manufacturability. In modern electronic system development, the design flow forms the backbone of circuit realization, linking conceptual design to final fabrication. A well-structured design flow integrates various EDA tools such as schematic editor, layout tools, simulators, verification engines, and physical design tools- into a seamless framework that supports correct and efficient circuit development. Each step in the design flow-from schematic creation, simulation and layout design to DRC, LVS verification, parasitic extraction, and final GDSII generation-relies on the proper configuration of technology files. These files, provides as part of the PDK, define the process-specific layers, design rules, device models, and fabrication constraints. As technology nodes evolve, differences in process parameters and manufacturing steps require precise activation of corresponding PDKs to ensure compatibility and accuracy. Fig. 3.12 illustrated the intermediate stages of the design flow, highlighting the interactions between different tools and the underlying technology data. By establishing a robust and automated flow, designers can achieve improved consistency, improved verification coverage, and enhanced productivity-whether targeting advanced silicon nodes or flexible, large-area printed electronics. Beyond the basic use of individual tool, embedding the correct technology data and PDK files within the flow ensures that the design environment reflects the specific fabrication process. This technology integrations allows to follow a clear, technology-driven flow that reduces manual effort, minimizes design errors, and accelerates time-to-tape out.

3.5.1 Flexible Hybrid Organic Process Design Kit (FH-OPDK)

PDK serves as the interface between device fabrication and circuit design, translating the physical characteristics of a technology into a standardized set of design resources that allow accurate simulation and layout implementation. In practice, the PDK ensures that circuit schematics, layout simulations correspond to the capabilities and constraints of the underlying manufacturing process. A typical PDK consists of several core components. First, the SPICE compact models describe the electrical behavior of the devices within the process. These models allow designers to simulate device performance and circuit functionality before fabrication. Second, DRC specify the geometric constraints required for reliable fabrications, including minimum spacing, widths, and overlap between layers. These rules ensure that the layout is manufacturable and help prevent fabrication defects. Third, the layer stack definition describes the physical structure of the process, including the available material

layers, their ordering, and their electrical roles such as electrodes, dielectric layers, and semiconductor regions. Together, these components allow EDA tools to support schematic capture, layout generation, verification, and circuit simulation within a consistent technological framework. For emerging electronic technologies, the availability of a PDK is particularly important. While novel devices may demonstrate promising performance at the device level, the absence of a standardized design infrastructure often prevents their adoptions in practical circuit design. By providing validated models, process information, and design rules, a PDK enables researchers and designers to explore circuit architecture, evaluate system-level performance and develop scalable applications. In context of organic electronics, the development of a dedicated OFET FH-OPDK represents a significant step toward bridging the gap between device research and functional circuit implementation as also illustrated in Fig. 3.12.

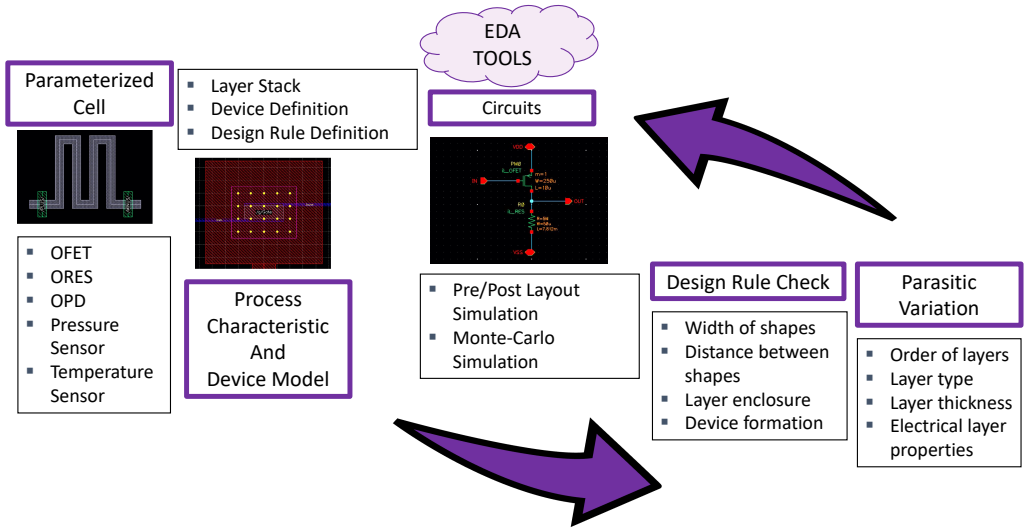


Figure 3.12: Process design kit flow enabling device modelling, circuit design, verification, and simulation. DATE 2022 tutorial presented by P. Gupta, J. Lukosiunas, and S. Stehlin [54].

The electronic design automation tool are specialized software applications used to design, analyze, verify, and implement electronics systems such as Integrated Circuit (IC), Printed Circuit Board (PCB), and nowadays printed electronics [16,52]. These tools make the task of design and optimizing the circuit much easier and cost effective. The tool automates complex and repetitive tasks in the design process, enabling engineers to handle high levels of design complexity, ensure performance specifications, and reduce development time EDA tools cover the entire design flow, including front-end design, such as schematic capture, behavioral modeling, and circuit simulation, as well as design verification through DRC, LVS, and back-end or physical design (layout creation). Cadence Design Platform is used as the EDA environment for work presented in this thesis. It is one of the most widely adopted electronic design automation tools in both industry and academia for integrated circuit design and verification [52,57].It provides a comprehensive suite of tools that supports the complete design flow. For the FH-OPDK design flow, several key tools are used:

- **Virtuoso Custom IC Design** is used for schematic capture and circuit design.
- **Spectre Circuit Simulator** enables pre-layout and post-layout circuit simulations.
- **Physical Verification System (Physical Verification System (PVS))** is used to verify the layout against the defined design rules, ensuring that the design is compatible with the fabrication process.
- **Quantus Extraction System** is employed for parasitic extraction, enabling accurate modeling of the parasitic resistances and capacitances introduced during the layout process.

3.5.2 Front to End design flow

A front-end to back-end design flow enables the systematic transition from a circuit concept to a manufacturable layout within a unified design environment. For emerging technologies such as organic electronics, a structured design flow is essential to ensure accurate simulation, verification, and physical implementation of integrated circuits. The FH-OPDK integrates compact device models, verification rules, and layout information into a cohesive workflow, allowing designers to move efficiently from schematic design through layout generation, physical verification, and final tape-out.

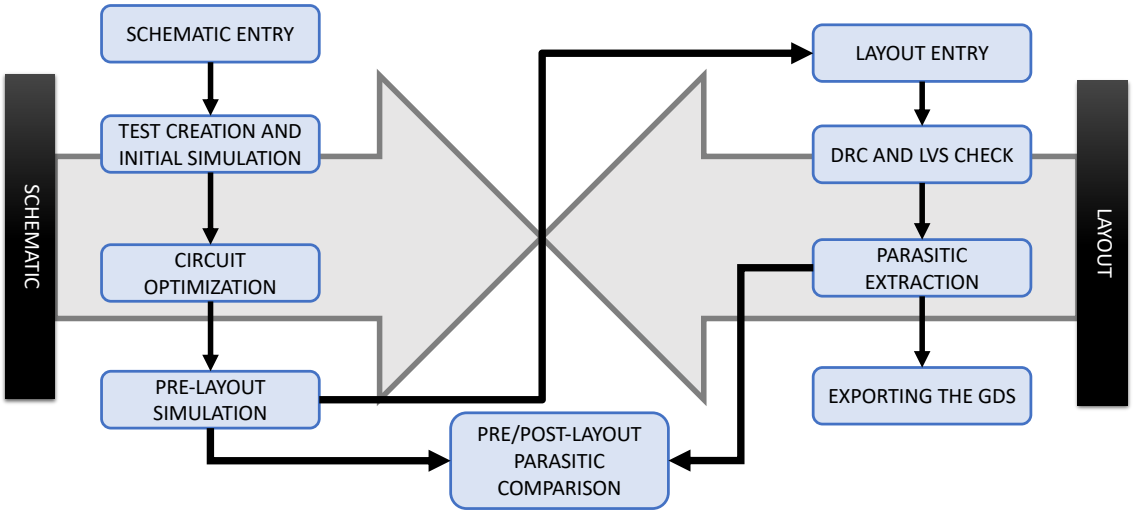


Figure 3.13: Front-to-back EDA tool design methodology integrating schematic design, pre-layout simulation, layout implementation, post-layout simulation and optimization.DATE 2022 tutorial presented by P. Gupta, J. Lukosiunas, and S. Stehlin [54].

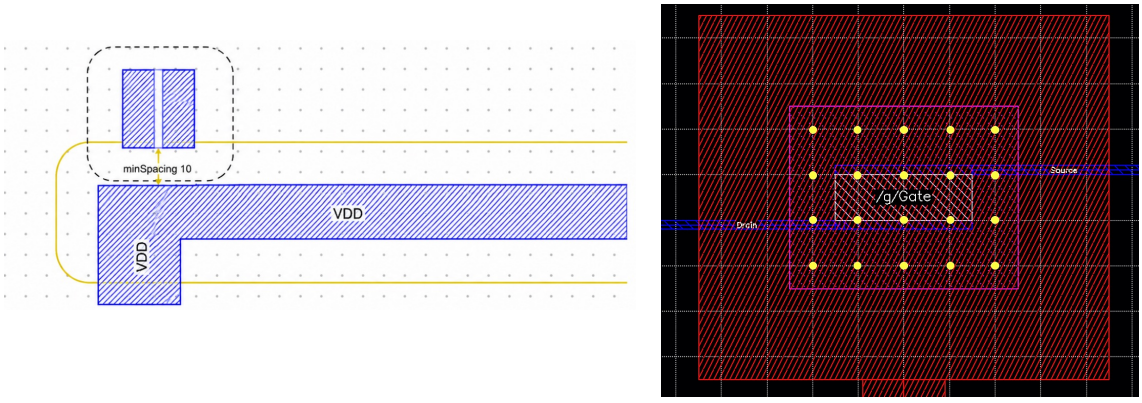
The FH-OPDK supports the complete front-end to back-end design flow which is illustrated in Fig. 3.13 and explained as follows:

- The circuit design process begins with hierarchical schematic entry in the Cadence Virtuoso Schematic Editor, where the design concept is translated into a functional circuit representation.

- The Cadence Spectre Circuit Simulator is used to evaluate the performance of the schematic and analyze the circuit behavior under different operating conditions.
- The Virtuoso Design Platform provides seamless circuit optimization through the tight integration between the analog design environment and the Spectre simulator.
- Pre-layout simulations are performed to evaluate the nominal circuit performance before considering the parasitic effects introduced during physical layout implementation.
- The Virtuoso Layout Suite provides extensive layout design capabilities, ranging from floorplanning and device placement to routing, enabling layouts to be created efficiently.
- The Cadence PVS performs DRC and LVS verification to ensure the correctness and manufacturability of the physical layout.
- The Quantus Parasitic Extraction System extracts parasitic resistances and capacitances from the physical layout, enabling accurate post-layout simulations to evaluate circuit performance and manufacturing yield.
- A comparison between the pre-layout and post-layout simulation results is performed to identify performance degradation caused by layout parasitics and to assess the expected circuit yield after fabrication.
- After successful design validation, the final layout is exported as a GDSII file for fabrication.

Assistive layout feature

The FH-OPDK design flow incorporate several assistive layout features that streamline the layout creation process and reduce the likelihood of design errors. One key feature is connectivity-driven layout, which maintains a direct correspondence between the schematic and the physical layout. This linkage enables designers to easily verify connectivity, detect missing connections, and perform updates efficiently during the layout process. The Annotation browser provides a clear overview of incomplete or unmatched components, helping designers quickly identify elements that still need to be implemented [54].



a) b)

Figure 3.14: Conceptual representation of a) metal routing and minimum-spacing design rule in integrated circuit layout and b) automatic grid snapping to further map the manufacturability process.
Adapted from: DATE 2022 tutorial presented by P. Gupta, J. Lukosiunas, and S. Stehlin [54].

The layout environment also supports automatic parameter recognition, where the system automatically adopts the appropriate layer type or line width based on the selected target object. Additionally, Design Rule Driven (DRD) editing provides real-time feedback by checking layout actions against the defined design ruledin the technology database. This immediate feedback helps prevent rule violations during layout creating, significantly reducing the number of sign-off verification iterations required later. Furthermore, automatic grid snapping ensures precise device placement. OFET devices automatically align to predefined manufacturing grids, improving layout consistency and ensuring manufacturability. The developed FH-OPDK and associated design flow enable reliable circuit design and layout implementation using OFET technology within a standardized EDA environment. Some examples are illustrate in Fig. 3.14.

3.6 Circuit Design

Following the development of the compact model and its integration into the FH-OPDK, the next step is the design and evaluation of representative circuits using the established design flow. This stage demonstrates the practical applicability of the developed modeling and design infrastructure. By implementing key circuit blocks, the accuracy of the models and the effectiveness of the FH-OPDK can be validated through comparison between simulated and measured hardware performance. In addition, multiple circuit topologies are explored to develop a standard cell library tailored for OFET technologies. These cells are optimized in terms of device geometry, layout efficiency, and electrical performance, providing designers with pre-characterized building blocks that facilitate scalable and reliable circuit design. Due to absence of n-type devices in the presented OFET technology, alternative circuit design strategies must be employed to realize functional logic circuits. Using FH-OPDK two primary topologies are designed, namely the 2-Transistor (2T) topology and 4-Transistor (4T) topology. The two topologies enable robust circuit

operation using only p-type OFETs. These topologies are further optimized using the developed FH-OPDK to achieve improved switching performance and voltage levels. The **2T topology** consists of two p-type OFETs connected in series, forming pull-up and pull-down network. The pull-up transistor is typically designed with a large channel geometry to ensure strong conduction when the input is at logic '0'. The pull-down transistor is biased using an additional supply voltage V_{SUP}, enabling controlled switching behavior. When the input is low, the pull-up device operates in saturation and drives the output to logic '1'. Conversely, when input is high, the pull-up transistor turns off, allowing the pull-down path to discharge the output to logic '0'. This topology offers a simple implementation with relatively good switching characteristics, achieving propagation delays in the millisecond range. The **4T topology**, commonly referred to as pseudo-CMOS, provides improved performance by introducing a totem-pole stage. In this configuration, two transistors form an input stage, while the remaining two transistors control the output stage. One of the transistors operates in a diode connected configuration, ensuring saturation operation and stable biasing. This topology improves the voltage transfer characteristics, particularly by achieving output levels closer to the supply voltage. Additionally, it enables better control over switching behavior and noise margins compared to 2T approach . Both topologies are extended to implement more complex logic gates such as NAND and NOR by incorporating diode load configurations and level shifting stages. Through simulation and experimental validation, the circuit parameters and device geometries are optimized to enhance performance, demonstrating the effectiveness of the proposed design methodologies within the FH-OPDK framework.

Measurement setup

To evaluate the performance of the designed circuits and validate the developed FH-OPDK, electrical measurements were carried out on fabricated OFET-based test structures. The measurement setup consists of a Voltcraft-8202 function generator used to apply the input pulse signal to the gate terminal, while a Keithley-2602 source meter provides the supply voltage V_{DD} and bias voltage V_{SUP}. The output signal is monitored using a passive probe with an input resistance of 10 MΩ and capacitance of 10 pF and recorded using a Yokogawa-DL1604 digital oscilloscope.

3.6.1 Standard cells

3.6.1.1 Logic gates

INV

Inverter represents the fundamental building block of digital circuits and serves as a key benchmark for evaluating the performance of FH-OPDK. Inverter circuits are implemented using both the 2T and 4T topologies to assess their suitability for organic electronics and to analyze the impact of circuit architecture on switching behavior and signal integrity. The circuit schematics and layout for both topologies are shown in Fig. 3.15.

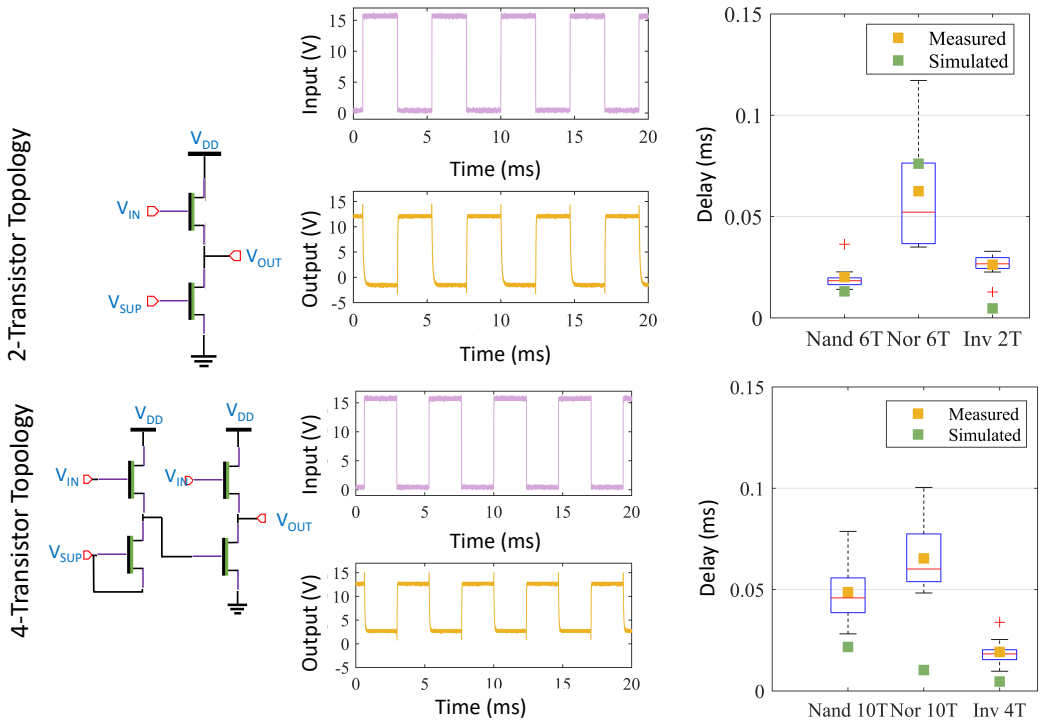


Figure 3.15: Inverter schematic, transient response, propagation delay using 2T and 4T topology [16], licensed under CC BY-NC-ND 4.0.

The 2T inverter consists of two p-type OFETs connected in series, where the pull-up transistor is typically designed with larger width to ensure sufficient drive strength. The pull-down transistor is biased at a fixed V_{SUP} enabling switching operation despite the absence of complementary n-type devices. When the input is at logic '0', the pull-up transistor is in conduction, resulting in a high output voltage logic '1'. Conversely, when the input is at logic '1', the pull-up device turns off and the pull-down dominates, switching the output to logic '0'. This basic switching behavior is confirmed through transient measurements, as shown in Fig. 3.15, where the output waveform follows the input signal with a measurable propagation delay. The voltage transfer characteristics of the inverter under different biasing conditions are presented in Fig. 3.15. It can be observed that the transition region shifts depending on the applied bias voltage, indicating the sensitivity if the switching threshold to operating conditions. Higher magnitude bias voltages result in improved switching sharpness and a more defined transition between logic states. However, the slope of the transfer curve remains relatively gradual compared to CMOS technology, reflecting the intrinsic limitations of p-type only OFETs. Further insight into the inverter performance is provided by the gain characteristics shown in Fig. 3.15. The gain peaks around the transition region, reaching values between approximately 1.5 and 2.5 depending on the transistor sizing. Increasing the width of pull-up transistor leads to higher gain, showing stronger drive capability and improved switching behavior. However, excessive sizing can also introduce increased parasitic capacitance, which may degrade dynamic performance [11].

NAND

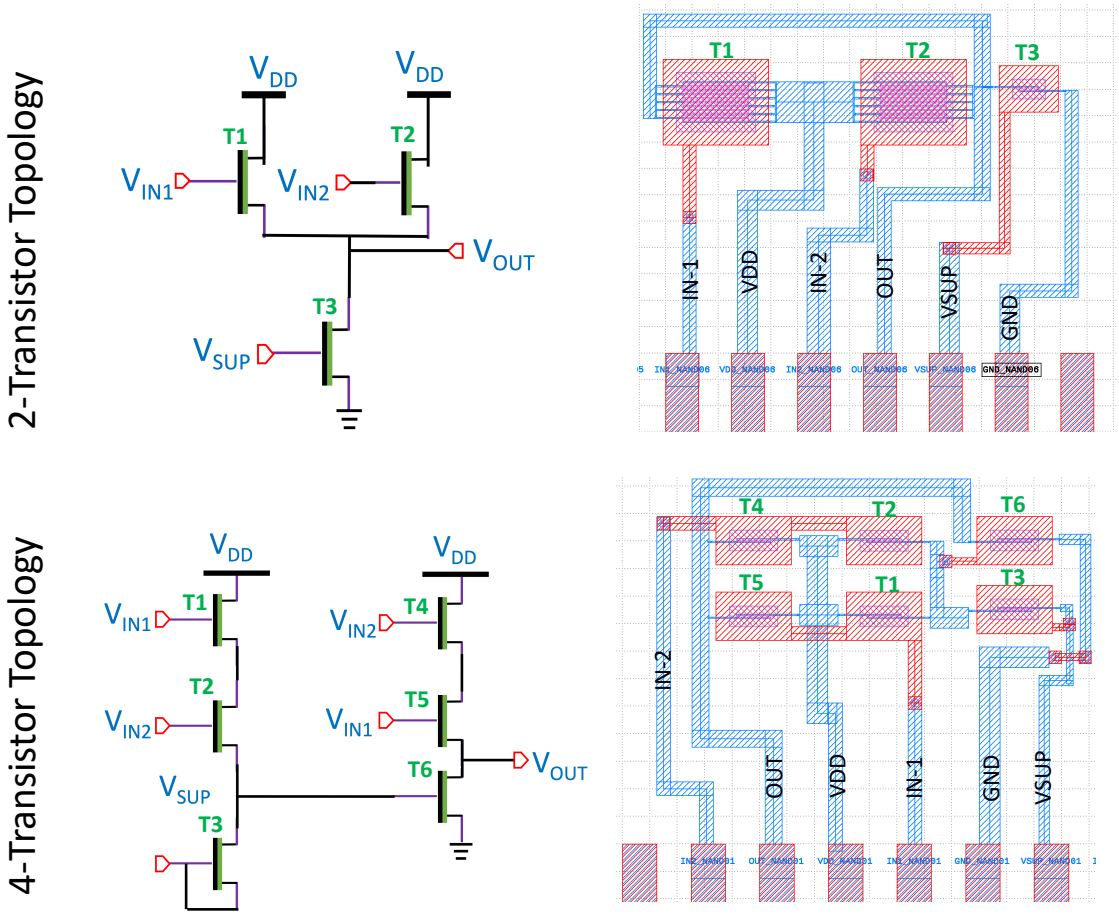


Figure 3.16: NAND schematic and layout using 2T and 4T topology [16], licensed under CC BY-NC-ND 4.0.

In additional to Inverter, a NAND gate was implemented. Both 2T topology and 4T topologies are explored to overcome the absence of complementary n-type transistors. The corresponding circuit schematic, layout and measure as shown in Fig. 3.16.

In the 2T topology, the NAND functionality is achieved by configuring the pull-up network using the two p-types OFETs in parallel, controlled by the input signals Input-1 and Input-2. The pull-down path is realized using a bias controlled transistor connected to V_{SUP}. When both inputs are at logic '1', the pull up transistors are turned off, allowing the pull-down network to discharge the output voltage node, resulting in a logic '0'. For all other input combinations, at least one of the pull-up transistors remains active, pulling the output to logic '1'. This configuration enables correct NAND operation despite the limited device polarity. The 4T topology enhance this behavior by incorporating a pseudo-CMOS structure. This configuration reduces output degradation and improves logic level restoration. The measured transient responses as shown in Fig. 3.16, confirm correct NAND functionality, with clear distinction between logic levels. Compared to the 2T topology, the 4T implementations exhibits improved output voltage levels, reduced signal degradation, and more stable switching behavior. While the 2T design offers a compact implemen-

tation, the 4T topology provides enhanced robustness, making it more suitable for cascading and complex circuit design.

NOR

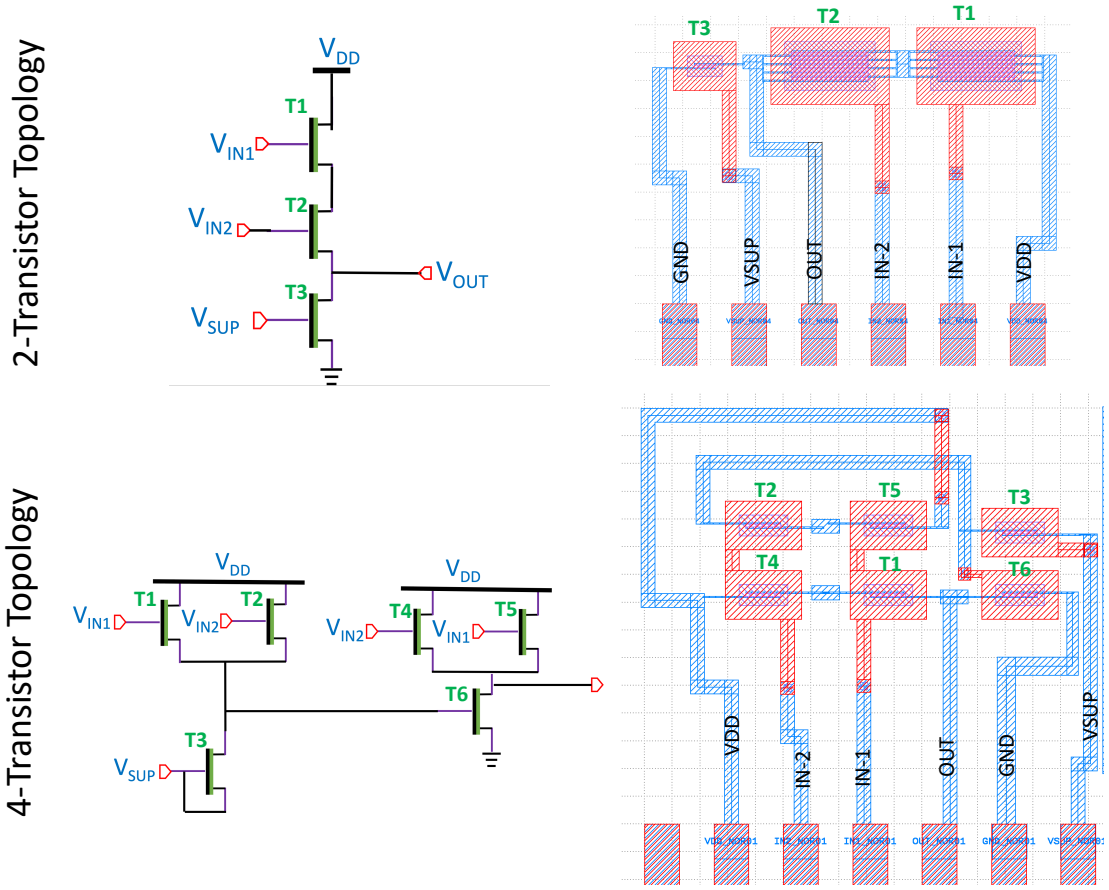


Figure 3.17: NOR schematic and layout using 2T and 4T topology.
Adapted from: Author's own publication [16], licensed under CC BY-NC-ND 4.0.

The NOR gate is implemented as a complementary combinational logic function within the FH-OPDK framework, utilizing 2T and 4T topologies. The schematic for both implementations as shown in Fig. 3.17.

In the 2T topology, the NOR function is realized by arranging the pull-up transistors in series, controlled by the input signal Input1 and input2. The pull-down path is implemented using a bias-controlled transistor connected to V_{SUP} . When both inputs are at logic '0', the series pull up path is active, allowing the output to be driven to logic '1'. However, if either input is at logic '1', the pull up path is interrupted, and the pull-down network discharges the output node, resulting in logic '0'. Due to series configuration, the effective drive strength is reduced, leading to slower switching behavior compared to the NAND implementation. The 4T topology improves upon this by introducing a pseudo-CMOS configuration with additional transistors enhancing the switching characteristics. The totem-pole arrangement improves voltage levels and mitigates signal degradation, particularly in the presence of multiple inputs.

Logic gate performance and Topology comparison

The performance of the implemented logic gates is evaluated using propagation delay analysis. As shown in Fig. 3.18 summarizes the measured and simulated timing characteristics, providing further validation of the developed compact model and the overall FH-OPDK design flow. As compared to the NAND gate, the NOR implementation exhibits higher propagation delay, primarily due to the reduced drive strength of the series-connected pull-up network. For the 2T topology, the inverter exhibits the lowest delay, approximately in the range of 0.02 - 0.03 ms, indicating efficient switching behavior for simple gate structures. The NAND gate shows slightly improved performance compared to NOR, with delays around 0.015-0.02 ms, whereas the NOR gate exhibits the highest delay among the three, reaching values up to 0.06-0.08 ms. This degradation in NOR performance can be attributed to the series conduction path and reduced effective drive strength in the pull-down network, which limits the switching speed.

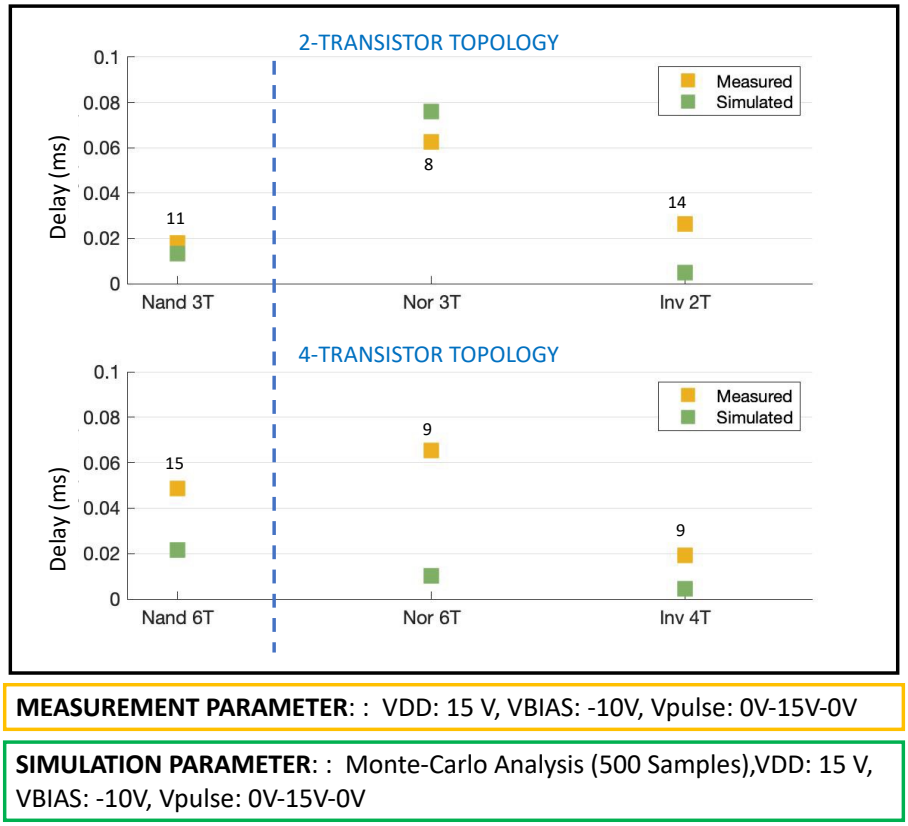


Figure 3.18: Measured vs simulated propagation delay characteristics of NAND, NOR, and inverter circuits using 2T and 4T topology.DATE 2022 tutorial presented by P. Gupta, J. Lukosiunas, and S. Stehlin [54].

In contrast, the 4T topology demonstrates a more balanced delay distribution across different logic gates. The inverter maintains low delay values (0.02 ms), similar to the 2T case, but with improved stability. The NAND and NOR gates exhibit delays in the range of 0.04 – 0.07 ms, with the NOR gate showing slightly higher delay due to its topology. However, compared to the 2T implementation, the variation between different gates is reduced, indicating improved robustness. Statistical analysis using box plots further highlights the variability in delay across multiple samples. The

2T topology shows a wider spread, particularly for the NOR gate, whereas the 4T topology exhibits tighter distributions, indicating improved consistency and reduced sensitivity to process variations. Overall, while the 2T topology offers lower delay for simple gates and reduced device count, the 4T topology provides improved uniformity, better controlled over switching behavior, and enhanced robustness. These characteristics make the 4T topology more suitable for scalable circuit design and reliable operation in OFET-based systems. The 4T topology exhibits moderate delay and asymmetric switching behavior due to the absence of a complementary pull-down network. In contrast, the 4T topology demonstrates improved voltage swing, higher gain, and more stable switching characteristics. Overall, while the 2T inverter offers a compact and simple implementation, the 4T topology provides enhanced electrical performance, including improved gain, output levels, and robustness.

3.6.1.2 Ring oscillator

To further evaluate the dynamic performance of the developed OFET PDK and the implemented inverter standard cells, a 5-stage transistor ring oscillator was designed using both 2T and 4T inverter topologies. Ring oscillators provide a compact and effective means to assess switching speed, delay accumulation, and overall circuit performance under oscillatory conditions. The frequency performance of the fabricated ring oscillators is summarized as in Fig. 3.19 for both topologies. The 4T ring oscillator achieves a higher oscillation frequency than the 2T implementation, indicating improved switching performance and reduced stage delays. While the simulated frequencies are higher than the measured values for both topologies, the observed trend is consistent, demonstrating reasonable agreement between simulation and measurement and validating the developed compact model.

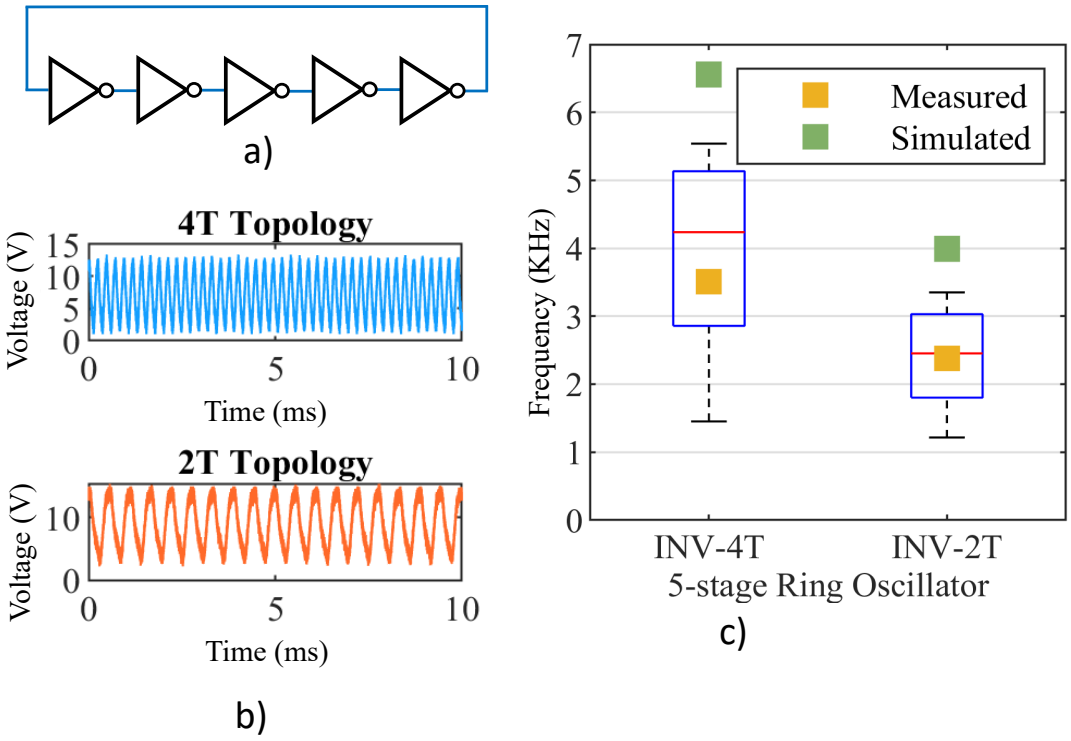


Figure 3.19: a) Circuit schematic, b) Measured transient characteristics, and c) Model-hardware correlation for single single stage delay of Ring oscillator based on 2T and 4T topology.

This can be attributed to the enhanced switching characteristics and better voltage transfer behavior of the 4T topology-based inverter, which reduces delay variations across various stages. In contrast the 2T topology-based ring oscillator exhibit lower frequencies and slightly larger spread, reflecting its limited pull-down capability and higher sensitivity to device variations. Furthermore, a good correlation between simulated and measured frequencies is observed, confirming the validity of the developed compact model and its suitability for circuit level predictions. Overall, the results demonstrate that while both topologies are functional, the 4T implementation offers superior dynamic performance, making it more suitable for high speed OFET based circuit applications. Based on the standard cell, an address decoder circuit is designed and simulated using the design flow discussed earlier.

3.6.1.3 4 to 16 binary decoder

An Address decoder is a combinational logic circuit than enables the selection of specific rows and columns within a matrix. In sensing applications, it is used to address individual sensor elements (sensel) located at the intersections of rows and columns. By systematically scanning the matrix and evaluating the electrical state of each sensel, the decoder facilitates the detection

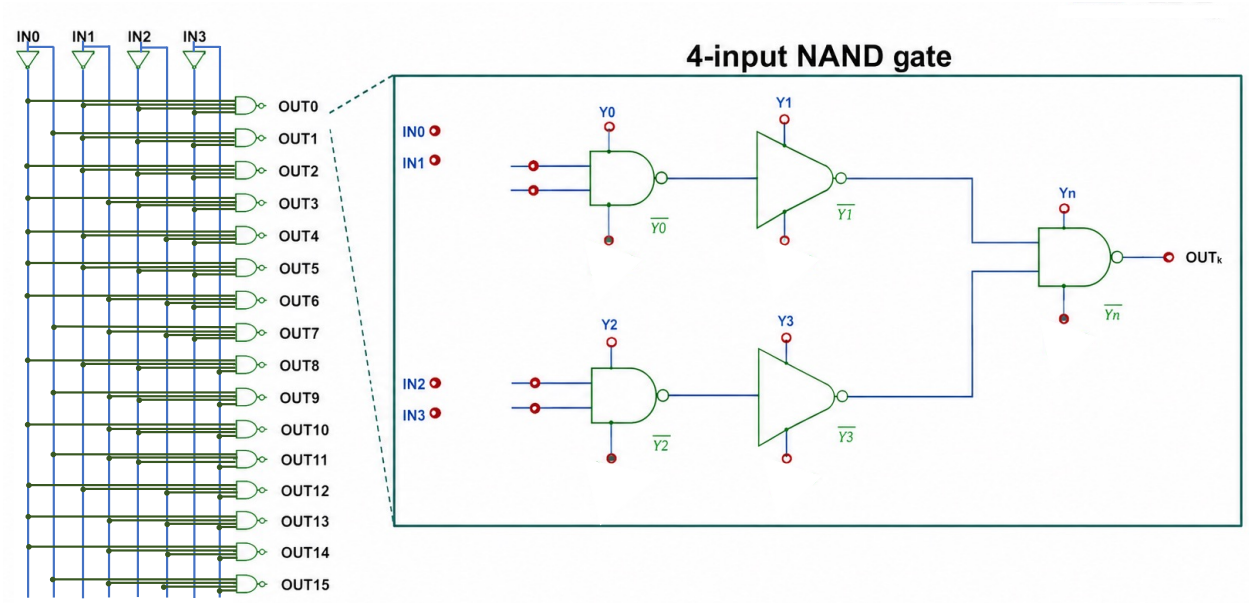


Figure 3.20: Hierarchical realization of a 4-input NAND gate used in a 4-to-16 decoder architecture.

Each row and column with matrix is assigned to a unique binary address. When a sensel is activated, it results in a change in its electrical characteristics, which is detected by the readout circuitry. The decoder then translates the input signals into a output address, identifying the exact location of the activated Sensel within the predefined address space. This information is subsequently processed and mapped onto a readout system, enabling visualization or further analysis of the sensed data. In Fig. 3.20, a 4-to-16-line binary decoder is implemented using logic gates based on developed FH-OPDK. Due to the unipolar nature of the technology, a 4T topology is employed to ensure reliable logic operation and improved voltage levels. The decoder architecture consists of 16 four-input NAND gates, each corresponding to one output line, and four inverters used to generate the complementary input signals required for full address decoding. Each NAND gate is designed to respond to a unique combination of input signals, ensuring that only one output line is activated for a given input address. The inverters provide both true and complemented versions of the input signals, enabling the realization of all possible logic combinations. This configuration ensures accurate decoding and minimizes ambiguity in address selection.

This can be attributed to the enhanced switching characteristics and better voltage transfer behavior of the 4T topology-based inverter, which reduces delay variations across various stages. In contrast the 2T topology-based ring oscillator exhibit lower frequencies and slightly larger spread, reflecting its limited pull-down capability and higher sensitivity to device variations. Furthermore, a good correlation between simulated and measured frequencies is observed, confirming the validity of the developed compact model and its suitability for circuit level predictions. Overall, the results demonstrate that while both topologies are functional, the 4T implementation offers superior dynamic performance, making it more suitable for high speed OFET based circuit applications.

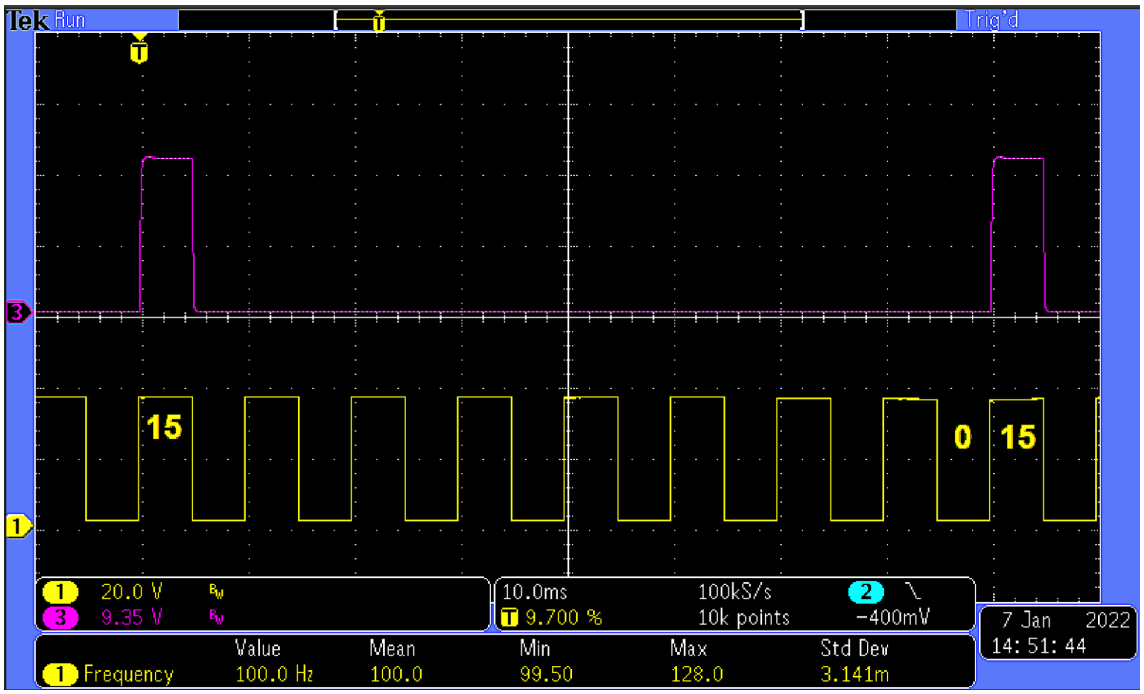


Figure 3.21: Measured transient output for 16th bit of 4 to 16 address decoder.

The complete decoder circuit is designed, optimized, and implemented using FHOPDK with cadence EDA environment. Special attention is given to device sizing layout optimization to ensure proper switching behavior and signal integrity across all output lines. The layout is verified using standard DRC and LVS validation for manufacturability. The decoder is optimized to operate at supply voltage 40-45 V, which aligns with the operating regime of OFET. Under these conditions, the decoder successfully identifies location of activated sensels by generating the corresponding output signals. The measured output for the 1 bit is shown in Fig. 3.21.
This demonstrates the capability of the developed FH-OPDK to support more complex digital circuits and highlights its potential for integration in large sensing and readout applications. The fabricated digital logic circuits designed, optimized, and, simulated using FH-OPDK are presented in Fig. 3.22.

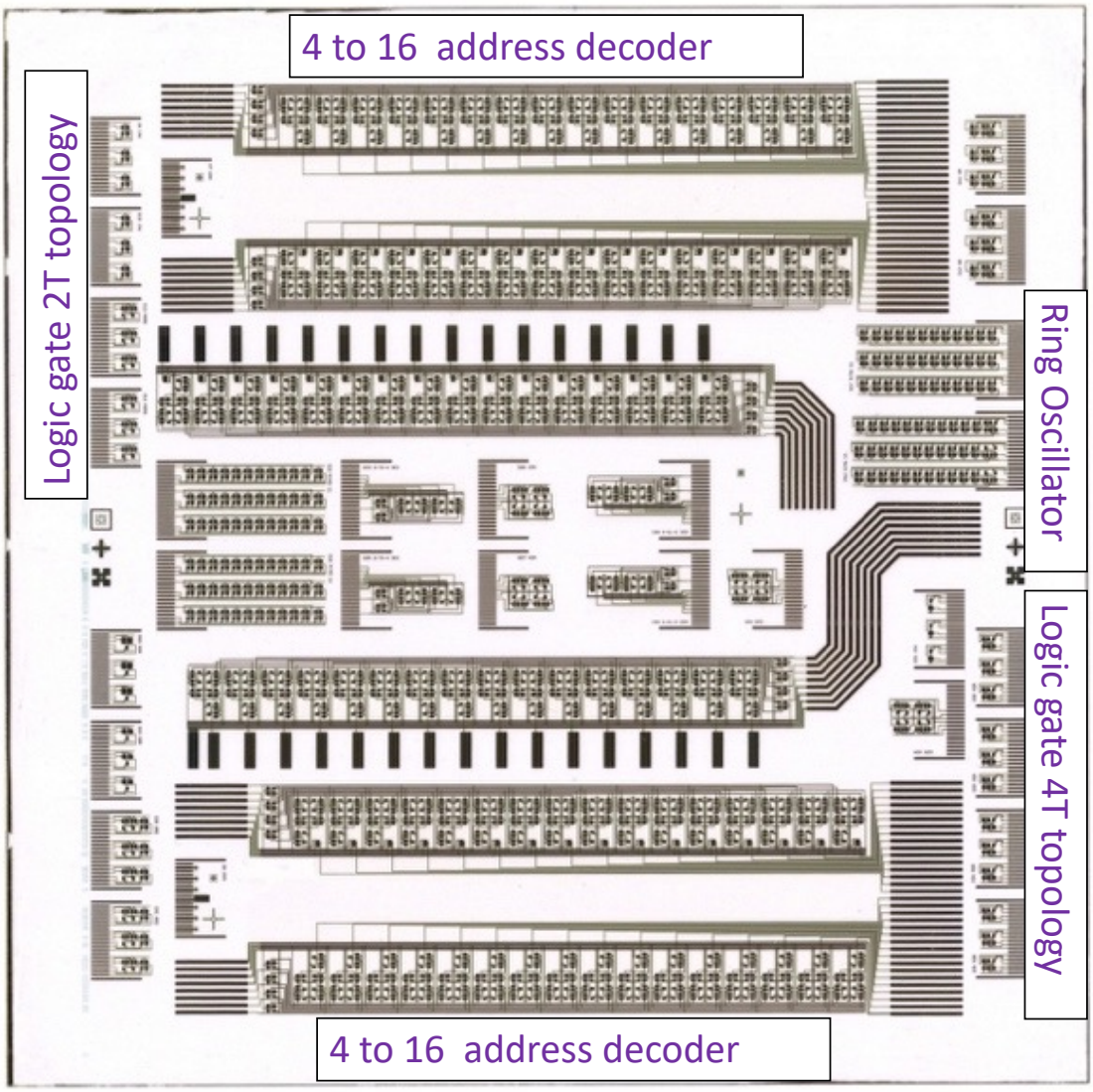


Figure 3.22: Test chip containing digital circuit designed and optimized using FH-OPDK [16], licensed under CC BY-NC-ND 4.0.

3.6.2 Hardware demonstrator

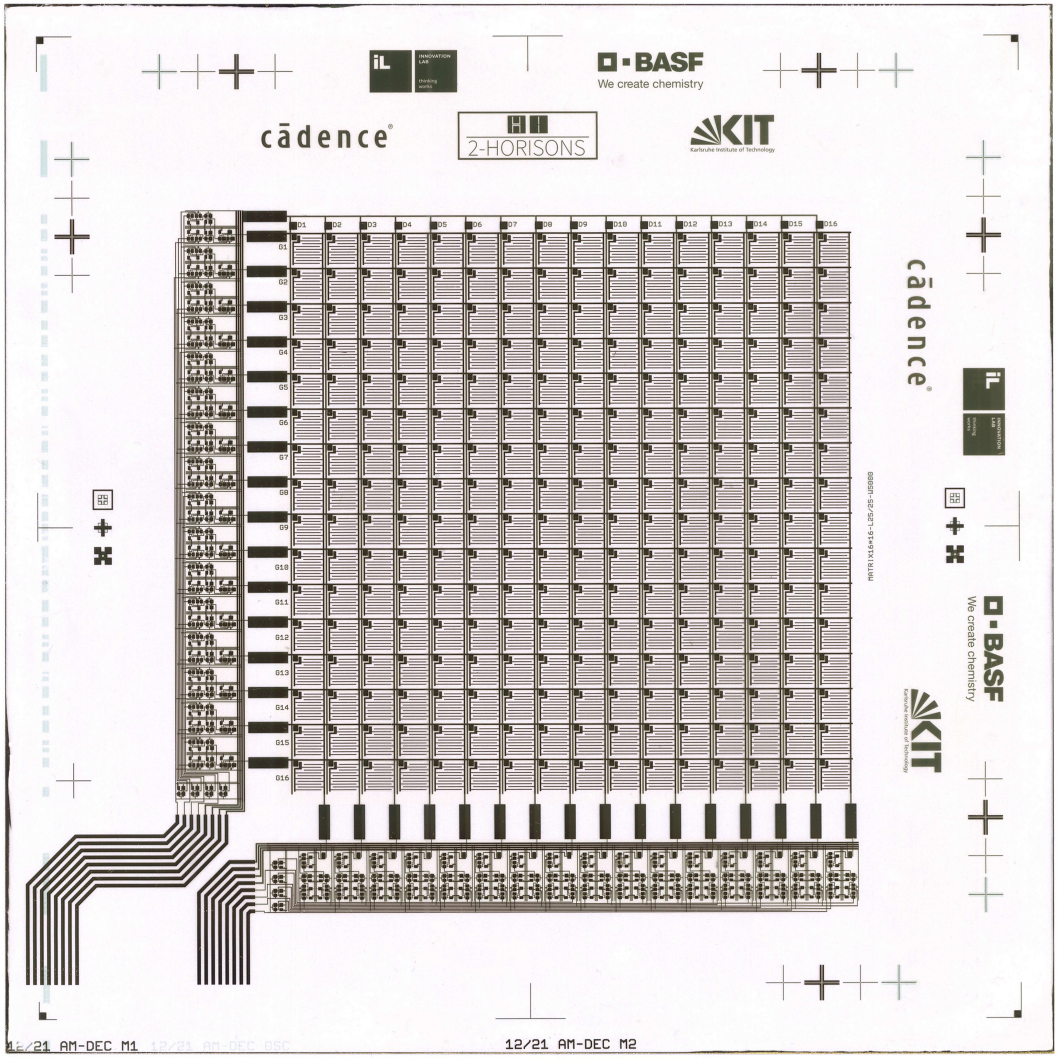


Figure 3.23: Fabricated layout for 16x16 matrix integrated with address decoder and operational amplifier.

Large area sensing platform

The large area sensing platform is designed to demonstrate the system level integration capability of the developed FH-OPDK. The complete printed circuit consist of a 16x16 pressure sensor matrix, two 4-to16 binary decoders and 16 to 1 multiplexer, as illustrated in Fig. 3.23. This architecture enables spatial detection and reads out pressure distribution across a large sensing area, highlighting the potential of organic electronics for flexible and large-area applications. Each individual sensing element, or Sensel, is formed by combining a pressure sensor with an OFET device. The matrix is organized into 16 rows and 16 columns, where each intersection corresponds to one Sensel. The rows and columns are connected to dedicated decoder circuits, which are responsible for addressing and selecting specific sensel within the matrix. By assigning a unique binary address to each row and column, the system can efficiently scan the entire sensing array. Two 4 to 16 decoders are employed to independently address the row and column lines. These decoders are implemented

using inverter and 4-input NAND gate structures, as described in the previous section. The use of decoders significantly reduces the number of required interconnects between the sensor matrix and the external circuitry, which is particularly important for large area systems. Instead of directly accessing each sensel individually, the matrix can be addressed by a compact set of binary input signals. The sensing elements are printed resistive sensors integrated with OFETs at each sensel, enabling local signal modulation. Materials such as carbon nanoparticle-polymer composites exhibit Negative Temperature Coefficient (NTC) behavior, allowing scalable, flexible, and low-cost large area sensing. The readout of the sensed data is achieved using a 16->1 multiplexer, which consists of 16 OFET based switching transistors. The multiplexer converts the spatially distributed sensors signals into a single analog output steam. This approach enables sequential readout of the matrix while maintaining a simplified interface to external electronics. When a sensel is activated due to applied pressure, it induces a change in the electrical state of the corresponding row and column lines. This change is detected and encoded by the decoders, resulting in a logic '0' at the selected row and column outputs. The selected signal is then routed through the multiplexer to the output, where it is measured and processed. By scanning through different address combinations, the complete pressure distribution across the matrix can be reconstructed and visualized on a display. The hardware demonstrated setup is illustrate in Fig. 3.24.

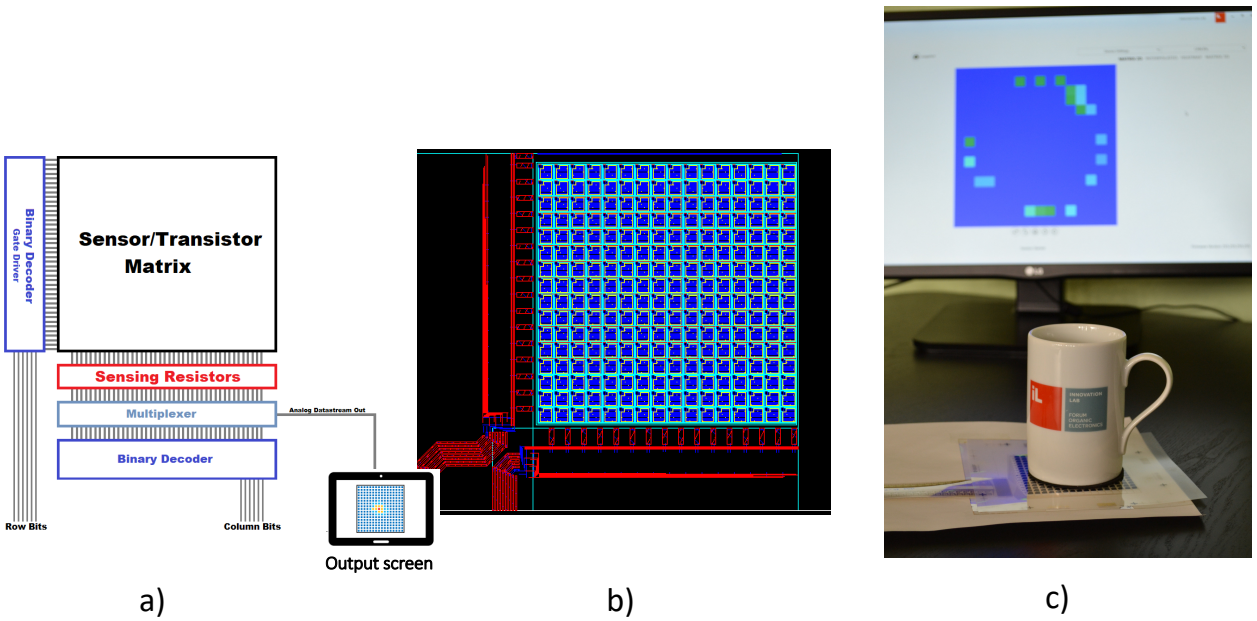


Figure 3.24: a) Hardware demonstrator of sensing Active matrix, Layout of active matrix with integrated decoder and, c) demonstration of active-matrix to sense the pressure of a coffee mug.

Due to current limitations in printed organic electronics, it is not yet feasible to implement the entire readout system using organic components alone. Therefore, an in house developed readout platform based on conventional silicon electronics is used to interface with the printed circuitry. This hybrid approach enables reliable control, signal acquisition, and data transfer to a computer for visualization. Despite this limitation, the presented system demonstrates a functional flexible hybrid sensing platform and highlights the potential for future fully integrated organic electronic systems.

3.7 Low frequency noise study

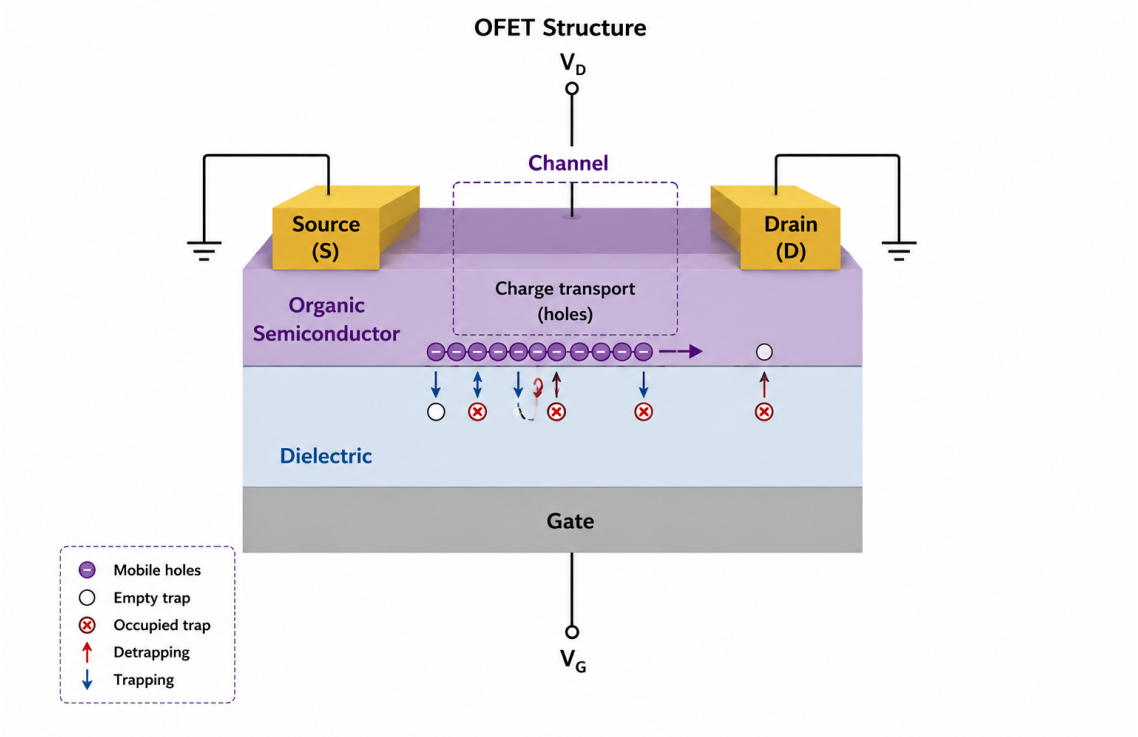


Figure 3.25: Conceptual representation of charge trapping-detrapping induced flicker noise in OFET.
Adapted from: AI-generated illustration created using OpenAI image-generation tools and adapted by author.

The low-frequency noise characteristics of the investigated p-type OFETs were evaluated by analyzing the drain current power spectral density(PSD) under varying gate bias conditions. The measured noise spectra, as shown in Fig. 3.25 exhibit a clear inverse frequency dependence over the investigated frequency range, following an approximately $1/f^{\gamma}$ dependence with γ close to unity. This frequency dependence is characteristics of flicker noise and is commonly observed in OFET [24, 58]. The underlying physical mechanism contributing to the observed noise are further investigated through the analysis of the bias dependence of the normalized noise spectral density. The PSD decreases with increasing frequency, with a slope close to -1 in the log-log scale, which is consistent with typical behavior reported for organic thin film transistors. A strong dependence of the noise magnitude on the applied

gate voltage is observed. As the absolute value of V_{GS} increases, the drain current increases leading to a corresponding rise in the measured noise level. This trait indicates that the noise is closely linked to the charge carrier density in the channel. At higher frequencies, the measured spectra approach the system noise floor, indicating that the measured low-frequency region is dominated by intrinsic device noise rather than limitations of the measurement setup [58–60]. To further analyze the noise origin, the normalized noise spectral density S_{ID}/I_D was evaluated and scaled with the device geometry. The normalized Power Spectral Density (PSD) shows a systematic reduction with increasing gate bias, suggesting a significant contribution from carrier number fluctuations. This response is typically associated with trapping and de-trapping processes at the semiconductor-dielectric interface, which modulate the effective carrier density in the channel. Furthermore, the extracted frequency exponent γ, obtained from fitting the PSD to a $1/f^{\gamma}$ dependence, is found to be close to unity across all devices and bias conditions. A comparison of γ values using different threshold voltage extraction methods reveals noticeable variations, highlighting the sensitivity of noise analysis to parameter extraction techniques. Overall, the result confirm that flicker noise in the investigated OFETs is governed by a combination of carrier number and mobility fluctuations, with trap-related effects playing a dominant role [24, 26, 58].

3.7.1 Measurement setup

For low frequency noise characterization, the drain current fluctuations of the device under test was measured using a low-noise analog chain optimized for high sensitivity in the sub-kilohertz frequency range.

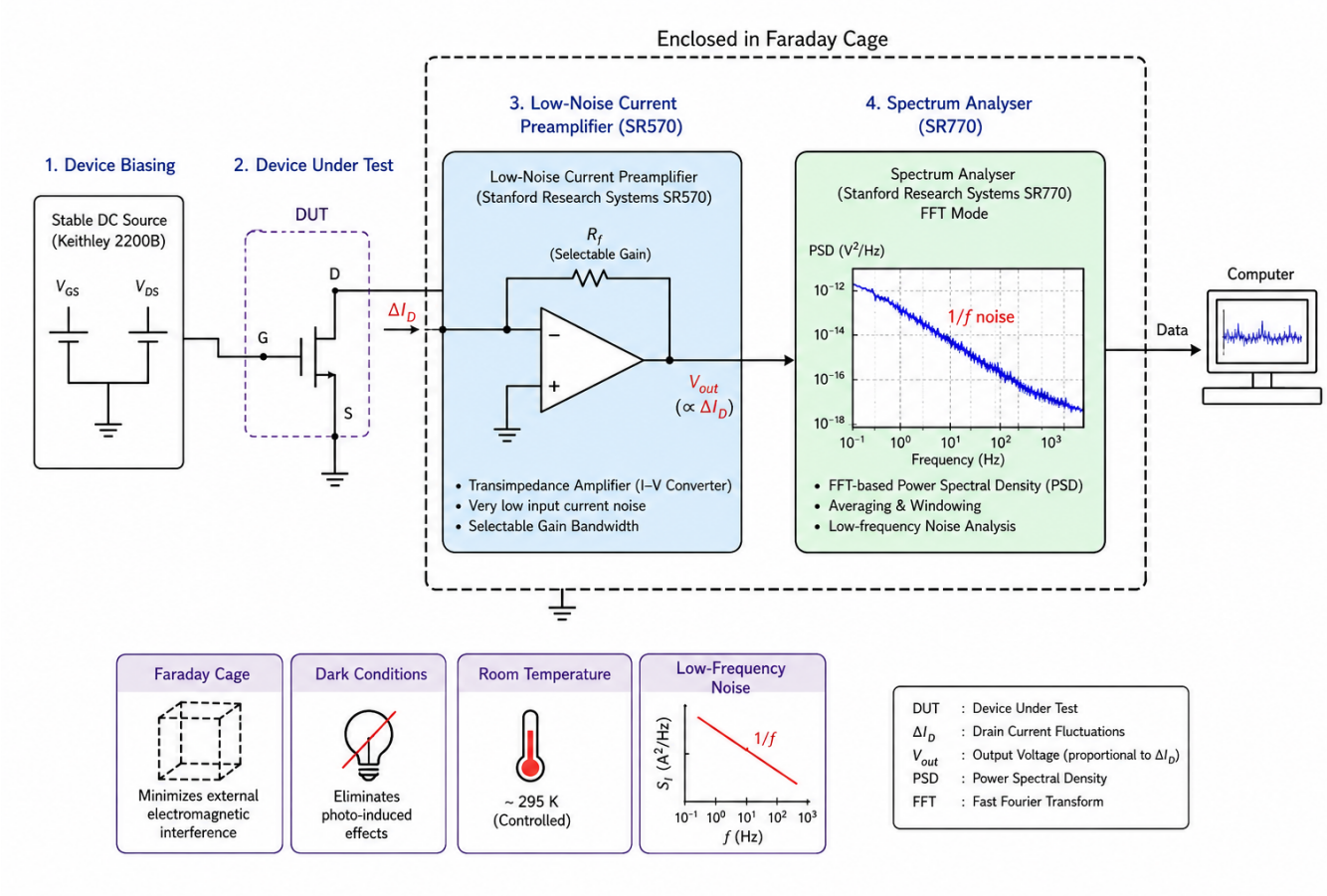


Figure 3.26: Experimental setup for low-frequency noise characterization using a low-noise current preamplifier and FFT-based spectrum analysis.
Adapted from: Generated using OpenAI image-generation tools based on the author's experimental methodology and adapted by the author.

The device was biased using a stable DC source, and the resulting drain current was routed to a Stanford Research Systems SR570 low-noise current pre-amplifier. This trans-impedance amplifier converts small current fluctuations(ΔI_D) into a proportional voltage signal through a selectable gain transistor, while maintaining a very low input noise level. Careful selection of the gain bandwidth settings ensures that the intrinsic device noise dominates over the measurement system noise, which is critical for accurate extraction of the power spectral density [61]. The amplified voltage signal was subsequently analyzed using Stanford Research Systems SR770 spectrum analyses operating in Fast Fourier Transform (FFT) mode. The FFT mode enables the conversion of time domain signals into the frequency domain, allowing accurate analysis of the spectral characteristic and noise components of the measured signal. The analyses computes the PSD of the signal by performing a FFT on the time domain data, allowing characterization of the noise as a function of frequency. Appropriate averaging and windowing techniques were applied to reduce statistical uncertainty and improve spectral resolution, particularly in the low-frequency regime where 1/f noise is dominant. To suppress external interference, the entire measurement setup was enclosed in a Faraday cage, shielding it from electromagnetic disturbances such as power-line noise. Measurements were conducted in dark conditions to eliminate photo-induced effects, and at a controlled

room temperature of approximately 295K. The experminatal setup is illustrated in Fig. 3.26.

3.7.2 Noise analysis

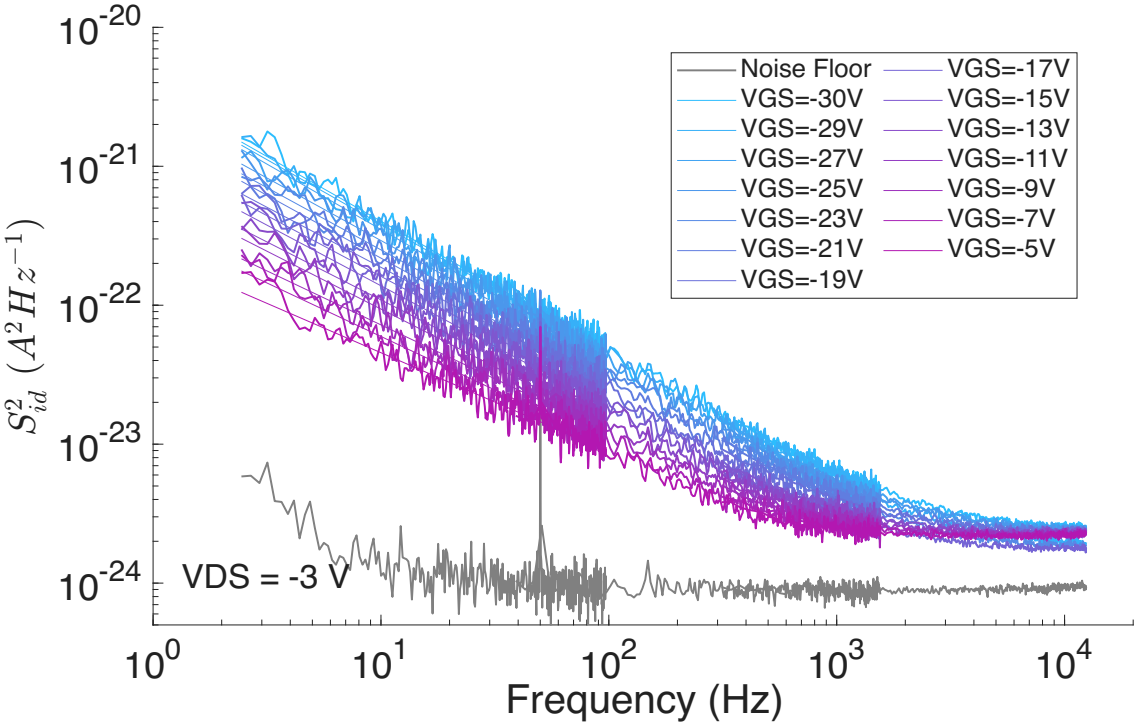


Figure 3.27: Noise power spectral density vs frequency of OFET.

To investigate the physical origin of the observed low-frequency noise, the dependence of the normalized current noise power spectral density on the gate overdrive voltage was analyzed as shown in Fig. 3.27. The normalized PSD was evaluated at a fixed frequency and fitted as a function of the effective gate voltage $(V_{GS} - V_{TH})$ with the following dependence:

$$\frac{S_{I_D}}{I_{DS}^2} \propto (V_{GS} - V_{TH})^{-\beta} \tag{3.8}$$

where β represents the gate overdrive exponent. The extracted exponent provides insight into the dominant fluctuation mechanism governing the low-frequency noise characteristic in OFETs.

Table 3.2: Threshold voltage values for four devices obtained using different extraction methods.

Extraction method	**Device 1**	**Device 2**	**Device 3**	**Device 4**
Trans-conductance method	−4.68	−5.12	−4.73	−3.60
Second derivative method	−3.19	−3.43	−3.43	−2.59

According to Hooge's mobility fluctuation model, the normalized PSD exhibits an inverse dependence on the gate overdrive voltage, resulting in β [24]. In this case the

low frequency noise originates primarily from fluctuations in carrier mobility caused by carrier scattering, structural disorder, grain boundaries, and localized defects within the organic semiconductor layer. In OFETs, these mobility fluctuations may additionally be influenced by interface roughness and dielectric induced disorder, which disturbs the carrier transport path in the accumulation channel.

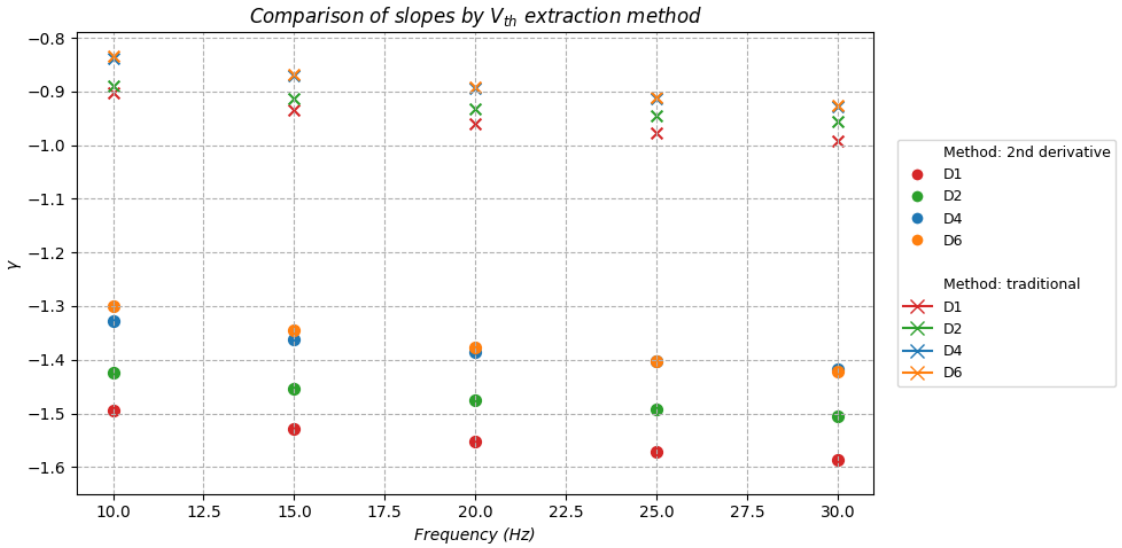


Figure 3.28: β value calculated using different value of threshold voltage using traditional trans-conductance and second derivative method.

In contrast, the Mc-Whorter carrier number fluctuation model predicts a stronger dependence of the normalized PSD on the gate overdrive voltage, corresponding to a gate overdrive exponent β close to two [26]. This mechanism is associated with trapping and de-trapping of charge carriers at trap states located near the semiconductor dielectric interface. These trapping event lead to fluctuation in the effective carrier concentration and induce fluctuations in the threshold voltage, thereby contributing to the observed 1/f noise. The extracted gate-overdrive exponent was found to be depend strongly on the threshold voltage extraction method. When the threshold voltage was determined using the conventional trans-conductance method, the extracted exponent remained closed to unity, suggesting a dominant contribution from mobility fluctuations. In contrast, the second derivative method resulted in intermediate exponent values between one and two, indicating a mixed noise mechanism involving both mobility and carrier number fluctuations. The value of β for each OFET device is presented inFig. 3.28, the threshold voltage used for extracting value of β can be seen in Table.3.2. The sensitivity arises because the gate-overdrive voltage, V_{GS}-V_{TH}, is directly affected by the extracted threshold voltage. Since, the gate-overdrive exponent is obtained from the slope of the normalized noise spectral density as a function of V_{GS}-V_{TH}, even relatively small differences in the extracted V_{TH}, can shift the fitting range and modify the resulting exponent. This effect is particularly relevant in OFETs, where the threshold voltage is not a uniquely defined physical quantity and can vary depending on the extraction method due to non-idealities such as contact resistances, trap states, and gradual channel formation. A more reliable interpretation can be achieved by comparing multiple threshold voltage extraction methods, evaluating the consistency of the obtained exponents, and

complementing the analysis with additional analysis of PSD. Furthermore, intermediate exponent value in the present work suggest that the investigated OFETs do not follow an ideal single-mechanism noise model. Instead, the low-frequency noise characteristic is likely governed by a coupled contribution of mobility fluctuation and carrier trapping processes. Such mixed characteristic is commonly reported in organic semiconductors due to structural disorder, non-uniform molecular ordering, and distributed interface trap states. Furthermore, the relatively thick gate dielectric employed in the present device architecture results in a lower gate capacitance, reducing the electrostatic control of the gate over the accumulation channel. Consequently, variations associated with interfacial trap states and threshold voltage extraction may have a more pronounced influence on the observed gate-bias dependence of the normalized noise, contributing to deviations from the ideal Hooge or McWhorter behavior [24, 26].

Table 3.3: Benchmark analysis of normalized noise PSD for organic semiconductor technologies based on reported literature.

Reference	**Semiconductor material**	**Process**	**Substrate**	WLS_{I_D}/I_{DS}^2 **(μm^2/Hz)**
This work	BASF material P3100	Inkjet printed	PEN	10^{-5}–10^{-7}
[62]	P3HT	Spin cast	Si wafer	10^{-5}–10^{-7}
[63]	PBTTT-C_{14}	Solution processed by edge-casting	Si wafer	10^{-2}–10^{-5}
[63]	C8-DNBDT-NW	Solution processed by edge-casting	Si wafer	10^{-3}–10^{-6}
[64]	DNTT/Cytop	Spin coat	PEN	10^{-5}–10^{-7}
[65]	DNTT	Vacuum-deposited small molecule	PEN	10^{-7}–10^{-8}
[66]	DNTT	Physical vapor deposition	Glass	10^{-7}–10^{-8}
[67]	Undoped SP500 polymer semiconductor	Spin coat over SAM	Plastic	10^{-5}–10^{-11}

To ease the direct comparison of noise performance across different studies, the noise PSD is normalized by drain current as a function of frequency as in Fig. 3.29. The normalized PSD with respect to the drain current and scaling it to the channel geometry, variations arising from device dimensions are minimized, allowing a meaningful benchmarking against reported p-type OFET technologies fabricated using different materials, substrates, and processing techniques in Table.3.3.

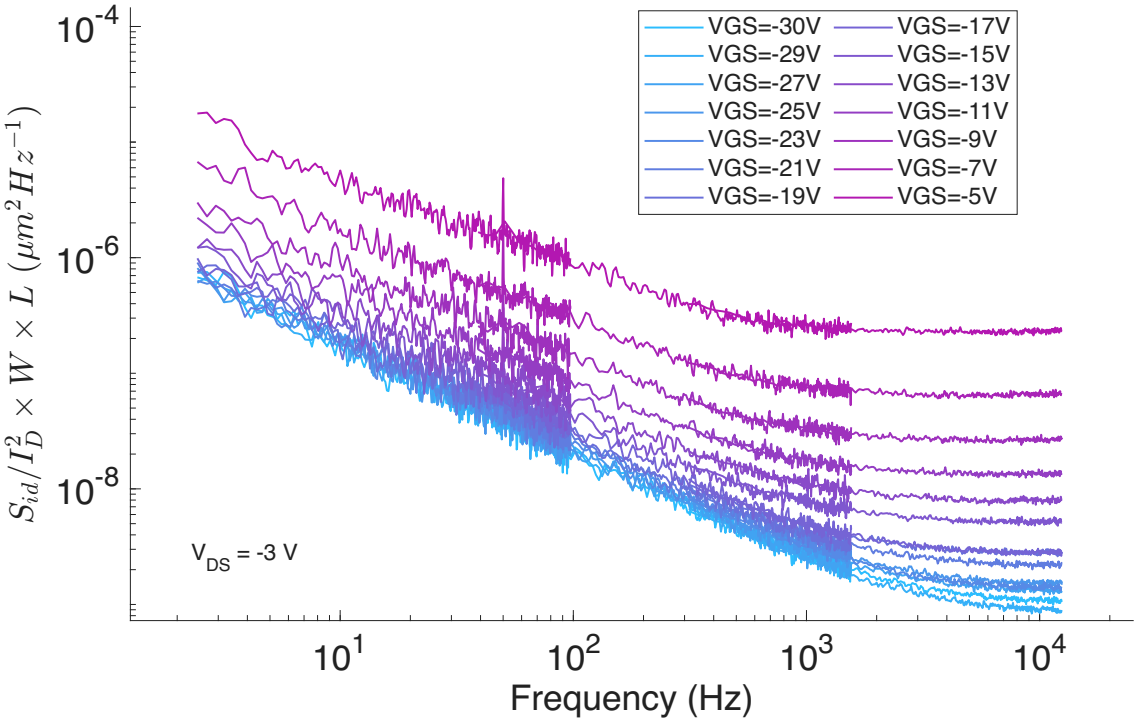


Figure 3.29: Normalized noise spectral density with channel width (250 µm) and channel length (10 µm) vs frequency.

The comparison indicates that the observed noise levels are consistent with previously reported values for printed and organic transistors [62–67]. In OFETs, low-frequency noise is predominantly attributed to a combination of mobility fluctuations and carrier number fluctuations arising from trap states at the semiconductor-dielectric interface. At lower gate bias conditions, where the carrier density in the channel is reduced, fluctuations in the charge transport pathway caused by structural disorder, molecular disorder, and grain boundaries can result in a stronger contribution from mobility fluctuation. With increasing gate bias, a large concentration of carriers is accumulated at the semiconductor electric interface, increasing the sensitivity of the channel current to charge trapping events and thereby enhancing the contribution of carrier number fluctuations. The relative importance of these mechanisms strongly depends on factors such as the semiconductor morphology, trap density, dielectric interface quality, and device processing conditions. Therefore, the mixed noise behavior observed in the present work is consistent with the complex transport mechanisms typically reported for polycrystalline organic semiconductors. Further improvements in semiconductor quality and interface engineering are expected to reduce trap-related fluctuations and improve the overall noise performance of printed OFET technologies. The low-frequency noise characteristics of flexible p-type OFETs were investigated through PSD analysis, demonstrating a dominant $1/f^{\gamma}$ dependence with $\gamma \approx 1$, characteristic of flicker noise. The results indicate that the noise originates from combined mobility and carrier-number fluctuations caused by charge trapping and de-trapping at the semiconductor–dielectric interface. Furthermore, the extracted noise mechanism is sensitive to threshold voltage extraction, highlighting the importance of accurate parameter determination for reliable OFET noise analysis and performance optimization.

3.8 Conclusion

This chapter presented the development of a FH-OPDK for a p-type OFETs fabricated on flexible substrates, providing a comprehensive design infrastructure for printed integrated circuits. Device characterization, including electrical measurements, variability analysis, and low-frequency noise characterization, enabled the development of an accurate compact transistor model that, together with the technology-specific layer definitions, material information, and fabrication design rules, formed the basis of the FH-OPDK. The integration of these elements within an EDA environment established a complete design flow for printed electronics, supporting schematic capture, circuit simulation, layout generation, and physical verification. The developed design framework was validated through a reusable standard -cell library and the successful realization of larger functional circuits, including a a 4×16 address decoder and a 16×16 active sensor matrix integrating sensing and amplification elements. The close agreement between simulation and experimental results demonstrates the reliability of the proposed design methodology and its capability to enable complex printed electronic systems. Future work will focus on improving device uniformity, refining compact model accuracy, and expanding the standard-cell library to support increasingly sophisticated integrated circuit for flexible sensing, wearable electronics, and intelligent large-area application.

4. Pass-gate-logic digital circuits using EGT

The realization of practical integrated circuits using emerging transistor technologies requires circuit-design methodologies that accommodate the electrical characteristics and fabrication constraints of the underlying devices. Since many printed transistor technologies are predominantly unipolar, conventional CMOS logic cannot be directly implemented, motivating the development of alternative logic families [10, 34, 36].

Among these technologies, EGTs are particularly attractive due to their low-voltage operation, solution-process compatibility, and suitability for flexible and large-area electronics. However, the lack of complementary p-type counterparts in typical printed EGT technologies limits the direct implementation of conventional CMOS logic, motivating the use of alternative circuit topologies for digital logic design. In this context, pass-gate logic offers an effective solution by employing transistors as electrically controlled switches, enabling compact and area-efficient digital circuits with a reduced number of devices [4, 13, 18, 38]. This approach simplifies circuit topology, lowers parasitic effects, and improves switching speed and energy efficiency, while also enhancing fabrication yield [18].

This chapter presents the design and implementation of pass-gate-logic circuits using indium-oxide-based EGTs [68]. Following device characterization and compact-model development, fundamental digital building blocks, including AND, OR, and XNOR gates, are designed, simulated, fabricated, and experimentally evaluated, demonstrating the feasibility of pass-gate logic for emerging printed transistor technologies [38, 69].

4.1 Device structure, materials, and fabrication of EGT

EGTs represent a class of thin-film transistors that utilize an electrolyte layer as the gate dielectric to achieve efficient channel modulation at low operating voltages. Unlike conventional field-effect transistors, where a solid dielectric is employed, EGTs rely on the formation of an Electronic Double Layer (EDL) at the electrolyte–semiconductor interface, as shown in Fig. 4.1. This EDL exhibits an extremely high

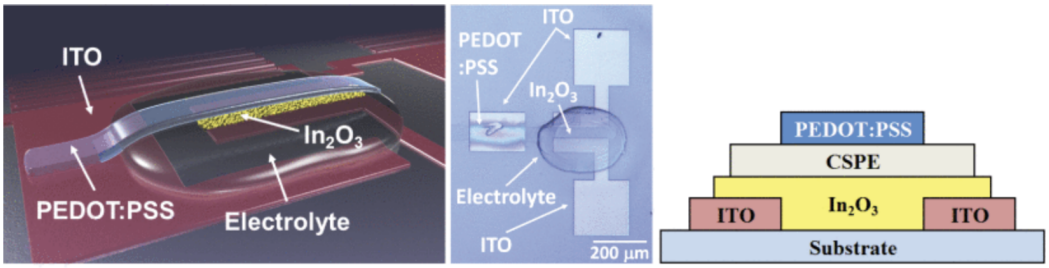


Figure 4.1: a)Graphical view, b)Optical view, and c)Cross sectional view of EGT [68], licensed under CC BY-NC-ND 4.0.

capacitance, enabling strong electrostatic control over the channel even at gate voltages below 1 V. Such characteristics make EGTs particularly attractive for printed and flexible electronics [70].

The typical structure of an EGT consists of a bottom-contact configuration with source and drain electrodes patterned on a substrate, followed by a semiconducting channel layer, an electrolyte layer, and a top-gate electrode. In the device presented here, indium oxide (In_2O_3) is used as the active semiconductor channel due to its high electron mobility and compatibility with solution-based processing. The source and drain electrodes are formed using indium tin oxide (ITO), while the gate electrode is realized using a conductive polymer such as PEDOT [71].

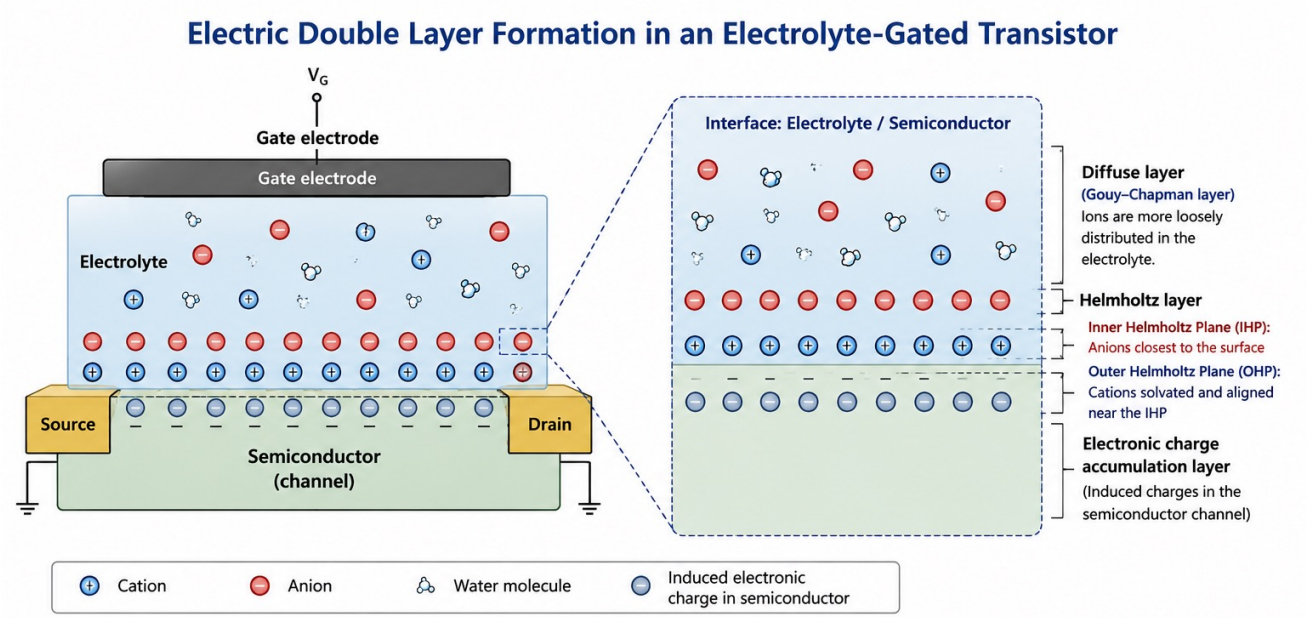


Figure 4.2: Electric double-layer formation in an electrolyte-gated transistor. Adapted from an illustration generated with AI assistance based on the author's concept and subsequently modified by the author.

The electrolyte layer, positioned between the gate electrode and the semiconductor channel, plays a crucial role in the operation of electrolyte-gated transistors. When a gate voltage is applied, mobile ions within the electrolyte migrate towards

the gate/electrolyte and electrolyte/semiconductor interfaces, forming EDLs as illustrated in Fig. 4.2. At the interfaces, oppositely charged ions accumulate in a compact region known as Helmholtz double layer, consisting of the inner and outer Helmholtz planes, while more loosely distributed ions extend into the electrolyte as the diffuse layer. The electric field generated by these ionic layers induced electronic charges in the semiconductor channel, creating an electronic double layer that modulates the channel conductivity. Due to extremely high interfacial capacitance of these nanometer-scale EDLs, efficient charge accumulation can be achieved at significantly lower operating voltages compared with conventional oxide-based gate dielectrics [36]. EGT can be fabricated using a wide range of material and systems and processing techniques depending on the targeted application and device architecture. Semiconductor layer may consist of organic semiconductors, inorganic metal oxide, or other solution processable materials, while the electrolyte can be implemented using liquid electrolytes, ion gels, or solid polymer electrolytes. Depending on the material choice, fabrication approaches can involve conventional micro-fabrication techniques such as photolithography and vacuum deposition, as well as low-cost solution-based methods including spin coating, screen printing, and inkjet printing [71]. In the context of printed inorganic EGTs, solution processable metal oxide semiconductors, such as indium oxide(In_2O_3) are commonly employed due to their high carrier mobility, optical transparency and, compatibility with large-area fabrication techniques. Indium oxide inks can be prepared from precursor solutions or nano-particle dispersions. Precursor-based inks generally required post-deposition thermal annealing at temperature between 300 °C and 450 °C to convert the precursor into a high-quality semiconducting oxide film. This process can produce films with excellent electrical properties; however, the relatively high annealing temperatures may limit compatibility with temperature-sensitive flexible substrates [72].

Table 4.1: EGT stack materials, fabrication techniques, and corresponding layer thicknesses [68].

EGT Stack	**Material**	**Fabrication Technique**	**Layer Thickness**
Active layer	In_2O_3	Ink-jet printing	100 nm
Dielectric	CSPE	Ink-jet printing	5 µm
Gate	PEDOT:PSS	Ink-jet printing	100 nm
Source/Drain	ITO	Laser ablation	150 nm

The electrolyte layer in printed EGTs is often realized using composite solid polymer electrolytes or ion gels. The EGT presented in this section consist of a composite electrolyte consisting of lithium perchlorate ($LiClO_4$) and a polymer matrix such as polyvinyl alcohol (PVA) is employed. Solvents such as dimethyl sulfoxide (DMSO) and propylene carbonate are used to facilitate ionic transport and processability. The resulting electrolyte formulation is compatible with inkjet printing and can be deposited at room temperature [72]. The fabrication of the electrolyte gates transistor follows a multi-step process. Initially, the source and drain electrodes are patterned on the substrate using laser ablation. Then the indium oxide channel layer is deposited using inkjet printing of precursor solutions, followed by

post processing steps of thermal annealing, to achieve the desired film properties. Next, the electrolyte layer is deposited over the channel region using inkjet printing. This step is critical, as uniform coverage and proper ionic properties are essential for device operation. Finally, the top gate electrode, typically composed of PEDOT, is printed over the electrolyte layer to complete the device structure. The entire fabrication process is compatible with scalable printing techniques, enabling the realization of large-area electronics systems. Additionally, variations such as top-gate and side-gate architectures can be implemented depending on design requirements. [73]. Overall, the combination of printable metal oxide semiconductors, inkjet-processable electrolytes, and scalable fabrication techniques makes printed inorganic EGTs a promising platform for the realization of next-generation low-cost and large-area electronic systems.

4.2 Electrical characteristics

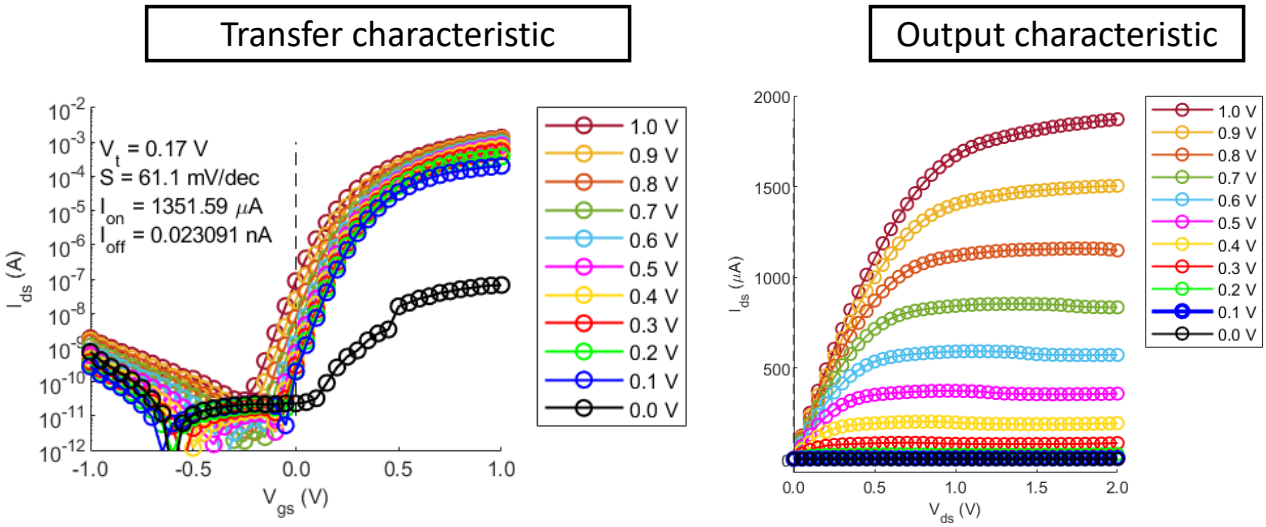


Figure 4.3: Transfer (V_{GS} vs I_{DS}) and Output (V_{DS} vs I_{DS}) characteristic of EGT [17].

In Fig. 4.3, the transfer and output characteristics of the EGT are shown. The extracted key device parameters include a threshold voltage of approximately 0.2 V, demonstrating low-voltage operation, and a subthreshold slope of approximately 74.8 mV/dec, indicating efficient gate control and sharp switching characteristics. Furthermore, the EGT exhibits a high on/off current ratio on the order of 10^6, ensuring a clear distinction between the logic states. The gate capacitance, reaching values as high as several μF/cm^2, is a direct consequence of electric double-layer formation and is significantly larger than that of conventional dielectric-based transistors. Additionally, a field-effect mobility of approximately 52 cm^2/(V $\cdot$ s) is achieved, highlighting the suitability of indium oxide for high-performance applications. These characteristics collectively demonstrate that EGTs can deliver high performance at low operating voltages, which is essential for energy-efficient printed electronics systems.

4.3 Digital circuit design

4.3.1 Resistor transistor topology

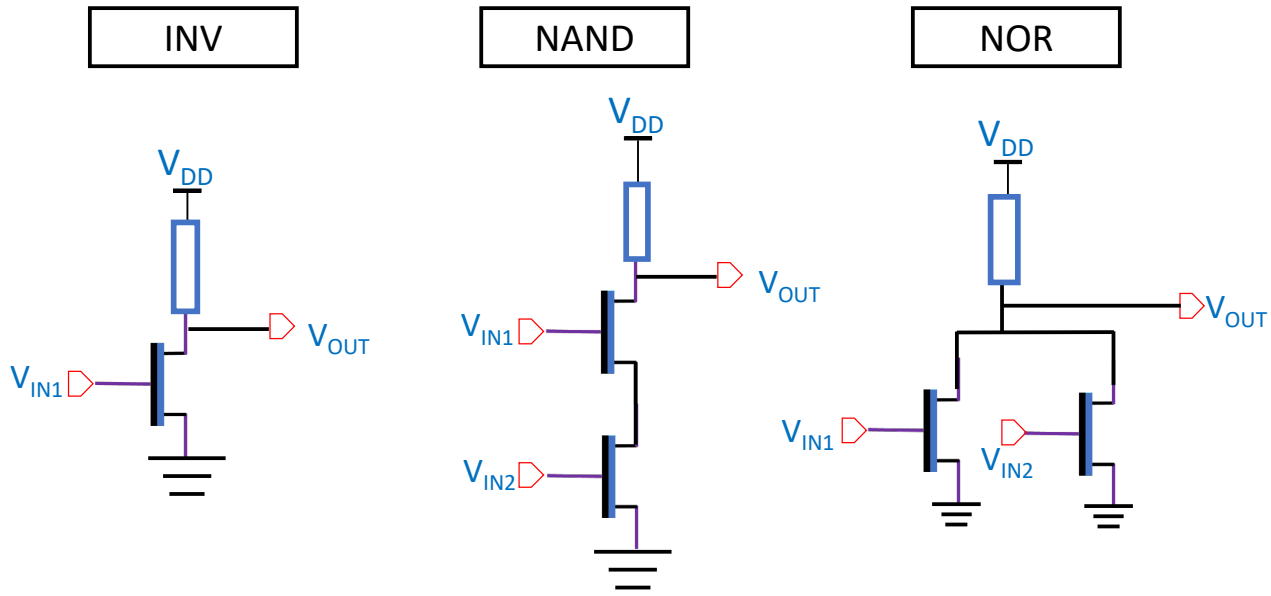


Figure 4.4: Circuit schematic of logic gates based on RTL topology using EGT.

Circuit level implementation becomes essential to evaluate the suitability of the here presented EGT technology for digital applications. As described in the previous work, accurate modeling of EGT behavior is achieved by combining different approaches for distinct operation regions [74]. The integration of this model into SPICE and PDK enables reliable prediction of circuit performance under varying conditions and corners [74]. Based on the developed compact modelling framework, initial digital circuits were implemented using RTL and TTL topologies. RTL is one of the earliest digital logic families, where resistive elements are used to establish the logic states and transistors acts as switching devices. Similarly, TTL employs transistors for both the switching operation and logic functionality, enabling improved switching speed and fan out compared with RTL . Although modern silicon-based integrated circuits predominantly rely on CMOS technology due to its high noise immunity, low static power consumption, and excellent scalability, the direct implementation of CMOS-like architectures in emerging printed electronic technologies remains challenging because of the limited availability of complementary p-type and n-type devices, larger process variations, and material non-idealities [18]. Therefore simpler unipolar logic approaches such as RTL and TTL, provide starting point for evaluating capability of OFET devices to realize digital functions. As shown in Fig. 4.4, fundamental logic gates including inverters, NAND, NOR can be constructed using these topologies. Their simple architecture and reduced fabrication requirements make them attractive for early-stage demonstrations and proof-of-concept printed circuits. However, the scalability of RTL and TTL circuits is limited due to their dependence on resistive loads, increased static power consumption, reduced noise margins, and sensitivity to device variability. The limitations become more pronounced when implementing complex circuits such as a full adder. An RTL-based full adder realized using multiple NAND gates requires a relatively

large number of transistors and interconnections, increasing the overall circuit area and fabrication complexity. In printed electronics, additional routing layers and overlapping conductive tracks are difficult to realize reliably with current printing technologies. Consequently, while RTL and TTL topologies are valuable for demonstrating basic logic functionality, more compact circuit approaches are required to enable scalable large-area printed electronic systems. To address these challenges, alternative circuit topologies are explored with the objective of reducing the overall transistor count and simplifying interconnect requirements. In parallel, efforts are made to investigate improved fabrication strategies that enable reliable realization of overlapping metal layers. This combined approach aims to enhance circuit feasibility, reduce fabrication constraints, and improve the overall performance of printed electronic systems. In this context, pass gate topologies offer promising approach by utilizing transistors as controlled switched.

4.3.2 Pass gate logic

Although RTL and TTL topologies provide a simple and effective means for realizing basic digital functions, their scalability toward complex printed electronic circuits remains limited. Resistive loading contributes to static power consumption, and the increased number of devices and interconnections results in larger parasitic resistance, capacitance and longer propagation delays. These challenges are particularly relevant for EGT-based circuits, where device variability, processing limitations, and relatively slower switching characteristics must be considered during circuit design. To address these limitations, pass-gate logic is explored as an alternative design methodology. In this approach, transistors act as voltage-controlled switches that directly transfer logic levels between nodes, eliminating the need for resistive elements. Hence, passive component and circuit complexity reduces. the intermediate modes minimizes parasitic resistance and capacitance. Also, the reduced transistor count enhances fabrication yield and simplifies layout design, which is particularly advantageous for large-area and printed electronic systems. The use of pass-gate logic is advantageous for printed transistor technologies, including EGT-based circuits, as it enables a reduction in transistor count and interconnect complexity. This is particularly beneficial in printed electronics, where large device dimensions, process variations, and limited multilayer interconnect capabilities can restrict circuit scalability. Nevertheless, issues such as threshold voltage loss, reduced noise margins, and signal degradation remain important design considerations. Further, individual gates such as AND, OR, and XOR are implemented using PGL, with simulation and experimental result.

4.3.2.1 AND gate

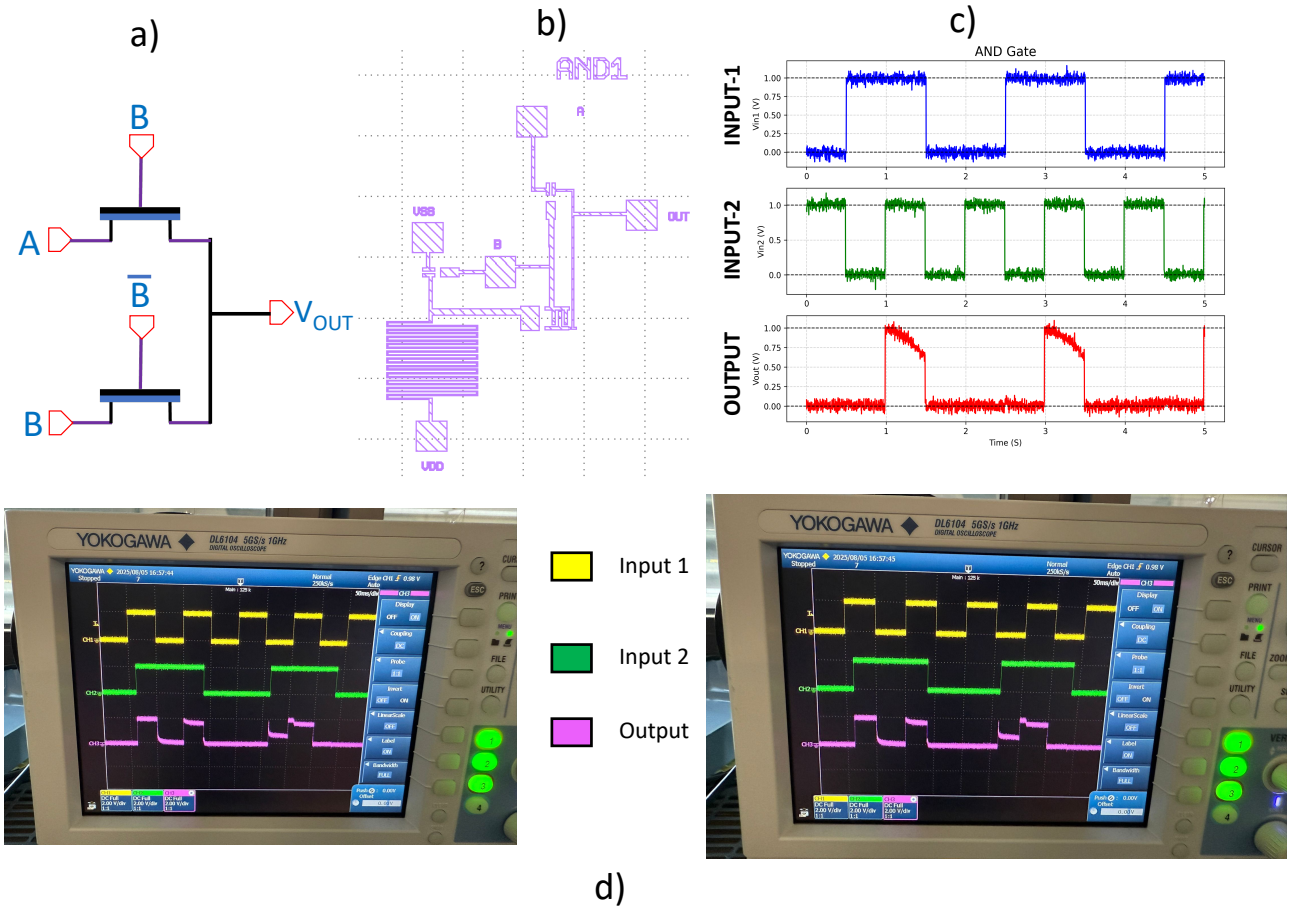


Figure 4.5: AND gate: a) circuit schematic, b) layout, c) simulated transient response and d) measured output waveform captured on oscilloscope.

The AND gate is implemented using two EGTs connected in a pass gate logic configuration, where the input combinations control the conduction paths to the output node. In this design, one EGT is driven by inputs A and B, while the second EGT is controlled by the complement of input B and input B, ensuring proper switching behavior. The output is determined based on whether a valid conduction path is established to pass a high logic level. For the input combination (A = 0, B = 0) both transistors remain off, resulting in a low output. When (A = 0, B = 1) the required conduction path is not fully established, and the output remains low. Similarly, for (A = 1, B = 0), the absence of simultaneous high inputs prevents conduction, yielding a low output. Only when both the inputs are high (A = 1, B = 1) the conduction path is activated, allowing the high logic level to propagate to the output, this realizing the AND functionality. The measured results as shown in Fig. 4.5, confirm correct logical behavior, with the output switching high only when both inputs are high. Minot deviations in signal levels and transition sharpness are observed, which can be attributed to variations in the printing process, material inconsistencies and device non idealities.

4.3.2.2 OR gate

The OR gate is implemented with 2 EGT connected in pass gate configuration where the combination of input signal decides the output behavior as in Fig. 4.6. In this design, the first EGT is controlled by input A and the complement of input B, while the second EGT is driven by input B. When A=1 and B = 0, the first EGT turns on, allowing the high logic level from A to propagate to the output. When B =1,

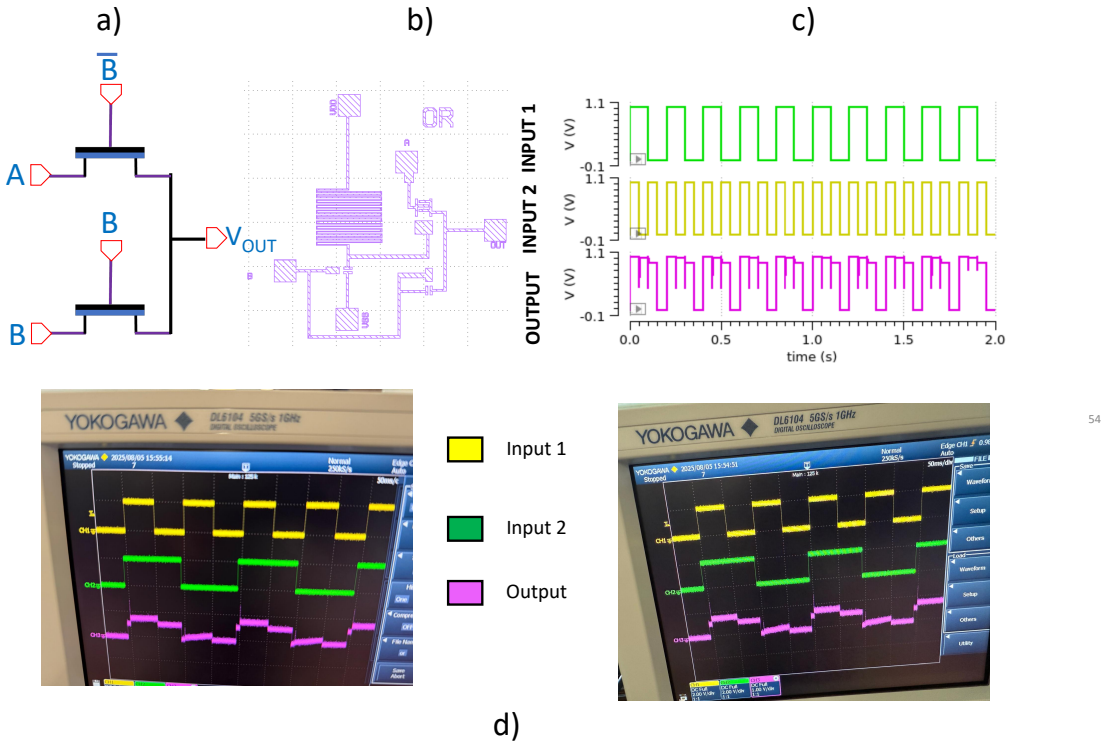


Figure 4.6: OR gate: a) circuit schematic, b) layout, c) simulated transient response and d) measured output waveform captured on oscilloscope.

regardless of the value of A, the second EGT conducts and directly passes the high level of B to the output. For the input combination A = 0 and B = 0, both transistor remains off, resulting in a low output. When both the inputs are high (A = 1, B = 1) the second EGT dominates and maintain a high output. This configuration ensures correct OR logic functionality while utilizing a minimal number of transistors in the pass-gate structure. Simulation results demonstrate the expected OR logic behavior with clear switching logic levels as in Fig. 4.6 . However, slight deviations from the ideal response are observed in the measured results, as shown in Fig. 4.6, which may be attributed to fabrication-induced variability inherent to printed electronic processes.

4.3.2.3 XNOR gate

The XNOR gate is implemented using a PGL configuration based on EGT device, enabling conditional signal transfer depending on the input combinations. The XNOR function leads to a high output when both inputs are equal and a low output when the inputs differ.

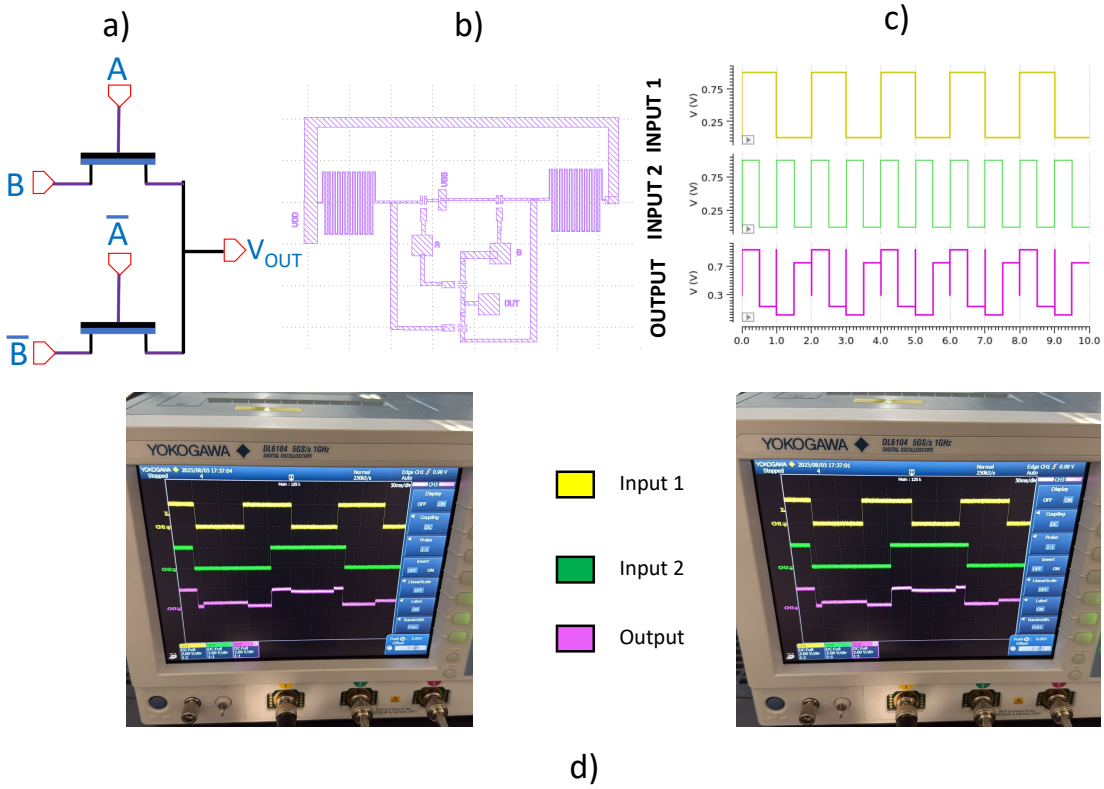


Figure 4.7: XNOR gate: a) circuit schematic, b) layout, c) simulated transient response and d) measured output waveform captured on oscilloscope..

This behavior is achieved selectively activating conduction paths that pass wither a high or low logic level to the output node. For the input combination (A = 0, B = 0), the corresponding conduction path allows a high logic level to be established at the output, resulting in logical '1'. When (A = 0, B = 1), (A = 1, B = 0), the switching configuration blocks the high-level propagation and instead pulls the output low, producing a logical '0'. For (A = 1, B = 1), both inputs activate the appropriate conduction path, again resulting in a high output. Simulation results confirm the expected XNOR functionality with clear logic transitions. Experimental measurements, as shown in Fig. 4.7 demonstrate similar behavior, although deviations in output amplitude and transition sharpness are observed.

4.3.2.4 Full adder based on XNOR gate

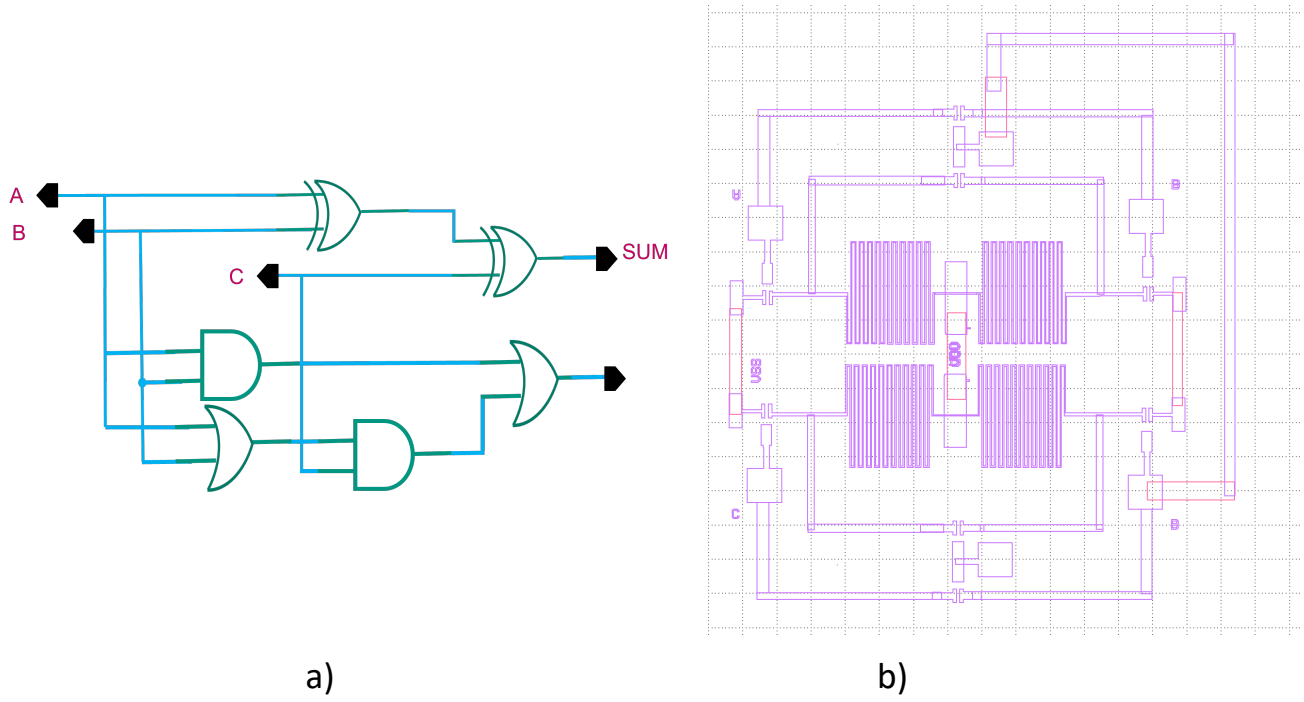


Figure 4.8: a) Full adder schematic using logic gates designed using pass gate logic, b) Corresponding full adder design.

Based on the implementation of AND, OR, and XNOR gates using pass-gate logic, a full adder architecture is proposed as a future step towards realizing more complex EGT-based digital circuits. The use of pass-gate logic reduces the number of transistors and interconnect complexity, making it suitable for printed electronic technologies where device density and fabrication constraints remain critical challenges. The proposed full adder utilizes the developed logic blocks to generate the sum and carry outputs from the three input signals, (A), (B), and C_{in}. The sum output is obtained through cascaded XNOR operations, while the carry output is generated using a combination of AND and OR gates. The corresponding schematic and layout are shown in Fig. 4.8 confirm the expected logical operation of the proposed architecture.

4.3.3 Conclusion

This chapter demonstrated the implementation of pass-gate logic circuits using indium EGTs for digital circuit realization in unipolar printed transistor technologies. Based on device characterization and compact model development, fundamental logic gates include AND, OR, and XNOR, were successfully designed, simulated, fabricated, and experimentally evaluated. The good agreement between simulation and measurement confirms the suitability of the developed models and validated PGL as an effective circuit design methodology for EGT technologies. By enabling compact and low-voltage digital circuit implementation, the presented work demonstrates the potential of PGL to the development of more complex printed integrated circuits. Future work can build upon these fundamental building block to realize larger combinational and arithmetic circuits, such a modular full address.

5. Industrial FinFET circuit design

Within the performance-driven evolution of silicon technology, the continued advancement of CMOS has been achieved through innovation in transistor architecture and process technology. As technology nodes continued to scale, conventional planar MOSFETs experienced increasing short-channel effects, leakage currents, and reduced electrostatic control of the channel [75]. To overcome these limitations, multi-gate transistor architectures were introduced, among which the FinFET has become the dominant device structure for advanced CMOS technologies [6]. By employing a three-dimensional fin-shaped channel surrounded by the gate on multiple sides, FinFETs suppress short-channel effects, reduce leakage currents, and enable continued improvement in performance, power efficiency, and integration density [76].

Industrial 16 nm FinFET technology represents a mature platform that combines an advanced transistor architecture with a comprehensive PDK and EDA environment, enabling the design, verification, fabrication, and characterization of complex integrated circuits [77]. As outlined in Chapter 1, this thesis investigates integrated-circuit enablement across different transistor technologies. This chapter focuses on the implementation of integrated circuits using an industrial FinFET PDK. It demonstrates the complete industrial design flow, from circuit design and layout to fabrication and experimental characterization, thereby extending the proposed design methodology to a mature silicon technology.

5.1 FinFET device structure

The FinFET represents a significant evolution from conventional planar MOSFET architectures, introduced to address the limitations associated with aggressive device scaling in deep-submicron technologies, as shown in Fig. 5.1 [78]. Unlike planar transistors, where the channel lies flat on the substrate, FinFETs utilize a three-dimensional structure in which the conducting channel is formed within a thin vertical silicon fin. The gate electrode wraps around the fin on multiple sides, typically forming a tri-gate structure, which provides superior electrostatic control over the channel. The key structural components of a FinFET include the source, drain, and

a vertically oriented fin that acts as the channel region. The gate stack, consisting of a high-k dielectric and a metal gate, surrounds the fin, allowing the electric field to effectively modulate the channel from multiple directions [6]. A defining characteristic of FinFET technology is the quantization of the effective transistor width. Unlike planar devices, where width can be continuously adjusted, the drive strength of a FinFET is determined by the number of fins employed. This introduces discrete sizing constraints that must be carefully considered during circuit design. However, this structure enables improved current drive per unit footprint and better scalability [4].

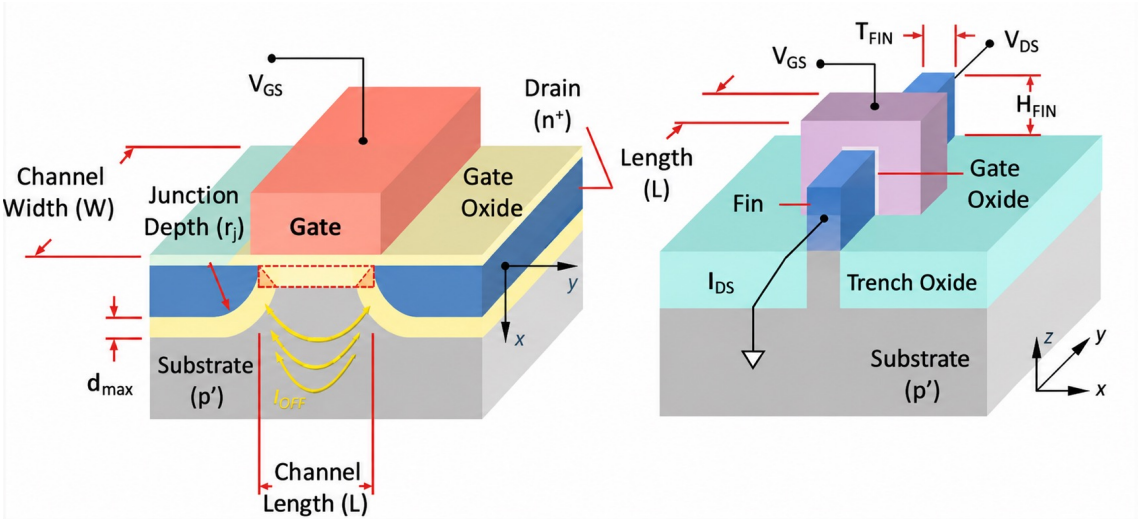


Figure 5.1: Structural comparison between conventional MOSFET and FinFET devices.

Furthermore, the three-dimensional geometry enhances carrier transport and reduces leakage currents, enabling lower operating voltages and improved energy efficiency. The use of advanced materials, including high-k dielectrics and metal gates, further enhances device performance by reducing gate leakage and improving threshold-voltage control [79, 80].

Overall, the FinFET structure provides a robust solution for continued CMOS scaling, offering improved performance, reduced power consumption, and enhanced reliability compared to conventional planar MOSFETs. These advantages make FinFETs the dominant device architecture in advanced technology nodes [79, 81].

5.2 Design Implementation

In addition to circuit-level simulations, the design flow was extended toward practical implementation using an industry-level 16-nm FinFET technology through a complete tape-out process. This step is critical in modern integrated-circuit design, as it enables validation of circuit functionality under real fabrication conditions and provides insights into layout-dependent effects that are not fully captured in schematic-level simulations.

The design process followed a standard digital-and-analog layout flow, including schematic design, layout generation, and verification stages such as DRC and LVS.

Particular attention was given to FinFET-specific design constraints, such as quantized transistor widths defined by the number of fins, restricted layout grids, and complex interconnect rules. These constraints required careful optimization of transistor sizing and placement to achieve the desired electrical performance while maintaining design-rule compliance. One of the main challenges encountered during the tape-out process was the increased complexity of layout design compared to conventional planar CMOS technologies. The three-dimensional device structure and stricter design rules necessitated precise alignment and routing strategies, especially in densely packed regions. Additionally, parasitic effects introduced by advanced interconnect stacks had to be considered to ensure signal integrity and reliable operation.

The complete layout was successfully verified and prepared for fabrication, demonstrating the feasibility of implementing the designed circuits in a state-of-the-art FinFET technology node. This experience highlights the importance of bridging the gap between simulation and physical realization, and it emphasizes the practical considerations required for advanced semiconductor design. The tape-out process not only validates circuit functionality but also provides a deeper understanding of technology-specific limitations and design trade-offs in nanoscale CMOS systems, as shown in Fig. 5.2.

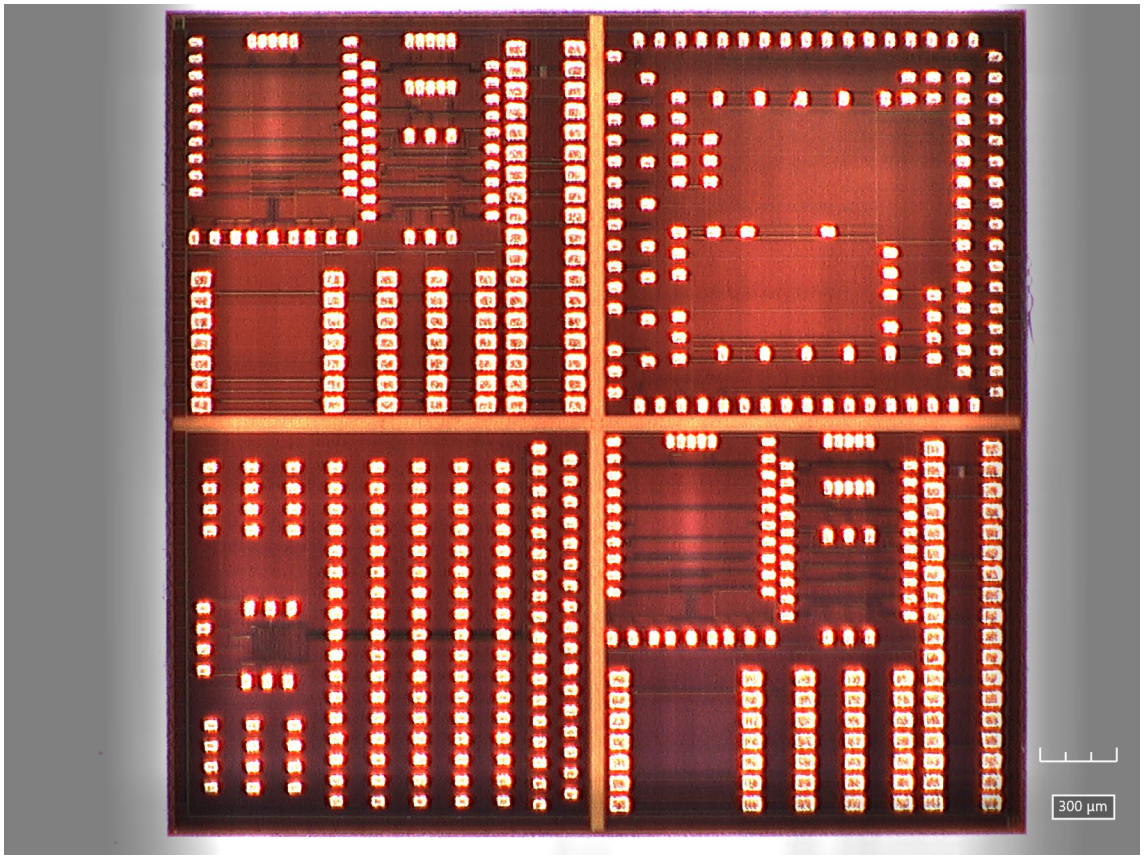


Figure 5.2: Test chip Callisto based on industrial FinFET technology.

5.3 Measurement setup

The test chip incorporates a structured pad frame with seven pads per row, comprising four signal pads (input/output), one supply pad (V_{DD}), and two ground pads (V_{SS}). Custom pads are implemented with dimensions of $67 \times 90\,\mu$m and a pad pitch of $100\,\mu$m, ensuring compatibility with probing and packaging constraints. All I/O pads are protected by Electro Static Discharge (ESD) structures consisting of a dual-diode network combined with an RC-triggered power clamp between V_{DD} and V_{SS}, providing robust protection against transient overvoltage events.

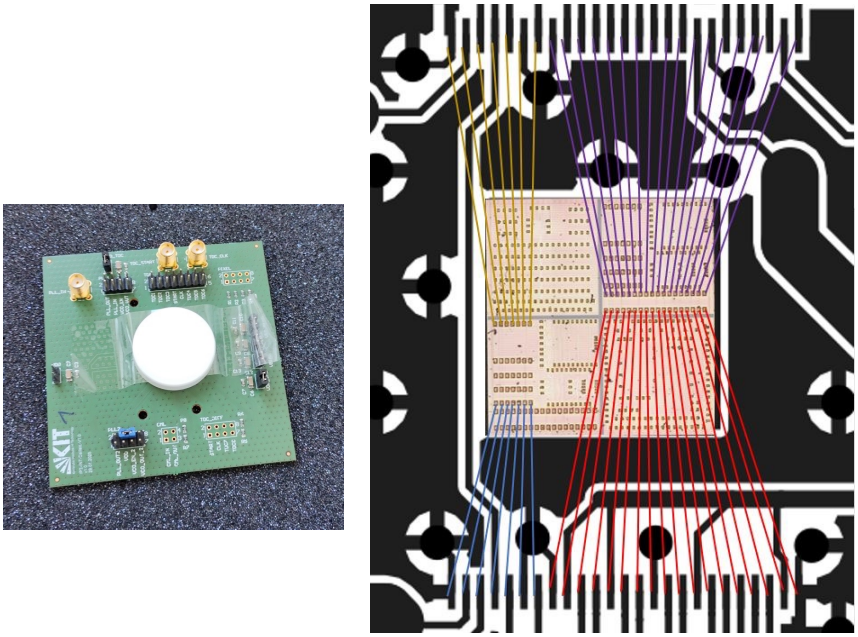
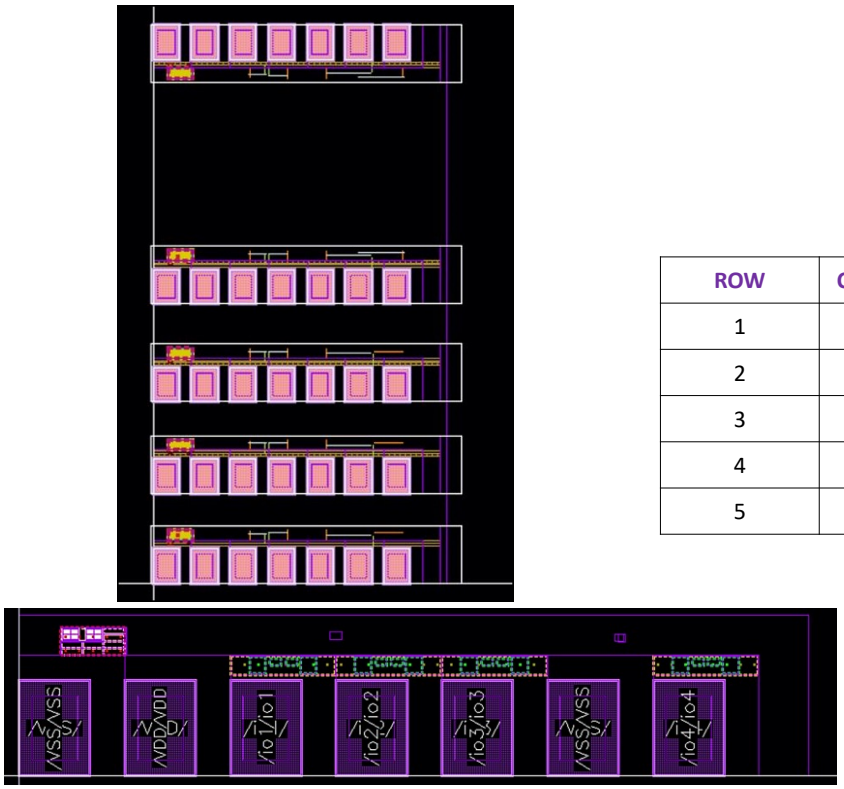


Figure 5.3: In-house designed PCB and chip bonding plan for measurement.

The chip was fabricated as bare-die chiplets featuring copper micro-bump interconnects. Initial electrical characterization was performed using a probe station; however, reliable contact was hindered by the circular geometry of the micro-bumps, which complicates precise needle alignment. Furthermore, the probe setup introduced additional parasitic resistance and capacitance due to extended cable lengths, adversely affecting high-frequency measurements. To mitigate these limitations, a dedicated in-house PCB was assembled, as shown in Fig. 5.3. The PCB enables stable biasing of multiple power domains via headers and incorporates decoupling capacitors across all major supply nets to suppress noise and voltage fluctuations. High-frequency single-ended signals are routed through SMA connectors to ensure controlled impedance and signal integrity. Additional signals are accessed via pin headers, while adjacent ground pins enable quasi-differential signal configurations.

5.4 Callisto chip

This test chip was designed to evaluate and characterize key timing and frequency-generation building blocks, including a Phased Look Loop (PLL), a standard-cell-based ring oscillator, and a Voltage Controlled Oscillator (VCO). Such circuits are fundamental in modern integrated systems for clock generation, synchronization, and signal processing. The chip serves as a silicon validation platform to compare simulated and measured performance under real operating conditions.



ROW	Circuit (Left)	Circuit (Right)
1	PLL	VCO
2	PLL	VCO
3	PLL	RINGO (ULVT)
4	PLL	RINGO (LVT)
5	PLL	RINGO (NOM)

Figure 5.4: Test chip floor plan and circuit allocation.

This chip was implemented in an industry-level 16 nm FinFET technology node as part of a university shuttle program, with a nominal supply voltage of 1.0 V. Attention was given to layout planning, routing considerations, and parasitic-effect minimization. In particular, the chip enables analysis of frequency stability, tuning behavior, and sensitivity to Process Voltage Temperature (PVT) variations. Additionally, it allows comparison between standard-cell-based and custom-designed analog blocks.

The test chip, **Callisto**, was the culmination of three designs from collaborators in academia and industry. The circuits contributed by the author include the PLL, a standard-cell-based ring oscillator, and the VCO. In addition, the chip includes a Time-to-Digital Converter (TDC) and noise-analysis circuits. The chip was funded as part of a university shuttle program with a semiconductor-industry partner.

5.4.1 Ring oscillator

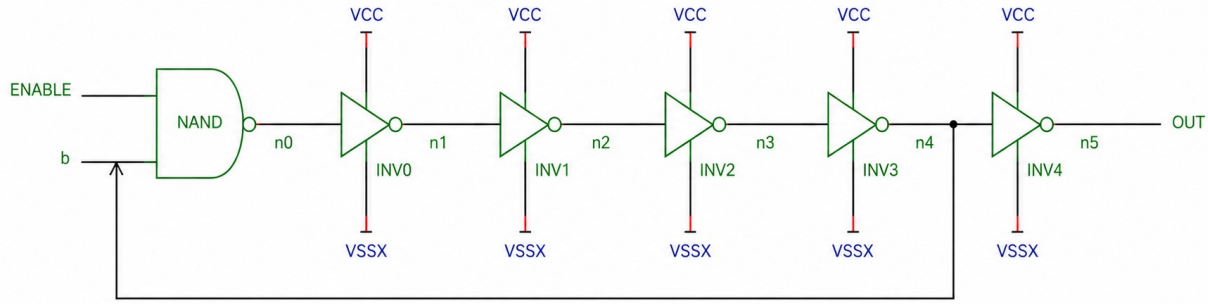


Figure 5.5: Circuit schematic of the ring oscillator.

This section presents the measurement results of the implemented ring oscillator. The ring oscillator is designed using a standard-cell-based odd-numbered inverter chain. The first stage is a NAND gate used to enable the ring oscillator, followed by four inverters. The inverters are based on n-type and p-type FinFET devices. The circuit serves as a test structure for delay characterization and process-sensitivity analysis.

Measurement parameters.

The oscillator output was measured across a supply-voltage range of $V_{DD} = 0.53$ V to 0.78 V, as shown in Fig. 5.5. Waveforms were captured using high-speed measurement equipment, and current consumption was recorded for each operating point.

Results and analysis.

From the output waveforms, oscillatory behavior is maintained up to an enable voltage V_{ENABLE} of 0.6 V. Beyond this value, the oscillation degrades or ceases, which may be attributed to changes in the operating conditions of the enable-controlled logic stage, affecting the feedback mechanism required for sustained oscillation. Furthermore, the current consumption increases nonlinearly with V_{ENABLE}, which can be attributed to increased switching activity and the associated short-circuit and dynamic power dissipation in the CMOS inverters. The measured oscillation frequency exhibits a positive correlation with the supply voltage V_{DD}, consistent with theoretical expectations, since a higher supply voltage reduces propagation delay and increases the switching speed of the inverter stages.

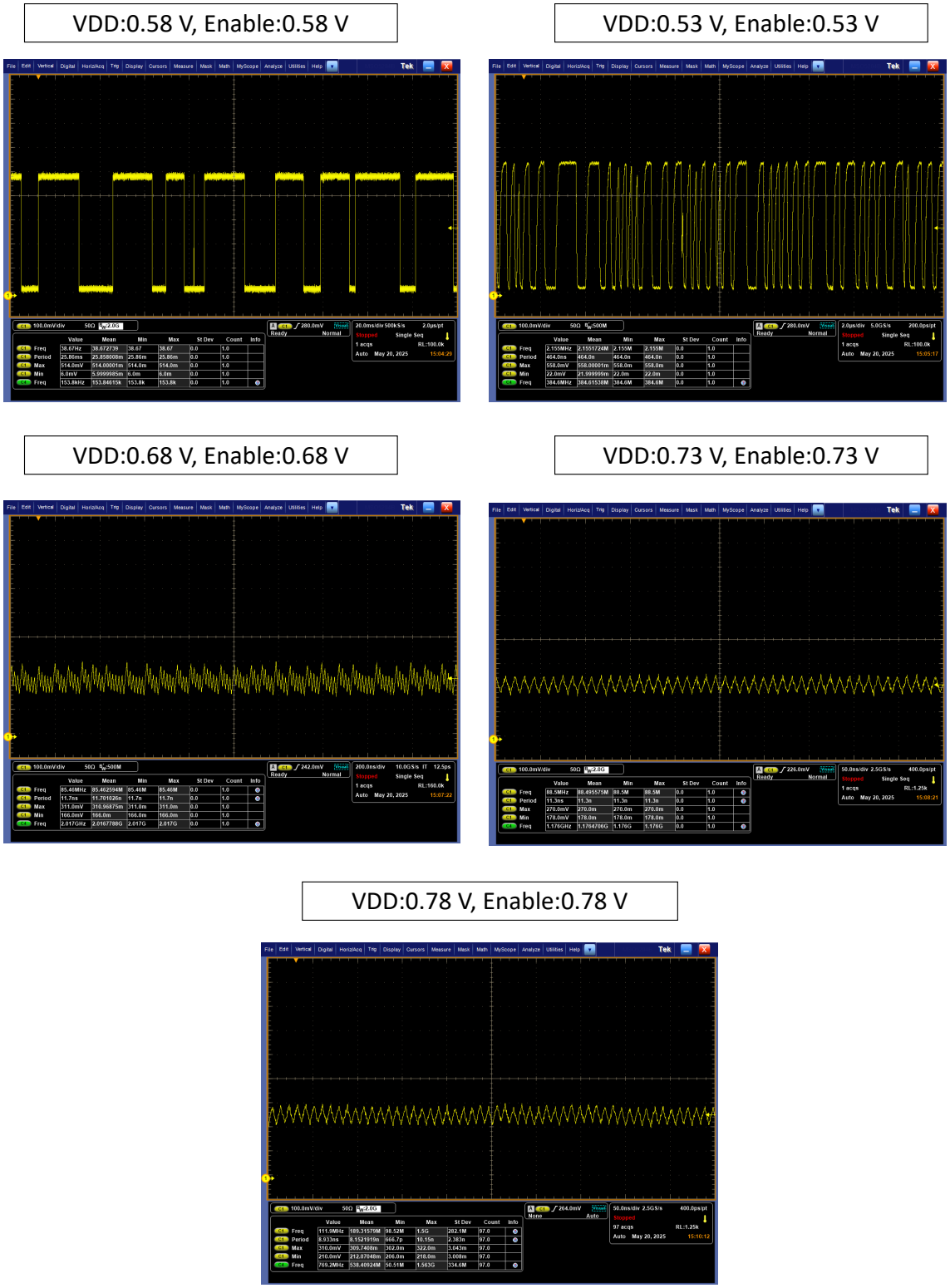


Figure 5.6: Measured output waveforms captured with an oscilloscope at different supply voltages (V_{DD}) and enable voltages (V_{ENABLE}).

Output waveforms.

In Fig. 5.6, the output waveforms were recorded for different V_{DD} levels. As the supply voltage increases, the propagation delay of the inverter stages decreases, result-

ing in a higher oscillation frequency. The waveforms demonstrate stable oscillation across the measured range.

5.4.2 Voltage-controlled oscillator

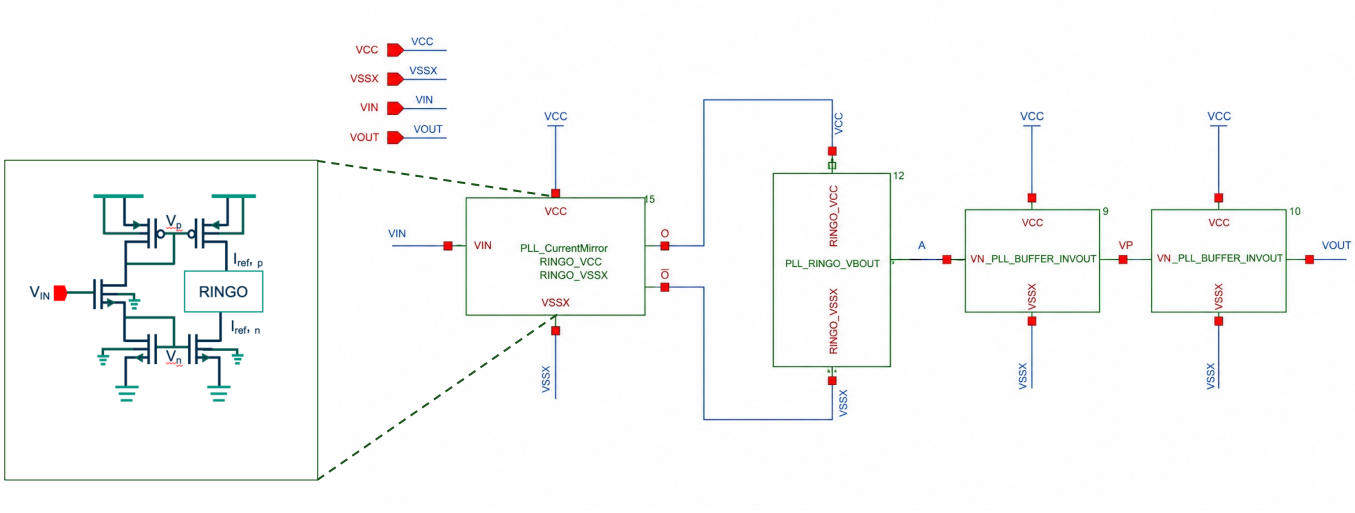


Figure 5.7: Circuit schematic of the voltage-controlled oscillator.

The VCO employs a current-starved ring oscillator architecture with a current mirror generating controlled bias currents $I_{ref,p}$ and $I_{ref,n}$, as shown in Fig. 5.7. By varying the input control voltage V_{IN}, the mirror modulates the charging and discharging currents of the inverter stages, thereby tuning the oscillation frequency. This approach enhances linearity and reduces sensitivity to supply variations.

The oscillator core consists of a 5-stage inverter chain, satisfying the Barkhausen condition for sustained oscillation. The oscillation frequency is determined by the propagation delay of each stage, which is inversely proportional to the bias current. Lower current increases delay and reduces frequency, while higher current enables faster switching and higher frequencies.

To ensure measurement reliability, two cascaded inverter buffers are used to isolate the oscillator from load effects, minimizing frequency pulling. Overall, the design achieves stable and controllable frequency tuning through current-regulated delay modulation.

Measurement parameters.

All measurements were performed at a fixed supply voltage of $V_{DD} = 0.8$ V. The VCO was characterized by sweeping the enable/control voltage from 0.3 V to 0.7 V, corresponding to a frequency from approximately 489 kHz to 60 MHz. The output frequency was extracted from recorded waveforms, while the supply current was measured for each operating point, ranging from 0.403 mA to 0.502 mA. Additional measurements were conducted using pulse inputs with varying amplitudes (100 mV_{pp}) and frequencies to evaluate the dynamic response.

Table 5.1: Measured oscillation frequency as a function of supply voltage.

V_{DD} **(mV)**	**Frequency** (MHz)
400	1.8
450	3.8
500	8.0
550	15.6
600	29.8
650	40.0
700	67.0
750	135.0
800	149.0

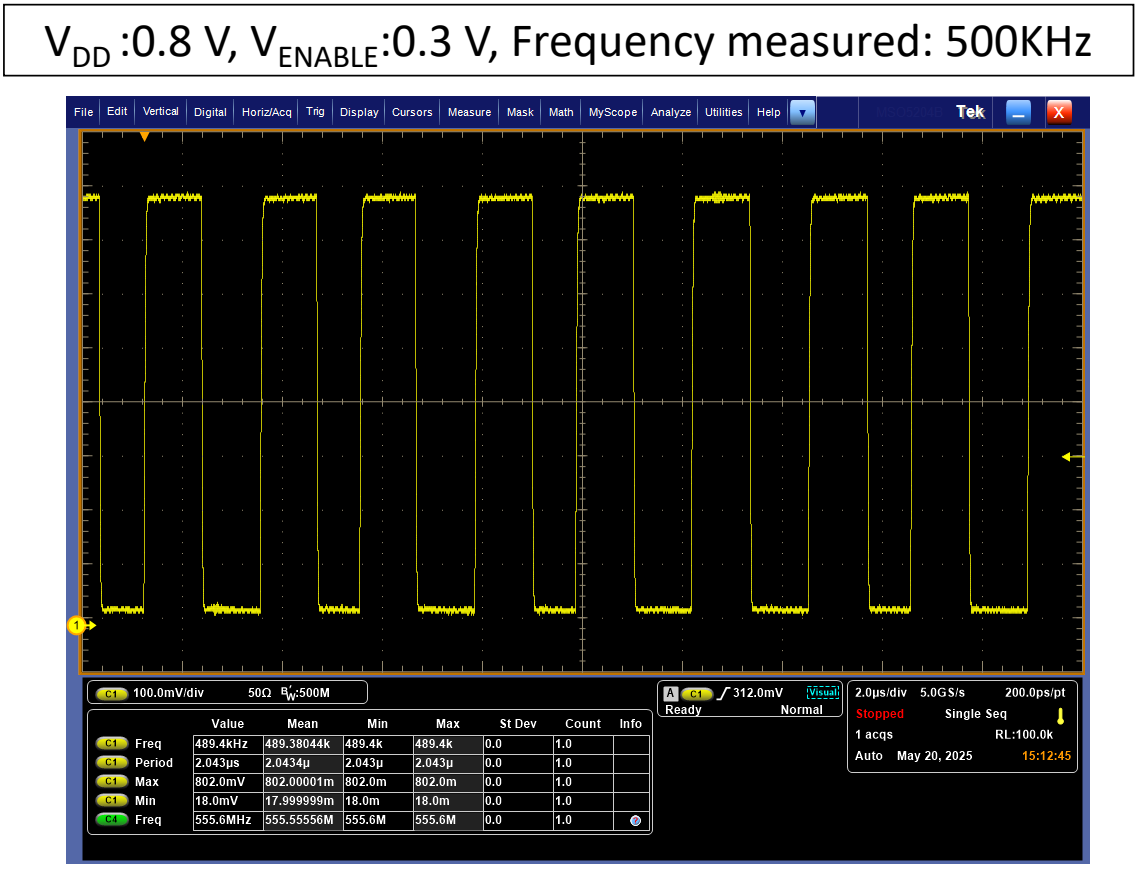


Figure 5.8: Measured VCO response captured with an oscilloscope.

The measured results demonstrate that the VCO operates reliably within a limited enable-voltage range. A fully stable oscillation is shown in Fig. 5.8. Stable oscillation is observed for enable voltages up to approximately 0.55 V, as seen in Table 5.1. Beyond this point, oscillatory behavior degrades and eventually ceases, likely due to the current mirror entering a non-ideal operating region where sufficient bias current is no longer maintained. This results in inadequate drive strength for the ring oscillator, preventing sustained oscillation. A strong dependence of oscillation frequency on the control voltage is observed, consistent with the expected behavior of a current-starved ring oscillator. As the enable voltage increases, the bias current

provided by the current mirror also increases, reducing the propagation delay of each inverter stage. Consequently, the oscillation frequency rises significantly from approximately 489 kHz at 0.3 V to 16 MHz at 0.58 V.

The results confirm a monotonic tuning characteristic within the functional range, indicating proper operation of the VCO mechanism. However, saturation or failure of oscillation beyond 0.55 V suggests limitations in the biasing network or possible nonlinearity in the current mirror. Overall, the measurements validate the expected relationship between control voltage, current, and oscillation frequency while highlighting practical constraints in the design.

5.4.3 Phase-locked loop

The implemented PLL consists of three primary blocks: a phase detector, Low Pass Filter (LPF), and VCO. The phase detector is realized using an XOR-based architecture derived from NAND-gate logic. The XOR phase detector generates an output proportional to the phase difference between the reference input signal and the feedback signal from the VCO.

The output of the phase detector is passed through a LPF, which translates the average phase error into a DC voltage. The resulting control voltage is then applied to the VCO, which is implemented as a current-starved ring oscillator. The VCO adjusts its oscillation frequency based on the control voltage, thereby closing the feedback loop and enabling frequency and phase synchronization.

Due to limitations in the measurement setup, particularly in generating and accurately probing high-frequency signals in the GHz range, full experimental validation of the PLL could not be performed. However, both simulation and measurement results of the individual building blocks, including the ring oscillator and VCO, demonstrate consistent and expected behavior. The strong correlation between simulation and measured results at the block level provides confidence in the overall design methodology and indicates that the integrated PLL is expected to function as intended under appropriate measurement conditions. The block diagram and layout of the PLL can be seen in Fig. 5.9 and Fig. 5.10.

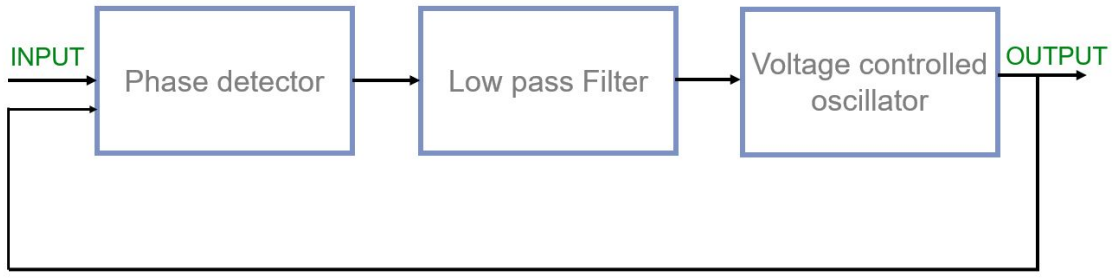


Figure 5.9: Block diagram of PLL.

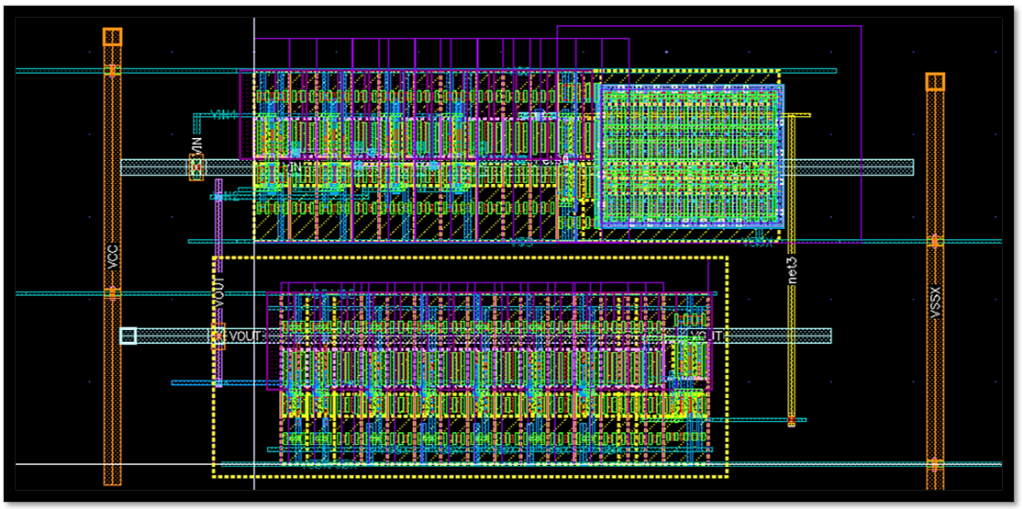


Figure 5.10: Layout of PLL.

5.5 Conclusion

This chapter highlights an advanced CMOS technology that complements the organic and inorganic approaches discussed in the previous chapters. A complete design and tape-out flow was carried out in industrial 16 nm FinFET technology, emphasizing both circuit-level design and physical implementation. Key challenges such as quantized transistor sizing, restrictive layout grids, and increased parasitic resistance and capacitance were addressed through careful design optimization. The successful completion of DRC and LVS verification confirms the viability of implementing mixed-signal building blocks in advanced technology nodes. The fabricated test chip, Callisto, integrates essential timing circuits, including a ring oscillator, a current-starved VCO, and a PLL. Measurement results of the ring oscillator and VCO demonstrate behavior consistent with theoretical expectations, particularly the dependence of oscillation frequency on supply and control voltage. Although full PLL characterization was constrained by measurement limitations at high frequencies, the strong agreement between simulation and experimental results at the block level provides confidence in the overall system functionality and design methodology. Looking forward, this work can be extended toward the integration of thinned silicon dies into flexible substrates, enabling applications in flexible and wearable electronics. Combining advanced FinFET-based circuits with flexible platforms presents new challenges in mechanical reliability, interconnect design, and thermal management, but also offers significant opportunities for next-generation, high-performance, and conformal electronic systems.

Summary and Outlook

This thesis addresses the challenge of enabling transistor technologies to evolve from individual device demonstrations into practical integrated-circuit platforms. While semiconductor technology has progressed along two complementary directions—performance-driven silicon technologies and application-driven printed electronics—both ultimately rely on mature integrated-circuit design methodologies. In contrast to silicon CMOS, many emerging transistor technologies continue to lack PDKs, compact models, and comprehensive EDA support. The primary objective of this work is therefore to bridge the gap between device-level research and practical integrated-circuit design.

The first contribution of this thesis addresses design enablement through the development of a FH-OPDK for hybrid printed OFET technology. Device characterization data are used to extract compact transistor models based on the VRHT mechanism, while statistical parameter variations are incorporated to accurately reproduce measured transistor behavior. The developed FH-OPDK contains compact models, technology files, layer definitions, design rules, verification utilities, and layout automation features, enabling complete front-end and back-end circuit design using commercial EDA tools. The application of the proposed design framework was demonstrated through the implementation of standard cells, decoder architecture, ring oscillators, and a pressure-sensor hardware demonstrator, confirming that printed transistor technologies can be designed using methodologies comparable to those employed in mature silicon CMOS technologies [16].

As part of the design infrastructure, the low-frequency noise behavior of printed OFETs was experimentally investigated to improve the understanding of device characteristics relevant to compact modeling. Noise measurements were analyzed using both Hooge mobility-fluctuation theory and McWhorter carrier-number-fluctuation theory [24, 26]. The extracted model parameters provide insight into the dominant physical mechanisms governing flicker noise and demonstrate that the relative contributions of mobility and carrier-number fluctuations depend on the transistor operating conditions and parameter-extraction methodology.

A second major contribution of the thesis focuses on circuit enablement for emerging transistor technologies. Since many printed transistor platforms are unipolar,

complementary CMOS logic cannot be directly employed. To address this limitation, pass-gate logic was investigated using indium oxide EGT. Fundamental digital logic gates (AND, OR, XNOR) were designed and experimentally validated, demonstrating that alternative circuit topologies can efficiently realize low-voltage digital functionality while reducing transistor count and accommodating the constraints of emerging transistor technologies [17].

The third contribution addresses system-level enablement through benchmarking against an industrial semiconductor design environment. Digital circuits were implemented using a commercial 16 nm FinFET PDK following the complete industrial design, verification, tape-out, and experimental characterization flow. Ring oscillators, voltage-controlled oscillators, and a phase-locked loop were successfully fabricated and evaluated.

Collectively, this thesis demonstrates that the successful realization of practical integrated circuits requires more than advances in transistor fabrication alone. By addressing complementary challenges in design infrastructure, circuit methodology, and industrial design validation, this work establishes a unified framework for integrated-circuit implementation using emerging transistor technologies. The presented methodology contributes toward bridging the gap between device innovation and system-level realization while supporting the development of future flexible, printed, and hybrid electronic systems.

Future work will focus on extending the proposed design framework to additional emerging transistor technologies, including complementary printed device platforms and heterogeneous organic–inorganic systems. The development of larger standard-cell libraries, automated synthesis methodologies, and enhanced compact models incorporating reliability and noise effects will further strengthen the applicability of the proposed FH-OPDK. Ultimately, the integration of emerging printed electronics with mature silicon technologies within unified design environments is expected to facilitate the realization of scalable hybrid electronic systems for next-generation wearable, biomedical, sensing, and large-area applications.

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