Hardware Implementation of the Opposite-Side Clamping Modulation and Gate-Drive Control for a 3-Level-ANPC Si/SiC Hybrid Converter

1st Yannik Becher
Institute of Electrical Engineering (ETI)
Karlsruhe Institute of Technology (KIT)
Karlsruhe, Germany
yannik.becher@kit.edu

2nd Marcus Becker
Institute of Electrical Engineering (ETI)
Karlsruhe Institute of Technology (KIT)
Karlsruhe, Germany
marcus.becker@kit.edu

3rd Nick Thönelt
Institute of Electrical Engineering (ETI)
Karlsruhe Institute of Technology (KIT)
Karlsruhe, Germany
nick.thoenelt@kit.edu

4th Rüdiger Schwendemann
Institute of Electrical Engineering (ETI)
Karlsruhe Institute of Technology (KIT)
Karlsruhe, Germany
ruediger.schwendemann@kit.edu

5th Marc Hiller
Institute of Electrical Engineering (ETI)
Karlsruhe Institute of Technology (KIT)
Karlsruhe, Germany
marc.hiller@kit.edu

***Abstract*—Three-level active neutral point clamped converters (3L-ANPC) provide improved output voltage quality. However, the large number of switching states and neutral current paths significantly complicates safe gate-drive control without operating the semiconductors outside the specifications. This paper presents a modulation strategy for a hybrid 3L-ANPC phase leg employing SiC MOSFETs as inner high-frequency switches and Si IGBTs as outer blocking devices. All 64 switching states are systematically classified, safe turn-on and turn-off rules with defined locking times are derived, and three gate-control strategies are comparatively evaluated.**

Opposite-side clamping is selected to minimize the semiconductor losses of the hybrid 3L-ANPC topology. Based on this strategy, detailed commutation sequences especially for zero-crossings are developed and analyzed to prevent overvoltages and short-circuit conditions. The resulting modulation and gate-drive control are implemented on an AMD Artix-7 FPGA using carrier-based 3L-SVPWM with zero-sequence injection.

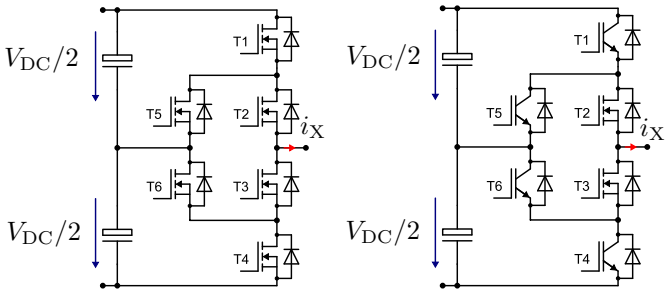
Experimental measurements on an Infineon hybrid 3L-ANPC module up to $800\,\mathrm{V}$ DC link voltage confirm fault-free commutation, the absence of critical overvoltages, enabling safe and efficient real-time operation of hybrid 3L-ANPC converters.

***Index Terms*—3L-ANPC, opposite-side clamping, modulation, hybrid topology**

I. Introduction

Three-level (3L) voltage-source converters offer several advantages over conventional two-level converters. They are particularly well suited for renewable-energy applications, such as grid-side interfacing and wind-turbine generator systems, as well as for automotive electric-drive applications. In particular, 3L inverters are highly attractive for supplying partially superconducting wind generators [1], which was the main driver for the development of this work.

The key advantages of a 3L topology include reduced semiconductor switching losses and an improved output-voltage waveform with lower harmonic distortion. This results in reduced harmonic filter losses on the grid or lower harmonic losses in the connected electric machine. A promising architecture is the three-level active neutral point clamped inverter (3L-ANPC). Its modular structure and the large number of degrees of freedom in the gate-drive strategy enable redistribution of semiconductor losses among the individual switches. This facilitates operation at higher voltage classes, up to the medium-voltage range, by means of series-connected power devices [2]–[4]. The main drawbacks are the increased component count, higher system cost, and greater control complexity. Fig. 1 illustrates two 3L-ANPC implementations: a full silicon carbide (SiC) metal-oxide-semiconductor field-effect transistor (MOSFET) configuration and a hybrid variant in which the outer switches T1/T5 and T6/T4 are replaced by silicon (Si) insulated-gate bipolar transistors (IGBTs). Although the hybrid topology reduces material costs, it generally results in higher semiconductor losses. However, these additional losses can be compensated by appropriate control strategies.



(a) Full-SiC (b) Si/SiC Hybrid

Fig. 1: 3L-ANPC topologies

TABLE I: Switching logic 3L-ANPC

(a) opposite-side clamping

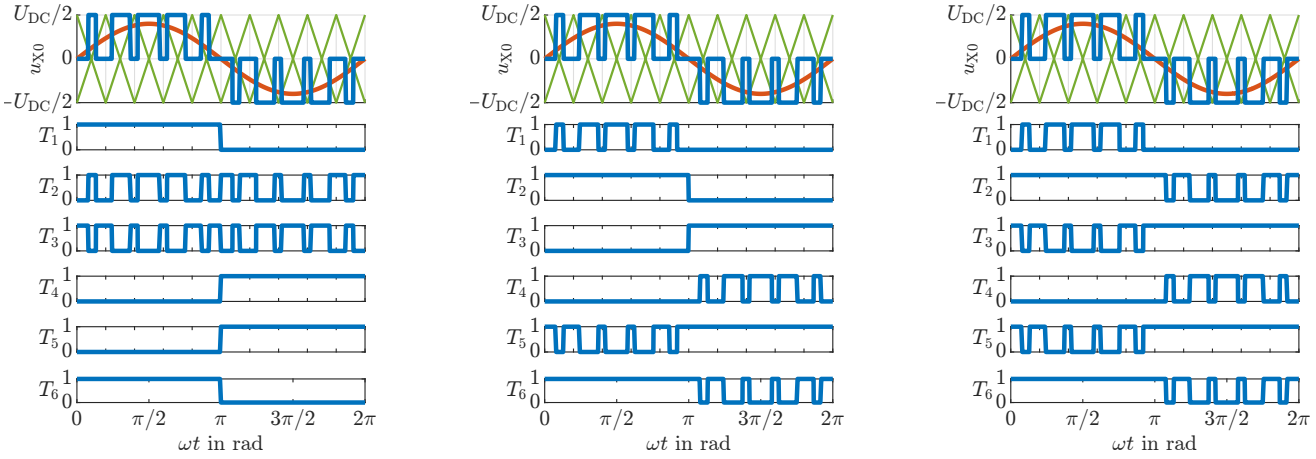
	v_{X0}	T_1	T_2	T_3	T_4	T_5	T_6
P	$+V_{DC}/2$	1	1	0	0	0	1
OL1	0	1	0	1	0	0	1
OU1	0	0	1	0	1	1	0
N	$-V_{DC}/2$	0	0	1	1	1	0

(b) same-side clamping

	v_{X0}	T_1	T_2	T_3	T_4	T_5	T_6
P	$+V_{DC}/2$	1	1	0	0	0	1
OU3	0	0	1	0	0	1	1
OL3	0	0	0	1	0	1	1
N	$-V_{DC}/2$	0	0	1	1	1	0

(c) full-path clamping

	v_{X0}	T_1	T_2	T_3	T_4	T_5	T_6
P	$+V_{DC}/2$	1	1	0	0	0	1
OUL1	0	0	1	1	0	1	1
N	$-V_{DC}/2$	0	0	1	1	1	0



(a) opposite-side clamping (b) same-side clamping (c) full-path clamping

Fig. 2: Logical gate signals T_X of the 3L-ANPC with 3L-CBPWM POD sinus, $f_{PWM}/f_{el} = 10$ and $m = 0.8$

II. 3L-ANPC Topology

A. Switching states

As shown in Fig. 1 3L-ANPC comprises six switches per phase, resulting in a total of $2^6 = 64$ possible switching states. Each transistor pair T1/T5, T2/T3, and T6/T4 forms a half-bridge. Every individual switch must be capable of blocking half of the DC-link voltage $V_{DC}/2$. At the output, the following three half-bridge voltage levels v_{X0} can be generated:

$$v_{X0} = \begin{cases} +V_{DC}/2 & \text{P} \\ 0 & \text{O} \\ -V_{DC}/2 & \text{N} \end{cases} \quad (1)$$

Out of the 64 possible switching states, only 27 are considered safe, whereas the remaining states are classified as critical or forbidden due to potential overvoltages or bridge short circuits [5]. For the neutral-point voltage $v_{X0} = 0$, a total of seven distinct neutral states O exist. This redundancy underlines the significantly increased control complexity of the 3L-ANPC compared to other three-level topologies.

B. Turn-on/off

In addition to avoiding critical or forbidden switching states, the correct turn-on and turn-off sequence of the transistors is essential [5]. In the idle condition, all switches are turned off except for the inner MOSFETs T2/T3. Keeping T2 and T3 turned on ensures that T1 and T4 each block half of the DC-link voltage $V_{DC}/2$, while maintaining an output voltage of $v_{X0} = 0$. Depending on the direction of the load current, a current path can be established through the free-wheeling diode of T5 or T6. After asserting the pulse-enable signal, it must be ensured that the inner switches T2/T3 and T5/T6 are turned on first. Only after a defined locking time may the outer switches T1 and T4 be turned on.
The turn-off sequence is initiated either by removing the pulse-enable signal or by the occurrence of a fault condition. In the first step, the outer switches T1 and T4 must be turned off. Subsequently, T2 and T3 are turned on to establish a defined blocking-voltage distribution. In the final step, T5 and T6 are turned off. Failure to follow the prescribed turn-off sequence may result in transient fault currents or overvoltages [5].

C. Gate control methods

For the mapping of the three half-bridge states $\{\text{P}, \text{O}, \text{N}\}$ to the logical gate signals $T_X \in \{0, 1\}$, several gate-drive concepts are available [6], [7]. These concepts mainly differ in the number and implementation of the zero states. Since multiple current paths exist for the neutral state O, the current loading – and consequently the semiconductor losses – can be deliberately redistributed among the switches. An appropriate selection of the blocking devices may additionally promote soft-switching conditions [4].
Tab. I summarizes the switching logic of three representative

gate-control strategies. Fig. 2 shows the resulting logical gate signals for these strategies using a naturally sampled three-level phase opposite disposition (POD) carrier-based PWM (3L-CBPWM) with a sinusoidal reference.

Opposite-side clamping: The switches T1/T5 and T6/T4 operate at the fundamental frequency f_{el} and commutate only once per electrical period. In contrast, T2/T3 are switched at the switching frequency f_{sw}. This strategy employs two neutral states: the lower neutral path OL1 for positive reference voltage ($v_{\mathrm{X}*} > 0$) and the upper neutral path OU1 for negative reference voltage ($v_{\mathrm{X}*} < 0$). As a result, the commutation loop extends to the opposite neutral branch and is comparatively long.

Same-side clamping: In this scheme, T2/T3 operate at f_{el}, while T1/T5 and T6/T4 switch at f_{sw}. The commutation loop follows the nearest neutral path and is therefore shorter.

Full-path clamping: All six switches operate at f_{sw} during half of the electrical period, leading to a more uniform thermal distribution among the devices. In the neutral state OUL1, the current is shared between both neutral branches.

All three gate-drive strategies generate identical external half-bridge voltage waveforms v_{X0}. However, they differ in their internal current distribution and, consequently, in the resulting semiconductor losses. For the hybrid topology (see Fig. 1), the opposite-side clamping strategy yields the lowest semiconductor losses, because the switching events are concentrated to inner MOSFETs. Since the influence of different clamping strategies on loss distribution has already been analyzed extensively in the literature [2]–[4], this work focuses on the hardware implementation of opposite-side clamping and the associated challenges.

III. Opposite-Side Clamping Commutation

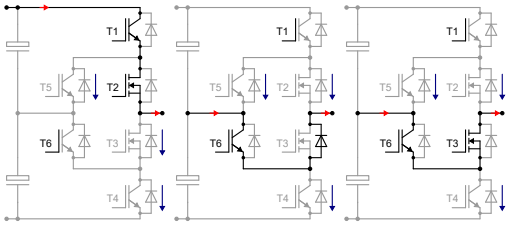
The commutation behavior of the 3L-ANPC employing opposite-side clamping is analyzed for a positive phase current $i_{\mathrm{X}} > 0$. For $i_{\mathrm{X}} < 0$, the same sequences apply analogously with mirrored switch roles. MOSFETs and IGBTs exhibit identical switching behavior when time-scale differences are neglected [5].

A. MOSFET commutation (P ↔ OL1)

During the positive half-wave ($v_{\mathrm{X}*} > 0$), the current commutates exclusively between MOSFETs T2 and T3, while the IGBTs remain inactive. A locking time $t_{\mathrm{lock,MOSFET}}$ is required to prevent a bridge short circuit. Fig. 3 illustrates the simplified current paths. The corresponding commutation steps, which are independent of the power-flow direction, are summarized in Tab. II. Devices marked with a blue voltage arrow block $V_{\mathrm{DC}}/2$, while all other devices are assumed to be voltage-free (0 V).

B. MOSFET commutation (N ↔ OU1)

For the negative half-wave ($v_{\mathrm{X}*} < 0$), the sequence represents the mirrored counterpart of the P–OL1 commutation, again respecting the locking time $t_{\mathrm{lock,MOSFET}}$.



(a) P #1 (b) #2 (c) OL1 #3

Fig. 3: MOSFET commutation P ↔ OL1 for $i_{\mathrm{X}} > 0$

TABLE II: P ↔ OL1 switching sequence

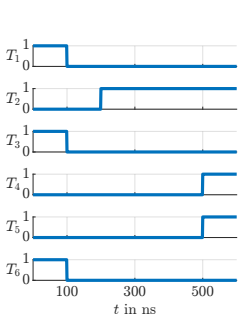
#		T_1	T_2	T_3	T_4	T_5	T_6	Transition	Locking time
1	P	1	1	0	0	0	1	turn-off T2	
2		1	0	0	0	0	1	turn-on T3	$t_{\mathrm{lock,MOSFET}}$
3	OL1	1	0	1	0	0	1	–	–

C. Zero-Crossing

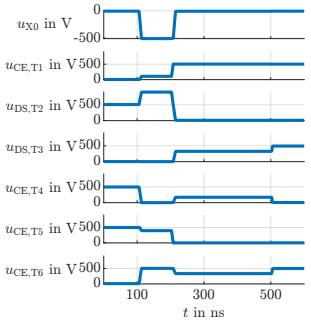
When the polarity of the reference voltage $v_{\mathrm{X}*}$ changes, all MOSFETs and IGBTs must be commutated. A locking time $t_{\mathrm{lock,IGBT}}$ must be maintained between the switch pairs T1/T5 and T6/T4, and the current must be transferred to the opposite neutral path.

The negative zero-crossing is examined in detail. A direct commutation from OL1 to OU1 would cause all three half-bridges to switch simultaneously. This hard commutation has been simulated in LTspice and is illustrated in Fig. 4. At $t = 100\,\mathrm{ns}$, all semiconductor devices are turned off. The current flows through the diodes of T3 and T4. Although T1 is turned off, it cannot block half of the DC link voltage because the parasitic nonlinear output capacitance of T1 can only be charged by a capacitive displacement current. This voltage rise is limited by the capacitive voltage divider. Consequently, T2 is forced to block nearly the full DC-link voltage. This critical overvoltage condition may destroy the module and must therefore be strictly avoided during operation.

1) Negative Zero-Crossing: To prevent this overvoltage, a defined commutation sequence is applied in which T1 must

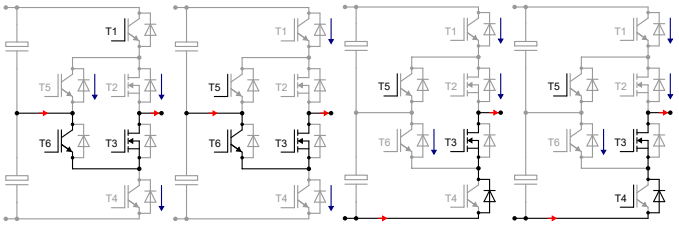


(a) Logical gate signals T_{X}



(b) Simulated half-bridge voltage v_{X0} and drain-source voltages v_{DS}

Fig. 4: LTspice simulation of a hard commutation 3L-ANPC: OL1 → OU1 for $i_{\mathrm{X}} > 0$



(a) OL1 #2 (b) #3#4 (c) #5 (d) N #6

Fig. 5: Commutation 3L-ANPC: OL1 → N for $i_{\mathrm{X}} > 0$

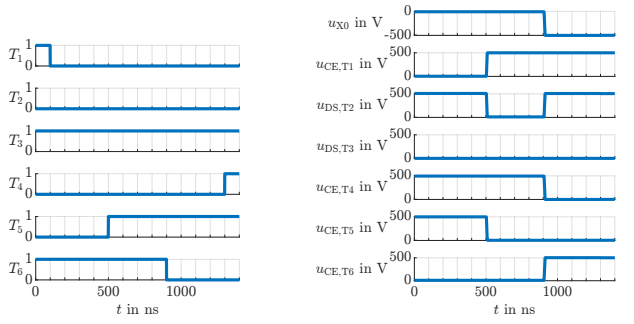
TABLE III: Commutation 3L-ANPC: OL1 / P → N / OU1

#		T_1	T_2	T_3	T_4	T_5	T_6	Transition	Locking time
1		1	0	0	0	0	1	turn-on T3	$t_{\mathrm{lock,MOSFET}}$
2	OL1	1	0	1	0	0	1	turn-off T1	$t_{\mathrm{lock,MOSFET}}$
3		0	0	1	0	0	1	turn-on T5	$t_{\mathrm{lock,IGBT}}$
4		0	0	1	0	1	1	turn-off T6	$t_{\mathrm{lock,IGBT}}$
5		0	0	1	0	1	0	turn-on T4	$t_{\mathrm{lock,IGBT}}$
6	N	0	0	1	1	1	0	turn-off T3	$t_{\mathrm{lock,IGBT}}$
7		0	0	0	1	1	0		$t_{\mathrm{lock,MOSFET}}$

take the blocking voltage. The current paths and corresponding switching steps for the transition OL1 → N are shown in Fig. 5 and Tab. III [8]. All switches are turned sequentially. Immediately after T1 is turned off, T5 is turned on to ensure that T1 can safely withstand the blocking voltage. This allows T3 and T4 to be switched without exposing T2 to an overvoltage condition. To enable a zero-crossing starting from P or OL1, the intermediate state #1 with duration $t_{\mathrm{lock,MOSFET}}$ is inserted while T2 and T3 remain off. Analogously, state #7 prepares the final step to N or OU1. According Tab. III the complete negative zero-crossing requires in this configuration $t_{\mathrm{du/dt}} = 3\,t_{\mathrm{lock,MOSFET}} + 4\,t_{\mathrm{lock,IGBT}} = 1900\,\mathrm{ns}$.

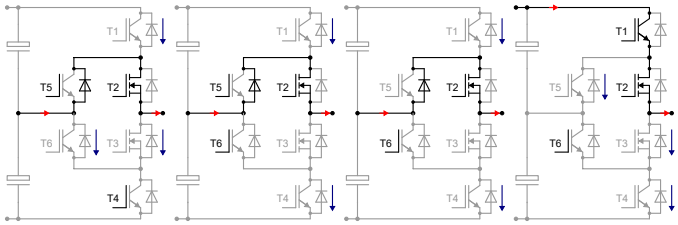
Fig. 8a shows the waveform of the logical gate signals T_{X} during the negative zero-crossing, while Fig. 6 presents the simulated voltage waveforms. No device is subjected to a critical overvoltage, and no bridge short circuit occurs.

2) Positive Zero-Crossing: The positive zero-crossing follows the symmetrical sequence shown in Fig. 7 and Tab. IV.



(a) Logical gate signals T_{X} (b) Simulated half-bridge v_{X0} and drain-source voltages v_{DS}

Fig. 6: LTspice simulation of 3L-ANPC commutation: OL1 → N for $i_{\mathrm{X}} > 0$



(a) OU1 #2 (b) #3#4 (c) #5 (d) P #6

Fig. 7: Commutation 3L-ANPC: OU1 → P for $i_{\mathrm{X}} > 0$

TABLE IV: Commutation 3L-ANPC: OU1/N → P/OL1

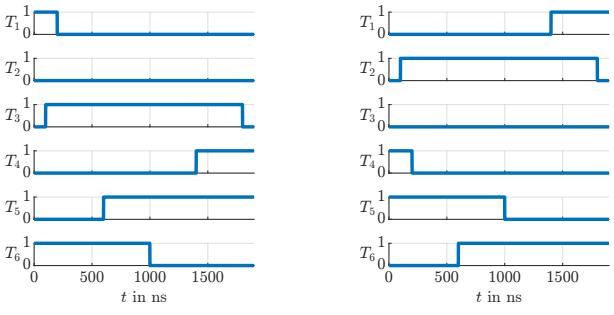
#		T_1	T_2	T_3	T_4	T_5	T_6	Transition	Locking time
1		0	0	0	1	1	0	turn-on T2	$t_{\mathrm{lock,MOSFET}}$
2	OU1	0	1	0	1	1	0	turn-off T4	$t_{\mathrm{lock,MOSFET}}$
3		0	1	0	0	1	0	turn-on T6	$t_{\mathrm{lock,IGBT}}$
4		0	1	0	0	1	1	turn-off T5	$t_{\mathrm{lock,IGBT}}$
5		0	1	0	0	0	1	turn-on T1	$t_{\mathrm{lock,IGBT}}$
6	N	1	1	0	0	0	1	turn-off T2	$t_{\mathrm{lock,IGBT}}$
7		1	0	0	0	0	1		$t_{\mathrm{lock,MOSFET}}$

The corresponding gate-signal waveforms are depicted in Fig. 8b. LTspice simulations again confirm the absence of overvoltages and short circuits.

All presented commutation sequences have been validated for both zero-crossing directions and for both load-current polarities using LTspice simulations. The turn-on and turn-off procedures described in Sec. II-A were verified accordingly.

IV. Hardware Implementation

The voltage pulse pattern which is independent from the 3L topology is generated using a carrier-based modulation scheme (3L-CBPWM). By injecting a zero-sequence voltage component into the reference signal, a space-vector-equivalent pulse pattern can be obtained [9], [10]. Since the midpoint between the two DC-link capacitors is floating, the neutral-point potential must be actively controlled. For power factors $\cos(\varphi) \approx 1$, the injected zero-sequence component can be utilized for neutral-point voltage balancing, analogous to the



(a) Negative zero-crossing (b) Positive zero-crossing

Fig. 8: Logical gate signals of the 3L-ANPC during zero-crossings

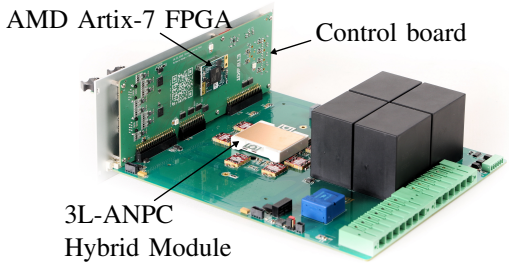


Fig. 9: Hardware setup: Infineon F3L11MR12W2M1_B74 3L-ANPC hybrid module + control board with AMD Artix-7 FPGA

TABLE V: Implementation & measurement parameters

DC link voltage	V_{DC}	800 V
Fundamental electric frequency	f_{el}	50 Hz
Carrier frequency	f_{PWM}	2.5 kHz
Modulation degree	$m = 2v_{\mathrm{X}}/V_{\mathrm{DC}}$	
Locking time MOSFET	$t_{\mathrm{lock,MOSFET}}$	100 ns
Locking time IGBT	$t_{\mathrm{lock,IGBT}}$	400 ns

selection of redundant switching states in space-vector modulation [11].

Due to real-time constraints, the modulation and gate control of a single phase are implemented on a Field-Programmable Gate Array (FPGA) operating at a clock frequency of 100 MHz. First, zero-crossing detection is performed by comparing the sign of the reference voltage $\mathrm{sign}(u_{\mathrm{X}*})$ with its previous value. A short trigger pulse initiates the corresponding switching sequence, while an SR flip-flop ensures that identical zero-crossings cannot occur consecutively. The individual switching steps are executed by means of a counter-based timing scheme. After each event, the trigger is blocked for 30 µs to prevent unintended retriggering.

The six gate signals are generated using case differentiation: if no zero-crossing is detected, only the MOSFETs are actively switched, whereas the IGBT states remain unchanged. The MOSFETs are commutated with a locking time of $t_{\mathrm{lock,MOSFET}} = 100$ ns.

Before applying the gate signals to the power stage, a pulse-release block verifies the current switching state against the predefined safe-state table. The turn-on and turn-off sequences are implemented via a delayed pulse-release path.

V. Measurement

Fig. 9 shows the experimental hardware setup. The control board generates the logical gate signals and transmits them to the gate drivers located on the power board with the 3L-ANPC hybrid module. The DC link is supplied with floating neutral point. A load inductance L connects the AC output terminal to the DC-link neutral point, forming a single-phase test configuration. The complete set of implementation and measurement parameters is summarized in Tab. V. All six drain–source voltages v_{DS} and collector–emitter voltages v_{CE} are measured using 100 MHz differential voltage probes.

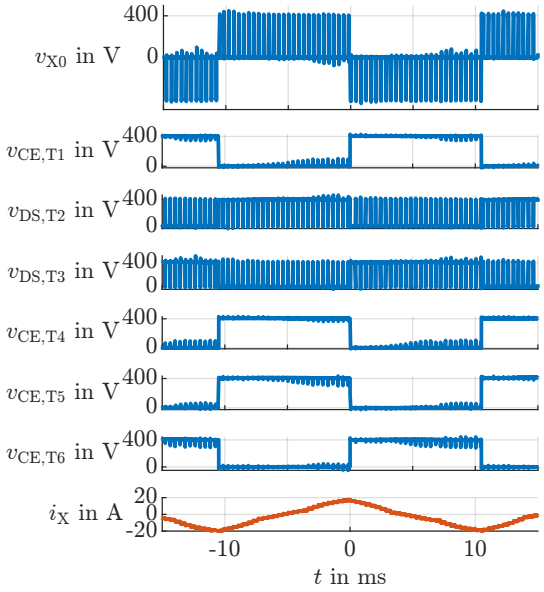


Fig. 10: Measured output voltage v_{U0}, drain-source v_{DS} / collector-emitter v_{CE} voltages and inductor current i_{X} for $m = 0.1$ and inductive load $L = 8$ mH

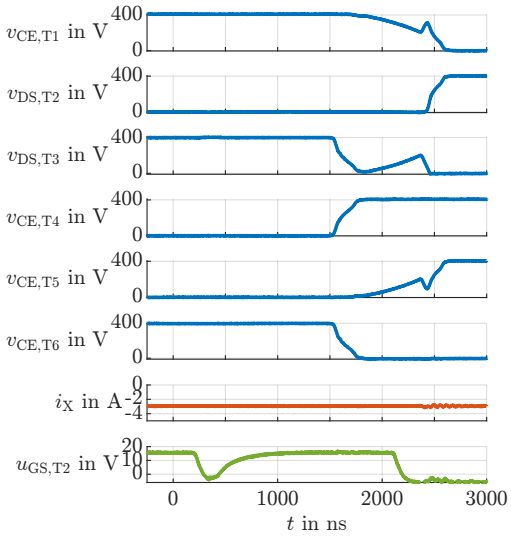


Fig. 11: Measured drain-source v_{DS} / collector-emitter v_{CE} voltages, inductor current i_{X} and gate-source voltage of T2 $u_{\mathrm{GS,T2}}$ during positive zero-crossing

Additionally, a 100 kHz current probe is used to measure the inductor current i_{X}.

Fig. 10 presents the measured drain–source and collector–emitter voltages together with the inductor current waveform.

The zero-crossing and turn-off are analyzed in detail. Fig. 11 shows the measured drain–source and collector–emitter voltages during a positive zero-crossing with $i_{\mathrm{X}} < 0$. As predicted by the simulation, no transitor experiences an

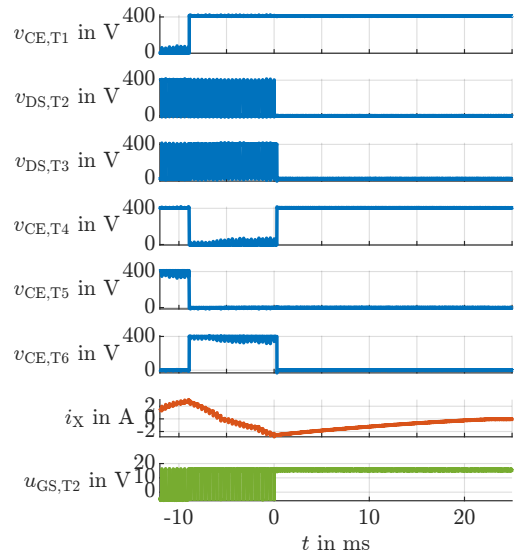


Fig. 12: Measured drain-source v_{DS} / collector-emitter v_{CE} voltages, inductor current i_X and gate-source voltage of T2 $u_{GS,T2}$ during turn-off of state OU1

overvoltage during the commutation sequence from state OU1 to P.

Fig. 12 presents the measured voltages during a turn-off of switching state OU1. The measurements were repeated for both zero-crossings and turn-off transitions, for both current directions, and for all relevant switching states. The results confirm the correct implementation of the proposed gate-control concept and validate the safe commutation sequences derived in Sec. III under realistic operating conditions.

In a final step, three single-phase converters were connected to form a three-phase system with a star-connected resistive load. Fig. 10 shows a representative three-phase measurement at approximately 6 kW output power.

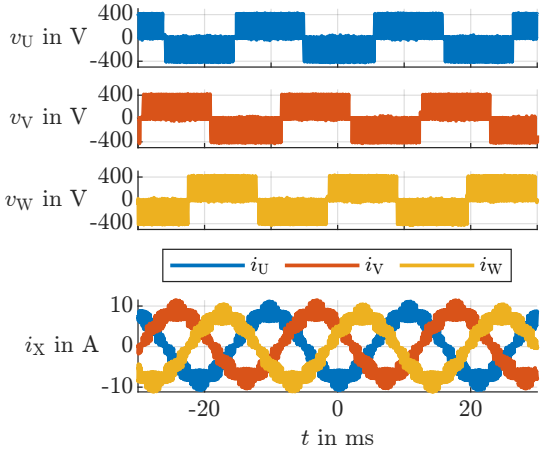


Fig. 13: Measured phase voltages v_X and phase currents i_X for $m = 1$ and a three-phase resistive load of $R = 50\,\Omega$

VI. Conclusion

This work presents a comprehensive analysis, control concept, and hardware demonstration of a hybrid 3L-ANPC phase leg employing SiC MOSFETs as inner high-frequency switches and Si IGBTs as outer devices. A systematic investigation of the switching states and commutation, together with the derivation of safe turn-on and turn-off rules including defined locking times, enables the reliable prevention of overvoltages and short-circuit conditions. Among the three investigated gate-control strategies, opposite-side clamping was selected for the hybrid topology due to its favorable loss distribution. Based on this strategy, dedicated commutation sequences for all transitions especially both zero-crossing directions were developed and verified in LTspice, demonstrating fault-free operation without critical voltage stress.

The proposed modulation and gate-drive control were implemented on an Artix-7 FPGA and validated experimentally using an Infineon hybrid 3L-ANPC module. The measurements confirm correct operation and the intended distribution of switching events and, consequently, of the switching losses. The presented approach therefore provides a practical and scalable foundation for safe and efficient real-time gate control of hybrid 3L-ANPC converters in future renewable energy applications.

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