pcim

Impact of Charge Carrier Trapping on GaN-HEMT Characteristics at Cryogenic Temperatures

Martin Fein [1], Philipp Swoboda [1], Simon Frank [1], Rüdiger Schwendemann [1], Marc Hiller [1]

[1] Karlsruhe Institute of Technology - Elektrotechnisches Institut, Germany

Corresponding author: Martin Fein, martin.fein@kit.edu
Speaker: Martin Fein, martin.fein@kit.edu

Abstract

This paper presents an investigation of the static and dynamic on-resistance $R_{\mathrm{DS,on}}$ using a fully automated, modular measurement setup, which enables the characterization of commercially available Gallium-Nitride-high-electron mobility transistors at cryogenic temperatures ($77\,\mathrm{K}$). The circuit is based on an extended modified double pulse test, enabling the characterization in an application-oriented setup over a wide temperature range while minimizing self-heating effects. The focus is on the investigation of charge-carrier trapping in terms of dynamic on-resistance $dR_{\mathrm{DS,on}}$ at cryogenic temperature. The presented setup enables systematic investigation of these effects, with distinguishable trapping sources. Measurements of the static on-resistance $R_{\mathrm{DS,on}}$ show a significant decrease due to the increased electron mobility at cryogenic temperatures. Results of dynamic on-resistance $dR_{\mathrm{DS,on}}$ analysis show a much reduced degradation of $dR_{\mathrm{DS,on}}$ compared to measurements at room temperature under soft-switching and hard-switching, as well as a negligible effect after the application of a drain-voltage-bias.

1 Introduction

High-electron mobility transistors (HEMTs) based on Gallium-Nitride (GaN) offer numerous advantages over conventional transistors. In contrast to Silicon (Si) or Silicon-Carbide (SiC) transistors, the conductive channel in GaN-HEMTs originates from the two-dimensional electron gas (2DEG) rather than from doping. Due to the absence of the carrier freeze-out effect in the 2DEG, GaN-HEMTs are more attractive than Si-/SiC-transistors for applications operated at cryogenic temperature (CT) [1]. Furthermore, as the temperature decreases, the electron mobility increases due to the reduced electron-phonon interaction, leading to a significant reduction in the static on-resistance $R_{\mathrm{DS,on}}$ of the GaN-HEMT [2]. Therefore, GaN-HEMTs emerge as a promising technology for cryogenic applications such as deep space components, electric aviation and quantum computing [3–5].

However, due to impurities within the GaN-HEMT structure, trapping effects still degrade the device's performance. These effects are mainly initiated by drain-voltage bias during the off-state of the transistor, by gate-voltage bias, as well as by hot-electrons during hard-switching (HS) events. The resulting trapping effects depend on the magnitude and duration of the applied voltage. They manifest as a threshold-voltage shift $V_{\mathrm{GS,th}}$, a dynamic increase of the on-resistance $dR_{\mathrm{DS,on}}$, or current collapse, and thus significantly influence the characteristics of the GaN-HEMT [6, 7]. Even if these effects are reversible, the relaxation time depends on the temperature and the previously applied bias voltage [8].

Whereas these effects are extensively studied at room temperature (RT), only specific aspects, such as the threshold-voltage instability $V_{\mathrm{GS,th}}$ caused by trapping, have been investigated at CT [9, 10]. At CT, the thermally activated emission of trapped carriers is strongly suppressed following the Arrhenius equation, leading to a freeze-out of trap occupancy and thus a stabilization of the threshold-voltage-shift $V_{\mathrm{GS,th}}$ compared to RT. However, non-thermal mechanisms, such as gate-bias-induced tunneling or hot-electron excitation, can still enable the de-trapping of these frozen carriers [11–13].

Besides the threshold voltage shift $V_{\mathrm{GS,th}}$, trapping also affects the on-resistance $R_{\mathrm{DS,on}}$ of the GaN-HEMT. While many publications, such as [14], investigate GaN-HEMTs under CT on device-level using a curve tracer and showing a general decrease in static on-resistance $R_{\mathrm{DS,on}}$ and increase in the transconductance g_{m} at CT, measurement setups for extracting trapping effects using pulsed I-V measurements are presented in [15, 16]. During pulsed I-V measurements, the device under test (DUT) is pre-stressed with a high-voltage (HV) and measured under low-voltage (LV) using a resistive load. A concept to explore the dynamic effects for a commercially available $650\,\mathrm{V}$ HEMT at CT is described in [16]. However, measurements at CT have not been presented yet. In [15], a non-commercial GaN-HEMT is investigated. It shows a largely suppressed dynamic increase of the on-resistance $dR_{\mathrm{DS,on}}$ at $150\,\mathrm{K}$ even after $25\,\mathrm{s}$ of stress. This was attributed to a very inefficient electron capture process, which holds a long capture time constant. However, in many power electronic applications, the HEMT is switched under an inductive load and higher voltages.

A more application-oriented test setup is the double pulse test (DPT), with the possibility to extract switching losses [17]. Due to the HS condition of the DPT causing hot-electrons, the dynamic on-resistance $dR_{\mathrm{DS,on}}$ is investigated under realistic switching conditions. It is found not to occur at CT [18]. However, the DPT lacks the ability to precisely control the pre-stress of the DUT and to distinguish between traps originating from the applied bias during the freewheeling phase or the HS event during turn-on or turn-off events. Therefore, in [19] a test setup was developed capable of soft-switching (SS) and HS and of applying a drain-bias $V_{\mathrm{DS,idle}}$. However, this setup does not guarantee an unbiased DUT for the extraction of the static on-resistance $R_{\mathrm{DS,on}}$ and a de-trapping state without gate-bias. Measurements under HS, similar to the DPT, do not agree with those from [18].

To overcome these issues, we developed a test setup in [20]. The adaptation of this test setup for CT and the test setup itself are explained in section 2. In section 3, the corresponding measurement procedure is presented. Finally, the measurement results are shown in section 4, including the verification of operation at CT, the static on-resistance $R_{\mathrm{DS,on}}$ from RT to CT, and the dynamic on-resistance $dR_{\mathrm{DS,on}}$ at CT compared to measurements at RT. The results demonstrate a decrease in the static on-resistance $R_{\mathrm{DS,on}}$ and reveal the influence of drain-bias and SS/HS operation on the dynamic on-resistance $dR_{\mathrm{DS,on}}$.

2 Cryogenic Test Bench for GaN-HEMT Characterization

To characterize GaN-HEMT at CT, the electrical measurement circuit is embedded into a mechanical setup. The mechanical setup must ensure safe operation conditions at CT by preventing condensation/icing but also limiting the heat input. The electrical measurement setup must ensure full functionality under the extreme conditions that prevail during CT.

2.1 Mechanical Design of the Test Setup

In Fig. 1, the test system for transistor characterization at CT is shown. It includes a $400\,\mathrm{mm}$ deep double-walled vacuum chamber with a diameter of $200\,\mathrm{mm}$. The entire test circuit, including the control mainboard, the DUT and the cryogenic cooling circuit, is located inside this chamber. For cooling, LN_2 $(77\,\mathrm{K})$ is filled from a cryogenic storage dewar via an electrically controlled magnet valve into the cryogenic cooling circuit, which is described in more detail later. The chamber is evacuated through a *DN40 ISO-KF* feedthrough in the $8\,\mathrm{mm}$ structural plate using a *HighCube classic* turbo-pump (*Pfeiffer Vacuum*) with dual pressure monitoring. A butterfly valve protects the pump during operation, while a spindle valve enables controlled ventilation. Pressure is monitored using a *PENNINGVAC PTR 90 RN* (*Leybold*), covering $1\,\mathrm{bar}$ to $1 \times 10^{-9}\,\mathrm{mbar}$, with digital readout and integration into the LN_2 control system.

The vacuum serves two main purposes: reducing thermal conductivity and ensuring electrical isolation. As particle density decreases, thermal conductivity drops, and at pressures below $1 \times 10^{-5}\,\mathrm{mbar}$ convective heat transfer becomes negligible [21]. During cool-down, the pressure further decreases due to cryopumping as gases condense on cold surfaces. To prevent icing and ensure insulation, residual humidity is removed by flushing the chamber with compressed air or N_2 before evacuation.

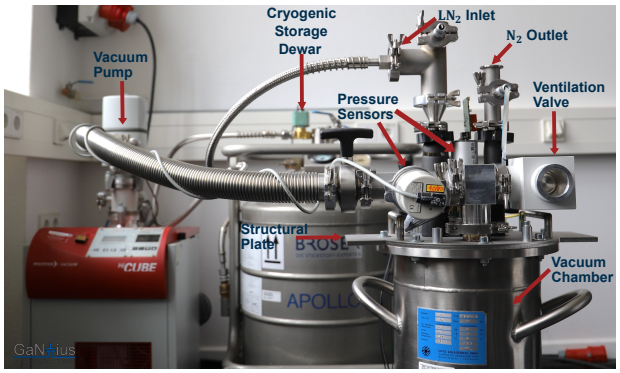


Fig. 1: Test bench including LN_2 tank and vacuum pumping unit

Although the open cooling circuit is located inside the vacuum chamber, it operates at ambient pressure and must thus be vacuum-tight. LN_2, with a density of $808.5\,\mathrm{g\,L^{-1}}$ [22], is therefore supplied through a vacuum-jacketed $12\,\mathrm{mm}$ inlet into a $1\,\mathrm{L}$ reservoir (see Fig. 2), providing stable cooling despite evaporation losses. The outlet uses a $19\,\mathrm{mm}$ vacuum-insulated pipe to handle the increased volume flow during phase change to GN_2 ($1.25\,\mathrm{g\,L^{-1}}$), at the cost of higher heat leakage [21]. A second reservoir acts as a low-pass filter, damping flow fluctuations with the hydraulic resistance – capacitance behavior. The system is connected to the heatsink via a pipe and bellow with a siphon structure that guides vapor flow, which enables loss estimation by measuring the GN_2 mass-flow rate and computing the resulting evaporation rate from it [23]. The thermal contact resistance to the LN_2 inside the heatsink is reduced by increasing the contact area by a factor of 3.6 using eleven cooling fins.

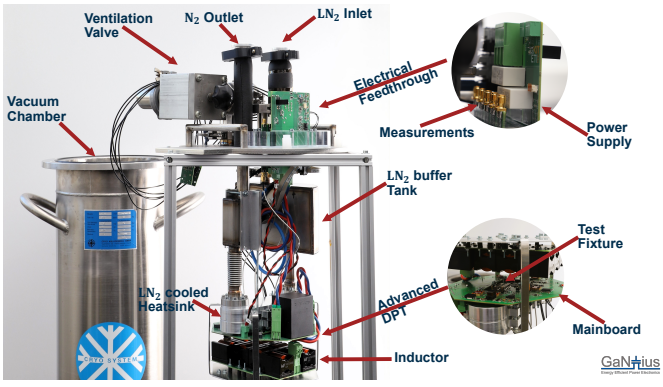
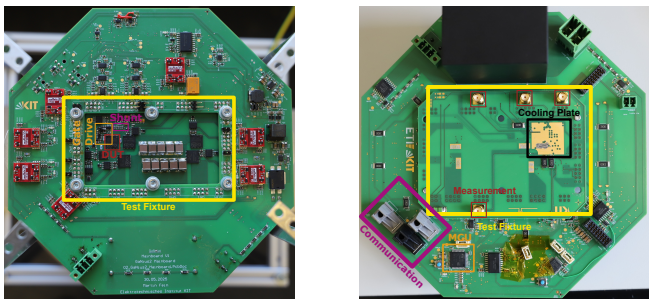


Fig. 2: Test bench for transistor characterization at CT

The entire pipe setup is made of *stainless steel 304L*, which is well suited for CT operation due to its low thermal conductivity and good weldability. The system is welded to the structural plate to ensure uniform thermal contraction. In contrast, the heatsink is made of *aluminum 2007* for its higher thermal conductivity and is mounted to the inlet and outlet flanges. As these components are in contact with cold regions, indium sealings are used due to their high deformability [22]. Non-cryogenic vacuum components are connected with rubber sealings.

2.2 Electrical Design of the Test Setup

The electrical test setup is based on the modified DPT presented in [8]. It is distributed across multiple boards: a mainboard containing the MCU and power supply, an inductor board, and the cryogenically cooled test fixture. The test fixture is cooled via the cooling plate shown in Fig. 3b. Together with the spring-loaded mainboard, they are mounted to the cooling plate of the heatsink. This separation thermally isolates the GaN-HEMTs, which are verified to operate at CT, from auxiliary components requiring special consideration at low temperatures [24]. In addition, the modular structure allows easy exchange of the test fixture and adaptation to different DUTs. The DUT in this paper, is the $50\,\mathrm{m\Omega}$ GaN-HEMT *GS-065-030-2L* from *Infineon* featuring a Schottky gate [25].



(a) (b)

Fig. 3: Mainboard and cryogenic test fixture of the modular GaN-HEMT test system

The cryogenically cooled test fixture contains the improved DPT circuit, which is depicted in Fig. 4a. The auxiliary switches HS1, HS2 and LS1, LS2 are similar to the DUT. As their gate drivers, the isolated *SI8271AB-IS* ICs from *Skyworks* are used. These CMOS-based drivers have been demonstrated to operate reliably down to $77\,\mathrm{K}$ [26, 27].

Since isolation of the DUTs drivers is not required, two non-isolated *1EDN8511BXUSA1* drivers from *Infineon* are used to form the adaptive gate driver presented in [20]. To ensure a high measurement accuracy of the on-state voltage $V_{\mathrm{DS,on}}$, the clamp circuit based on [8] is realized with a bidirectional GaN-HEMT *EPC2121* from *Efficient Power Conversion* and *GS-065-004-6-L-MR* from *Infineon* [8].

The primary DC-link consists of ten $200\,\mathrm{nF}$ NP0 ceramic capacitors, reducing overall ESR and ESL. Due to their temperature stability, NP0 capacitors are used throughout the test fixture. Furthermore, temperature-stable thin-film resistors are implemented [24]. The DUT is thermally connected via 55 vias to the cooling plate on the bottom side of the PCB and mounted to the heatsink using a TIM foil [28, 29].

While keeping the gate loops and commutation cells as small as possible, the secondary $140\,\mathrm{\mu F}$ film capacitor is located on the mainboard. The isolated power supply for the gate-drivers is realized with the dual-rail *Murata MGN1D050603MC*. Due to their limited efficiency at light loads and the resulting heating, they are combined with additional heating resistors to form a thermal barrier for the MCU and signal processing. The DUT is supplied with variable gate voltage utilizing a combination of low-dropout regulator (LDO) and charge pump controlled by the microcontroller unit (MCU) *STM32G491RE* from *STMicroelectronics*. Temperature monitoring is implemented at all critical components with the *PT1000* temperature sensors from *Innovative Sensor Technology* and the sigma-delta analog-to-digital converter (ADC) *ADS1115* from *Texas-Instruments*.

The power and signal supplies from ambient into the vacuum chamber are implemented using a feedthrough PCB encapsulated in resin within a Polycarbonat (PC) window mounted on the chamber's structural plate. To monitor the level of the coolant within the test system, PCBs incorporating *PT1000* temperature sensors are placed vertically in the reservoirs and heatsink. All PCBs are connected via a CAN bus, enabling the temperature data to control the magnet valve of the LN_2 tank and maintain a constant coolant level. A separate feedthrough PCB transfers measurement signals from the vacuum to the ambient. However, to minimize the number of conductors fed in and out of the chamber, the inductor $L_{\mathrm{DPT}} = 90\,\mathrm{\mu H}$ is placed beneath the mainboard, thermally isolated on a separate PCB.

3 Measurement Procedure

In comparison to a conventional DPT, the modified DPT (Fig. 4a) includes three additional transistors HS2, LS2, LS1. The transistor LS1 is connected in parallel to the DUT [8].

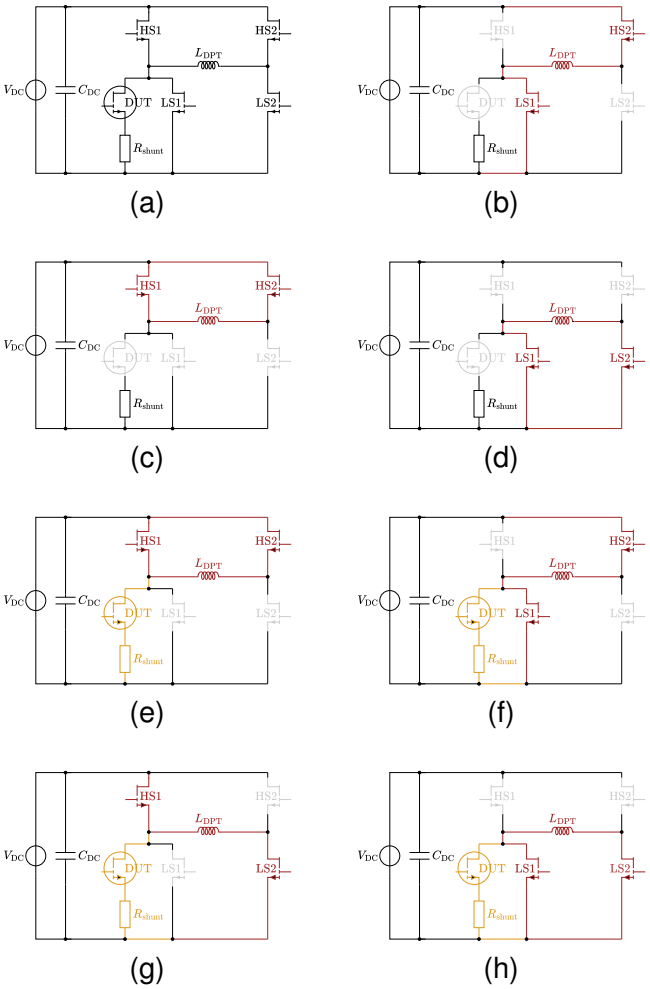


Fig. 4: Measurement procedure of the modified DPT (inactive HEMTs are greyed out)

For positive currents I_{D}, the inductor L_{DPT} is charged during t_{charge} as shown in Fig. 4b, where LS1 conducts the current, indicated by the red path, to minimize self-heating of the DUT. This is followed by the freewheeling time t_{fw}, where either the lower path (Fig. 4d) ensures a bias-free condition or the upper path (Fig. 4c) applies V_{DC} to the DUT.

Depending on the selected path, commutation, indicated by the orange path, to the DUT occurs under SS or HS conditions (Figs. 4e to 4h). In SS, LS1 conducts before current commutation, whereas in HS the current transfers from HS1 to the DUT. After the DUT has reached on-state, the clamp circuit is activated and the measurement of $R_{\mathrm{DS,on}}$ starts. After the measurement interval, the system returns to the selected freewheeling state [8, 20]. Throughout the pulse interval, the test fixture is disconnected from the supply to prevent ground loops during data acquisition.

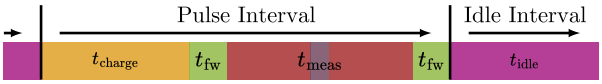


Fig. 5: Timing of measurement procedure

The measurement is followed by the idle interval t_{idle} (Fig. 5), during which the DUT can either be biased with V_{DC} using the upper freewheeling path (Fig. 4c) or remain unbiased using the lower path (Fig. 4d). In addition to SS and HS, zero-voltage-switching (ZVS) operation with negative device current I_{D} is achieved by charging the inductor L_{DPT} negatively via HS1 and LS2. The measurement duration and thus the on-time of the DUT is fixed to $t_{\mathrm{meas}} = 5\,\mu\mathrm{s}$.

Measurements are acquired using the *Teledyne LeCroy WaveSurfer 4104HD* oscilloscope. The current I_{D} is measured with five parallel temperature-stable shunt resistors, each with $R_{\mathrm{Shunt}} = 200\,\mathrm{m\Omega}$. Since the setup is disconnected during measurement, preventing common-mode currents, I_{D} is sensed via a BNC connection. The on-state voltage $V_{\mathrm{DS,on}}$ of the DUT, as well as gate voltage V_{GS} and unclamped output voltage V_{DS}, are measured using optically isolated *PMK FireFly FF1500A* probes with $\pm 10\,\mathrm{V}/\pm 25\,\mathrm{V}/\pm 250\,\mathrm{V}$ tips. The probes are calibrated before each measurement to compensate for any temperature drift.

4 Measurement Results

This section presents the experimental results, starting with the validation of the modified DPT under cryogenic conditions. It then analyzes the static and dynamic on-resistance $R_{\mathrm{DS,on}}$ at RT and CT. The results highlight pronounced differences in trap dynamics between the investigated temperature regimes.

4.1 Validation of the modified DPT at CT

To verify the functionality of the setup, HS transients at RT $(296\,\mathrm{K})$ and CT $(85\,\mathrm{K})$ are compared in Fig. 6. The transients at CT are plotted in dashed and compared to the solid at RT. The green section marks the freewheeling time (upper path) within the pulse interval, while the red section indicates the DUTs on-time t_{meas}, starting with turn-on of the DUT followed by activation of the clamp circuit, enabling a measurement range limited to $1\,\mathrm{V}$. The on-resistance $R_{\mathrm{DS,on}}$ is extracted by averaging the measured current I_{D} and voltage $V_{\mathrm{DS,on}}$ over an interval of $500\,\mathrm{ns}$ in the middle of the t_{meas} time (highlighted in blue in Fig. 6).

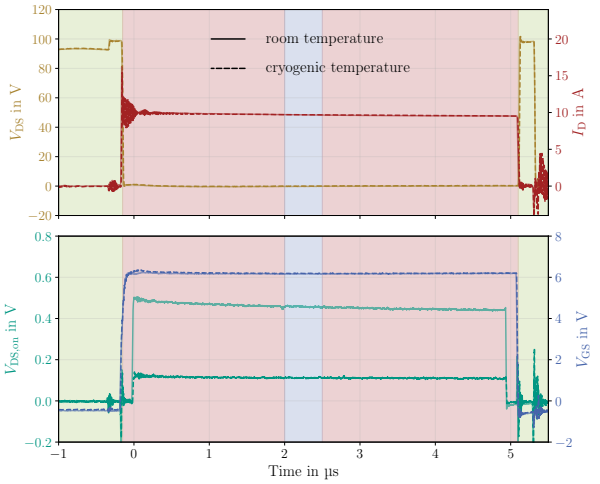


Fig. 6: Switching transients at RT and CT

A significant difference in $R_{\mathrm{DS,on}}$ is observed and will be discussed in detail in section 4.2. Furthermore, Fig. 6 demonstrates that gate control and current I_{D} remain unaffected by temperature, the latter due to the thermally decoupled mainboard and inductor. Here, the DUT is supplied with $V_{\mathrm{GS}} = -0.5\,\mathrm{V}/6\,\mathrm{V}$ at a load current of $I_{\mathrm{D}} = 10\,\mathrm{A}$. This ensures consistent measurement conditions for the DUT over the entire temperature range from RT to CT.

However, the measured temperature of the DUT differs from the junction temperature T_{j}, as the *PT1000* sensor is placed next to the DUT on the PCB. Due to the low thermal conductivity of *FR4* $(0.2 - 0.5\,\mathrm{W/mK})$, the temperature deviation is estimated to be approximately $10\,\mathrm{K}$ according to the $R_{\mathrm{DS,on}}$ as a temperature-sensitive electrical parameter (TSEP) and will be addressed in future work.

4.2 Static On-Resistance from RT to CT

To measure the static on-resistance $R_{\mathrm{DS,on}}$, the lower freewheeling path with SS is used (Figs. 4b, 4d and 4h), ensuring an unbiased DUT without hot-electron effects. This corresponds to a datasheet-like measurement (*IEC 60747-8:2010*) of $R_{\mathrm{DS,on}}$ [25]. Measurements are taken every $t_{\mathrm{idle}} = 7\,\mathrm{s}$ during a $2\,\mathrm{h}$ cool-down from RT to CT. To reduce noise on the measurement signals, a low-pass filter with $20\,\mathrm{MHz}$ is used.

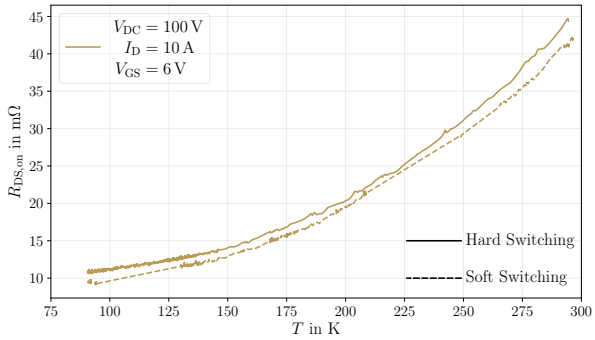


Fig. 7: Static on-resistance $R_{\mathrm{DS,on}}$ from RT to CT

Due to reduced electron–phonon interaction at low temperatures, carrier mobility increases, resulting in a decrease of $R_{\mathrm{DS,on}}$ by a factor of approximately 4.5, from $42\,\mathrm{m\Omega}$ to $9.6\,\mathrm{m\Omega}$, as shown in Fig. 7. Self-heating is minimized by the applied pulse pattern due to LS1. Repeating the measurement under HS conditions (similar to a conventional DPT measurement) shows an additional increase of about $2\,\mathrm{m\Omega}$, attributed to either elevated junction temperature T_{j} or trap effects caused by hot-electrons.

4.3 Dynamic On-Resistance at RT and CT

The dynamic on-resistance $dR_{\mathrm{DS,on}}$ originates from either off-state drain-bias or hot-electron effects [20]. HS (Figs. 4e and 4g) generates hot-electrons, whereas SS (Figs. 4f and 4h) enables zero-voltage commutation. By varying the voltage across the DUT during the idle state t_{idle}, the influence of pure drain-bias can be separated, allowing the additional effect of hot-electrons to be extracted by comparison.

Figure 8 shows $dR_{\mathrm{DS,on}}$ for varying $V_{\mathrm{DS,idle}}$ under SS and HS at $V_{\mathrm{GS}} = 6\,\mathrm{V}$ and $I_{\mathrm{D}} = 10\,\mathrm{A}$. In phase I ($t_{\mathrm{I}} = 3\,\mathrm{min}$), the DUT remains unbiased ($V_{\mathrm{DS,idle}} = 0$). In phase II ($t_{\mathrm{II}} = 15\,\mathrm{min}$), a drain-bias $V_{\mathrm{DS,idle}} = V_{\mathrm{DC}}$ is applied. In phase III ($t_{\mathrm{III}} = 15\,\mathrm{min}$), the unbiased condition is restored.

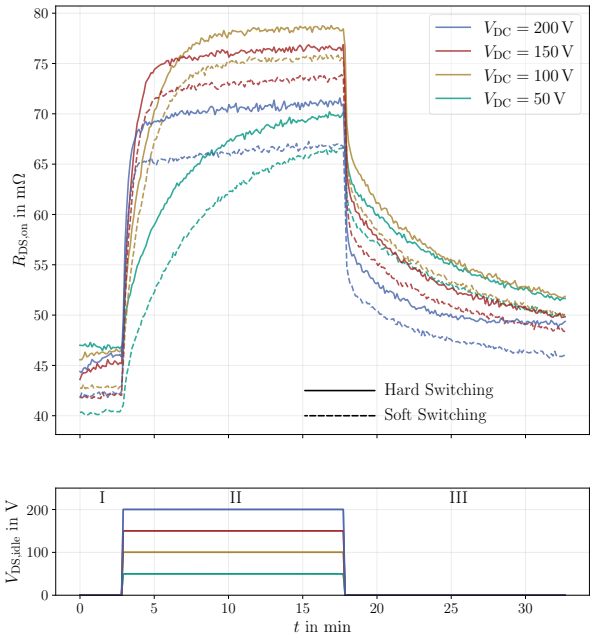


Fig. 8: Dynamic $dR_{\mathrm{DS,on}}$ for different $V_{\mathrm{DS,idle}}$ at RT

The influence of $V_{\mathrm{DS,idle}}$ is clearly visible in both SS and HS measurements. The dynamic increase of $R_{\mathrm{DS,on}}$ peaks at $100\,\mathrm{V}$ and decreases at higher and lower voltages. HS introduces an additional offset due to hot-electron effects, as seen in phase I. In phase II, the trapping time constant τ_{trap} decreases with increasing $V_{\mathrm{DS,idle}}$, while no significant dependence of the de-trapping time constant $\tau_{\mathrm{de-trap}}$ is observed in phase III. Thus, this setup enables a clear separation of drain-bias and hot-electron effects, as demonstrated experimentally. The influence of the short bias of $t_{\mathrm{fw}} = 1\,\mu\mathrm{s}$ during commutation under HS will be addressed in the future, but is expected to be insignificant.

This procedure is repeated at CT of $100\,\mathrm{K}$ (Fig. 9). In addition to the reduced static $R_{\mathrm{DS,on}}$, the dynamic variation is limited to within $\pm 1\,\mathrm{m\Omega}$. The peak at $100\,\mathrm{V}$ disappears, indicating reduced sensitivity to $V_{\mathrm{DS,idle}}$ at CT. These results agree with DPT-measurements in [18] and show a significantly reduced impact of HS compared to higher temperatures [15]. At SS, a minimal increase can be observed during phase II, when $V_{\mathrm{DS,idle}}$ is applied.

The suppression of dynamic effects is attributed to trap freeze-out at CT [9]. Thermally activated emission of trapped charge carriers is strongly reduced, limiting trapping and de-trapping dynamics and resulting in a nearly constant $R_{\mathrm{DS,on}}$.

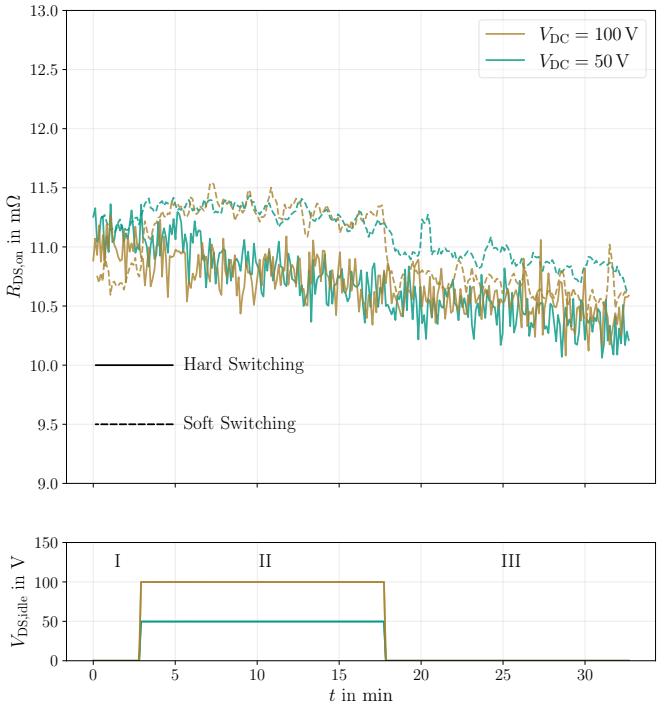


Fig. 9: Dynamic $dR_{\mathrm{DS,on}}$ for different $V_{\mathrm{DS,idle}}$ at CT

The slight decrease in $R_{\mathrm{DS,on}}$ observed at CT can be attributed to residual temperature variations during the measurement. Due to the absence of active temperature control, the DUT temperature is not fully stabilized, leading to a gradual cooling and consequently a minor reduction in $R_{\mathrm{DS,on}}$. Future work will include implementing a temperature controller to stabilize the DUTs temperature and extending stress durations to investigate long-term trapping effects at CT.

5 Conclusion

This paper presents static and dynamic on-resistance $R_{\mathrm{DS,on}}$ measurements of a commercially available Gallium-Nitride (GaN)-high-electron mobility transistor (HEMT) at cryogenic temperature (CT) ($77\,\mathrm{K}$), performed using an automated, modular test setup. Measurements at RT confirm the correct functionality of the setup and show good agreement with the literature.

The influence of different trapping mechanisms is investigated separately. At RT, off-state drain-bias $V_{\mathrm{DS,idle}}$ significantly increases the dynamic on-resistance $dR_{\mathrm{DS,on}}$, while additional hot-electron effects from HS further enhance this degradation. In contrast, at CT, these effects are largely suppressed due to trap freeze-out. In addition to the pronounced reduction of the static on-resistance $R_{\mathrm{DS,on}}$, no significant dynamic variation of $dR_{\mathrm{DS,on}}$ is observed at CT, neither from drain-bias nor from hot-electron stress.

With the presented modular and automated setup, comprehensive characterization of GaN-HEMTs, including transfer and output characteristics using the modified DPT, as well as the investigation of threshold-voltage shifts over a wide temperature range, is enabled for future work. Its flexibility allows easy exchange of DUTs, facilitating comparative studies across different GaN-HEMT technologies. In addition, long-term automated measurements open the path for precise extraction of trapping and de-trapping time constants over extended time scales and temperatures.

6 Acknowledgments

This work was funded by the *German Research Foundation (DFG)* within the priority program *SPP 2312: Energy Efficient Power Electronic "GaNius"*. The name of the partial project is "Characterization and Application of GaN-HEMTs at Cryogenic Temperatures" with the project number *546257378*.

References

[1] Ruirui Chen and Fei Fred Wang. "SiC and GaN Devices with Cryogenic Cooling". In: *IEEE Open Journal of Power Electronics* 2 (2021), pp. 315–326. DOI: 10.1109/OJPEL.2021.3075061.

[2] Ren Ren, Handong Gui, Zheyu Zhang, Ruirui Chen, Jiahao Niu, et al. "Characterization and Failure Analysis of 650-V Enhancement-Mode GaN HEMT for Cryogenically Cooled Power Electronics". In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* 8.1 (2020), pp. 66–76. DOI: 10.1109/JESTPE.2019.2949953.

[3] Fei Fred Wang, Ruirui Chen, and Zhou Dong. "Power Electronics: A Critical Enabler of Future Hydrogen–Electric Systems for Aviation". In: *IEEE Electrification Magazine* 10.2 (2022), pp. 57–68. DOI: 10.1109/MELE.2022.3165954.

[4] Hendrik Schefer, Wolf-Rüdiger Canders, Jan Hoffmann, Regine Mallwitz, and Markus Henke. "Cryogenically-Cooled Power Electronics for Long-Distance Aircraft". In: *IEEE Access* 10 (2022), pp. 133279–133308. DOI: 10.1109/ACCESS.2022.3228161.

[5] Lieven Vandersypen and Antoni van Leeuwenhoek. “1.4 Quantum Computing - The Next Challenge in Circuit and System Design”. In: *2017 IEEE International Solid-State Circuits Conference (ISSCC)*. 2017, pp. 24–29. DOI: 10.1109/ISSCC.2017.7870244.

[6] Benedikt Kohlhepp, Daniel Breidenstein, and Thomas Dürbaum. “Test Setup to Study Threshold Voltage Shift of GaN-HEMTs under Short- and Long-Term Gate and Drain Bias”. In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* (2024), pp. 1–1. DOI: 10.1109/JESTPE.2024.3464613.

[7] Maximilian Goller, Christian Schwabe, Nick Thoenelt, Gengqi Li, Josef Lutz, and Thomas Basler. “Precise Determination of Dynamic RDSon in AlGaN/GaN Power HEMTs under Soft Switching Condition”. In: *PCIM Europe 2022; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*. 2022, pp. 1–8. DOI: 10.30420/565822138.

[8] Philipp Swoboda, Simon Robin Frank, Andreas Liske, and Marc Hiller. “Improved Test Circuit for Characterization of the Dynamic On-Resistance of GaN-HEMTs over a Wide Operating Range”. In: *Energy Conversion Congress & Expo Europe (ECCE Europe)*. 2024, pp. 1–8. DOI: 10.1109/ECCEEurope62508.2024.10751914.

[9] Zuoheng Jiang, Xinyu Wang, Junlei Zhao, Junting Chen, Jinjin Tang, et al. “Roles of Hole Trap on Gate Leakage of p-GaN HEMTs at Cryogenic Temperatures”. In: *IEEE Electron Device Letters* 44.10 (2023), pp. 1612–1615. DOI: 10.1109/LED.2023.3311395.

[10] Mohammad Sajid Nazir, Pragya Kushwaha, Ahtisham Pampori, Sheikh Aamir Ahsan, and Yogesh Singh Chauhan. “Electrical Characterization and Modeling of GaN HEMTs at Cryogenic Temperatures”. In: *IEEE Transactions on Electron Devices* 69.11 (2022), pp. 6016–6022. DOI: 10.1109/TED.2022.3204523.

[11] Chuan Song, Wen Yang, Weijian Wang, Jianlang Liao, Peng Wu, et al. “Trap Thawing-Induced Threshold Voltage Instability in p-GaN HEMTs at Cryogenic Temperatures During Pre-Stress”. In: *IEEE Electron Device Letters* 46.8 (2025), pp. 1289–1292. DOI: 10.1109/LED.2025.3577493.

[12] Xinyu Wang, Zuoheng Jiang, Junting Chen, Junlei Zhao, Han Wang, et al. “Threshold Voltage Instability of Schottky-type p-GaN Gate HEMT down to Cryogenic Temperatures”. In: *2023 35th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*. 2023, pp. 115–118. DOI: 10.1109/ISPSD57135.2023.10147433.

[13] Chuan Song, Wen Yang, Weijian Wang, Huaxing Jiang, Sheng Jiang, et al. “Bidirectional Threshold Voltage Shift After Positive Bias Temperature Instability of p-GaN HEMTs at Cryogenic Temperature”. In: *2025 IEEE International Reliability Physics Symposium (IRPS)*. 2025, pp. 1–5. DOI: 10.1109/IRPS48204.2025.10983869.

[14] Luca Nela, Nirmana Perera, Catherine Erine, and Elison Matioli. “Performance of GaN Power Devices for Cryogenic Applications Down to 4.2 K”. In: *IEEE Transactions on Power Electronics* 36.7 (2021), pp. 7412–7416. DOI: 10.1109/TPEL.2020.3047466.

[15] Yangqian Wang, Yitian Gu, Xing Lu, Huaxing Jiang, Haowen Guo, et al. “Comparative Study on Dynamic Characteristics of GaN HEMT at 300 K and 150 K”. In: *IEEE Journal of the Electron Devices Society* 8 (2020), pp. 850–856. DOI: 10.1109/JEDS.2020.3013656.

[16] Charley Shi, Suzanne Lo, Duleepa J. Thrimawithana, Francesca Adams, Aaron Wadsworth, et al. “A Circuit for Evaluating GaN HEMT Dynamic Rds(on) at Cryogenic Temperatures”. In: *2024 IEEE 9th Southern Power Electronics Conference (SPEC)*. 2024, pp. 1–6. DOI: 10.1109/SPEC62217.2024.10893110.

[17] Mahmoud Mehrabankhomartash, Shiyuan Yin, Alfonso J Cruz, Lukas Graber, Maryam Saeedifard, et al. “Static and Dynamic Characterization of 650 V GaN E-HEMTs in Room and Cryogenic Environments”. In: *2021 IEEE Energy Conversion Congress and Exposition (ECCE)*. 2021, pp. 5289–5296. DOI: 10.1109/ECCE47101.2021.9595593.

[18] Xin Yang, Zineng Yang, Matthew Porter, Linbo Shao, and Yuhao Zhang. “First Characterization of Si IGBT, SiC MOSFET, and GaN HEMT at Deep Cryogenic Temperatures Down to 10 Millikelvins”. In: *IEEE Transactions on Power Electronics* 41.2 (2026), pp. 1704–1717. DOI: 10.1109/TPEL.2025.3601008.

[19] Tian Qiu, Zheyu Zhang, Purushottam Khadka, Ahmed Siraj, and Dilip Rana. “Automated Characterization Platform for Comprehensive Dynamic Rdson Assessment of GaN HEMTs from 50 K to 400 K”. In: *2025 IEEE Applied Power Electronics Conference and Exposition (APEC)*. 2025, pp. 1040–1046. DOI: 10.1109/APEC48143.2025.10977105.

[20] Philipp Swoboda, Martin Fein, Simon Frank, Andreas Liske, and Marc Hiller. “Application-Oriented Test Setup for Measuring Dynamic Output and Transfer Characteristics of GaN-HEMTs”. In: *IEEE Applied Power Electronics Conference and Exposition (APEC)*. 2025, pp. 2348–2355. DOI: 10.1109/APEC48143.2025.10977237.

[21] Thomas M. Flynn. *Cryogenic Engineering, Second Edition, Revised and Expanded*. CRC Press, 2004.

[22] Hermann Sicius. *Handbook of the Chemical Elements*. Springer Berlin Heidelberg, 2024. DOI: 10.1007/9783662689219.

[23] S.R. Frank, T. Stroebele, P. Swoboda, R. Schwendemann, and M. Hiller. “A Cryogenic Gallium Nitride Full Bridge for Use in a Thermally Insulating Dual Active Bridge”. In: *IEEE Energy Conversion Congress and Exposition (ECCE)*. 2024, pp. 6798–6805. DOI: 10.1109/ECCE55643.2024.10861612.

[24] Handong Gui, Ruirui Chen, Jiahao Niu, Zheyu Zhang, Leon M. Tolbert, et al. “Review of Power Electronics Components at Cryogenic Temperatures”. In: 35.5 (2020), pp. 5144–5156. DOI: 10.1109/TPEL.2019.2944781.

[25] *GS-065-030-2-L Bottom-Side Cooled 650 V E-Mode GaN Transistor Datasheet*. GaN Systems Inc. 2022.

[26] Mustafeez-ul-Hassan, Yuxuan Wu, Vyacheslav Solovyov, and Fang Luo. “Investigation about Operation and Performance of Gate Drivers for Power Electronics Converters for Cryogenic Temperatures”. In: *2022 24th European Conference on Power Electronics and Applications (EPE’22 ECCE Europe)*. 2022, pp. 1–9.

[27] Mustafeez ul Hassan, Yuxuan Wu, Fang Luo, and Vyacheslav Solovyov. “Development of Gate Drive Configuration for GaN Based Cryogenic Power Electronics Converters”. In: *IEEE Transactions on Industry Applications* 59.6 (2023), pp. 7039–7051. DOI: 10.1109/TIA.2023.3304618.

[28] Rahil Samani, Maryam Alizadeh, Ruoyu Hou, Juncheng Lu, and Majid Pahlevani. “Thermal Design Considerations for GaN-Based Power Adapters”. In: *2022 IEEE Applied Power Electronics Conference and Exposition (APEC)*. 2022, pp. 186–192. DOI: 10.1109/APEC43599.2022.9773448.

[29] Teledyne e2v HiRel Electronics. *Thermal Design for GaNPX® Packaged Devices*. Application Note TD002. Teledyne Defense Electronics, Mar. 2023.