

Graphene on boron nitride microwave transistors driven by graphene nanoribbon back-gates

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We have designed ultra-thin graphene microwave transistors by using pre-patterned metal or graphene nanoribbon back-gates and hexagonal boron nitride as a dielectric substrate. Despite the inhomogeneities induced by the graphene transfer process, we show that it is possible to operate these types of devices across a broad range of microwave frequencies. For the graphene nanoribbon gates, we observe a deviation of the current gain from the usual $1/f$ trend that can be attributed to the large gate resistance of these systems as we demonstrate with our small-signal model. The scattering parameter analysis shows a very limited back-action from the channel onto the graphene nanoribbon gates. Our work thus proves that graphene microwave transistors could be driven by graphene nanoribbon gates. © 2013 American Institute of Physics. [<http://dx.doi.org/10.1063/1.4788818>]

The remarkable properties of graphene field-effect transistors (GFET) are mirrored in the amount of recent efforts to push the transit frequencies f_T to new limits^{1–5} setting the current record to $f_T = 427$ GHz.⁶ Aside from transistor optimization, whole integrated GFET circuits have been designed.^{7,8} Finding appropriate substrates and dielectrics is crucial to improve GFET characteristics. Common material like SiO₂ has a certain roughness⁹ and contains charge traps¹⁰ which both induce Coulomb scattering centers and residual charge carrier inhomogeneities into the graphene channel, ultimately limiting the GFET performance.^{11,12} A promising substrate candidate for graphene is hexagonal boron nitride (h-BN).¹³ h-BN offers several benefits: it has the same morphology as graphene with a lattice mismatch of just 1.7%.¹⁴ It is an atomically flat crystal which contains a very limited number of charge traps and dangling bonds, permitting very high mobilities.¹³ Moreover, h-BN is an insulator and can therefore also be used as a gate dielectric. Here, we report on the fabrication of GFET on h-BN substrates where we have studied the possibility to use graphene nanoribbons as a gate material that operates at microwave frequencies.

We have proceeded along two GFET device layouts. In the first design, we patterned the dual-finger back-gate on a sapphire substrate^{15,16} by electron beam lithography (EBL) followed by the evaporation of a thin Ti/Au bilayer (1/30 nm) and lift-off in acetone. Then, we transfer h-BN flakes onto the pre-patterned back-gate (see Fig. 1(a) for a schematic drawing). We used high purity h-BN crystals, grown as described in Ref. 17. These crystals are superior to CVD-grown h-BN films whose quality is degraded by wrinkles and step edges.¹⁸ The h-BN serves both as the gate dielectric and the substrate for the graphene channel which is transferred in a subsequent step. The connections to the microwave transmission line were defined by EBL, metal evaporation (Ti/Al 10/100 nm) in

ultra high vacuum ($\sim 10^{-9}$ mbar), and lift-off in acetone. In total, four GFET with this layout have been fabricated and characterized, all working in a similar fashion. Here, we present the data of one of these devices.

In Fig. 1(d), the ratio of the drain current I_{ds} to the minimum current I_{ds0} at the Dirac point is plotted versus the back-gate voltage V_g . Note that the Dirac point is very close to zero gate voltage which implies low unintentional doping of the graphene sheet. With increasing drain voltage V_{ds} , we observe a shift towards positive gate voltages as expected with the additional bias-inducing doping of the channel. In addition, the on/off ratio decreases. Both are due to short-channel effects.^{19,20} Fig. 1(e) shows I - V curves of the same device, reaching current densities of up to 0.6 mA/ μ m.

High frequency measurements were carried out on a probe station using a Rohde & Schwarz ZVA40 vector network analyzer (VNA) under ambient conditions. De-embedding was performed by measuring “open” and “short” structures on-chip and extracted from the measured scattering (S) parameters using conventional two-port network analysis.²¹ These structures are located right next to the actual device. Great care was taken to achieve an identical layout. We extracted the small-signal current gain $|h_{21}|$ from both the bare measured and de-embedded S-parameters to determine the corresponding transit frequencies as described in Ref. 22. Fig. 1(f) shows $|h_{21}|$ of the device (h-BN thickness $d = 12$ nm, gate length $l_g = 100$ nm, source-drain distance $l_{sd} = 300$ nm, total channel width $w_{ch} = 16$ μ m) at $V_g = 0.48$ V and $V_{ds} = 0.8$ V. Maximum values $f_T = 6.4$ GHz (extrinsic) and $f_T \approx 60$ GHz (intrinsic) have been found. The current gain follows the ideal $1/f$ slope over the whole measurement range from 0.01 to 40 GHz. The extracted rf transconductance g_m^f is 90 μ S/ μ m at 1 GHz for $I_{ds} = 9.2$ mA and stays almost constant in the measured bandwidth.

The intrinsic transit frequencies of our h-BN supported GFETs exceed those of the devices presented so far.^{18,23,24} However, the performance of our devices is most probably

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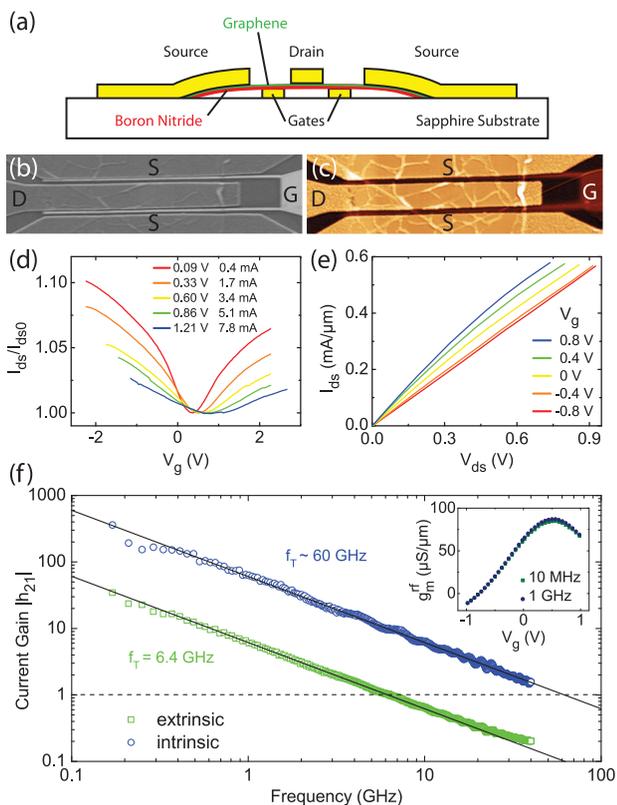


FIG. 1. (a) Schematic of the metal back-gate device layout. (b) SEM and (c) AFM images of the active area. Note the wrinkles in the graphene due to transfer. (d) Ratio of I_{ds} to I_{ds0} vs. V_g . The drain voltages V_{ds0} at the minimum drain currents I_{ds0} are indicated by the legend. (e) I_{ds} vs. V_{ds} for various V_g . (f) Current gain $|h_{21}|$ vs. frequency extracted from as-measured (green squares) and de-embedded (blue circles) S-parameters. The achieved maximum transit frequencies are $f_T = 6.4$ GHz and $f_T \approx 60$ GHz, respectively. The ideal $1/f$ dependence is indicated by black lines. The inset shows the rf transconductance g_m^{rf} vs. V_g .

limited by ripples in the graphene due to the (wet) transfer process.²⁵ These inhomogeneities can be clearly seen in the SEM and AFM images in Figs. 1(b) and 1(c). Additionally, the finite thickness of the metallic back-gate leads to a bending of both the h-BN crystal and graphene, ultimately introducing even further inhomogeneities in the channel. Motivated by this last issue, our second device layout uses a few-layer graphene nanoribbon back-gate (Fig. 2(a)) with a thickness of less than 2 nm and a gate length of 100 nm. Together with the very thin h-BN flakes of about $d = 4$ nm and a monolayer graphene with a channel length of 500 nm and a total channel width of $30 \mu\text{m}$, the cumulative device height is $\leq 7\text{nm}$ (excluding metallic electrodes).

Figs. 2(b)–2(g) depict the various steps of the device fabrication process. We begin by exfoliating natural graphite onto our sapphire substrates. Using optical microscopy, we singled out suitable flakes for the back-gate. The dual-finger gate layout is patterned by EBL using a negative resist (ma-N 2401). We use oxygen plasma to pattern the flakes. Then, the resist is removed by acetone and the sample is cleaned in a vacuum furnace. The h-BN and graphene flakes are transferred using an optimized wedging technique.¹³ Accurate alignment of the order of $\sim 1 \mu\text{m}$ is achieved with the high-precision piezo stage of our home-made transfer set-up. In the last step, the source, drain, and gate electrodes are defined by EBL, and a Ti/Al

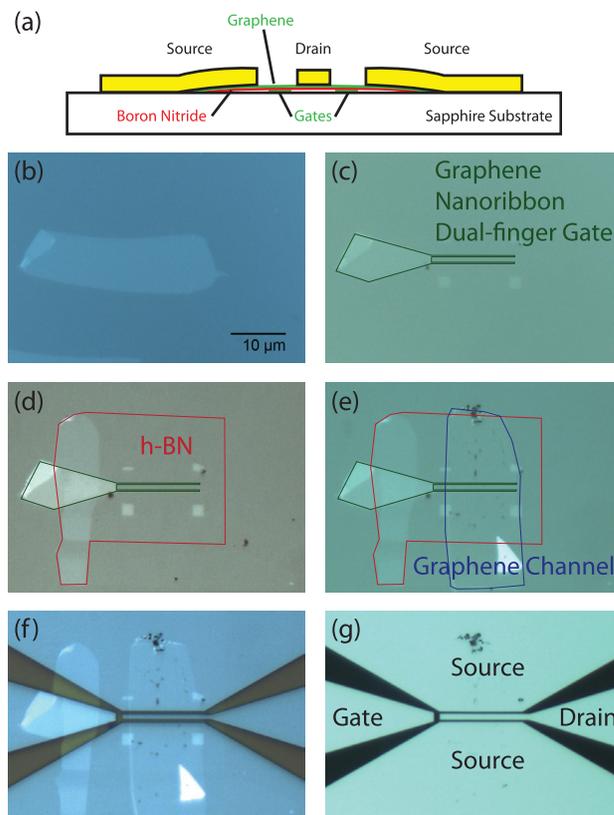


FIG. 2. (a) Schematic of the graphene nanoribbon back-gate device layout. (b)–(g) Optical micrographs of the sample fabrication steps: (b) Exfoliation of graphene (few layer of ~ 2 nm thickness) for back-gate defined by EBL and etched using reactive ion etching (c). (d) Transfer of a thin layer of h-BN covering the gate fingers. (e) Transfer of a monolayer graphene flake (channel). (f) Patterning of the contacts and gate electrode by EBL. (g) Metal evaporation Ti/Al.

bilayer (10/100 nm) is evaporated in UHV. Two devices were fabricated and measured, both showing similar performances.

We find that the Dirac point is slightly shifted with respect to zero gate voltage indicating low doping level (see Fig. 3(a)). I - V curves show clear gate dependence (see Fig. 3(b)). In Fig. 3(c), the high frequency measurement results are plotted. At $V_{ds} = 0.53$ V, the cut-off frequencies are $f_T = 4.8$ GHz before and $f_T \approx 30$ GHz after de-embedding the parasitic capacitances of the contact pads. A full open/short de-embedding process however was impossible to perform since the graphene back-gate would have to be replaced by normal metal conductors in the dummy structures. A clear indication of this issue is the departure of the de-embedded current gain from the usual $1/f$ dependence at the highest frequencies.

Although the performance does not fully reach that of our metal-gate devices, it is still surprisingly high given the extreme reduction of the gate thickness (30 nm versus 4 nm) and the larger gate resistance R_g of the graphene nanoribbon back-gates. Gate resistance should be as small as possible in high frequency transistors.^{26,27} We observe that the extrinsic current gain curve starts to deviate from the ideal $1/f$ characteristic before reaching the optimum cutoff frequency. This is strong evidence of the very high gate access resistance R_g . The $|h_{21}|$ behavior can be understood by a simplified small-signal model,²⁸ which accounts for the access resistance R_g ,

the total gate capacitance $C_g = C_{gs} + C_{gd}$ of the GFET²⁹ (C_{gs} and C_{gd} corresponding to gate to source and gate to drain capacitances, respectively) and the contact pad capaci-

tance C_{pg} . The circuit used to model our system is depicted in Fig. 3(e). We found that the resulting frequency dependence can be described by

$$h_{21}(\omega) = \frac{(g_m - i\omega C_{gd}) \cdot (\omega R_g (C_{gd} + C_{gs}) - i)}{\omega(1 + i\omega R_g (C_{gd} + C_{gs})) \cdot (i\omega R_g (C_{gd} + C_{gs}) C_{pg} + C_{pg} + (C_{gd} + C_{gs}))},$$

where its module is used to fit our raw data. We keep C_{pg} and g_m as static parameters while only leaving R_g and C_g as fitting parameters, we show that our model fits well the behavior of $|h_{21}|$. For a measured transconductance of $g_m = 2.6$ mS, $C_{pg} = 31.2$ fF (extracted from the open structure), we obtain a $C_{gs} \sim 2.9$ fF, $C_{gd} \sim 13.8$ fF, and $R_g \sim 3.3$ k Ω . Despite this large gate resistance R_g (approximately two orders of magnitude larger than R_g of the metal back-gate transistor), Fig. 3(d) shows a high rf transconductance of the device. At 10 MHz, g_m takes on comparable values as the metal back-gate device. At higher frequencies, however, we observe a notable decrease, mainly affected by the large gate resistance of our graphene nanoribbon gate devices.

The analysis of the S-parameters offers a deeper insight into the quality of the GFET. Figs. 4(a) and 4(b) show polar

plots of the recorded S-parameters for the metal and the graphene gate, respectively. S-parameters relate incoming and reflected voltages of the two-port transistor devices, one port being defined by gate and source and the other by drain and source.²¹ S_{11} gives the impedance mismatch to the characteristic impedance Z_0 which in almost all rf applications is given by 50 Ω . While intuitively, one would expect stronger reflection for higher frequencies in the graphene gated device,³⁰ we find indeed the opposite. We may attribute this results to the effect of the quantum capacitance that will become increasingly dominant for decreasing gate dielectric thickness,^{31,32} as well as to the very thin graphene nanoribbon back-gate and its reduced fringing fields compared to thicker metal-gates.

Another important impact of the graphene nanoribbon back-gate can be seen when comparing the frequency development of S_{12} which indicates the back-coupling of the electromagnetic fields from the channel into the gate. This process is strongly suppressed in the graphene-gated device at high frequencies. For cases in which good source/load back-action isolation is needed, this might be of benefit. S_{21} and S_{22} are mainly governed by the chosen operating point of the transistor. In both devices, the transconductance g_m at the operating point is ~ 2 mS and the differential output conductance $g_{ds} = \frac{dI_{ds}}{dV_{ds}}$ is of the order of 100 mS. S_{21} being the voltage amplification factor is therefore rather low in all devices but comparable to those reported on GFET in the literature, and deviates at higher frequencies mainly due to the strong difference in gate access resistance as discussed above. We aim to improve device performance, especially with respect to voltage amplification, by increasing current saturation³³ (i.e., increasing the w_{ch}) and therefore g_{ds} using very thin high- κ gate dielectrics as suggested in Ref. 8.

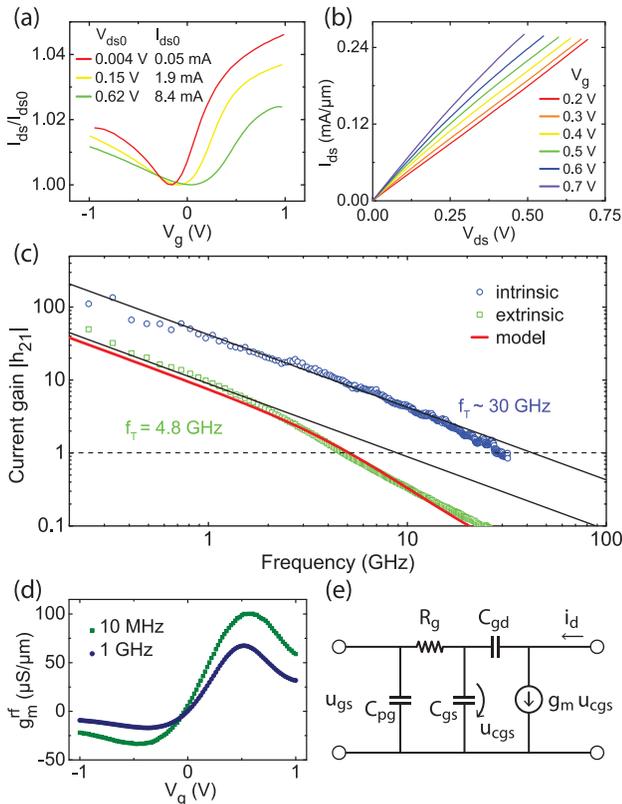


FIG. 3. Graphene back-gate device: (a) Current ratio I_{ds}/I_{ds0} vs. back-gate voltage V_g . (b) I_{ds} vs. V_{ds} for varying back-gate voltages V_g . (c) At $V_g = 0.48$ V and $I_{ds} = 8.5$ mA, maximum transit frequencies of $f_T = 4.8$ GHz (extrinsic) and $f_T \approx 30$ GHz (intrinsic) are found (green squares and blue circles, respectively). The red curve corresponds to the fit with our small-signal model. (d) The rf transconductance at 10 MHz is comparable to the first metal-gate device but decreases with increasing frequency. (e) small-signal model used to fit our GFET current gain $|h_{21}|$.

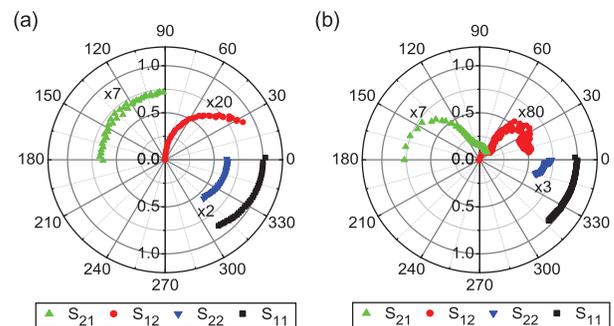


FIG. 4. Polar plot of the S-parameters before de-embedding of (a) the metal back-gate and (b) graphene back-gate device. The frequency range from 10 MHz to 40 GHz has to be read clockwise.

In conclusion, we have presented graphene field-effect transistors on h-BN substrates with metal as well as graphene nanoribbon back-gates of the same length. Despite their large gate resistance, GFET with few-layer graphene nanoribbon gates can be driven at microwave frequencies. These ultra-thin devices represent a further step towards all- sp^2 carbon electronics.

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