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Persistent hysteresis in graphene-mica van der Waals heterostructures

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Abstract

We report the study of electronic transport in graphene-mica van der Waals heterostructures. We have designed various graphene field-effect devices in which mica is utilized as a substrate and/or gate dielectric. When mica is used as a gate dielectric we observe a very strong positive gate voltage hysteresis of the resistance, which persists in samples that were prepared in a controlled atmosphere down to even millikelvin temperatures. In a double-gated mica-graphene-hBN van der Waals heterostructure, we found that while a strong hysteresis occurred when mica was used as a substrate/gate dielectric, the same graphene sheet on mica substrate no longer showed hysteresis when the charge carrier density was tuned through a second gate with the hBN dielectric. While this hysteretic behavior could be useful for memory devices, our findings confirm that the environment during sample preparation has to be controlled strictly.

Keywords: graphene, mica, boron nitride, heterostructure, hysteresis

(Some figures may appear in colour only in the online journal)

1. Introduction

As a membrane of only one atomic layer of sp^2-hybridized carbon, graphene is extremely sensitive to its environment. Therefore, it is important to understand the interaction of graphene with the supporting substrate or gate dielectric materials. This is particularly relevant when graphene is integrated into a stack of other two-dimensional (2D) materials, forming a new material with properties that will be defined by interfacial effects and by the interaction of its components. The building blocks of these so-called 'van der Waals heterostructures' [1] are materials with layered crystal structures in which single or few layers can be isolated and manipulated using the same techniques that are being used to isolate and manipulate graphene sheets.

Out of the variety of dielectric materials, so far, hexagonal boron nitride has been the center of attention [2], allowing the discovery of the effect of a Moiré superlattice on the electronic transport in graphene [3–5].

Other promising candidates that have not yet been investigated as comprehensively are the members of the mica group of naturally occurring sheet silicates. The most commonly used one is muscovite mica, with the formula $KAl_2[Si_3, Al]O_{10}(OH)_2$ [6]. The structure is a stack of triple layers, each consisting of two identical tetrahedral layers of $(Si, Al)_2O_5$ sandwiching a layer of octahedrally coordinated aluminum atoms. The triple layers are negatively charged due to the substitution of about one fourth of the fourvalent Si by trivalent Al. They are separated and only weakly bound by interlayer potassium cations, compensating for the negative charge. The layered structure allows cleaving the crystals along the (001) planes using either a scalpel or Scotch tape, leading to macroscopic, atomically flat surfaces. In this process, the potassium ions get distributed between the cleaved surfaces, causing a varying, high electrostatic surface potential [7] and making the surface strongly hydrophilic.

Depending on the humidity, this leads to the formation of water adlayers, which have been studied using various techniques [8–12].

Mica is a common material for electronic components such as capacitors. Due to its high dielectric strength and permittivity of $\varepsilon_r = 6.4$–9.3 [13, 14] it is used for insulation. In particular, in high frequency applications its high resistivity and low loss tangent are valuable. Furthermore, mica is flat, transparent, flexible and cheap. These properties also make mica an appealing substrate and dielectric for graphene devices [15, 16]. So far, thin mica layers have been utilized as a dielectric for organic electronics [17–19] and carbon nanotube field-effect transistors [20].

It was shown that graphene on mica conforms to the atomically flat mica substrate and becomes atomically flat itself [21]. On the other hand, Xu *et al* showed that water adsorbed on the surface due to the strong hydrophilicity can be encapsulated between graphene and the mica surface [22, 23]. As for the electronic properties, Shim *et al* [24] used Raman spectroscopy to probe substrate-induced charge doping. Ponomarenko *et al* [25] and Kretinin *et al* [26] measured the conductivity of graphene on various substrates, including mica, to investigate the role of charged impurities on charge carrier mobility in graphene. However, no detailed study of electronic transport in graphene-mica systems has been reported yet. Here, we show electronic transport experiments in graphene-mica heterostructures in which mica is used as a gate dielectric and/or substrate. We find a very strong positive hysteretic behavior of the resistance with respect to tuning the gate voltage. It persists down to millikelvin temperatures and can be strongly tuned by varying the sweeping speed, the sweeping range and the charging time at a fixed gate voltage. In addition, we show that when mica is only used as a substrate, no hysteresis is observed. Finally, we discuss the possible mechanisms responsible for the behavior.

2. Experiments, results and discussions

In our study, we have designed different graphene-mica heterostructures to investigate the role of mica as a dielectric and as a substrate. In total, twelve different samples were fabricated and characterized. Electronic transport experiments have been performed in a two-terminal configuration using standard low-frequency lock-in detection and/or using a LR700 resistance bridge. We have used a cryo-free dilution refrigerator BlueFors LD250 for the low temperature measurements.

Our first sample design is depicted in figure 1(a). Thin mica crystals (muscovite mica V1 grade, supplied by Plano GmbH) are directly deposited onto a heavily doped Si wafer with 320 nm SiO_2 using mechanical exfoliation [27]. Using an optical microscope, mica crystals below 10 nm thickness can easily be located, as the apparent color of the SiO_2/mica stack heavily depends on the crystal's thickness [20]. Then, a graphene sheet is transferred on top using a PMMA-based dry transfer at ambient conditions [2]. Figure 1(b) shows the resistance versus the gate voltage for a device that consists of

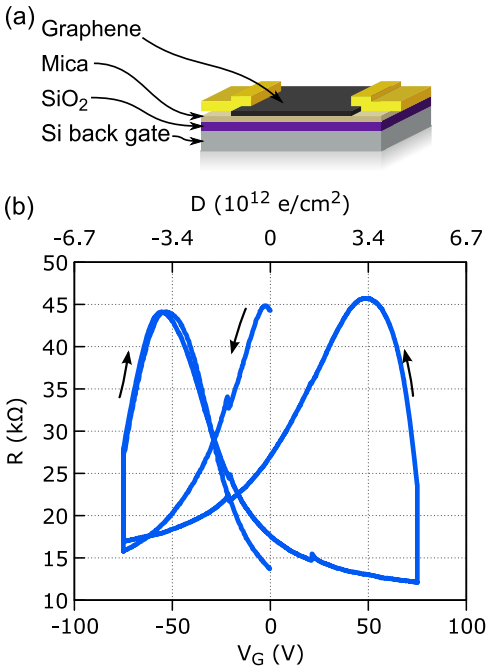

Figure 1. (a) Sketch of a graphene on mica field-effect device. (b) Gate sweep at 0.25 V s^{-1} with a charging time of two minutes at ±75 V measured on a graphene monolayer on a 320 nm SiO_2/31 nm mica dielectric bilayer. The second *x*-axis shows the displacement field, defined as $D = \frac{\varepsilon_0 \varepsilon_r^{SiO_2}}{d} \cdot V_G$. The charge neutrality point for the up and down sweeps shift by 104.5 V.

a stack of 320 nm SiO_2 and 31 nm mica. The gate sweep (figure 1(b)) was performed with a ramping speed of 0.25 V s^{-1} and a charging time (pause) of two minutes at the highest and lowest gate voltage. Starting at a back gate voltage of $V_{BG} = 0$ V, the sample seems to be undoped at first. However, after decreasing the gate voltage to −75 V one can clearly see a very large hysteresis on the following gate sweeps in which the charge neutrality point is shifted from −55.5 V on the up sweep to +49 V on the down sweep. With the charge neutrality point shifting upward (downward) for positive (negative) gate voltages, the sample shows positive hysteresis. In this situation, the charge carrier density cannot be directly related to the gate voltage through the simple capacitor model $n = \frac{\varepsilon_0 \varepsilon_r}{ed} \cdot V_G$ anymore. The potential at the graphene sheet will instead be the sum of the potential from the back gate and an unknown time and gate voltage dependent potential V_H that is responsible for the hysteresis [28]. After the stay at maximal gate voltage, V_H almost completely compensates for V_G. The two potentials thus are of the same order of magnitude in the present case. As the additional potential changes during the gate sweeps, the curves get distorted, and the intrinsic properties of the graphene sheet cannot be properly determined [29, 30]. The positive gate hysteresis observed here can be caused by charge trapping in adsorbates, in bulk or in surface charge traps [31, 32] and/or electrochemical effects in water in the vicinity of the graphene sheet [30, 33]. It has been argued that the first water adlayers that form on a cleaved mica surface are dipole-ordered, forming a layer of ferroelectric ice [11, 34].

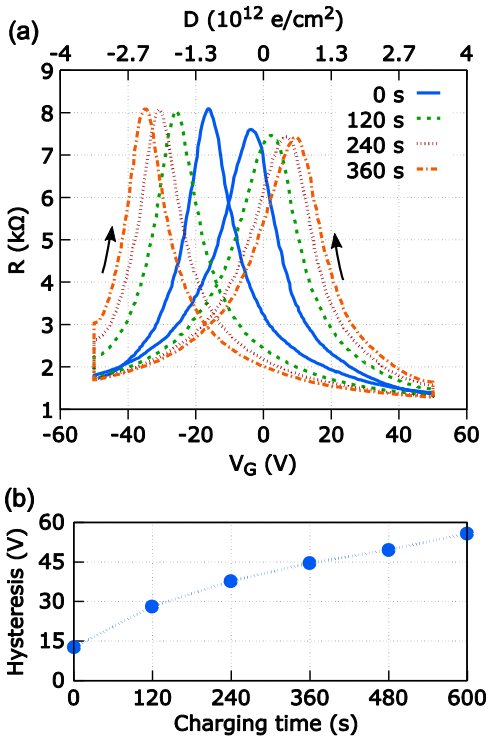

Figure 2. Sample prepared in a controlled atmosphere: (a) the sweeps were performed starting at −50 V with a sweeping speed of 0.83 V s^{-1}. The gate was kept at ±50 V before each up and down sweep for the given time. (b) Gate voltage difference of the position of the charge neutrality points in (a) with respect to the charging time at maximal gate voltage.

However, like in the experiments using ferroelectric coatings by Zheng *et al* [35, 36], the sole polarization of H_2O molecules should induce a negative hysteresis [31, 37]. Thus, if there are effects caused by the polarization of water molecules, they are obscured by the much stronger positive hysteresis.

In order to elucidate the effect of trapped water at the graphene-mica interface, we have prepared samples inside of a glove bag in a nitrogen atmosphere with relative humidity <5%. Additionally, the sample stage and mica substrate were heated to 140 °C during the transfer to further reduce the amount of water adsorbed on the surface that could get trapped at the mica/graphene interface. The amount of water that is adsorbed by the mica surface depends on the humidity, and it was reported that it completely disappears below 2% relative humidity (RH) [22]. Graphene sheets on suspended PMMA membranes were prepared in advance outside of the glove bag. Then, all of the following procedures were done within the controlled nitrogen atmosphere: mica was cleaved and exfoliated onto a SiO_2 substrate, a suitable crystal was selected using an optical microscope and the graphene was transferred on top before the sample was removed from the glove bag so that one could consider that water was not trapped between the graphene and the mica.

Figure 2 shows the resulting gate sweeps of graphene on a stack of 320 nm SiO_2 and 12 nm mica, together with the effect of varying the charging time at the minimal and

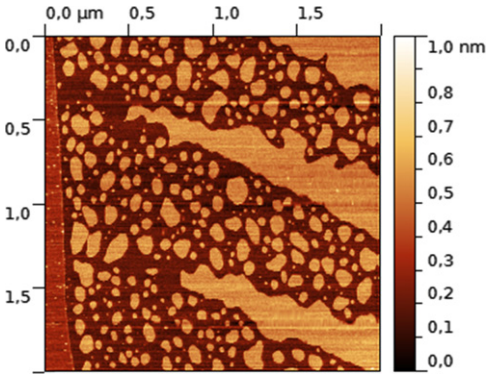

Figure 3. AFM image of the edge of exfoliated graphene on mica. The graphene was exfoliated onto freshly cleaved mica in an argon glovebox. Nevertheless, encapsulated water is visible.

maximal gate voltage before reversing the sweeping direction. To decrease distortions, the sweep speed was increased to 0.83 Vs^{-1}, and the sweeping range was decreased to ±50 V. Still, a very large hysteresis remains, which can be strongly tuned by varying the charging time (here, from 0 to 6 min). Figure 2(b) shows the difference between the position of the charge neutrality points for the up and down sweeps with respect to the charging time. Starting at 12 V for the direct reversion of the sweeping direction, the hysteresis increases up to 56 V for a charging time of 10 min without showing a sign of saturation. Raman spectroscopy measurements have shown that a direct contact between the graphene and the mica surface can cause strong p-doping, which gets suppressed by interfacial water layers [26]. As we don't observe this doping effect, it seems likely that despite the preparation in a dry atmosphere, water might get trapped at the interface between mica and graphene after exposure to ambient air, suppressing the charge transfer. As shown in figure 3, we observe interfacial water even when graphene was directly exfoliated onto mica inside an argon glovebox with <5 ppm water. The image was recorded at 30% relative humidity and shows islands of water with a height of 0.4 nm at the edge of the graphene sheet. In the inner part, the water formed a closed film. The mobility of the interfacial water seems to depend on details of the sample fabrication [38]. While Xu *et al* [22] see a clear dependence of the amount of trapped water with respect to the humidity during graphene deposition and report that graphene permanently traps and immobilizes water adlayers for weeks, Severin *et al* [39] observe reversible dewetting of the mica/graphene interface when changing the humidity.

Although a lot of charges seem to accumulate in the vicinity of the graphene sheet during the gate sweeps, which effectively screen the gate, the curves only get shifted, while their shape does not show a dependence on the charge neutrality point's position. Thus, either the trapped charges are too far away from the graphene to act as scatterers, or the density of fixed charge impurities is much higher than the density of additional trapped charges.

In order to investigate the difference between using mica as a substrate and as a gate dielectric, as well as the role of

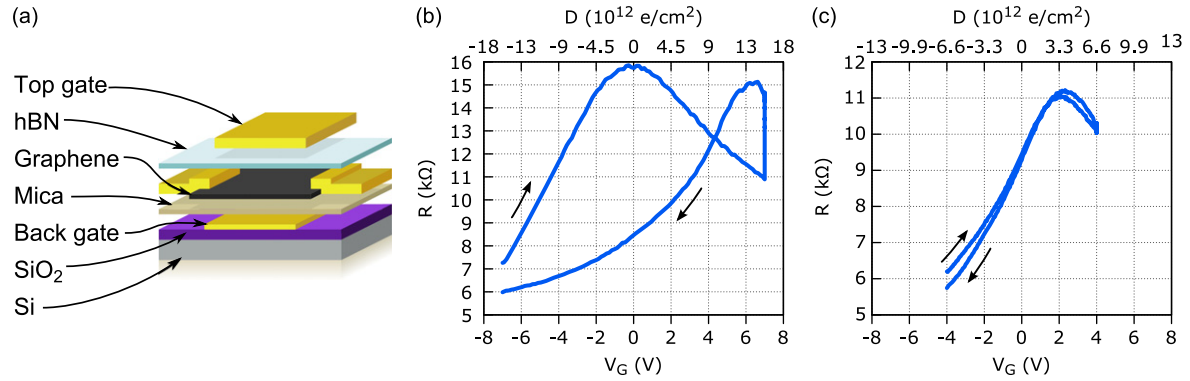

Figure 4. Double-gated sample with both a mica back gate and hBN top gate. (a) Sample structure. The graphene is encapsulated between two metal gates with mica (global back gate) and hBN (local top gate) dielectrics. The same area of graphene can thus be tuned using mica as a gate dielectric or only as a substrate. (b) When tuning the mica back gate, a very large hysteresis is observed. (c) The same graphene sheet shows a vanishing hysteresis when the top gate with the hBN dielectric is used.

impurities and adsorbates on top of the graphene sheet, we designed a mica-graphene-hBN van der Waals heterostructure. Instead of the dual layer SiO_2/mica dielectric, the mica crystals were directly exfoliated onto pre-patterned metal back gates. After the transfer, connection and etching of a graphene sheet, a thin crystal of hexagonal boron nitride was added on top; finally, a metal top gate was created in another electron beam lithography step. The sample thus features a single graphene sheet sandwiched between a back gate with a 20 nm thin mica dielectric and a local top gate with a 13 nm thin hBN dielectric (figure 4(a)). The resulting gate sweeps are shown in figures 4(b) and (c). The second x-axis shows the displacement field $D = \frac{\varepsilon_0 \varepsilon_r}{d} V_G$ for $\varepsilon_r^{mica} \approx 8.1$, $\varepsilon_r^{hBN} \approx 3.9$. First, the back gate was swept from −7 V to +7 V and back at a sweeping speed of 0.12 V s^{-1} with a charging time of one minute between the sweeps. Then, the top gate was swept from −4 V to +4 V and back, with the back gate at 0 V. While the gate sweep using the mica back gate again showed a very strong hysteresis of 6 V, which corresponds to a difference in the displacement field strength of $1.4 \cdot 10^{13}$ e cm^{-2}, the hysteresis in the resistance curve for the sweep using the top gate with hBN dielectric almost vanishes. As both measurements were performed not only on the same sample but on the same area of graphene, this excludes adsorbates, PMMA residues or water on top of the graphene sheet as dominant sources for the gate hysteresis, as their effect should still be visible in the top-gated measurement. We can conclude that the hysteresis must therefore be caused by charge trapping either in the bulk mica crystal or at the graphene/mica interface.

Finally, the temperature dependence of the gate hysteresis was investigated in another sample featuring a 50 nm thin mica dielectric on top of a metal back gate. Graphene on SiO_2 devices typically shows some hysteresis due to charge traps in the oxide. Lowering the temperature is known to freeze out charge traps and therefore suppresses the gate hysteresis [40] (different behavior was observed in [41] on one device). In our sample, the back gate voltage was swept from −10 V to 10 V and back with a sweeping rate of 0.06 V s^{-1} and a charging time of one minute before each sweep. Figure 5

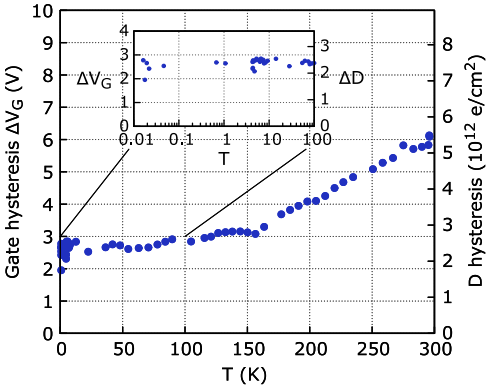

Figure 5. Gate voltage hysteresis (and its equivalent displacement field) versus temperature (see text) down to 7 mK. The gate was swept between −10 V and +10 V, with a charging time of one minute.

shows the temperature dependence of the gate voltage hysteresis, i.e. the shift of the gate voltage of the charge neutrality point between the up and down gate sweep. Starting at a shift of 6 V at room temperature, which corresponds to a displacement field of $5.5 \cdot 10^{12}$ e cm^{-2}, the hysteresis is reduced by cooling the sample until it reaches about 3.1 V or $2.8 \cdot 10^{12}$ e cm^{-2} at 150 K. Astonishingly, further cooling only slightly lowers the hysteresis to about 2.7 V or $2.5 \cdot 10^{12}$ e cm^{-2}, which even remains down to 7 mK and unexpectedly does not vanish.

How can we explain this hysteretic behavior? Electrochemical effects, such as those proposed by Veligura *et al* [30], are most likely suppressed at these very low temperatures. Instead, we believe the hysteresis is caused by electrons tunneling into charge traps at the graphene/mica interface or in the bulk mica.

Interlayer water might play a crucial role [42], especially since potassium ions, such as those that exist on the mica surface, are known to cause dissociation of water molecules on metal surfaces. The valence electron of potassium adsorbed on an ice adlayer on a metal substrate can tunnel into the metal substrate, leaving behind an ion, which causes the dissociation through electrostatic perturbation and creates trap

sites [43, 44]. This effect is further enhanced by the application of an external electric field. A similar mechanism could be responsible for charge traps in ice adsorbed on the mica surface. Here, the potassium ions already exist at the surface, randomly distributed after cleaving the crystal. The dissociation of water molecules causes trapping sites in the ice adlayers at the mica surface. Charge carriers in graphene might then tunnel into these traps when a gate voltage is applied. This layer of trapped charges underneath the graphene will then screen the gate. It remains to be investigated where the trapped water originates from and eventually how it can be avoided. This could be achieved by further reducing the humidity during sample preparation and ideally measuring the sample without ever exposing it to moisture.

3. Conclusions

To conclude, we have investigated the use of mica as a substrate and/or gate dielectric for graphene field-effect devices. When using mica as a gate dielectric, we find a pronounced hysteresis of the sample resistance with respect to the gate voltage. The hysteresis persists even at millikelvin temperatures, but it vanishes in a double gated device when the mica is used only as a substrate and the charge carrier density is modulated through a top gate with hBN dielectric. This behavior can be explained by charge trapping at the graphene-mica interface in which the interplay between potassium ions at the surface of mica crystals and water enclosed in the interface may enhance the charge trap density. Avoiding the formation of interfacial trapped water layers turned out to be difficult; solely reducing the relative humidity and heating the substrate during sample preparation did not lead to the desired effect. While the hysteretic behavior could be exploited in memory applications, the use of mica in graphene devices requires strict control over the manufacturing conditions to adjust the amount of trapped water. Furthermore, it could be necessary to encapsulate graphene-mica devices to prevent the intrusion of water into the interface even after sample preparation.

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