# Investigation of the operation modes and the switching behaviour of a switchable flux - flow resistor at 4.2 K

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The electrical properties of a switchable flux - flow resistor (SFFR) have been investigated. The maximum superconducting current in the channel can reversibly be varied by gate voltages in the range of 2.5 to 7 V. Gate voltages above a threshold voltage yield a depression of the pinning force in the channel. The SFFR allows for three different operation modes. The operation modes have been characterised by static and transient measurements. A special layout for transient measurements with high resolution was developed. Possible applications of superconducting three terminal devices are discussed.

**Key Words:** superconducting three terminal device, transient measurement with high resolution, applications of the three terminal device

Many different concepts for three terminal devices have been proposed in the past [1]. The essential electrical properties of the SFFR based on niobium technology have already been described in [2]. Some additional properties and the switching behaviour of the SFFR are presented in this paper.

The cross section of the SFFR in Fig. 1 reminds of a field effect transistor with a superconducting channel. To estimate the strength of a possible field effect, the characteristic parameter $\alpha = L_D / \xi(0)$ [3] has been evaluated, where $L_D$ is the Debeye length and $\xi(0)$ the coherence length at 0 K. The value $\alpha_{Nb} = 2.6 \cdot 10^{-3}$ indicates a negligible small field effect. The function of the SFFR is based on other physical effects, which will be discussed in the next section. Although there is no field effect, the usual notations for field effect devices will be used. The channel layer of the SFFR is a 30 nm thick Nb film with a critical current density in the range of $j_C = 10^7$ A/cm$^2$ and a critical temperature $T_C = 9.3$ K. The channel region of the SFFR is covered with a 10 nm thin $Nb_xO_y$ layer. The gate electrode is realised with an Al - Nb double layer, alternative gate materials are discussed in [3]. The leads to the gate electrode are on top of an 300 nm thick SiO layer. A detailed description of the fabrication process is given in [4].

**Operation modes of the SFFR**

As reported earlier [2], the critical current of the channel can be varied reversibly by applying a suitable gate voltage. In Fig. 2 the critical current in the channel and the gate current are plotted as a function of the gate voltage.

The gate current shows a non-linear voltage dependence above a positive and below a negative threshold voltage. There are different possibilities for such a carrier transport through an insulating film [5]. A linear dependence between the logarithm of the normalised gate current and the inverse temperature was found [4] indicating a carrier transport according to the Poole - Frenkel effect [5,6]. This model explains the strong increase of the gate current at the threshold voltages by localised electrons in the gate oxide, which become mobile due to the strong electric field. The gate current versus voltage has been calculated according to [6] and plotted as a solid line in Fig.

2 with the oxide thickness as the only fitting parameter.

The critical current of the channel is strongly reduced above the threshold voltages $|V_{TH}|$. This effect is caused by the increase of the gate oxide conductivity by more than two orders of magnitude, which changes the boundary conditions at the top of the channel layer. In the switched - off state, for gate voltages $|V_G| < |V_{TH}|$, the SFFR can be considered as a superconductor - insulator system. In the switched - on state, for gate voltages $|V_G| > |V_{TH}|$, the SFFR changes to a system superconductor - normal conductor. The thickness of the superconducting channel layer is smaller than the coherence length, so that a strong interaction between the two layers takes place, enhanced by the absence of a Schottky barrier between the Nb channel and the 'quasi - metallic' $Nb_xO_y$ gate oxide [2]. The energy gap of the superconductor is reduced in such systems [7], so that the critical current and the critical temperature are decreased.

To understand the function of the SFFR, it is necessary to measure the channel current versus the voltage drop along the channel in the switched - on state as shown in Fig. 3. There is a finite resistance $R_F = 5\ \Omega$ between the points 0 and A, which is independent from the gate voltage in the switched - on state. The section A - B marks the transition into the normal conducting state. The differential channel resistance between the points B and C is $R_N = 50\ \Omega$, which corresponds to the calculated resistance in the normal conducting state of the channel. The different positions of the points A (transition to the normal conducting state) and D (return from the normal conducting state) is caused by thermal heating of the device. For gate voltages $|V_G| < |V_{TH}|$ the points A and D are on the vertical axis indicating a superconducting channel.

Beside the normal conducting state the SFFR exhibits a second kind of conductivity for gate voltages $|V_G| > |V_{TH}|$ and channel currents smaller than the corresponding critical current of the channel. In this range flux - flow motion [8] owing to the applied gate voltage is assumed to take place. To test the assumption, the mean pinning force $f_p = I_C * B$ per unit length of a vortex was measured at 6.15 K for different gate currents in external magnetic fields oriented perpendicular to the device [2]. It could be demonstrated, that gate voltages above $V_{TH}$ yield a strong depression

of the pinning force, so that the channel region switches from a type II superconductor with pinned vortices to an ideal type II superconductor with flux flow [8].

The correlation between the reduction of the energy gap and the depression of the pinning forces is yet not understood, so that additional experiments are needed to explain the physical behaviour of the SFFR in more detail.

There are three possible operation modes of the SFFR: the zero voltage state, the normal conducting state and the flux - flow state. The range of these operation modes are shown in Fig. 4 as a function of the channel current $I_K$ and the gate voltage $V_G$. Typical values for the threshold voltages are within the range 2.5 V < $|V_{TH}|$ < 5 V. The maximum gate voltage $V_{Gmax}$, where the superconducting current in the flux flow state approaches zero, is between 4 to 7 V.

The channel output voltage in the flux - flow state is given by $U_K = R_F \cdot I_K$, where $R_F$ is the resistance in the flux - flow state and $I_K$ is the channel current. This voltage is limited by the maximum heat extraction power $P_{MAX}$, which must be larger than the actual electrical power $P_{EL} = R_F \cdot I_K^2$. If the channel current gets too large, the electrical loss heats the channel up so that the transition temperature of the channel will be exceeded and the SFFR switches into the normal conducting state. In this state the electrical loss increases, because the channel resistance is much larger than in the flux - flow state and further heating takes place. In this way the SFFR latches in the normal conducting state, even when the gate voltage is taken away. To return into the flux - flow state, the channel current must be decreased below a value $I_{MIN}$, given by the condition $I_{MIN}^2 \cdot R_N = P_{MAX}$, where $R_N$ is the resistance in the normal conducting state.

To avoid latching owing to heating in the normal conducting state the channel current must be kept very small in the range of 2 mA. According to Fig. 4, gate voltages in the range of $V_{TH} < V_G < V_{Gmax}$ are necessary to switch into the normal conducting state. Gate voltages near $V_{Gmax}$ often have destroyed devices owing to electrical breakdown i.e. strong electrical fields, so that only few measurements in this mode could be achieved. To avoid these problems alternative operating points at higher channel currents with lower gate voltages $V_G$ have been tested. In this

way higher output voltages $V_K$ without thermal latching could be reached. The return to the zero - voltage superconducting state caused a relaxation oscillation of the channel voltage with a frequency of 400 kHz and a typical relaxation time of 5 µs. For technical applications the flux - flow state is favoured, where thermal latching does not occur.

A SFFR with a typical threshold voltage of $V_{TH}$ = 3.5 V could be used as an electrical switch by biasing the gate with an offset voltage of $V_{G0}$ = 3.25 V, so that an additional input voltage of $\Delta V_G$ = 0.5 V is sufficient to switch the SFFR into the flux - flow state. The resulting channel voltage at a channel current of 20 mA and a flux - flow resistance $R_F$ = 50 Ω would be 1 V, so that a voltage gain of about 2 seems feasible.

**Measurement of characteristic switching times**

To measure the expected small switching times of only few picoseconds the coplanar waveguide layout in Fig. 5 has been developed. A SFFR with a channel resistance in the normal conducting state of $R_N$ = 50 Ω is integrated at the shorted end of a coplanar waveguide with a characteristic impedance of 50 Ω matching that of the measurement equipment. The length of the waveguide has been 25 mm, allowing for a separate detection of the signal from the SFFR and possible spurious signals by reflections at the input of the transmission line. The lead to the gate electrode is also realised as a coplanar waveguide with a characteristic impedance of 50 Ω. In this case, however, the central line and the ground electrodes are in different layers, rather than in the same plane.

The basic idea behind this structure has been to measure the reflection coefficient in the zero voltage state (ρ = -1) and the normal conducting state (ρ = 0) under control of a suitable gate voltage pulse. Since the normal conducting state was unpractical due to voltage breakdown, the SFFR has been switched in the flux - flow state. However, for the given devices the reflection coefficient in the flux - flow state happens to be very close to -1 difficult to use for measurements in the time domain. Therefore a different kind of measurement procedure was applied to

investigate the switching behaviour. For a given bias current in the channel $I_K$ the voltage drop along the channel $V_K$ as the response of a gate voltage pulse has been measured as a function of time.

The rise and the fall time of the voltage drop in the channel $V_K$ has been measured with a sampling oscilloscope of 50 GHz bandwidth between 10% and 90% of the voltage magnitudes $V_{KM}$. The delay between the rising slopes of input and output has been defined in two different ways: $t_{D1}$ has been the time between 50% of the difference of the magnitude of the gate pulse $V_{GM}$ and of the threshold voltage $V_{TH}$ and 50% of the channel voltage magnitude $V_{KM}$; $t_{D2}$ has been defined as the difference of the time at the threshold voltage $V_{TH}$ and 50% $V_{KM}$.

The pulse wise measured values of the threshold voltage differed from the static value up to a factor of 2 for gate pulses of 4 ns width and rise fall times of 670 ps.

The measured input and output pulse in the flux flow state is given in Fig. 6. The channel has been biased with $I_K$ = 10 mA and the magnitude of the gate pulse has been $V_{GM}$ = 3.5 V. The time delay between the signals in the two channels has been calibrated with a capacitive coupled spike at the rising slope of the gate voltage (point A in Fig. 6).

The switching times are strongly dependent on the channel current $I_K$ and the magnitude of the gate pulse $V_{GM}$. The dependence of the delay times defined above and the rising time of the gate voltage are given in Fig. 7. The delay times have been cut down with increasing gate pulse amplitudes; however, the rise time only slightly. The delay could also be reduced by increasing the channel current, while the rise time could not be influenced. To measure the fall time another test structure has been used to avoid problems with reflections from the shorted end of the waveguide. In this case the end of the waveguide was terminated with a resistance of 50 Ω. The measured values for the fall time between 100 and 400 ps were independent of the operating point. These characteristic times seem to allow for switching frequencies up to 1 GHz in the flux - flow state.

A measured switching transient into the normal conducting state is shown in Fig. 8. The channel

current has been 25 mA and the gate pulse magnitude 3.5 V. The delay time between the gate and channel pulse could not be detected, because of the insufficient precision of the capacitive calibration. The rise and fall time have been in the same order as that of the gate pulse.

The strong difference between a switching in the flux - flow and the normal conducting state indicates that they are caused by different physical effects. Although the normal conducting state seems to allow a faster switching operation, voltage breakthrough hampers technical application. The physical reasons of the strong delay of a transition into the flux - flow state are still not completely understood.

**Applications of the SFFR**

As discussed in the first section, the flux - flow state is the most promising operation mode. The normal conducting state can be used, if the problems of thermal heating and voltage breakdown are solved.

The SFFR is not easily used as a transistor - like voltage amplifier, because the transition region of the channel voltage $V_K$ between the superconducting state and the flux - flow state versus the gate voltage $V_G$ is very small and in addition temperature dependent. On the other hand, a bistable operation seems feasible where only a transition between the superconducting state and the voltage state is required.

<u>a) Digital Logic</u>

The SFFR can be used for implementing a basic logic circuit, i.e. an inverter as shown in Fig. 9. The voltage state of the SFFR is defined as a logical ‘1’, the zero - voltage state as logical ‘0’. The gate electrode is biased with a voltage $V_{G0}$ smaller than the negative threshold voltage $-V_{TH}$, so that a channel current $I_{K0}$ causes a channel voltage $V_K$. The SFFR can be switched into the zero - voltage state by applying an additional input voltage $\Delta V_G$, so that $V_{G0} + \Delta V_G > -V_{TH}$. In this way a logical ‘0’ at the input generates a logical ‘1’ at the output and vice versa. Other logical functions such as NAND or NOR circuits are feasible by choosing the appropriate bias gate voltages.

The channel resistance of the SFFR can be designed to yield an output voltage of the circuit $V_K = I_{K0} \cdot R_F$ larger than the input voltage $\Delta V_K$. SPICE simulations with a simplified model demonstrate, that complex logical circuits operate properly, if the voltage gain is larger than 1.5. The logical circuits are resistor coupled. Logic circuits could reach switching frequencies up to the range of Josephson latching logic circuits, but with larger, CMOS compatible output voltages.

b) High frequency circuits

The transmission of high frequency circuits can be changed with switchable resistors.

A simple filter circuit as sketched in Fig. 10a has been investigated to demonstrate the application potential. The characteristics of this filter can be changed by applying a gate voltage at the SFFR larger than the threshold voltage.

The filter comprises lossless 50 Ω waveguides and a λ/4 - stub terminated by a SFFR with the channel resistance of $R_F$ = 1 kΩ in the flux - flow state. If the gate voltage of the SFFR is smaller than the threshold voltage, the channel resistance is zero and hence the stub line is shorted. This short is transformed by the λ/4 - line into a open load at the other end of the stub. In this way the input power can pass the filter without losses. If the gate voltage is larger than the threshold voltage, the channel resistance of the SFFR is 1 kΩ and the stub can be considered as an open load. The open load at one end of the stub line is transformed into a short at the other end, so that no power can pass the filter at the frequency where the length of the stub corresponds to λ/4. The calculated transmission coefficient $S_{21}$ is plotted in Fig. 10b.

The rejected frequency band can be enlarged by adding more stub lines with slightly different lengths. Filters with similar characteristics have already been realised with optically activated switches for communication applications [9].

The SFFR could also be used for the calibration of network analyser measurements in a liquid Helium bath, where the exchange of calibrated loads is time consuming owing to the usual warm up and cool down process. Moreover, most resistors have different values at room temperature

and 4.2 K. Usual three loads are needed: a short, an open and 50 Ω. A superconducting short can hardly be appoximated with semiconductor devices. At least two of the loads, e.g. a short and an 50 Ω resistor, can be implemented with a SFFR at the end of a coplanar waveguide at 4.2 K under control of room temperature electronics.

**Conclusion**

Three different operation modes of the SFFR have been determined and discussed. Static and transient measurements have been performed. The flux - flow state offered switching frequencies up to 1 GHz. A further improvement seems feasible by optimising the preparation technology and the layout of the test structures. Potential device applications for the SFFR are discussed.

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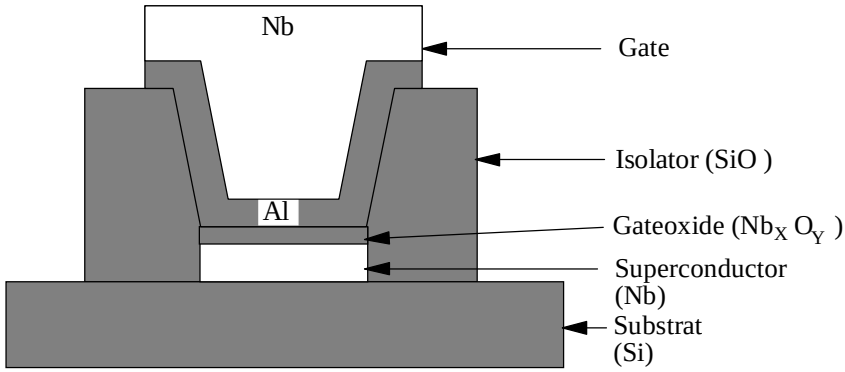



Fig. 1: Cross sectional sketch of the SFFR

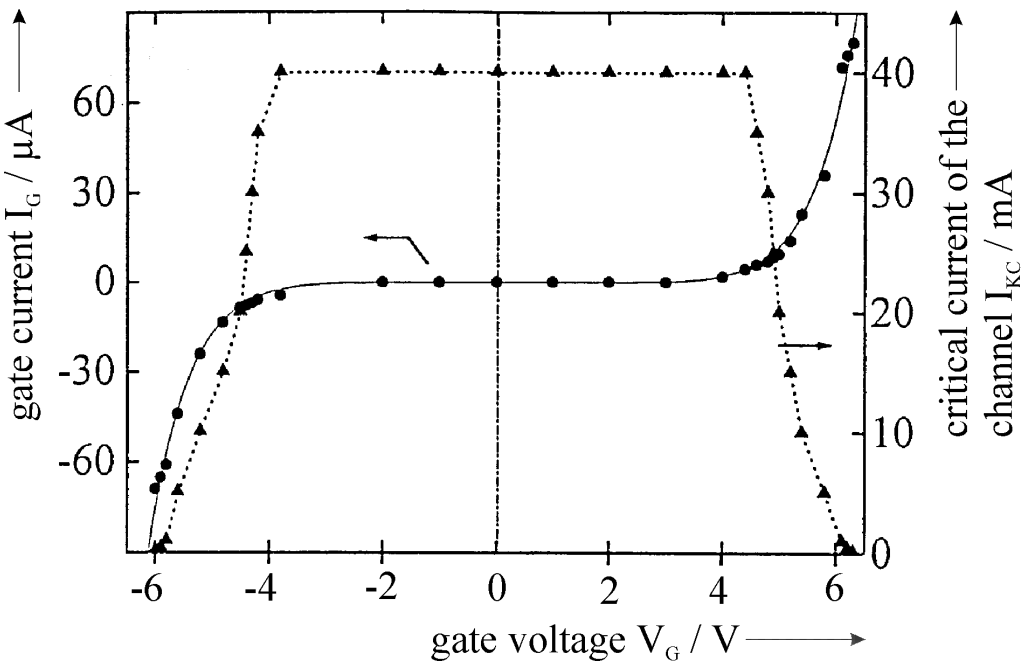



Fig. 2: Critical current of the channel $I_{KC}$ and gate current $I_G$ versus gate voltage $V_G$

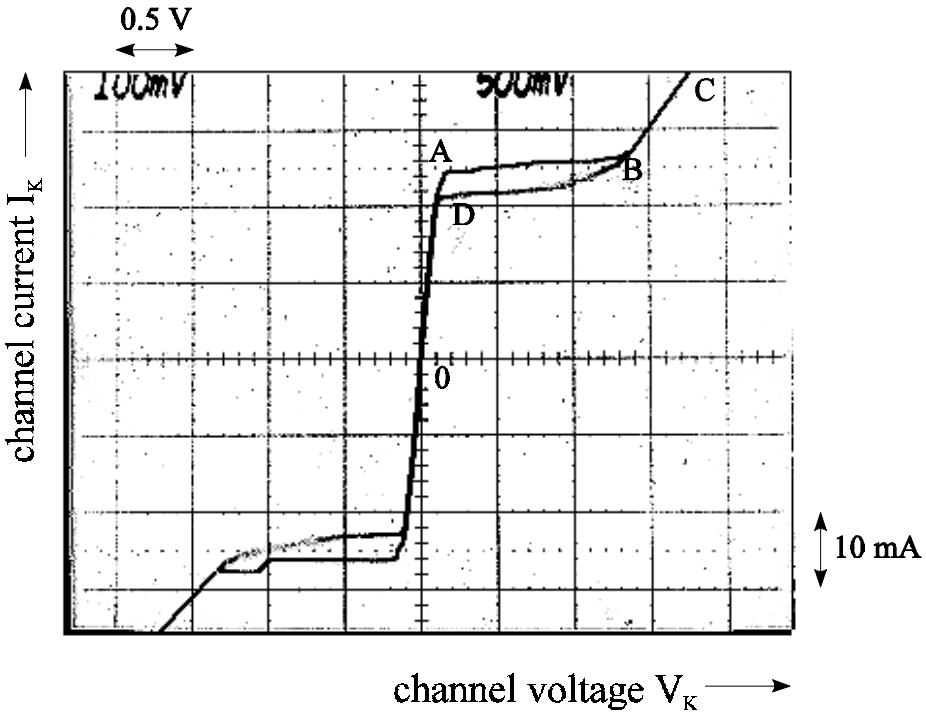



Fig. 3: Current in the channel $I_K$ versus the voltage drop along the channel $V_K$ for an applied gate voltage above the threshold voltage $V_G > V_{TH}$. Between 0 and A the flux flow resistance $R_F$ and between B and C the normal conducting resistance $R_N$ are defined.

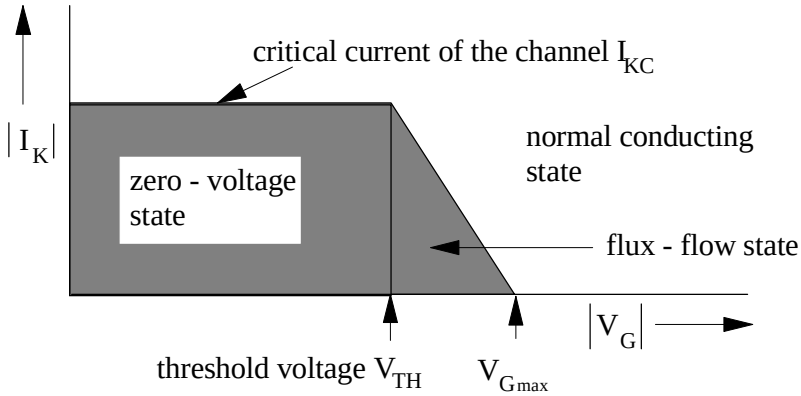



Fig. 4: Range of operation modes as a function of the channel current $I_K$ and the gate voltage $V_G$

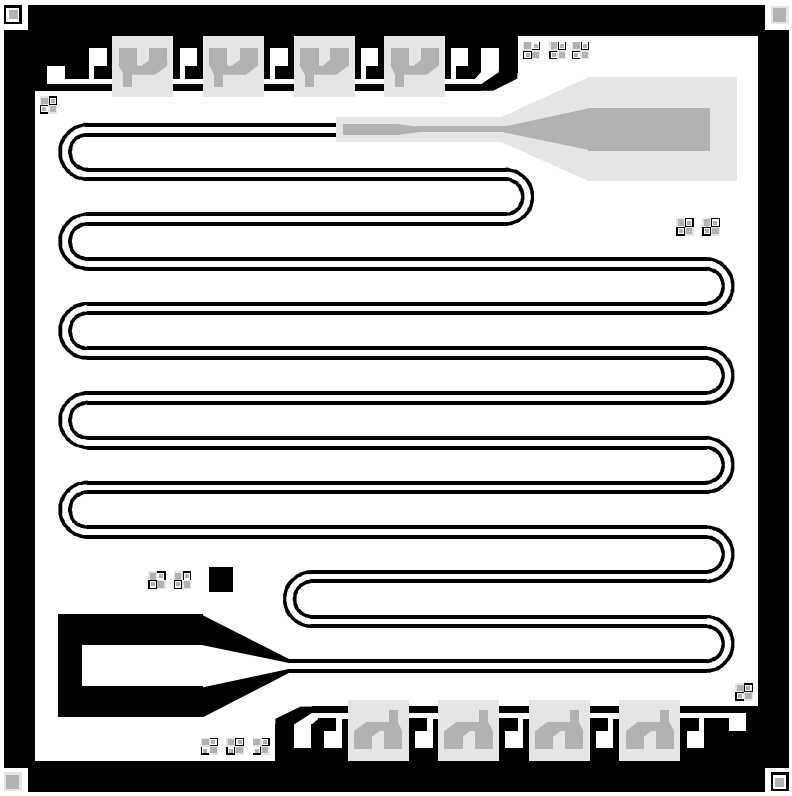


Fig. 5: Layout of the test structure for the transient measurements. Near the border there are eight devices for dc measurements

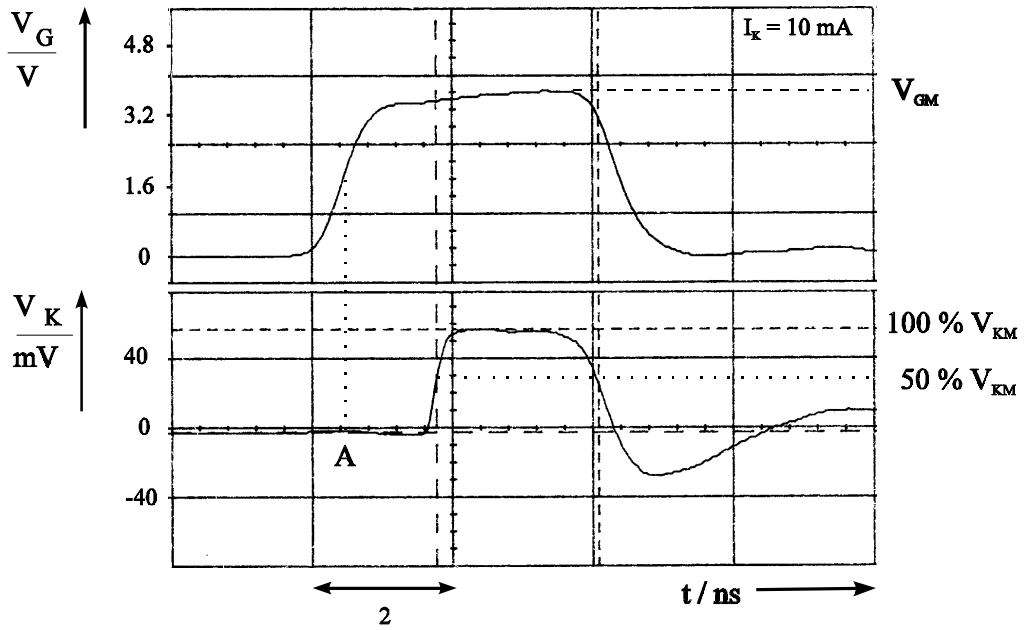



Fig. 6: Measurement of the pulse response in the flux - flow state at a current bias $I_K$ = 10 mA

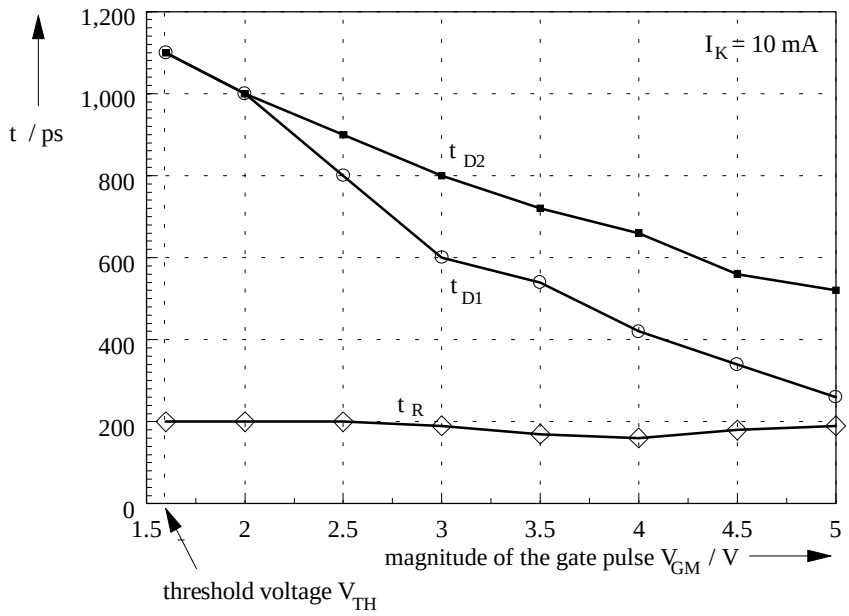



Fig. 7: Rise time $t_R$ and delay times $t_{D1}$ and $t_{D2}$ of the voltage responses for a current bias $I_K$ = 10 mA as a function of the gate pulse magnitude $V_{GM}$.

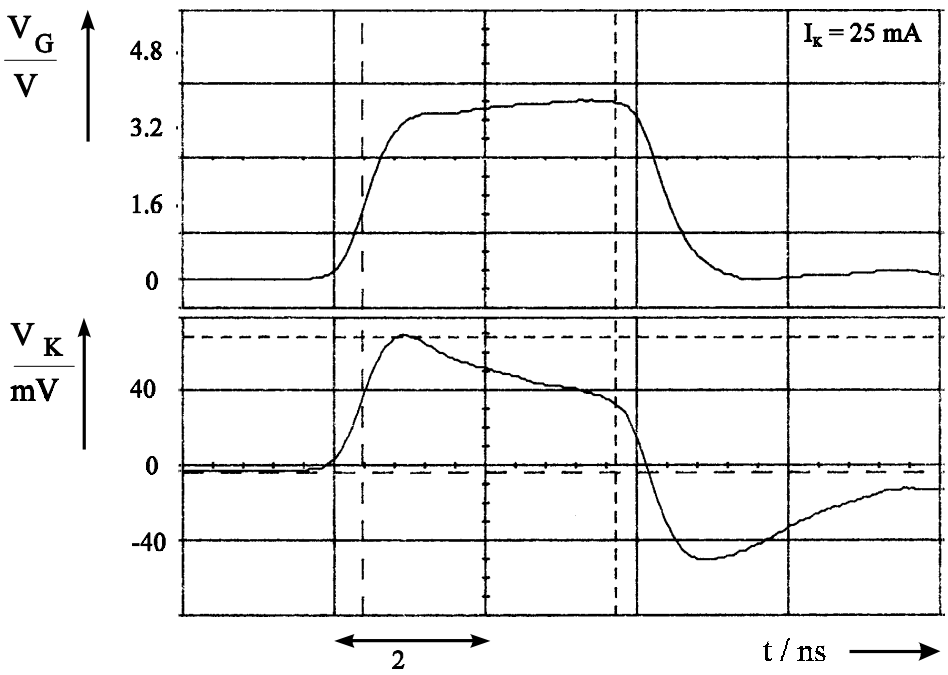



Fig. 8: Measurement of the pulse response in the normal conducting state at a current bias $I_K$ = 25 mA

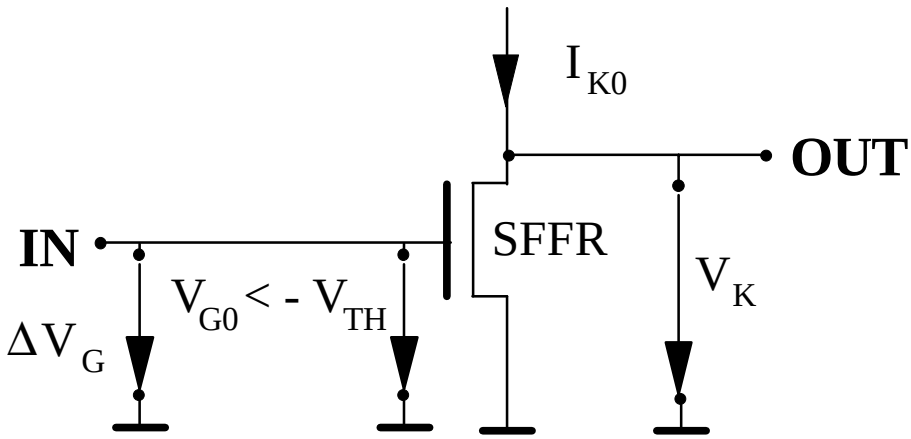
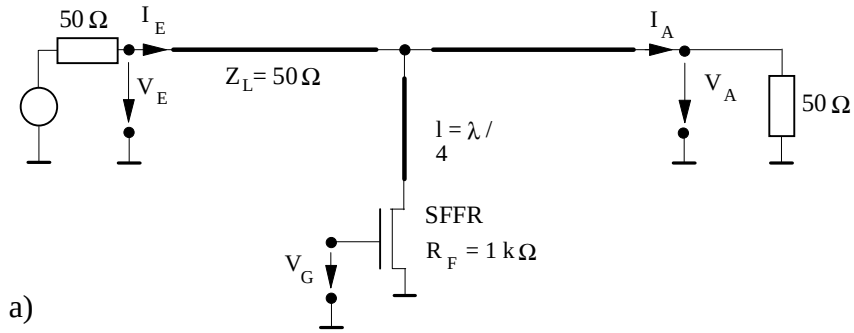



Fig. 9: Equivalent circuit of an inverter realised with the SFFR in the flux - flow state



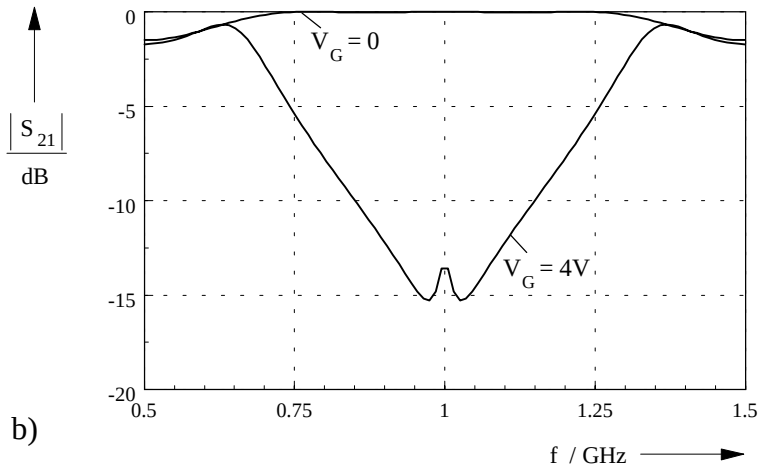




Fig. 10: Switchable filter. a) equivalent circuit b) calculated transmission coefficient $S_{21}$ for an applied gate voltage above the threshold voltage