A Low Power 12 Bit Flux Shuttle Shift Register with Nb Technology

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***Abstract* --A 12 bit Flux Shuttle shift register with a new write and readout gate has been simulated and fabricated using Nb/Al_2O_3/Nb Josephson junctions. Write, shift and read operations have been tested successfully at 4.2 K. Drive currents are independent from input bit sequence. Although measurements were disturbed by trapped flux, minimum margins are ΔI = ± 10 %. The power dissipation of a shift register cell is 9 nW / GHz. Total power losses caused by terminating resistors are 70 μW. The minimum line width may be scaled down to 0.5 μm, because power losses per unit area of long Flux Shuttle shift registers are extremely low.**

I. INTRODUCTION

Shift registers with Nb-Al_2O_3-Nb Josephson junctions can operate at high clock frequencies and have a low power dissipation. Recently many shift register families have been presented. Shift registers with MVTL-gates [1] assign the information "0" or "1" to the zero voltage or voltage state of Josephson junctions. In SFQ-logic data is represented by presence or absence of a single flux quantum in a superconducting loop. Shift registers in RSFQ- and QFP- logic have been tested successfully [2,3,4]. The Flux Shuttle SFQ-shift register [5,6] allows for large margins of shift operation [7,8].

II. CIRCUIT DESCRIPTION

The Flux Shuttle shift register consists of a long, uniform interferometer with three superconducting loops per bit.Three clock currents I_{C1}, I_{C2} and I_{C3} are needed to determine the shift direction. They are coupled magnetically into the loops. A shift register cell with write gate is sketched in Fig. 1.

A flux quantum, representing a "1", causes a circulating current I_{ring} in a storage loop. The induced clock current of the next loop, e.g. I_{C1}, and I_{ring} sum up in the common Josephson junction and the critical current I_{0S} is exceeded. The Josephson junction switches at the rising edge of I_{C1} and its phase

$$\Delta\varphi = \frac{2\pi}{\Phi_0} \cdot \int U_j dt \qquad (1)$$

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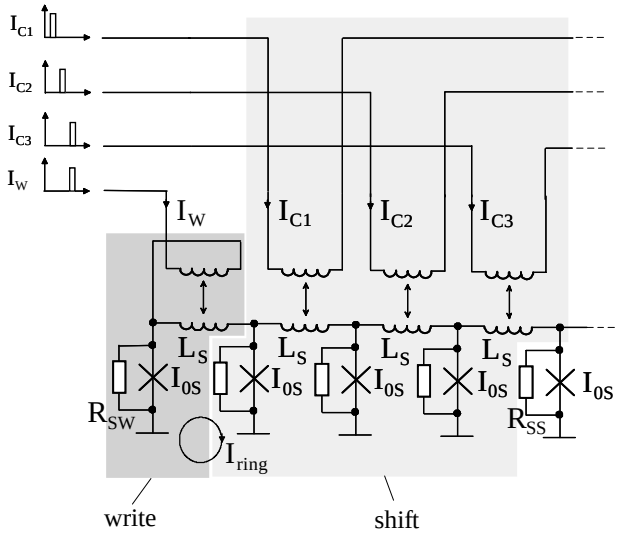

Fig. 1. Circuit diagram of a Flux Shuttle shift register cell with write gate.

turns to $\Delta\varphi = 2\pi$. U_j is the voltage of the switching Josephson junction and Φ_0 = 2.068 mVps one flux quantum. During the switching operation a flux quantum is shifted to the next loop. At the falling edge the flux quantum is stored in the next loop, because the characteristic phase

$$\lambda_S = \frac{2\pi}{\Phi_0} \cdot L_S \cdot I_{0S} \qquad (2)$$

is $\lambda_S = 2\pi$. The flux quantum is shifted to the end of the shift register cell during a clock cycle by the clock pulses I_{C2} and I_{C3}.

If no flux quantum is stored, the induced clock current does not exceed the critical current I_{0S}. The Josephson junction does not switch, and a "0" is shifted with $\Delta\varphi = 0$.

Shifting a flux quantum, the phase is exactly $\Delta\varphi = 2\pi$ if the McCumber damping parameter is

$$\beta = \frac{2\pi}{\Phi_0} \cdot R_{SS}^2 \cdot C_j \cdot I_{0S} \le 1 \qquad (3)$$

where C_j is the junction capacitance and R_S the shunt resistor of the junction. Margins have been calculated in [7,8]. The experimental test of a 1-bit shift register has been described in [9].

The structure of the write gate is similar to the storage loop with same parameters I_{0S} and L_S. It is connected in front of the first shift register stage. The input signal I_W is magnetically coupled into the loop instead of clock currents I_{C1}, I_{C2} or I_{C3}. To increase the margins, I_W is also injected directly into the first junction of the long uniform interferometer, similar as in MVTL circuits. Input pulses I_W appear simultaneously to clock pulses I_{C3}. The Josephson

junction of the write gate is strongly damped with $R_{SW} < R_{SS}$ to avoid writing two flux quanta into the first storage loop. After the data is stored in the write gate, it is shifted by clock pulses I_{C1}, I_{C2} and I_{C3} to the last loop of the first shift register cell.

III. READOUT GATE

The readout gate [10] can easily be connected to a shift register stage by replacing the shunt resistor R_{SS}. It is sketched in Fig. 2 with the last shift register cell. The readout gate consists of a two junction SQUID and is connected to the shift register by the coupling resistor R_R. The critical current ratio of the Josephson junctions is I_{0S} : I_{0R2} : I_{0R1} = 4 : 2 : 1 The amplitude of the pulsed bias I_R does not exceed the SQUID threshold current. The readout voltage is $U_R = 0$, if no flux quantum is shifted. I_R is synchronous with I_{C3}.

During the shift operation of a flux quantum at the rising edge of the clock pulse I_{C3}, the voltage at the switching junction is $U_S > 0$. U_S causes a damping current I_S in R_R and the readout SQUID. The threshold current of the SQUID is exceeded and the readout voltage rises to $U_R > 0$. U_R remains in the voltage state, because the McCumber damping parameter of the readout SQUID is

$$\beta = \frac{2\pi}{\Phi_0} \cdot R_D^2 \cdot C_{0R2} \cdot I_{0R2} >> 1 \qquad (4)$$

with the junction capacitance C_{0R2}. The output voltage falls to $U_R = 0$, when the bias is set to $I_R = 0$. In a certain range the output voltage U_R increases with increasing shunt resistor R_D. The output voltage is $U_R > 1$ mV at a clock frequency of f_c = 14 GHz. The readout operation is dynamic and nondestructive. Minimum margins of the readout gate are $\Delta I_{0R2} / I_{0R2} = \pm 24\%$.

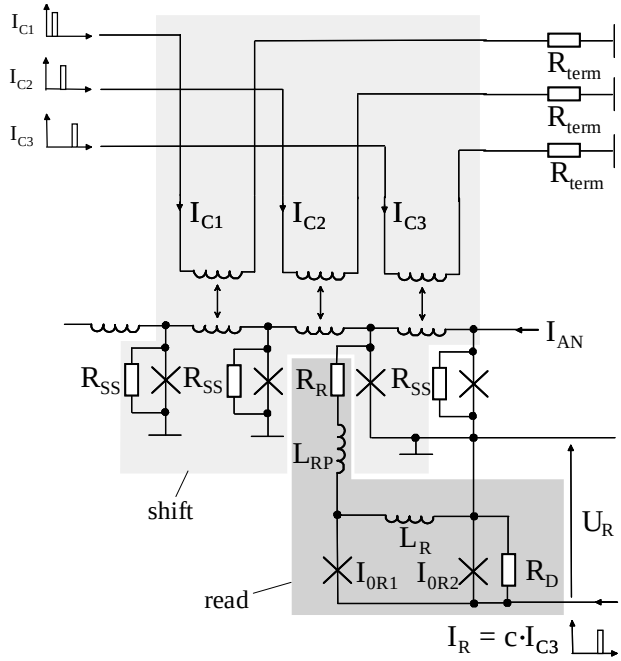

Fig. 2. Circuit diagram of the last Flux Shuttle shift register cell with readout gate.

A dc-current I_{AN} is injected into the last Josephson junction of the shift register to destroy flux quanta in the last storage loop.

IV. LAYOUT

A 12-bit Flux Shuttle shift register prototype has been fabricated with write- and readout gate using a four superconducting Nb-layer technology with SiO_2-insulators, Pd-resistors and Nb-Al_2O_3-Nb Josephson junctions having a current density of j_{max} = 1 kA / cm² [11]. The layout of the last two cells with readout gate is shown in Fig. 3.

All three clock lines run in the top layer without cross over. They are terminated with their characteristic impedance R_{term} = 17 Ω. Clock currents I_{C1}, I_{C2} and I_{C3} couple magnetically into the stripline with inductance L_S between two junctions. The layout of all three clock lines yields the same propagation time along the shift register. The clock lines have a break in the subjacent quasi ground Nb-layer to prevent trapping of flux into a parasitic, superconducting loop. It should be possible to decrease the normalized cell area A_{FS}' = 1620 of the prototype. Normalized cell area of the readout gate is A_r' = 190.

Write gate and storage loop have a similar layout. The current I_W of input line is injected into the first junction. Normalized cell area of the write gate is A_w' = 460.

V. POWER DISSIPATION

Each clock line of the Flux Shuttle is terminated with a resistor R_{term}. Additional resistors on the chip match the 50 Ω characteristic impedance of clock lines, write line and readout bias from room temperature to the low characteristic impedance of the shift register lines. The power dissipation is rather independent of the number of shift register cells. If the clock signals have a pulse duty factor of 1 : 3, power losses are $P_{res} \approx 70\mu W$, independent of the operation frequency.

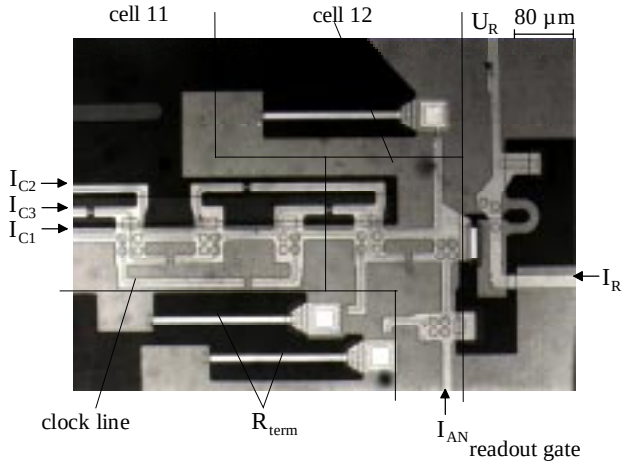

Fig. 3. Photograph of the last two shift register cells with readout gate.

Power dissipation in a shift register cell only appears in the shunt resistor of switching junctions, while a flux quantum is shifted. The power losses depend on the operation frequency and are 9 nW / bit / GHz. They can be neglected, if the shift register has only 12 bits. The Flux Shuttle concept is well suited for long shift registers, because the losses per bit are extremely small. A 1024-bit shift register has power losses of $P_{1024} \approx 170\ \mu W$ at an operation frequency of 10 GHz.

Contrary to the Flux Shuttle, MVTL- and RSFQ- shift registers need a resistor network to supply each cell with a bias current. The network should be matched to the external 50 Ω generator source, because the bias current of MVTL-circuits is pulsed. The power dissipation of a stage with two MVTL-gates is $P_{bit} \approx 7\ \mu W$ [12] and of a 1024-bit shift register $P_{1024} \approx 7.4$ mW. RSFQ-shift registers only need a dc power supply. The power loss of a buffered cell is $P_{bit} = 3\ \mu W$ [2] and of a 1024-bit shift register $P_{1024} = 3.1$ mW.

The one dimensional margins are simulated by varying one parameter at a time while all other parameters are kept constant at their nominal values. The one dimensional shift operation margins of Flux-Shuttle-, RSFQ- and MVTL shift registers are in the same order, ±43%, ±31% [2] and ±43% [12] respectively. Normalized cell area is

$$A' = A / L_{min}^{\ 2}$$

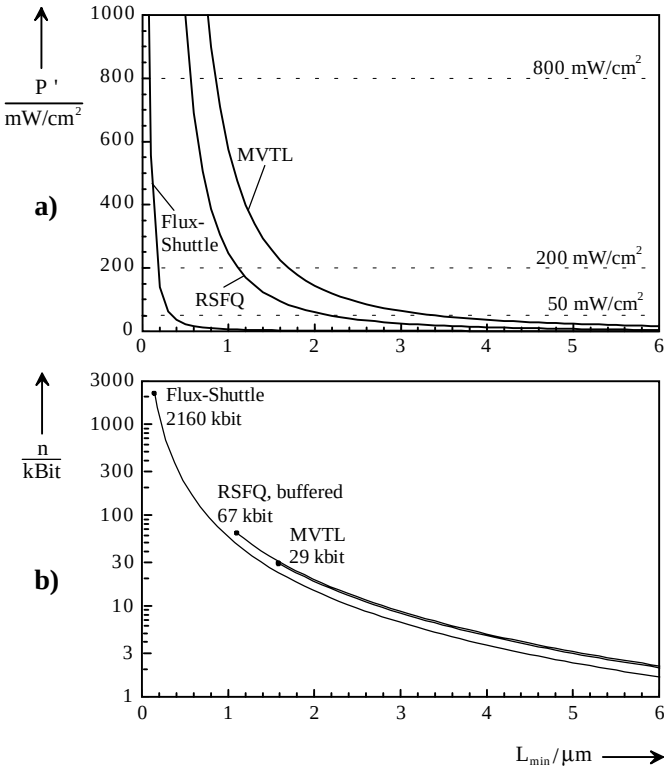

Fig.4. a) Power dissipation per area P' of MVTL-, RSFQ- and Flux Shuttle shift registers versus minimum line width L_{min} at 10 GHz. Dashed lines are thresholds in liquid helium for film boiling (800 mW / cm²), insignificant nucleate boiling (200 mW / cm²) and three stage pulse tube refrigerator at 4.2 K (50 mW / cm²).
b) Maximum number of bits n versus minimum line width L_{min} on a 1cm² chip for P' = 200 mW / cm².

with the cell area A and the minimum line width L_{min}. The Flux Shuttle shift register cell area is $A_{FS}' = 1620$. The terminating resistor area may be negligible small compared to the area of a long Flux Shuttle shift register. The terminating resistor area of a MVTL-shift register stage is estimated to be in the same order as the shift register cell [12], hence the normalized cell area is $A_{MVTL}' = 1260$. A buffered RSFQ-shift register has a normalized cell area of $A_{RSFQ}' = 1200$ [2].

The shift register layout in Fig. 3 may be scaled down in reducing all lateral dimensions by K while keeping constant all vertical dimensions. Since the characteristic phase must be unaffected by scaling, the Josephson current density increases with K^2 [13].

The power losses per area of long shift registers versus minimum line width L_{min} are sketched in Fig. 4a. Dashed lines mark the threshold of film boiling at the chip surface in a helium bath at 800 mW / cm², insignificant nucleate boiling in helium at 200 mW / cm² and the estimated heat extraction capability of a three stage pulse tube cooler at 4.2 K [14]. At a threshold of 200 mW / cm² the minimum line width of a MVTL and RSFQ- shift register is L_{min}= 1.6 µm and L_{min}= 1 µm, respectively. The Flux Shuttle shift register could be scaled down to $L_{min} = 0.5\ \mu m$, not limited by the power dissipation but rather by the fabrication yield of the maximum Josephson current density at $j_{max} = 100$ kA / cm² [15].

The maximum number n of bits on a 1 cm² chip area versus minimum line width is sketched in Fig. 4b. At a threshold of P' = 50 mW / cm² the numbers of shift register cells are $n_{MVTL} \approx 7$ kbit ($L_{min} = 3.4\ \mu m$), $n_{RSFQ} \approx 17$ kbit ($L_{min} = 2.2\ \mu m$) and $n_{FS} \approx 400$ kbit ($L_{min} = 0.4\ \mu m$). Power losses per area of the Flux Shuttle at $L_{min} = 0.5\ \mu m$ are P' = 23 mW / cm² with n ≈ 240 kbit on a 1 cm² chip.

VI. LOW SPEED TEST

To assign the output data clearly to the input and clock pulses, a low speed test frequency of 2.5 MHz has been chosen. The shift operation of a periodic input sequence I_W '1100...' and the output U_R are shown in Fig. 5. The drive and readout pulses drop down to zero as simulated. The output voltage is $U_R = 1.2$ mV.

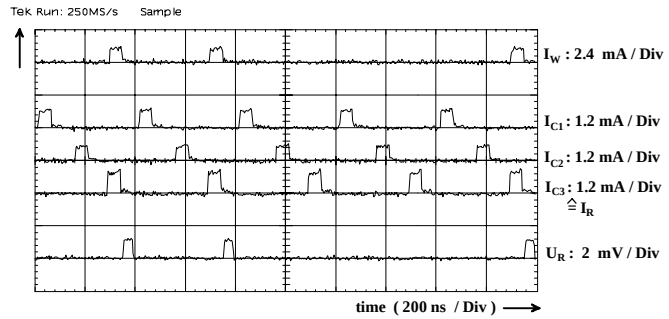

Fig.5. Shift operation: input I_W '1100', clocks I_C and output U_R written 12 clock cycles earlier.

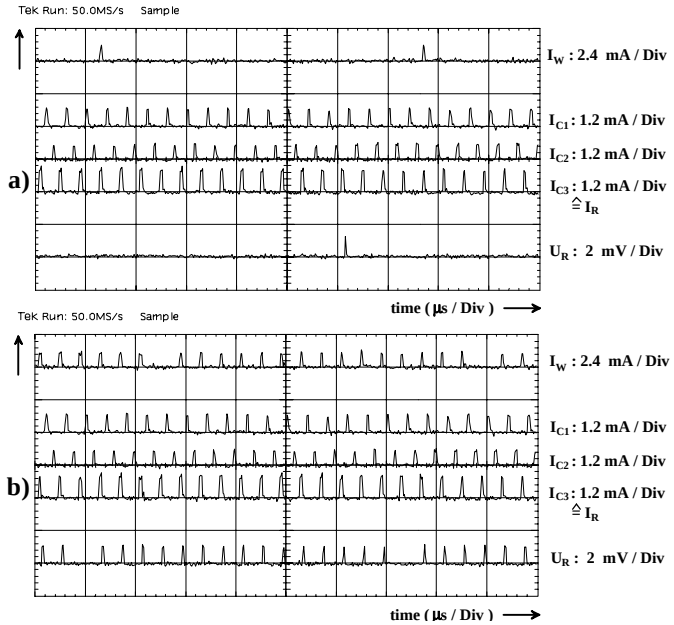

Fig.6. Shift operation in the 12-bit Flux Shuttle shift register for two data words:
a) Data is "1000000000000000...".
b) Data is "0111111111111111...".
Output data U_R can be assigned to input data I_W via the clock signals I_{C1}, I_{C2} and I_{C3}.

In a second test a single flux quantum is generated and shifted. The measurement result is sketched in Fig. 6a.

Clock signals I_{C1}, I_{C2} and I_{C3} do not overlap. I_W and I_R are in phase with I_{C3}. Output pulses U_R can be measured 12 clock cycles after the input pulse is applied. In one period there are fifteen "0" and one "1" to check the shift operation. A sequence of 15 flux quanta, corresponding t "1", is applied to the shift register in Fig. 6b. All output pulses can be assigned to their input pulses via the "0"-signal.

In comparison to Fig. 6a only the input bit sequence has been changed, i.e. the clock currents I_{C1}, I_{C2}, I_{C3}, I_R, the amplitude of I_W and the dc curent I_{AN} have been kept constant. Measured and simulated one dimensional margins are compared in table I. Differences between measured and simulated margins are probably caused by trapped flux near the shift register. Margins differ after a thermal cycling, but minimum margins are at least ± 10 %.

TABLE I
ONE DIMENSIONAL MARGINS OF THE FLUX SHUTTLE

	$\Delta I_W/I_W$	$\Delta I_{C1}/I_{C1}$	$\Delta I_{C2}/I_{C2}$	$\Delta I_{C3}/I_{C3}$	$\Delta I_R/I_R$	$\Delta I_{AN}/I_{AN}$
simulated	± 40 %	± 38 %	± 38 %	± 33 %	± 33 %	± 75 %
measured	± 40 %	± 24 %	± 38 %	± 10 %	± 10 %	± 28 %

VII. CONCLUSION

The 12 bit Flux Shuttle shift register operates with margins of ± 10 %, although measurements have been disturbed by trapped magnetic flux. New write and readout gates have been tested successfully. The test frequency was limited by the available pulse generators to 30 MHz. Measurements up to 2 GHz are in progress. At a clock frequency of 10 GHz and a minimum line width L_{min} = 5 µm the power losses per area of 1024 bit Flux Shuttle-, RSFQ- and MVTL-shift registers are $P_{FS}' : P_{RSFQ}' : P_{MVTL} \approx 1 : 25 : 60$, respectively.

Power dissipation of Flux Shuttle shift registers would not prevent scaling down to $L_{min} < 1$ µm.

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