A 4 bit $YBa_2Cu_3O_{7-\delta}$ Bicrystal Josephson Junctions Flux Shuttle Shift Register

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***Abstract* — A flux shuttle shift register with master and slave sections is implemented with YBCO Josephson junctions along only one straight grain boundary of a bicrystal substrate. The investigated prototype comprises a write circuit, four master/slave shift register cells and a dynamic read out circuit for single flux quanta. The simulation results and the layout are presented.**

I. Introduction

Junctions along a grain boundary of the substrate are very promising for fabricating Josephson circuit test vehicles since small standard deviations of the maximum Josephson current around 10% can be achieved, in contrast to other types of junctions. As substrates with two adjacent straight grain boundaries are expensive and not always available, this study is concentrated on a shift register circuit with only one grain boundary along a straight line. RSFQ circuits requiring two junctions in series to ground are not treated here [1,2]. The flux shuttle type is chosen for its simplicity with only one junction to ground.

Flux shuttle shift registers with three magnetically coupled clock currents have already been implemented with the Nb-Al_2O_3-Nb technology [3]. They can have extremely low power dissipation of 9nW/bit/GHz [4]. Flux shuttle shift registers with a single clock line are also feasible [5] at the expense of smaller margins than with three clock lines.

A two bit shift register with a directly coupled clock scheme has already been realized with $YBa_2Cu_3O_{7-\delta}$ (YBCO) step edge junctions [6]. In this paper a 4 bit shift register with only one magnetically coupled clock line is presented, because a suitable arrangement of three clock lines in one plane over grain boundary junctions on a bicrystal substrate is difficult. The write and read circuit scheme demonstrated with niobium [3] has been modified for the present YBCO - technology.

II. Circuit description

The equivalent circuit of the proposed shift register cell comprises two loops, the master and the slave as shown in Fig. 1. It differs from the inhomogeneous flux shuttle [7] by the magnetic coupling of the clock line and the kind of biasing. The master comprises two Josephson junctions with the same critical current, $I_{Mn} = I_{Sn} = I_0$, and the inductance L_{Mn}. The characteristic phase of the master $\lambda_M=2\pi L_M I_0/\Phi_0$ is smaller than π. The slave comprises the Josephson junctions J_{Sn}, J_{Mn+1} and the inductance L_{Sn}. The

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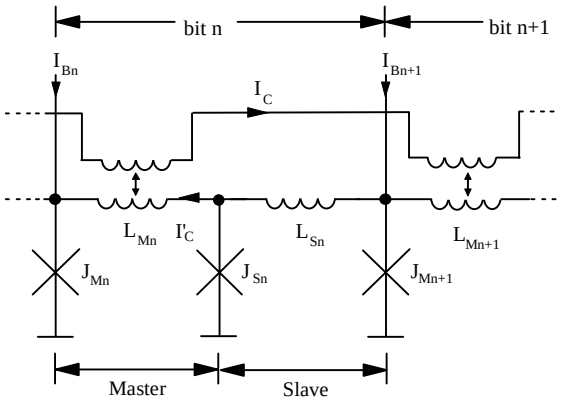

Fig. 1: Equivalent circuit of the n-th shift register cell according to one bit

characteristic phase of the slave λ_S is 2π. The Josephson junctions require a McCumber parameter $\beta=2\pi R_N^2 C_J I_0/\Phi_0 <1$. R_N is the resistance of the junction in the normal conducting state and C_J the junction capacitance of the junctions.

The clock current I_C can be both a sinusoidal signal with a DC offset or a pulse. The clock line is coupled magnetically with the master inductance L_{Mn}. The junction J_{Mn} is biased by the current I_{Bn} to determine the shift direction.

A. Flux Shuttle with one clock line

If a flux quantum, corresponding to a "1", is stored in the slave of the shift register cell n-1 at the rising edge of the clock current I_C, the corresponding ring current, the magnetically coupled clock current I_C' and the bias current I_{Bn} add in the junction J_{Mn}. As the critical current of J_{Mn} is exceeded, the junction switches and the flux quantum in the slave n-1 is destroyed while a new one is generated in the master n. When the clock current I_C has fallen down, no flux quantum is able to exist in the master, since λ_M is smaller than π. As the junction J_{Mn} is biased, the junction J_{Sn} switches, destroying the flux quantum in the master n and writing a new one in the slave n.

If no flux quantum is stored in the slave n-1 at the rising edge of the clock current I_C, the junction J_{Mn} does not switch, so that no flux quantum, i.e. a "0", is shifted.

B. Write and read circuit

The write circuit in Fig. 2 can be implemented with a single junction to ground as in the storage section of the flux shuttle without unduly large parasitic inductances.

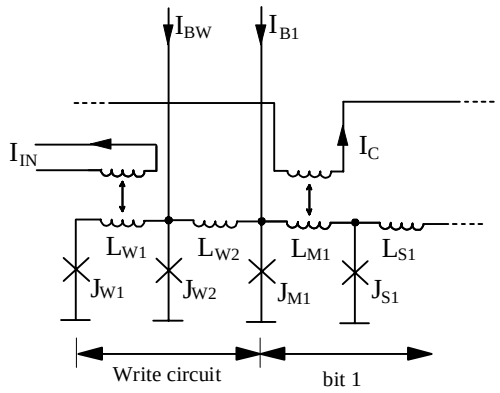

Fig. 2: Write circuit connected to the first stage of the shift register

The input stage consists of two loops, an input loop comprising of J_{W1}, J_{W2} and L_{W1} with $\lambda_{W1} < \pi$ and a storage loop of J_{W2}, J_{M1} and L_{W2} with $\lambda_{W2} = 2\pi$. The input current is coupled magnetically into the input loop, the junction J_{W1} switches and a flux quantum in the input loop is generated. The corresponding loop current adds with the bias current I_{BW} in the junction J_{W2} to exceed its critical current. The junction switches and the flux quantum is transferred into the storage loop. During the next rise of the clock current I_C the information is transferred into the slave of bit 1 of the shift register.

The design of a read out circuit for single flux quanta presents some problems, if Josephson junctions are available only along a straight grain boundary. The measurement of average values of pulse voltages yields a first, but not sufficient, indication of correct logic operation [2,8,9]. For instance the data word 10101010..." would yield the same average output voltage as "11001100...". The SFQ/DC converter of the RSFQ logic family [1] requires small inductances and two Josephson junctions in series to ground, which cannot be realised by the given technology. The stored information could be detected with a two junction interferometer coupled magnetically [10] to the slave loop of a shift register cell. Unfortunately, the present YBCO technology allows for only one superconducting plane with small magnetic coupling between a SQUID and an adjacent shift register cell.

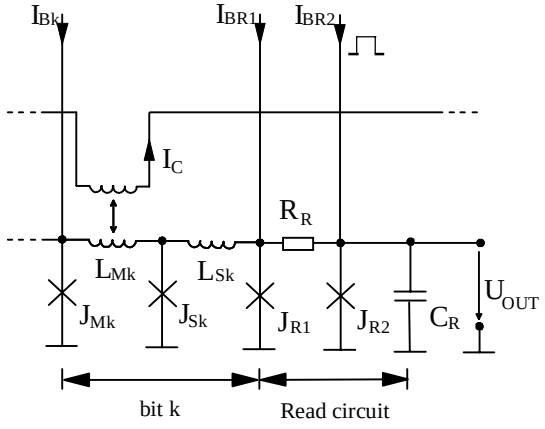

Fig. 3: Read circuit connected to the last shift register cell.

To avoid the difficulties described above, a similar read circuit as described in [4] and sketched in Fig. 3 has been used. The output stage comprises a pulse biased hysteretic Josephson junction J_{R2} and a coupling resistor R_R. As there are no hysteretic junctions with YBCO technology available up to now, a normal grain boundary junction was shunted with a suitable capacitor to achieve a resulting McCumber parameter of about $\beta = 10$.

The coupling resistor avoids a superconducting feedback from the output voltage to the shift register. The characteristic parameter λ_{Sl} of the slave of the last shift register cell k has to be smaller than π, to achieve an asynchronous flux transfer from the master k to the readout circuit.

If a flux quantum is transferred from the last shift register cell to the read circuit, the biased "hysteretic" junction J_{R2} switches into the voltage state. After the bias current pulse I_{BR2} is reduced to zero, the voltage of junction J_{R2} returns into the zero - voltage state with a plasma oscillation.

This circuit allows output voltages up to the I_0R_N product of the junctions, which can be easily detected with the conventional measurement equipment. The maximum frequency for correct digital operation is limited by the plasma oscillation attenuation of the read out circuit. It is in the order of a few GHz.

C. Simulation Results

A four bit shift register with the write and read circuits described above has been investigated by SPICE simulations and designed for grain boundary junctions on bicrystal YSZ substrates with an misorientation angle of 36.8°. A critical current density of 31 kA/cm^2 and a product I_0R_N = 300 µV for an operation temperature of 40 K have been assumed. The minimum line width used for the layout was 5 µm. The simulations and the margin calculations were performed with a realistic layout including all parasitic inductances and all magnetic couplings between the inductances, which cannot be neglected due to the absence of a superconducting ground plane. A simulation result of the complete shift register at a clock frequency of 2 GHz is shown in Fig. 4.

The optimum parameter values have been approximated with the Monte Carlo method of design centering [12] similar as in other locations [13]. The probability of a parameter in its given span is assumed to be equal. Within the span of the parameters a set is chosen according to the Monte Carlo method. SPICE simulations of each parameter set yield an answer whether the digital criterion is fulfilled or not. The difference of the average values of hits and failures is a measure for the direction to search for hits and the difference multiplied by the probability of hits for the amount. A program has been written for an automatic parameter optimisation by design centering, running both on DEC Alpha Workstations and IBM RS/6000 SP parallel computer.

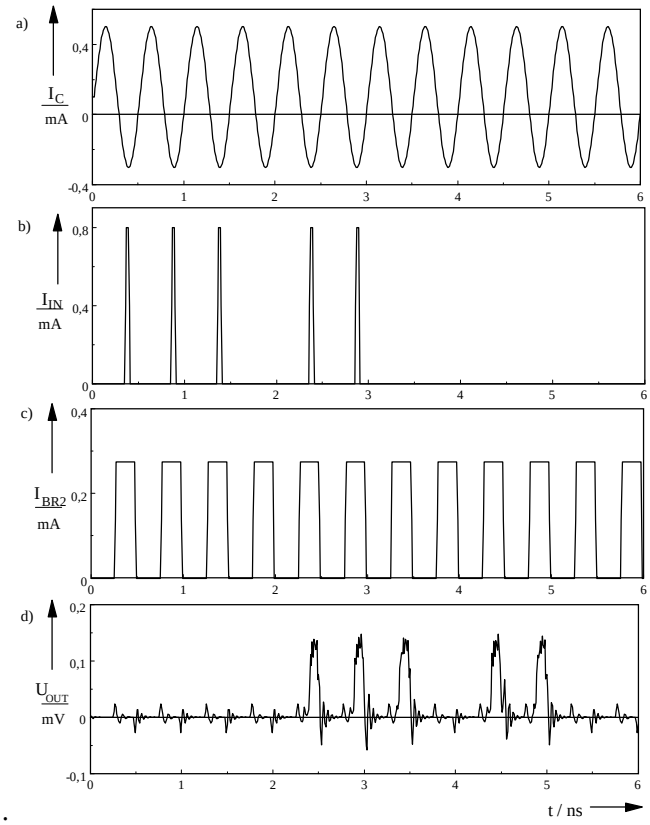

Fig. 4: Simulation result of the four bit shift register including write and read circuit: a) sinusoidal clock current I_C b) input current I_{IN} c) pulsed bias current of the "hysteretic junction I_{BR2} d) output voltage U_{OUT}

Thus, almost optimum parameters are found after a finite number of SPICE runs and are called nominal parameters. The one - dimensional margins Δ_{1n} are calculated in varying one parameter while keeping all other parameters at their mentioned nominal values [11].

For the 2nd of four shift register cells the margins Δ_{1s2} are plotted in Fig. 5. The smallest margin is found for the master Josephson current $-19 \leq \Delta_{1s} \leq +24\%$. The corresponding values for the read circuit and write circuit are $-32\% \leq \Delta_{1W} \leq +27\%$ and $-16 \leq \Delta_{1R} \leq +17\%$, respectively.

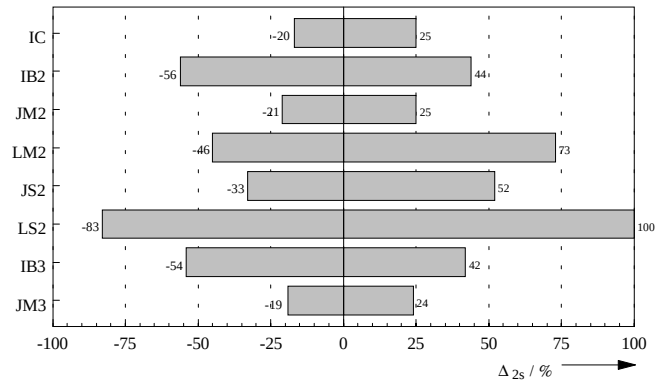

Fig. 5: One - dimensional margins Δ_{1s2} of the second shift register cell

The multi - dimensional margins Δ_n are smaller than the one - dimensional since all parameters are allowed to fluctuate simultaneously around their optimum values in the sense of a multidimensional cube, very similarly as in an actual experiment. The calculated multi - dimensional margins are calculated for the write circuit, the shift register cell and the read circuit were $\Delta_{nW} \leq \pm 21\%$, $\Delta_{nS} \leq \pm 16\%$ and $\Delta_{nR} \leq \pm 11\%$.

To determine the electrical power loss of a shift register cell different contributions have to be taken into account. Power is dissipated in the bias resistors of the bias currents. For bias resistors of 10 Ω the power loss is 0.22 µW per bit. The normal conducting clock line causes a power loss of 6.3 nW per bit. The power dissipation in the terminators of the 50Ω clock line is 9 µW.

The circuit and the layout must be designed to reduce the influence of thermal noise. A Josephson current I_0 = 300 µA at T = 40K correspond to $\Gamma = 2\pi k_B T/(\Phi_0 I_0) = 5.6\ 10^{-3}$. The effect of thermal noise was investigated by simulations with the network analysis program SPICE using a suitable noise model [14]. In some cases it turned out to be helpful to simulate the circuits at elevated temperatures of the noise sources, while all other temperature dependent parameters were kept at the values of the operation temperature to increase the number of failures during the available computation time.

RSFQ shift registers [1] are very sensitive to thermal noise, since only one out of two junctions in series to ground should switch depending on the stored information. Thermal noise can cause false outcomes and the operating range of these circuits is reduced. As in the flux shuttle shift register only one junction over ground is needed and all junctions switch sequentially one after an other as described above, the influence of thermal noise can be kept sufficiently small at 40 K.

III. Fabrication technology

The circuits were fabricated on symmetric 36.8° YSZ bicrystal substrates. A 200 nm thin YBCO film is evaporated by a laser ablation or a sputter process. For a better lattice matching an intermediate 10 nm CeO_2 - film was deposited on the YSZ - substrate. The film is patterned by a standard lithographic process and Ar^+ ion milling. The resistors of the circuit are realised by a 70 nm thin Palladium film, which is dc - sputtered on the structured YBCO plane and patterned by a lift-off process. The insulating layer is achieved in RF - sputtering amorphous $NdGaO_3$ at room temperature to avoid a thermal damage of the orthorhombic YBCO plane. The insulting layer is patterned by a lift-off process to realise the vias between the superconducting plane and the normal conducting Aluminium or gold plane, which is sputtered on top of the insulator. The Al wiring plane is also structured by a lift-off process.

A micrograph of an implemented 4 bit shift register with write and read circuit is shown in Fig. 6.

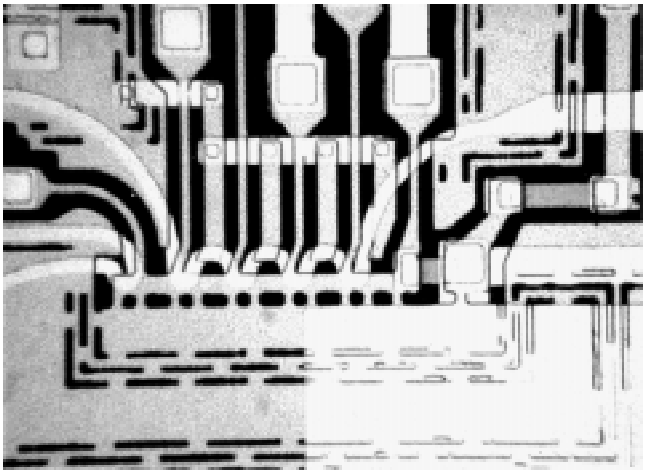

Fig. 6: Flux - shuttle shift register in YBCO - technology

IV. Measurements

Several Josephson junctions, resistors, capacitances and vias have been measured successfully in test structures on the shift register chip. The overall performance of the shift register could not yet been demonstrated completely. However, the technological faults are known and will be eliminated soon.

V. Conclusion

A YBCO technology for integrated circuits with bicrystal Josephson junctions, inductors, resistors, capacitors and a normal conducting wiring plane has been developed. As a test vehicle, a 4 bit flux shuttle shift register has been designed, simulated and laid out for an operation at 40 K. The simulated margins of the flux shuttle are sufficiently large for an implementation of the present technology.

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