Entwicklungsarbeit am Spurendetektor für das CDF Experiment am Tevatron

Zur Erlangung des akademischen Grades eines

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von

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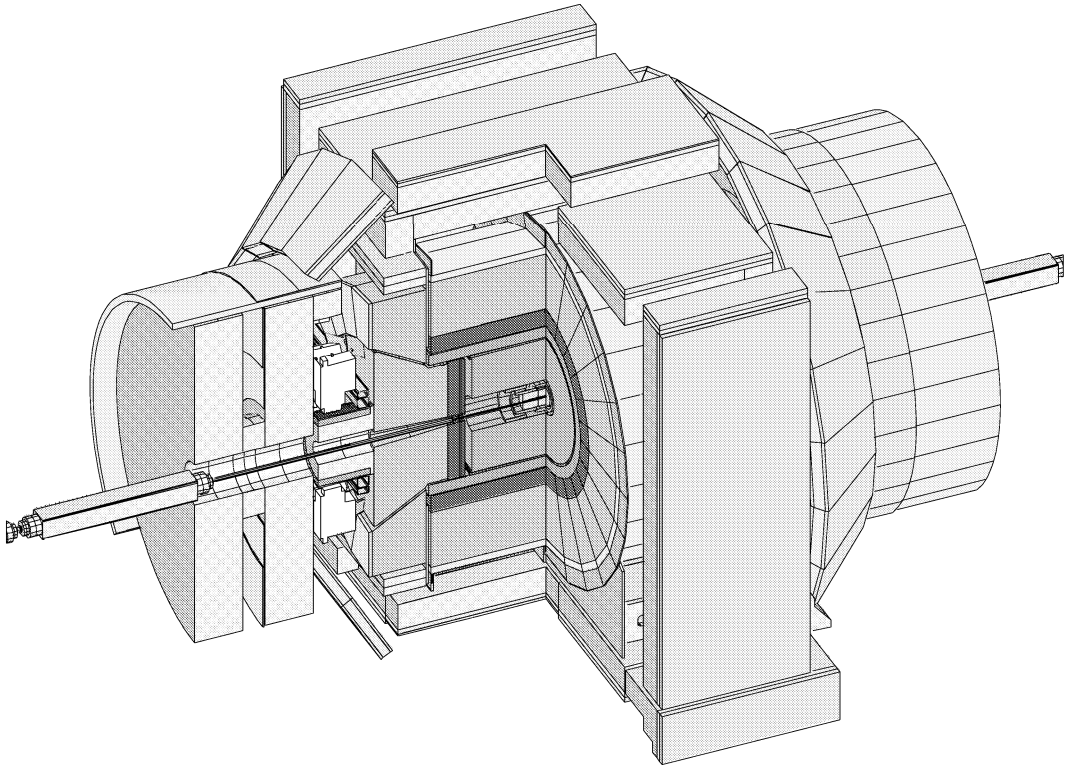


CDF II

TO SARA

Chapter 0

Entwicklungsarbeit am Spurendetektor für das CDF Experiment am Tevatron (Eine Zusammenfassung)

Der energiereichste Protonen — Antiprotonen Beschleuniger der Welt wird für eine neue Datennahme Periode vorbereitet und erweitert. Die Schwerpunktsenergie wird von $\sqrt{1.8}\ TeV$ auf $\sqrt{2.0}\ TeV$ erhöht, die Luminosität auf 2×10^{32} cm$^{-2}s^{-1}$ [2].Das Tevatron wird bis zum Large Hadron Collider (LHC) als einziges Experiment in der Lage sein, das Unitaritätsdreieck und damit die CKM Matrix mit den Messungen

- $sin(2\beta)$ mit $B^0/\bar{B}^0 \longrightarrow J/\Psi K^0_S$
- $|V_{td}/\lambda V_{ts}|$ mit $B^0 - \bar{B}^0$ und $B^0_S - \bar{B}^0_S$ Flavour Oszillationen.
- ($sin(2\alpha)$ in $B^0/\bar{B}^0 \rightarrow \pi^+\pi^-$

vollständig zu bestimmen. Es ist zur Zeit das einzige Experiment, welches die Eigenschaften des Top Quarks präzise messen kann, und in dessen Reichweite auch die eventuelle Entdeckung des Higgs Bosons liegt. Die hohe Energie ermöglicht weiterhin die Messungen an B_s, B_c und Λ_b, Teilchen, welche bei den momentanen b-Fabriken nicht erzeugt werden können.
Die beiden Experimente, der "Collider Detector at Fermilab" (CDF Abbildung 1)[2] und "D0"[4] werden aufgerüstet, um die erhöhte Datenrate verarbeiten zu können. Die Sensitivität wird besonders in Bezug auf die interessanten physikalischen Phänomene stark erhöht. Der totale b-Quark Produktionsquerschnitt von $\sigma_{b\bar{b}} \approx 50\ \mu$b ist wesentlich größer, als der aller anderen aktuellen Experimente. In Bezug auf den gesamten Wirkungsquerschnitt ist er jedoch verschwindend gering: $\sigma_{b\bar{b}}/\sigma_{Tot} \approx 0.001$. Ein Grossteil der interessanten physikalischen Ereignisse enthält jedoch b-Quarks. Dies erfordert eine exzellente b-Identifizierung, verwirklicht durch ein neues System von Spurendetektoren

und einem angepassten Trigger. Das System der Spurendetektoren für CDF wird komplett erneuert, es ist in Abbildung 2 und 3 dargestellt. Die innerste Spurendetektorlage, bestehend aus einseitigen Silizium-Detektoren mit R-ϕ Auslese, wird direkt auf das Strahlrohr gesetzt (Radius = 1.6 cm; Layer00), gefolgt von einem 87 cm langen, aus 5 Lagen doppelseitigen Silizium-Streifen-Detektoren mit 2-dimensionaler Auslese (Radien =2.7 bis 10.7 cm; SVX II). Komplettiert wird das innere Spurensystem durch den "Intermediate Silicon Layers" Detektor (Radius = 20 cm und 28 cm; ISL), einem 195 cm langen zweilagigen Detektor aus doppelseitigen Silizium-Streifen-Detektoren. Der ISL erweitert den aktiven Bereich bis $\eta = 2.0$ und bietet dem Rekonstruktionsalgorithmus in der Region zwischen dem inneren Bereich und der äusseren Driftkammer (COT) zwei zusätzliche Spurpunkte als Ankerpunkt. Mehrdeutigkeiten werden durch diese zusätzlichen Lagen mit Stereo Auslese vermindert. Dieses elaborierte System

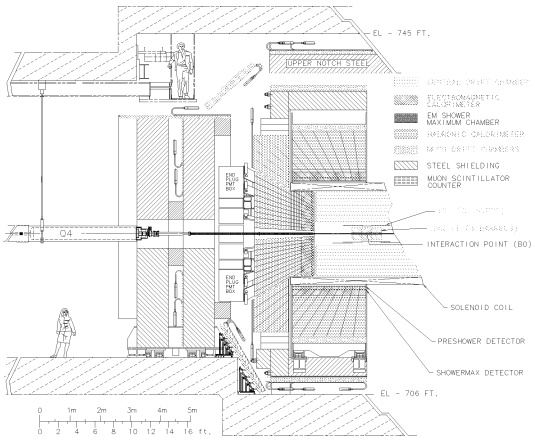


Figure 1: **CDF II.**

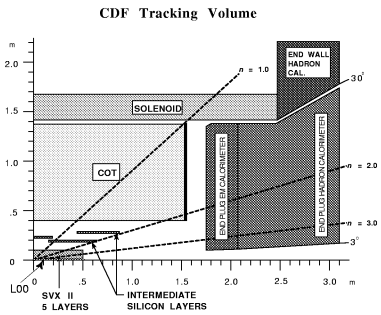


Figure 2: **Das Spurensystem.**

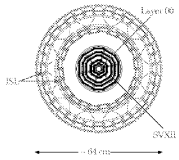


Figure 3: **Das innere Spurensystem.**

ermöglicht eine gute b-Identifizierung.

Detektor Konfiguration	Einzel tag Eff.(%)	Doppel tag Eff.(%)
SVX'+CTC [1]	37.6 ± 1.0	6.9 ± 0.5
SXV II+COT	46.7 ± 1.1	8.7 ± 0.6
SVX II+ISL+COT	60.1 ± 1.0	15.1 ± 0.8

Table 1: *Effizienz ein oder zwei b-Quarks [2] in $t\bar{t}$ Monte Carlo Ereignissen zu identifizieren, bezüglich verschiedener Detektor Konfigurationen ('Tag' bedeutet Markierung).*

[1] SVX' Silicon Vertex Tracker von CDF in der Datannahme Periode '92 - '96 (RUN I);
CTC Central Tracking Chamber (Zentrale Spurkammer aus Run I)

Der Spurendetektor des CDF Experimentes stellt den aktuell größten Silizium Spurendetektor bis zur Verwirklichung des LHC dar. Um die Fläche von etwa 7.5 m^2 Silizium (L00 + SVX II 3.8 m^2 + ISL 3.7 m^2) zu verwirklichen wurden ein Großteil der Detektoren in 6 Zoll Technologie hergestellt. Diese Technologie vergrößert den Arbeitsbereich der Siliziumscheiben von 42 cm^2 auf 100 cm^2. Im Falle von CDF konnten deshalb zwei Sensoren in einem Produktionsvorgang hergestellt werden, 2 identische für den ISL und zwei unterschiedliche für den SVX II Detektor. Dies führte zu einer signifikanten Kostenreduktion. Zum weltweit ersten Mal für die Herstellung von Silizium-Streifen-Detektoren verwendet, gab es jedoch neuartige Probleme, die nur durch Zusammenarbeit aller Beteiligten frühzeitig erkannt und behoben werden konnte. In Abbildung 4 ist die Funktionsweise eines Silizium-Mikro-Streifen-Detektors dargestellt.

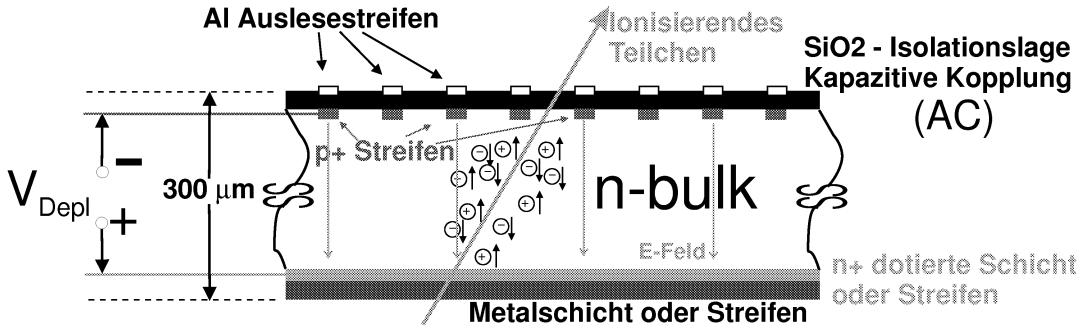


Figure 4: *Prinzip eines Silizium-Mikro-Streifen-Detektors.*
Der Sensor wird durch die Depletionsspannung (V_{Depl}) vollständig von freien Ladungsträgern verarmt. Ein durchdringendes geladenes Teilchen erzeugt freie Ladungsträger, die entlang des E-Feldes zu den p^+- bzw. n^+-Streifen wandern. Dort werden die Ladungen kapazitiv (AC-Kopplung) auf die Auslesestreifen induziert und gelangen schließlich zur Ausleseelektronik.

Alle 6" Sensoren für ISL und SVX II bestehen aus 300 μm dickem, n^--dotiertem Silizium. Die Sensoren sind doppelseitig, die Oberflächen sind in Streifen segmentiert, eine Seite mit p^+ (p-Seite), die andere mit n^+ (n-Seite) dotierten Streifen-Implantaten. Die Aluminium-Auslesestreifen sind durch eine SiO_2 Schicht kapazitiv von der Auslese Strom entkoppelt. Die 3-dimensionale Auslese wird verwirklicht, indem die Streifen auf der n-Seite um 1.2^o gegen die p^+ Streifen ausgerichtet sind. Am Ende einer Reihe von 3 Sensoren (Leiter) befindet sich die Ausleseelektronik. Die Ladungsträgerverarmung (Depletion) am pn-Übergang erfolgt durch hochohmige Widerstände aus Polysilizium (Bias Widerstände; R_{bias}) von einem Kontaktring (Bias Ring) zu den Implantaten führend. Die Streifenisolierung der p-Seite erfolgt durch zusätzliche p^+-Dotierung (p-stop-Design) zwischen den n^+-dotierten Streifen. Die einzelnen Komponenten sind in Abbildung 5 dargestellt.

Design des ISL Silizium-Streifen-Detektor in 6" Technologie.

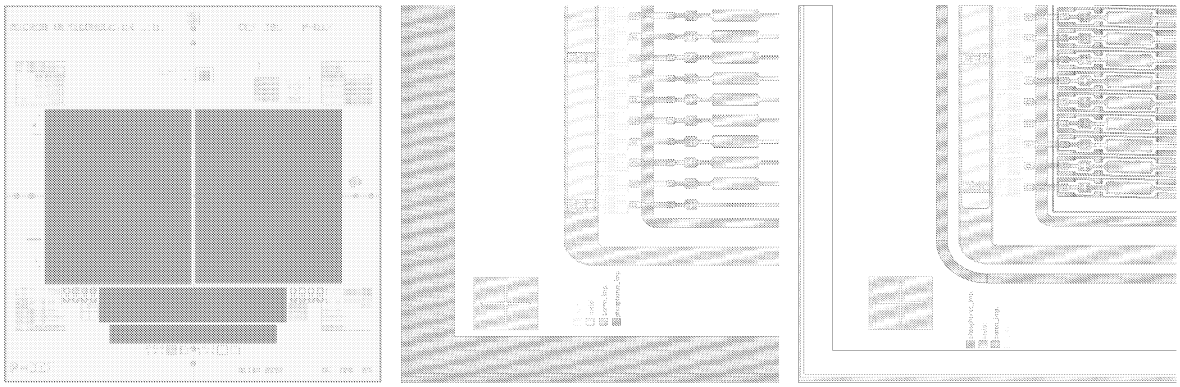


Figure 5: **Der ISL Sensor: Layout (Links) —— Struktur p-Seite (Mitte) —— Struktur n-Seite (Rechts).**

Derzeit (1996 - 1999) ist Micron Semiconductor [28] in England der einzige Hersteller von doppelseitigen 6" Silizium-Streifen-Detektoren. Im folgenden sollen die Problematiken aufgezeigt werden, welche sich bei der Produktion von doppelseitigen Silizium-Streifen-Detektoren in 6" Technologie ergeben:

- **Hoher Leckstrom einzelner Streifen**, herbeigeführt durch Unregelmäßigkeiten in den Implantaten. Spitzen oder fehlende Ecken führen zu 'lokal' hohen Feldstärken und damit zu extrem hohen Strömen.
  Verbesserung der Reinräume und Kontrolle der Staubpartikeldichte verringerten die Häufigkeit dieser Fehler.

- **Bereiche hohen Leckstroms** auf der p-Seite des Sensors, bewirkt durch einen Kurzschluss zwischen dem Implantat und dem 'p-stop' auf der n-Seite. Der n^+-Streifen wird dadurch auf das Potential der Depletionsspannung gehoben und bewirkt damit eine starke Feldverzerrung, welche auch auf die 15 gegenüberliegenden[2] Streifen auf der p-Seite starken Einfluss ausübt. Dieser Defekt entstand durch Staub-Kurzschlüsse oder einem p^+-Implantat Überlauf.
  Verbesserung der Reinräume und Kontrolle der Staubpartikeldichte verringerten die Häufigkeit dieser Fehler.

- **Kurzschlüsse zwischen den Implantaten und den Aluminium-Auslesestreifen** (Pinhole) bewirken eine Strom-Kopplung. Die Ausleseelektronik ist jedoch nach dem Prinzip der Ladungsverstärkung aufgebaut, der entstehende Stromfluss ist nun aber durch die Depletionsspannung und nicht mehr durch kleine Rauschströme bestimmt. Die Folge sind mehrere gestörte Kanäle. Ein solcher Defekt kann ganze

[2]Durch die 1.2^o-Ausrichtung sind es 15 gegenüberliegenden Streifen.

Detektor Bereiche beeinflussen.
Verbesserung wurde durch Optimierung der "nassen" und "trockenen" SiO_2 Prozessierung erreicht.

- **Verminderung der Kopplungskapazitäten am Rande des Sensors.** Eine inhomogene Verteilung der Kopplungskapazitäten ermöglicht keine einheitliche Kalibrierung der Kanäle. Dieses Problem entstand primär durch eine uneinheitliche Metallisierung entlang der Detektorfläche. Der nachfolgende Ätz-Prozess zur Auslesestreifenbildung ätzte aufgrund der verschiedenen Materialdicken, auch unter die Aluminium-Streifen, deshalb entstanden unterschiedliche SiO_2 Schichtdicken.
  Verbesserung wurde durch Neueinrichtung des Metallisierungsprozess, eine Optimierung für 6" Wafer erreicht.

- **Defekte Isolierung zwischen den Auslesestreifen:**

  - **Ionische Kontaminierung:**
    Unreines Stickstoffgas beim Tempern und eine Stahlunterlage beim Passivieren begünstigten die Kontamination des n^--dotiertem Silizium und führten zu stark erhöhter Leitfähigkeit zwischen den Streifen (gestörter pnp Bereich).
    Verbesserung: Austausch der Stahlplatte mit einer Aluminiumplatte und der Wechsel von der "unreinen" N_2 Haus-Gas-Anlage auf ultrareines Gas aus der Flasche (N_2 und Argon) löste das Problem.

  - **Elektrostatische Aufladung:**
    Einige Detektoren (ca. 30) veränderten ihr Verhalten bezüglich der Zwischenstreifenwiderstände nach der Herstellung und der Micron internen Qualitätskontrolle. Die Erniedrigung wurde durch statische Aufladung während des Transports durch Baumwohlfasern in der "neuen" Verpackungsgaze der Sensoren bewirkt. Das Problem wurde vor dem Einbau der Sensoren in einer zweiten Qualitätskontrolle in Karlsruhe erkannt. Alle Sensoren konnten durch Reinigung in de-ionisiertem Wasser wieder in den ursprünglichen Zustand gebracht werden.
    Verbesserung: Schutzmaßnahmen gegen elektrostatische Aufladung, Benutzung elektrostatische Verpackungsboxen und Wiedereinführung der Baumwollfaserfreien Gaze lösten das Problem. Ein zusätzlicher Reinigungsschritt mit de-ionisiertem Wasser wurde eingeführt.

  - **Temporäre Erniedrigung der Zwischenstreifenwiderstände im Bereich der Gaszuflüsse während der Passivierung:**
    Verunreinigungen in den Gaszuflüssen führte zu Bereichen mit niedrigen Zwischenstreifenwiderständen.
    Verbesserung wurde durch gezielte Reinigung der Gaszuflüssen erreicht.

- **Bereiche mit unterschiedlichem Depletionsverhalten:**
  In der Erstqualifizierung durch Micron wurden die Depletionsspannungen $V_{depletion}$ anfangs nur an Teststrukturen (einzelne Dioden, siehe Abbildung 5 links.) an den Seiten der Wafer gemessen. Diese Messung hat stark 'lokalen' Charakter, diverse Inhomogenitäten des spezifischen (elektrischen) Widerstand (ρ) über den kompletten Wafer werden hierbei nicht berücksichtigt. Aufgrund der V-ρ-Abhängigkeit $V_{depletion} = \frac{w^2}{2\epsilon_{Si}\rho\mu}$ (μ: Mobilität; w: Breite der Verarmungszone) führen Inhomogenitäten in ρ zu Unterschieden bei den Depletionsspannungen von 40 V bis zu 100 V zwischen den Messungen an Testdioden und an den direkten Sensoren. Das Betreiben eines Halbleiterdetektors unterhalb der Depletionsspannung führt zu einer Schicht freier Ladungsträger an der Oberfläche des Detektors, im Bereich der Streifen. Das Ergebnis sind stark erniedrigte Zwischenstreifenwiderstände, dies wiederum führt zu einer starken Erhöhung der indivuellen Streifenleckströme, da durch jeden Streifen der Leckstrom aller Nachbarstreifen fließt. Eine solche Erhöhung sollte also direkt in der Erstkontrolle bei Micron gefunden werden, selbst wenn solche Erscheinungen nur in bestimmten Bereichen auftreten. Die Halbleiter-Halbleiter-Übergänge sind allerdings aufgrund der unterschiedlichen Strukturen auf n- und p-Seite (p-Seite: p^+n^- und n-Seite: n^-n^+) unterschiedlich effektiv. Die vollständige Depletion wird auf der n-Seite erst viel später als auf der p-Seite erreicht. In Karlsruhe werden die Depletionsspannungen der einzelnen Detektoren und nicht der Testdioden gemessen. Die Streifenleckströme auf der n-Seite werden *ausschließlich* in Karlsruhe gemessen. Auf der n-Seite wurden isolierte Bereiche mit stark erhöhten Leckstrom gefunden, es wurden Werte im μA Bereich anstatt pA gemessen. Die Zwischenstreifenwiderstände sind außerdem stark erniedrigt, ebenso wie die Bias Widerstände, welche jetzt ein paralleles Netzwerk bilden. Die Bereiche sind auf Inhomogenitäten des spezifischen Widerstands der Siliziumwafer zurückzuführen.
  Lösung: Die Depletionsspannungen werden jetzt auch bei Micron direkt an den Sensoren gemessen, auch Leckstrommessungen auf der n-Seite wurden eingeführt. Die Sensoren von Januar 1999 bis November 1999 wurden reklassifiziert und ca. 50 neue Detektoren werden momentan produziert.
- **Schlechter Kontakt der Mess-Pads zu den Streifenimplantaten.**
  Um Leckströme zu messen und Pinholes zu finden, müssen die Streifenimplantate einen direkten Zugang besitzen. Es werden Aluminium Mess-Pads auf dem Detektor aufgebracht und direkt leitend mit den Implantaten durch Unterbrechung der isolierenden SiO_2-Schicht verbunden. Bei einigen Detektoren führten schlechte oder fehlende Kontakte zu Fehlmessungen, alles wies auf einen Kontaktfehler hin. Die mehrfachen Überprüfungen der Messergebnisse führten vereinzelt sogar zu Kratzern auf den Detektoroberflächen.
  Lösung: Es existiert noch eine zusätzliche Diodenstruktur zu den Implantaten führend (der Guardring: verantwortlich für die Feldformung im Außenbereich). Durch Anlegen einer Spannung werden die fehlerhaften Kontakte 'durchgebrannt'.

- **Stark erhöhte Bias Widerstände:**
  Produktionsfehler und Ölkontamination[3]führten zu einem zusätzlichen Ätz-Prozess, dabei wurden die Breiten der Polysilizium Widerstände verringert. Dies führte zu erhöhten Bias Widerständen (9 - 11 MΩ anstatt 4 - 6 MΩ).
  Lösung: Die Sensoren werden im Experiment eingesetzt, die erhöhten Widerstände haben außer einer geringfügig anderen Entladezeit (RC-Glied) keine negativen Auswirkungen. Das Rauschen ist für erhöhte Widerstände mit $\sim \sqrt{kT/R}$ sogar geringer. Die Prozessierung wurde verbessert und Ölrückstände beseitigt.
- **Stark erniedrigte Bias Widerstände:**
  Einige Polysilizium Widerstände wurden zu stark implantiert, was zu einer Erniedrigung führte (0.9 - 1 MΩ).
  Verbesserung: Die Detektoren wurden nicht akzeptiert, die Erhöhung des Rauschens wäre zu groß. Die Anlagen wurden neu justiert.

Die endgültige Auswirkung der Streifendefekte sind in Abbildung 6 dargestellt. Alle angeschlossenen Kanäle haben ein erhöhtes Rauschen, gegenüber nicht angeschlossenen Kanälen. Das Rauschen wird durch die angehängte Kapazität, den noch existenten Dunkelstrom und den Bias Widerstand erzeugt. Streifen mit erhöhten Leckströmen besitzen ein stark erhöhtes Rauschen und werden in der endgültige Auslese nicht berücksichtigt. Kurzschlüsse zwischen zwei Auslesestreifen besitzen die doppelte Kapazität eines Einzelstreifens und haben deshalb ein erhöhtes Rauschen, das eigentliche Problem besteht hier aber in der Chiparchitektur; die beiden Auslesekanäle befinden sich auf gleichem Potential und das Reset-Signal des einen Kanals stört das des anderen. Bei Streifen mit Unterbrechungen wird nur ein Teil des Kanals ausgelesen. Der Strom durch ein Pinhole wird allerdings nicht mehr durch den Leckstrom bestimmt, sondern durch den Stromkreis, der für die Depletionsspannung verantwortlich ist. Starke Verzerrungen der Signale werden erzeugt, auch auf den Nachbarstreifen. Diese Kanäle müssen vor dem ersten Anschluss an die Ausleseelektronik identifiziert werden, da die entstehenden Ströme oftmals den Vorverstärker zerstören.

Im Rahmen einer kollaborationsinternen Qualitätskontrolle in Karlsruhe wird der Gesamtleckstrom und die Leckströme, Pinholes und Bias Widerstände aller Streifen beider Seiten eines einzelnen Detektors gemessen. Für einen Großteil wurden auch die Zwischenstreifenwiderstände gemessen. Die Depletionsspannungen wurden für jeden Detektor mittels der Kapazitätsabhängigkeit von der Depletionsspannung bestimmt: $C_{bulk} = \sqrt{\frac{\epsilon}{2\mu\rho V_{bias}}}$. Bei einigen Detektoren wurden auch die Kopplungskapazitäten und Zwischenstreifenkapazitäten gemessen.

[3]Die Firma IBS in Frankreich, zuständig für die Streifenimplantierung, war für diesen Fehler verantwortlich.

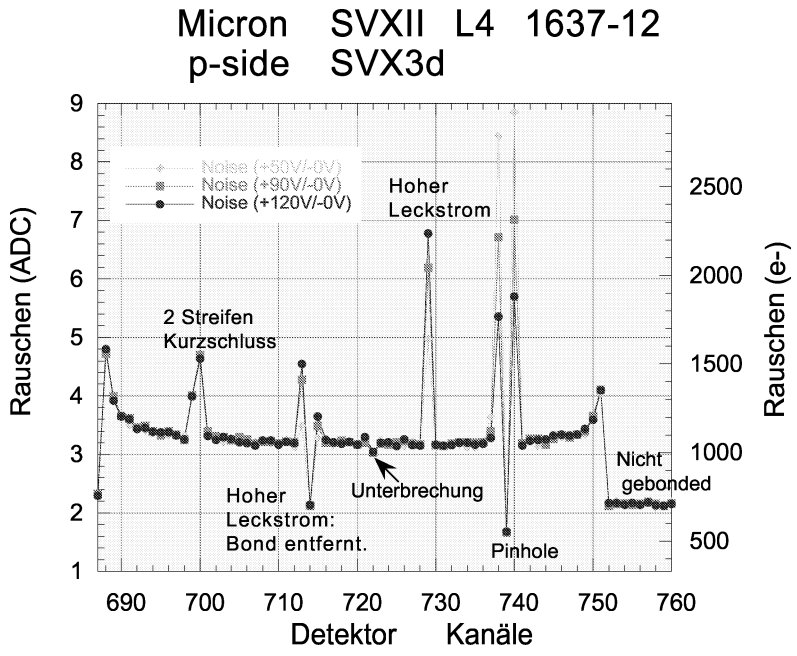


Figure 6: **Auswirkungen der Streifenfehler auf die SVX3 Auslese.***[22]*

Im Rahmen dieser Arbeit wurden auch die Montage-Vorrichtungen für die Silizium-Trägerstrukturen, die Leitern und Module entwickelt und hergestellt. Die Problematik bestand darin, eine Präzission von ± 1 μm in X,Y-Richtung und von ± 10 μm in der Planarität zu erlangen, um im entgültigen Detektor eine wesentlich bessere Positionierung der Siliziumdetektoren zu erhalten, als die geplante Spurauflösung von 25 μm. Besonders die Planaritätsbedingung ist bei der Gesamtlänge eines Moduls mit 6 Sensoren von 50 cm nicht trivial zu maschinieren. Die Grundidee besteht darin, die Präzission der Positionierung nur mit Hilfe der Siliziumdetektoren und des Elektronikhybrids zu erlangen. Die Kohlefaserrahmen dienen lediglich zur Versteifung. Ausschließlich die ausgerichteten Elektronikhybride werden mit der endgültigen Trägerstruktur verbunden. Ihr Präzissionsloch dient als zentraler Punkt, auf den die Sensoren hin ausgerichtet werden. Mittels zweier Linear-Verschiebetische, und einem Rotations-Verschiebetisch werden die einzelnen Sensoren unter ständiger Kontrolle einer 3D Koordinaten-Messmaschine ausgerichtet. Abbildung 7 illustriert die Montage einer ISL Leiter mit 3 Sensoren und einem Hybrid. Nachdem die Sensoren und das Hybrid gegeneinader ausgerichtet wurden, wird der unterhalb liegende Kohlefaserrahmen mit Klebstoff versehen und mittels zweier Lineartische (in Z-Richtung) angehoben. Abbildung 8 zeigt die Vorrichtung, um zwei Leitern zu einem Modul zu verbinden.

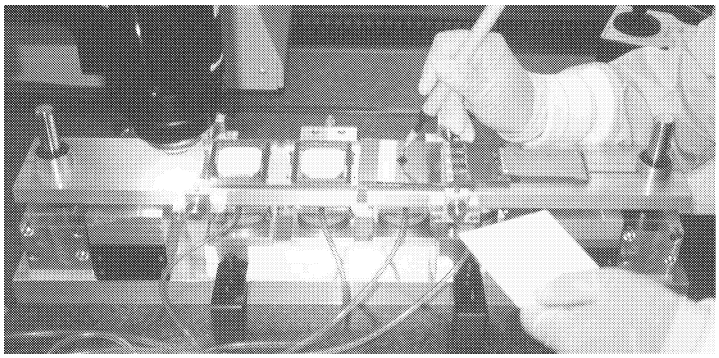


Figure 7:
Bau einer Leiter – Schritt 2: Auflage eines Silizium-Sensors.

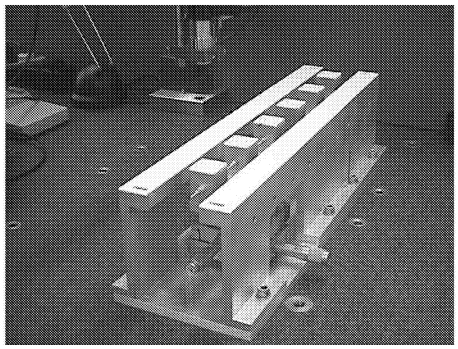


Figure 8:
Montage-Vorrichtung für ein Modul (6 Sensoren).

Im Rahmen dieser Arbeit wurde der momentan weltweit größte Silizium-Microstreifen-Vertex-Detektor verwirklicht, in Kollaboration mit den Siliziumexperten und Technikern von CDF. Einige Erfahrungen können direkt auf das Großprojekt CMS übertragen werden: Die Konstruktion eines Vertexdetektors in einem Kolliderexperiment birgt wesentlich mehr Schwierigkeiten als ein normaler Spurendetektor in einem Fix-Target-Experiment. Das zugehörige Design muss alle Kabel- und Kühlleitungen einplanen. Das Design der Sensor Trägerstrukturen muss so einfach als möglich gehalten werden, um eine zuverlässige Automatisierung der Konstruktion, des Klebens und des Bond-Vorgangs zu gewährleisten. Der Bond-Vorgang kann nur nach einer sehr sorgfältigen Auswahl der Bondparameter automatisiert werden, um Schäden zu vermeiden. Die komplette Elektronik muss rechtzeitig entwickelt, und in ausreichender Anzahl am Anfang der Konstruktion vorhanden sein. Der Schritt von 4" auf 6" Technologie ist machbar, allerdings müssen alle Verfahrensschritte der Herstellung angepasst werden, um eine homogene Prozessierung über die gesamte Fläche zu gewährleisten. Ein besonderes Augenmerk sollte auf das Silizium Basismaterial gelegt werden, Inhomogenitäten können leicht zu späteren Ausfällen führen (niedere Resistivität führt beispielsweise zu erhöhten Depletionsspannungen). Von der Verwendung doppelseitiger Siliziumdetektoren in großen Stückzahlen sollte abgesehen werden. Alle Hersteller hatten technische Probleme und eine geringe Ausbeute. Die zuletzt georderten einseitigen Detektoren für den Layer 00 wurden zuerst fertig gestellt. Es müssen auf jeden Fall *alle* Detektoren auf Pinholes und Streifen mit hohen Leckströmen getestet werden, als Minimumanforderung würde ich sagen jeder dritte bis vierte Streifen muss getestet werden um Defektbereiche auszuschliessen. Im Falle doppelseitiger Sensoren müssen beide Seiten getestet werden. Alle Teile müssen in einer webbasierten Datenbank katalogisiert werden, damit jeder Beteiligte jederzeit direkten Zugriff auf alle verfügbaren Informationen hat [58]. Letztendlich muss der Zeitplan die Konstruktion großzügig berechnet werden, da immer wieder benötigte Teile nicht rechtzeitig zu Verfügung stehen.

Zusammenfassend kann man sagen, dass die Realisierung eines 270 m^2 großen Silizium-Spuren-Detektors im Rahmen der CMS Experimentes in einem vernünftigen Zeitraum möglich ist. Folgende Rahmenbedingungen sollten beachtet werden:

- Einseitige Detektoren
- Einfaches Modul Design
- Automatisierung
- Eine genügend große Anzahl von Reinräumen mit Koordinaten-Meßmaschinen und Bondern wird benötigt.

In der folgenden Tabelle ist der aktuelle Zeitplan wiedergegeben (12/1999):

ISL fertig	7/26/2000
SVX II fertig zum Einbau in den ISL	19.9.2000
(SVXII und ISL) fertig zum Einbau	13.11.2000
Zentraldetektor fertig zum Einbau	8.1.2001
CDF: Bereit für die erste $p\bar{p}$ Kollision	1.3.2001
LHC	2005

Bis zur Realisierung des LHC wird die CDF Kollaboration noch einige relevante Ergebnisse in der Hochenergiephysik hervorbringen.

Das Ziel dieser Arbeit, die Erweiterung des 'Collider Detector at Fermilab (CDF)' zu unterstützen wurde, durch die Mitentwicklung des 'Intermediate Silicon Layers Detector (ISL)' und des gesamten Inneren Silizium Spurendetektors erreicht. Ein weiterer Beitrag war die Mitentwicklung des 'Consumer Online Monitoring Software' Paketes, welches im laufenden Experiment die Datenintegrität überwacht, und wichtige Histogramme und Tabellen über eine schnelle Socketverbindung und das 'World Wide Web' allen Kollaborationsmitgliedern in Echtzeit zugänglich macht (Bsp.: Die Triggeraktivitäten (TRIGMON), Spurinformationen der inneren Siliziumdetektoren (SVX), Physikalische Ereignisse (PHYSMON), die Luminosität (LUMON), etc.).

Contents

Chapter 1

Introduction

Silicon, the element, which revolutionized the development of electronics, is known as an important and multiusable material, dominating todays electronic technology. It's properties are well investigated and today well known. Silicon is used in solar cells, computers and telecommunications. Since the Sixties semiconductors have been used as particle detectors. Initially they were operated in fixed–target experiments as calorimeters and as detectors with a high precision track reconstruction. Since the Eighties they are widely used in collider experiments as silicon microstrip or silicon pixel detectors near the primary vertex. Silicon sensors have a very good intrinsic energy resolution: for every 3.6 eV released by a particle crossing the medium, one electron-hole pair is produced. Compared to 30 eV required to ionize a gas molecule in a gaseous detector, one gets 10 times the number of particles. The average energy loss and high ionized particle number with 390 $eV/\mu m \sim 108\ (electron-hole\ pairs)/\mu m$ is effectively high due to the high density of silicon. These detectors allow a high precision reconstruction of tracks, primary and secondary vertices, which are especially important for b flavour tagging.
The Tevatron and its detectors are being upgraded for the next data taking run starting in 2001 (RUN II). The Collider Detector at Fermilab (CDF) [2] for the upcoming Run II and its upgraded components are described in chapter 2. The main upgrade project is the design and construction of a completely new inner tracking system. It consists of the Layer00 detector (a single sided silicon sensor resting on the beam pipe), the SVX II (a double sided 5 layer silicon detector) and the 2 layer Intermediate Silicon Layers Detector (ISL). The ISL is presently being built by a collaboration of Bologna, Fermilab, Karlsruhe, LBL, Padova, Pisa, and Tsukuba. The co-development of the ISL [6] together with the whole inner tracking system is my main contribution to the project, hence is described in detail in chapter 3. It is presently, with a length of $\sim$2 m and $\sim$7.5 m^2 silicon surface, the largest silicon tracking system until the construction of CMS[11] and ATLAS[10], the main detectors at the Large Hadron Collider at CERN.
I give an overview of the physics, benefiting mainly from the tracking system and its elaborate b-tagging capabilities in chapter 4.

Apart from Layer00, the silicon tracking system consists completely of double sided sensors. CDF is the first collider experiment using a large significant number of double sided silicon microstrip sensors. For the first time in a tracking detector, approximately half of the sensors are produced in 6" technology[1]. The basics of silicon material characteristics are described in chapter 5, whereas a more detailed overview of silicon microstrip detectors, their working principle and design is given in chapter 6. This work contributed to the realization of these devices and their quality for the final detector. Starting by evaluating the prototypes of all the three potential suppliers (chapter 7), Micron Semiconductors [28], Seiko Instruments [30] and Hamamatsu Photonics [29], the quality control of the 6" Micron sensors was conducted in Karlsruhe and is described in chapter 8. Together with the design of silicon sensors, I present the tests of the production-grade silicon detectors in chapter 9. In particular the problems and solutions from the manufacturing of double sided silicon sensors in 6" technology is described. Finally the construction of the complete detector is described in chapter 10. All mounting fixtures for the module construction were designed and constructed in Karlsruhe. A conclusion and an extrapolation to the CMS experiment at the LHC is given in chapter 11.

Since I devoted a large amount of time to the development and programming of the 'Consumer Online Monitor' software package, a new framework to distribute data summaries online in real time is outlined in appendix E.

[1] 6" refers to the size of the silicon wafer.

Chapter 2

The Tevatron and CDF II

2.1 The Tevatron

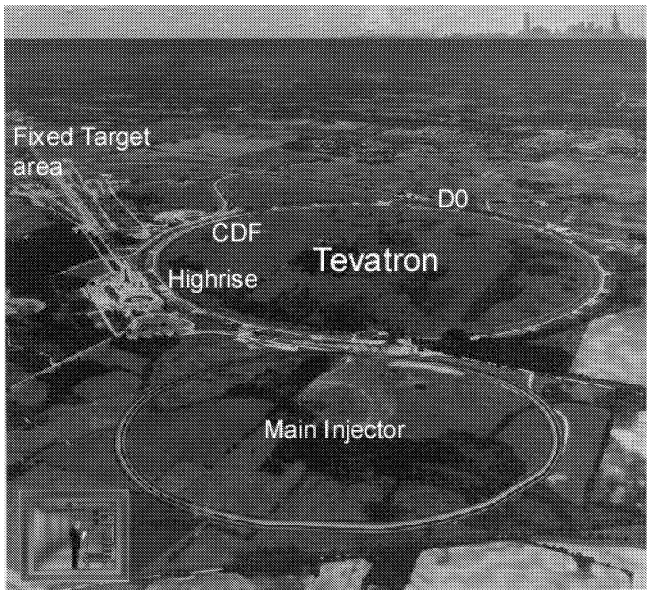


Figure 2.1: **Aerial View of the Tevatron.**
CDF and D0 [4], the two main experiments can be seen at the perimeter of the Tevatron ring. The ring structure on the lower half shows the new structure mainly responsible for the luminosity increase.
The skyline in the distance is Chicago, Illinois.
The site is a governmental natural preserve, where many deer, countless wild geese, raccoons, coyotes, beavers and some bisons reside.

Currently the Tevatron, the world's most powerful accelerator, a proton-antiproton collider with a circumference of about six kilometers is being upgraded for the upcoming Run II starting in 2001. The stated goal of the initial phase[1] of 2 years of Run II is the accumulation of 2 fb^{-1} at $\sqrt{s} = 2.0$ TeV, using luminosities up to 2×10^{32} cm$^{-2}s^{-1}$ [2]. The modest increase in energy from $\sqrt{s} = 1.8$ TeV to $\sqrt{s} = 2.0$ TeV has little impact on the detector performance, but a major impact on physics (e.g. increasing the $t\bar{t}$ yield by 40%). The luminosity upgrade is mainly achieved by introducing the new Main Injector, which can be seen in the aerial view in picture 2.1 and the Recycler

[1]The new goal is 10 fb^{-1} and more.

Ring. An increased number of bunches and shorter time between crossings require new detectors with newly designed readout electronics and data storage. Detectors with a long collection time experience pile-up. The trigger and readout latency requires a pipelined readout. One of the major concerns for the upgrade is the new time structure, the other is a better tracking detector and better calorimetry. A comparison of run conditions is shown in table 2.1 [1]. The acceleration scheme is similar to the last run. The protons are accelerated by a Cockcroft-Walton accelerator to 750 keV and fed into a linear accelerator. The 400 MeV linear accelerator of 150 m length feeds the Booster. This 8 GeV synchrotron ring injects protons into the Main Injector. The protons and antiprotons are pre-accelerated to 120 GeV in the Main Injector and fed into the Tevatron. To produce the antiprotons some of the protons from the Main Injector are directed to a tungsten target. The antiprotons from the resulting $p\bar{p}$ pairs are collected in the Debuncher where the antiproton beam is stochastically cooled. The antiproton beam is monochromatic when fed into the Main Injector. The complete accelerator sequence is visualized in figure 2.2. The Tevatron is currently the only accelerator capable of producing top quarks, and will remain the only one until the Large Hadron Collider (LHC) turns on.

	Run IB	Run II
p per bunch	2.3×10^{11}	2.7×10^{11}
$\bar{p}$ per bunch	5.5×10^{10}	5.5×10^{10}
Bunches	6	36 (108)
Energy	900 GeV	1000 GeV
Luminosity	1.6×10^{31}	$1.0\ (2.0) \times 10^{32}$
Bunch spacing	3500 ns	396 ns (132 ns)

Table 2.1: **Operation conditions of the Tevatron for Run 1B and Run II[2].**

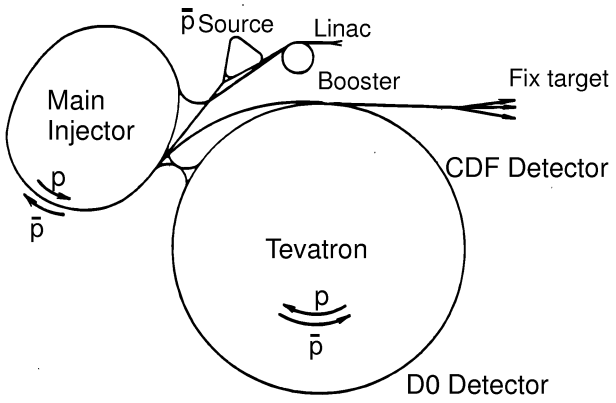


Figure 2.2: **The Fermilab accelerator complex – $p\bar{p}$ acceleration.**

[2]The Tevatron design targets 2 sets of operating conditions: 296 ns and 132 ns bunch spacing

2.2 The Collider Detector at Fermilab

The Collider Detector at Fermilab (CDF) has recorded an integrated luminosity of 130 pb^{-1} on tape with a delivered integrated luminosity of 175 pb^{-1} in the years 1992 to 1996. Together with the D0 [4] collaboration the top quark was discovered in 1994/95 [41]. In 1998 B_C was discovered [40]. CDF has published the first measurement of the CP-violating parameter $sin2\beta$ from $B^o/\bar{B}^o \rightarrow J/\Psi K_s^o$ decays [47]. The Tevatron is the only machine capable of producing a vast number of B_S and Λ_B until the LHC turns on. According to the new conditions at the Tevatron the Collider Detector at

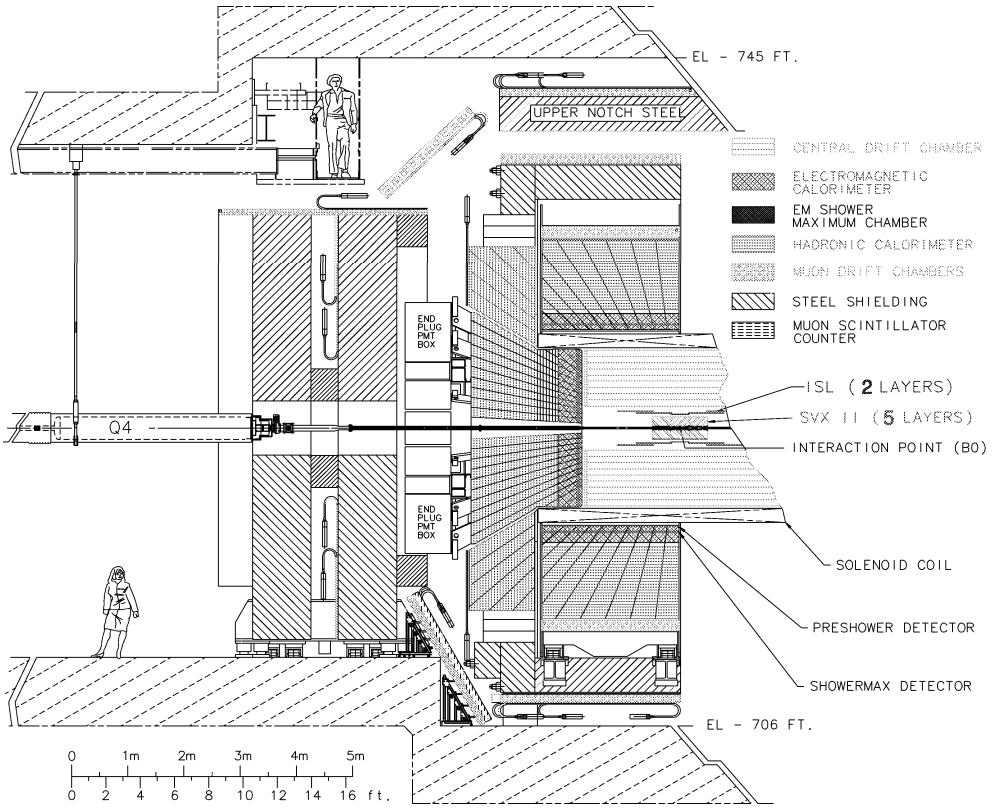


Figure 2.3: *Elevation view of half of the CDF II detector.[2]*

Fermilab is currently being upgraded. Figure 2.3 shows the new upgraded detector for Run II, a conventional multi purpose hadron collider detector. Starting in the center, we have the beryllium beam pipe, followed by the inner tracking system, consisting of three silicon subdetectors Layer 00, SVX II and ISL encompassed by the open cell drift chamber. The tracking volume rests completely inside the 1.41 T solenoid. The calorimeter, divided into the electromagnetic and hadronic part, is located outside of the solenoid. Outside the solenoid return yoke we finally have drift chambers for muon detection.

2.2.1 Tracking System

Efficient precision charged particle tracking is mainly important for CDF analysis technique. Reconstruction for both high p_T (m_W) and low p_T ($B \rightarrow J/\Psi K$) is required. The combination of track, calorimeter and muon chamber information with an excellent purity at both the trigger and offline level is possible. Precision and efficient b-tagging is essential for top physics and new phenomena searches. The CDF II tracking system consists of an inner silicon vertex tracking system and a large drift chamber. The Inner Tracker consists of a very inner layer (Layer 00 at 1.6 cm), glued to the beam pipe, a five layer silicon detector (SVX II at R= 2.7 to 10.7 cm) with two-dimensional readout in each layer. It is encompassed by a third two layer silicon detector (ISL R= 20 and 28 cm) and finally an 8 layer open cell drift chamber (COT at R = 44 cm - 132 cm). The full tracking volume can be seen in figure 2.4 and figure 2.5 giving an expanded view of the inner part. The inner and outer tracking systems are capable of standalone tracking. This enables track–track matching instead of the normal track–spacepoint fit. The COT gives Level-1 trigger information and the inner silicon tracking system provides Level-2 information.

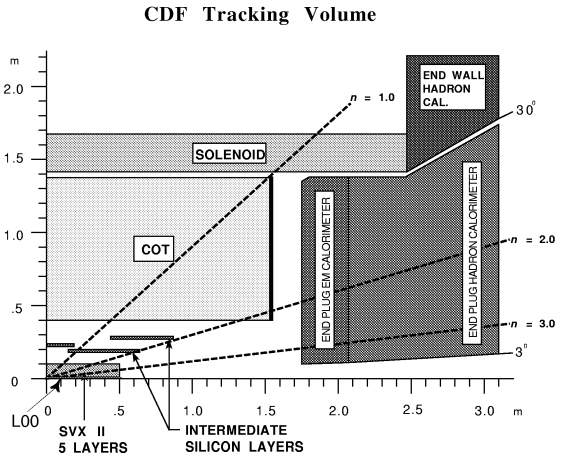


Figure 2.4: **Longitudinal View of the CDF II Tracking System.**

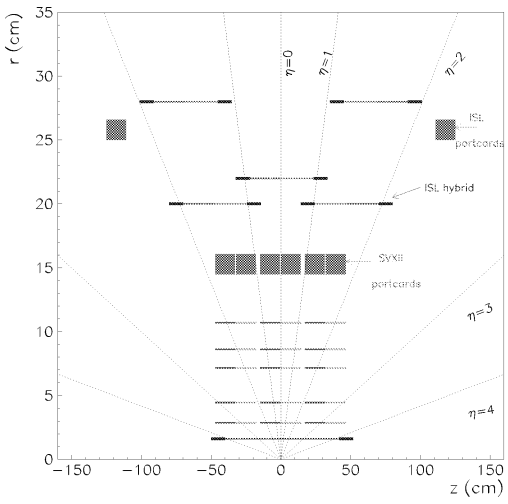


Figure 2.5: **Layout of the *Inner* Tracking System.**

Silicon Vertex Detector (SVX II)

The SVX II is divided into twelve wedges in $r\phi$ and in 3 barrels in rz (beam axis), with a length of 29 cm each. This results in a total length of 87 cm. It has 5 double-sided silicon layers measuring the $r\phi$ and rz coordinates. Three layers (0, 1 and 3) have 90^o stereo angle, allowing high-resolution rz measurements, layers 2 and 4 have a 1.2^o stereo angle. Figure 2.4 and 2.5 show the location of the ISL and the SVX II detector. Figure 3.2 on page 19 shows the embedding in the ISL. The SVX II replaces the former SVX —a 4 layer, single sided silicon microstrip detector.

Intermediate Silicon Layers (ISL)

The Intermediate Silicon Layers 5 and 6 consist of double sided silicon strip detectors measuring both the $r\phi$ and rz coordinates. The strips on one side of the wafers are parallel to the beam axis (rz axis), while the strips on the other side are tilted by 1.2^o. This allows the measurement of the rz coordinate with low ambiguity[3]. The ISL layers are mounted at the radii 20 cm and 28 cm. The overall length of the ISL is 195 cm, covering the pseudo-rapidity region $\mid \eta \mid \leq 2$. A more detailed description is given in chapter 3.

Central Outer Tracker (COT)

The COT is an open drift chamber with an inner radius of 44 cm, an outer radius of 132 cm and a coverage in η up to $\mid \eta \mid \leq 1$. It replaces the CTC (Central Tracking Chamber), used in Run I. Four axial and four stereo 'superlayers' will provide 96 measurements[4], resulting in a total of 2520 drift cells and 30240 readout channels. The different wire angles with respect to rz in each 'superlayer' are $+3^o$ 0 -3^o 0 $+3^o$ 0 -3^o. The location is shown in figure 2.3 and 2.4. The main changes in the upgrade are the small drift cells with a maximum drift distance of 0.88 cm and fast gas, to limit drift times to less than 100 ns. The readout is realized via a pipelined TDC[5] system. The COT is also equipped with the possibility to measure dE/dx for particle identification. The measurement is complementary to the Time-Of-Flight method; both separation powers are displayed in figure 2.9. A more detailed description is given in [2].

[3]The angle of 1.2^o allows to connect strips of several consecutive sensors to one single electronic readout channel, as opposed to layers with a stereo angle of 90^o, where multiple strips are connected to one routing line, hence to one readout channel.

[4]One 'superlayer' provides 12 measurement

[5]TDC: Time to Digital Converter

2.2.2 Beyond the Baseline

Two additional subdetectors to improve tracking and particle identifications were proposed in [5]. The additional silicon layer (Layer 00) and the new Time-Of-Flight (TOF) are displayed in figure 2.6 and 2.8.

Layer 00

A 8-wedge layer is mounted directly on the Beryllium beam pipe with single sided silicon microstrip sensors, each 10 cm long. The mechanical structure is shown in figure 2.6. The length of Layer 00 is approximately 80 cm, its average radius is 1.6 cm (see figure 2.5). The extremely small distance to the beam spot will greatly improve the impact parameter resolution (see figure 2.7). The usage of low-mass silicon strips minimizes multiple scattering effects in Layer 00. Silicon is supplied by Hamamatsu Photonics.

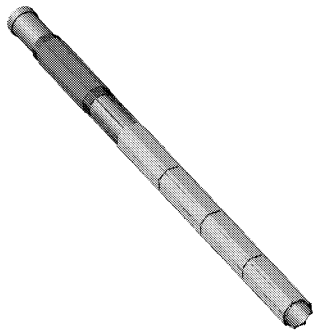


Figure 2.6: **One half of Layer 00.** *The two silicon barrels are each 40 cm long, with electronics in the forward region.*

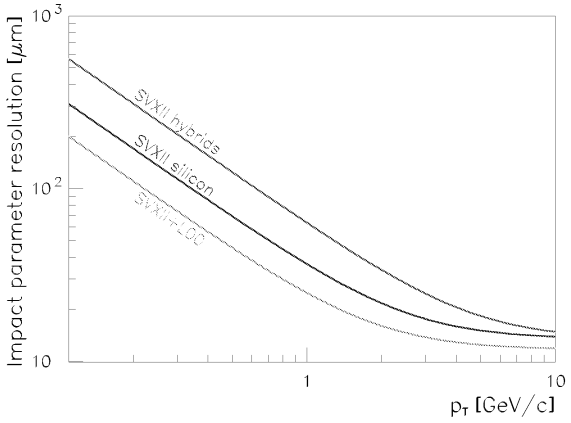


Figure 2.7: *Impact parameter resolution of the inner Tracking system for the different configurations [5].*

Time of flight

The Beyond the Baseline Proposal also suggests a Time-Of-Flight detector (TOF), installed inside the solenoid coil directly outside the Central Outer Tracker (COT) at a radius of 140 cm (see figure 2.8). The TOF consists of 216 scintillator bars (Bicron 408), 3 m in length. Every bar has a fine mesh 19-stage 1.5 inch Hamamatsu photomultiplier tube mounted to each end. The TOF will extend CDF's capability to do particle identification. This will increase CDF II's sensitivity to CP–violation and B mixing. The capability to identify kaons is ultimately important for the measurement of B_S mixing. In the measurement of CP asymmetries b flavor tagging is a crucial component. The TOF will improve the Same-Side tagging technique and also a tagging technique, based on opposite-side kaons identification by selecting pions over kaons (see chapter 4.1).

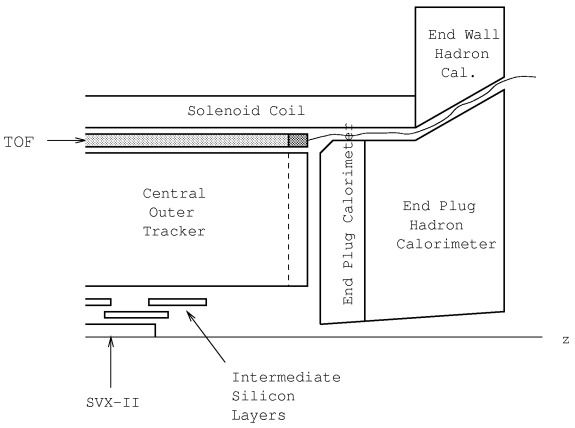


Figure 2.8:
Side view of CDF II showing the location of the **Time-Of-Flight** *subdetector.*

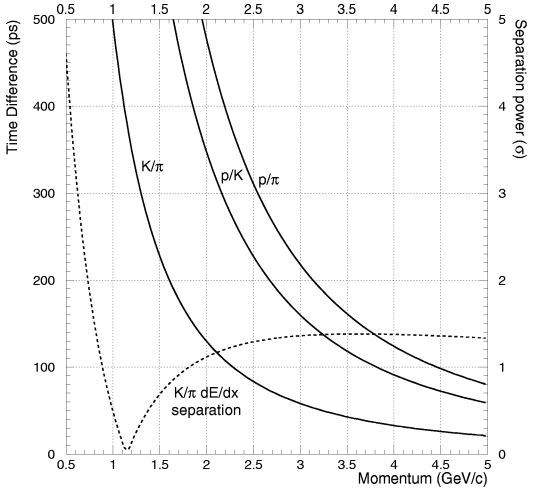


Figure 2.9: **Particle identification with dE/dx and with Time-Of-Flight.**
Time difference as a function of momentum between K/π, p/π and K/p traversing a distance of 140 cm, expressed in ps and separation power, assuming a resolution of 100 ps. The dashed line shows the K/π separation power from the dE/dx measurement in the COT. [5]

2.2.3 Calorimetry

The solenoid and tracking volume of CDF is surrounded by calorimeters which cover 2π in azimuth and in pseudorapidity $\mid \eta \mid \leq$ 4.2. They are segmented in azimuth and in pseudorapidity to form a projective tower geometry, which points back to the nominal interaction point. There are three η regions of calorimeters, central, end-plug, and forward. Each region has an electromagnetic calorimeter (CEM, PEM, FEM[6]) with lead absorbers and an hadronic calorimeter (CHA/WHA, PHA, FHA) with iron absorbers. The existing scintillator-based calorimeters continue to perform well in Run II. The gas calorimeters in the region $|\eta| > 1$ are incompatible with the crossing rates for Run II, and are replaced with a new scintillating tile plug calorimeter. Its electromagnetic section has a energy resolution of approximately $16\%/\sqrt{E}\ GeV\ +\ 1\%$ constant term. The overall segmentation of the calorimeters is shown in Table 2.2.

$\|\eta\|$ Range	$\Delta\phi$	$\Delta\eta$
0.0 - 1.1(1.2h)	15°	~ 0.1
1.1(1.2h) - 1.8	7.5°	~ 0.1
1.8 - 2.1	7.5°	~ 0.16
2.1 - 3.64	15°	$0.2 - 0.6$

Table 2.2: *Segmentation of the CDF II calorimeter. A detailed description is given in [2].*

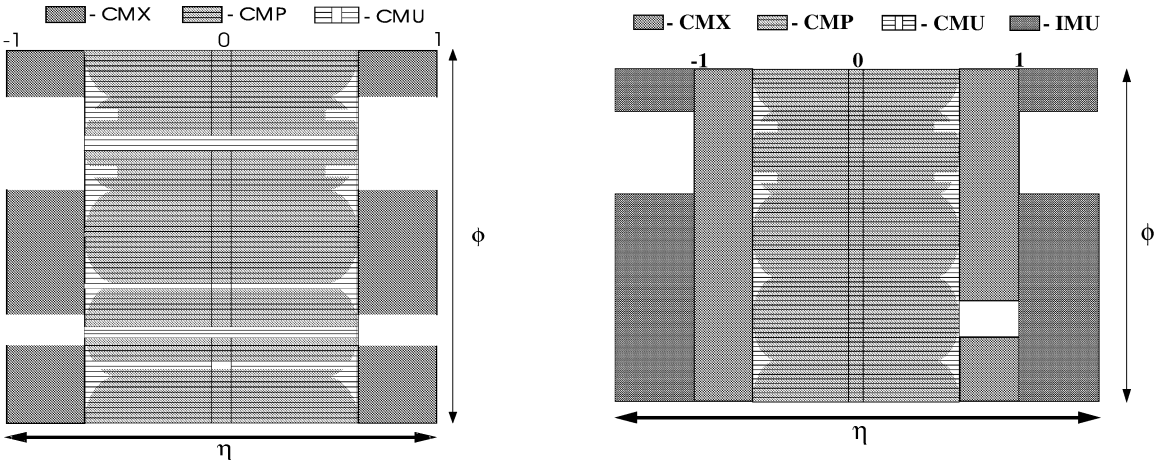
[6]C for central; P for plug and F for forward calorimeter respectively

2.2.4 The Muon Systems

The central calorimeter functions as a hadron absorber for the central muon detection system (CMU). The CMU consists of four layers of drift chambers located outside the central hadronic calorimeter. It covers 84% of the solid angle for the pseudorapidity interval $|\eta| < 0.6$ and can be reached by muons with a transverse momentum greater than 1.4 GeV. In 1992 the system was upgraded by adding 0.6 m of steel behind the CMU and additional four layers of drift chambers behind the steel. This new system is called central muon upgrade (CMP). For $|\eta| < 0.6$ the CMP covers 63% of the solid angle while both systems overlap in 53% of the solid angle. In addition, the pseudorapidity range of $0.6 < |\eta| < 1.0$ is covered by the central muon extension (CMX) to 71% of the solid angle. The changes for Run II in the muon systems represent incremental improvements. New Chambers are added to the CMP and CMX systems to close gaps in the azimuthal coverage. The forward muon system is replaced with the *intermediate muon system*, IMU, covering from $1.0 \leq |\eta| \leq 1.5$. Table 2.3 gives an overview of the different muon systems. The muon coverage in Run I and Run II is displayed in figure 2.10. A detailed description is given in [2].

	CMU	CMP/CSP	CMX/CSX	IMU
Pseudorapidity coverage	$\|\eta\| < 0.6$	$\|\eta\| < 0.6$	$0.6 < \|\eta\| < 1.0$	$1.0 < \|\eta\| < 1.5$
Total counters (Run I)		128	256	none
Total counters (Run II)		269	324	864
Min p_T of detectable μ	1.4 *GeV*	2.2 *GeV*	1.4 *GeV*	$1.4 - 2.0$ *GeV*

Table 2.3: *Design parameters of the CDF II muon detectors.*



Muon coverage in Run I. **Muon coverage in Run II.**

Figure 2.10: Location of the Run I and Run II muon components in azimuth ϕ and pseudorapidity η. Most of the uninstrumented regions in Run I are covered in Run II.

2.3 Trigger

The CDF electronics systems are substantially altered to handle Run II accelerator conditions. The increased instantaneous luminosity requires a similar increase in data transfer rates and the reduced separation between accelerator bunches a new architecture for the readout system (see figure 2.11). To accommodate a 132 ns bunch-crossing time and a 4 μs decision time for the first levels trigger, all front electronics are fully pipelined, with on board buffering for 42 beam crossings. The first level trigger (Level-1) is fed by the calorimeter, the COT and the muon chambers. There are four local second trigger level (Level-2) buffers. Level-2 is an asynchronous system with an average decision time of 20 μs. An example of these 42-crossing-pipelines and four-fold buffers is illustrated for the SVX3 chip in chapter 3.4.2. The different detector components and their role in the triggering scheme is displayed in figure 2.12. A Level-2 trigger accept flags an event for readout. Data are collected in DAQ[7] buffers. A computer network finally analyzes the complete event at trigger Level-3. An accepted event is written out to permanent storage. At Level-3 the data is also sorted into different streams; specially important events are stored to be analyzed the next day. Statistics of these events can also be viewed by online monitoring running on other workstations. In section 2.4 we give a short overview about the Online Monitor Project, in which the author largely participated.

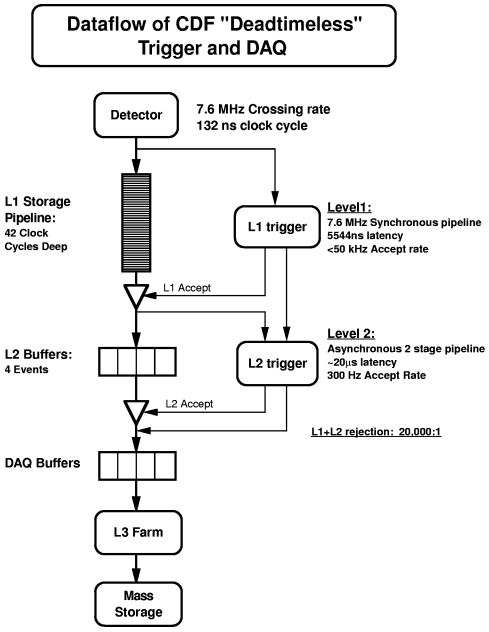


Figure 2.11: **Functional block diagram of the CDF II data flow.**

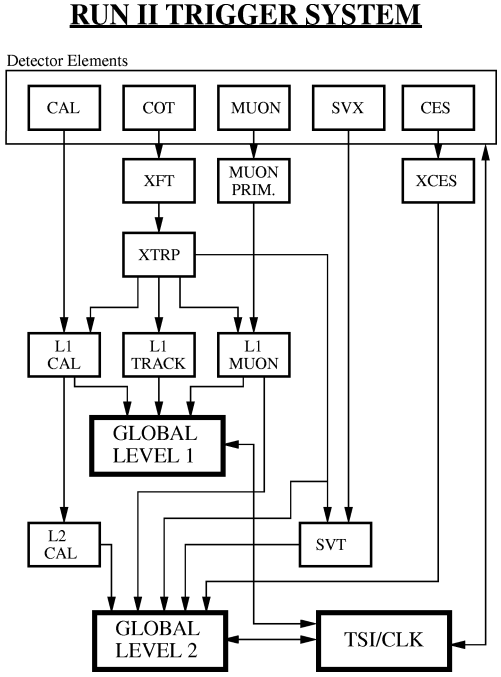


Figure 2.12: **Block diagram of the CDF II trigger systems.**

[7]DAQ: **D**ata **AQ**uisition.

The main trigger extension are: extended lepton detection coverage, the presence of COT tracking information at Level-1 and the Level-2 trigger information from the silicon vertex trigger on large impact parameter tracks. A detailed description of the trigger designs and strategies can be read in [8]

Silicon Vertex Tracker (SVT) – Secondary Vertexing.

The ability to use impact-parameter information in the trigger to detect secondary vertices can substantially increase the physics reach of a hadron collider experiment. Background can be quite substantially reduced, e.g. for the process $Z \longrightarrow b\bar{b}$. The B-decay studies will also be greatly enhanced. Some physics processes not involving b quarks will also profit from the SVT, e.g. the high P_T inclusive muon trigger, needed for the W-mass measurement, has a high Level-2 rate. The SVT can both reduce the accidental rate by demanding an SVX II-ISL track pointing to the primary vertex and remove lower P_T muon background by using improved momentum resolution to tighten the P_T threshold. In order to obtain impact-parameter information at Level-2, the silicon tracker is read out after each Level-1 trigger. The SVT combines data with the Level-1 tracking information from the COT and computes track parameters (ϕ, P_T, and impact parameter d) with a resolution and efficiency comparable to full offline analysis [2]. The complete SVT architecture is shown in figure 2.13

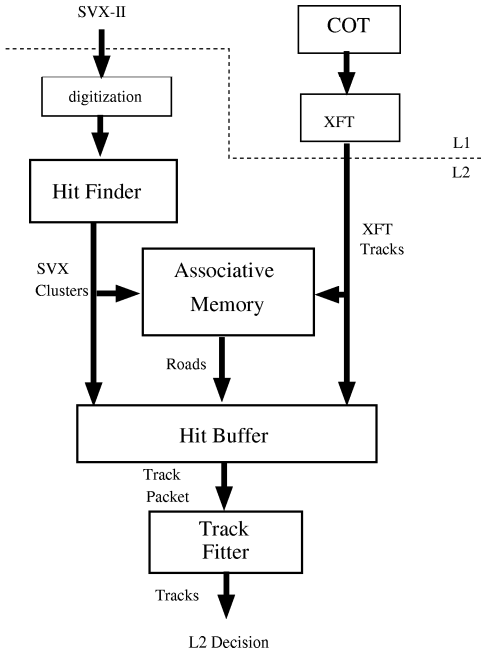


Figure 2.13: **Architecture of the SVT trigger [2].**

2.4 Data Acquisition – Online Monitor Server

CDF will start Run II with a significantly different detector, trigger system, data format and software environment. Therefore, the programs which served to monitor the data stream (Consumers: YMON, LUMON, TRIGMON, etc) during Run I have to be rewritten. All the data have to be accessible in real time, at least in the control room. In the new concept we plan to transfer *only small objects* like histograms, table or status information. All the CPU-load associated with displaying graphics is transferred to the remote machine. This concept enables the data distributing processor to serve many clients at once. The functional block diagram is illustrated in figure 2.14. The (Display) Server is a program based on the ROOT package [59] that allows the display/viewers programs (Display Clients) to connect to it as a client and to access the information in the shared memory in real time. Since the Display Server needs access to shared memory it has to run on the same machine as the consumers. One server program is able to handle more than one consumer. Each consumer is writing its data to one shared memory area, which can be accessed completely by all sub-processes of the server program. Multiple display/viewer programs can connect from anywhere in the world without having any effect on the consumer itself. To handle many display/viewer programs independently and individually, the server spawns[8] a new child process to handle all requests. The Display Server is also able to distribute the data via the World Wide Web (WWW). Status information on the WWW is also provided by the Display Server. The Display Client, a full functional GUI[9] can access the data directly from shared memory, from the WWW or via a fast socket connection. A more detailed description is given in appendix E.

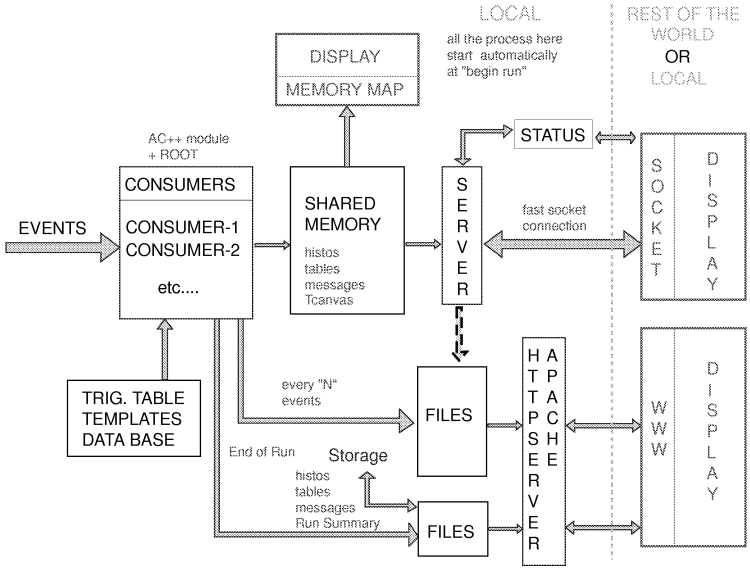


Figure 2.14: *Schematics of Consumer, Display Server, the Internet and the Display Client.*

[8]The corresponding Unix system command is fork(); a new process with original behavior, but a new process ID and separate process memory is allocated.

[9]GUI: **G**raphical **U**ser **I**nterface

Chapter 3

Intermediate Silicon Layers detector – ISL

3.1 Motivation

The Intermediate Silicon Layers Detector (ISL) is an integral part of the CDF II tracking system, consisting of three concentric subdetector systems. Closest to the beampipe is the Silicon Vertex Detector (SVX II), consisting of 5 silicon layers at radii between r=2.45 cm and 10.60 cm. The ISL is an almost 2 m long silicon detector, with one central layer ($|\eta| < 1$) at radial position r=22 cm and two layers in the forward region ($1 < |\eta| < 2$) at radial positions r=20 cm and 28 cm respectively. The third detector, the Central Outer Tracker (COT), is a large drift chamber with a length of 3 m, covering a radial span beginning at 40 cm and ending at 137 cm. The ISL provides one or two additional space points in the intermediate region (r=10.6 cm up to 40 cm), which improves the linking probability between SVX II tracks and COT tracks. Its fine granularity helps to resolve ambiguities in dense track environments. The complete tracking system, consisting of Layer 00, SVX II, ISL and COT, provides high momentum resolution for $|\eta| < 1$ ($\sigma_P/P_T^2 = 0.09\%(GeV/c)$ at $P_T = 10\ GeV/c$) [2]. In addition, SVX II together with the ISL forms a standalone, 3D silicon tracker, with up to 7 axial and 7 stereo measurements extending the tracking capabilities out to $|\eta| \leq 2$. The 3D tracking performance and the momentum resolution of the SVX II are largely improved by the ISL and enable good b tagging in the forward region (see figure 3.1). Increasing the acceptance, the ISL has a significant impact on the double b-tag efficiency (see Table 3.1).
The new inner tracking system replaces the former SVX of Run I, a 4 layer silicon-microstrip-detector with single sided readout in $r\phi$. Figure 3.2 illustrates the improvement related to the combination of SVX II+ISL in comparison to the former SVX.

Detector Configuration	Single tag eff.(%)	Double tag eff.(%)
SVX+CTC [1]	37.6 ± 1.0	6.9 ± 0.5
SXV II+COT	46.7 ± 1.1	8.7 ± 0.6
SVX II+ISL+COT	60.1 ± 1.0	15.1 ± 0.8

Table 3.1: *Efficiency for single and double b-tagging [2] in $t\bar{t}$ Monte Carlo events for different detector configurations. The results are from a parametric study, including geometry, acceptance cuts and tracking efficiencies.*

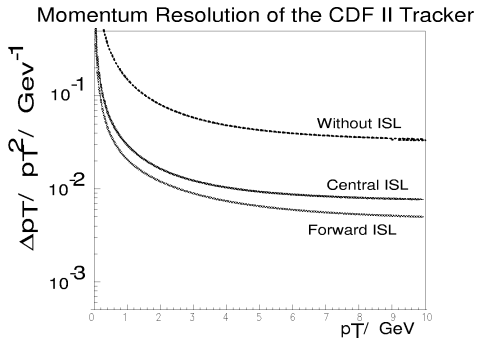


Figure 3.1: *Improvement of the momentum resolution for different configurations. [9]*

3.2 Conceptual Design Considerations

The ISL project started in October 1996. The short time available until the insertion scheduled for late 1999[2] required a quick yet innovative design and aggressive construction schedule. To minimize R&D and to allow easy integration into CDF, the ISL uses the same readout electronics and data acquisition (DAQ) as the SVX II [2, 31]. The design takes advantage of the large radial position, the radiation damage occurs more slowly and the hit occupancy is lower. It is therefore possible to use longer strips and a large readout pitch to reduce the number of readout channels and subsequently the cost of front-end electronics and data acquisition. The mechanics of the ISL called for a new design. Given the large volume between SVX II and the COT, it was possible to design a light-weight yet robust support structure (see section 3.3). For the ISL we estimate 1.5% radiation length in the central region and 2% radiation length in the forward region, including 1% radiation length due to hybrids, endcaps, cooling.
The result is a detector with 888 large area, double-sided silicon microstrip sensors with a total of 303104 channels.

[1] SVX Silicon Vertex Tracker of CDF for the running period of '92 - '96 (Run I);
CTC Central Tracking Chamber of Run I

[2] Insertion was delayed until late 2000, Run II start will be march 2001

The basic ISL unit is the ladder, composed of three silicon sensors bonded together and their readout electronics located on a hybrid at the end. The support structure is built of carbon fiber[3]. 296 ladders are paired to form 148 modules of 55 cm length each. The modules are mounted on carbon fiber rings to form barrels, which are then assembled into a spaceframe (see section 3.3).

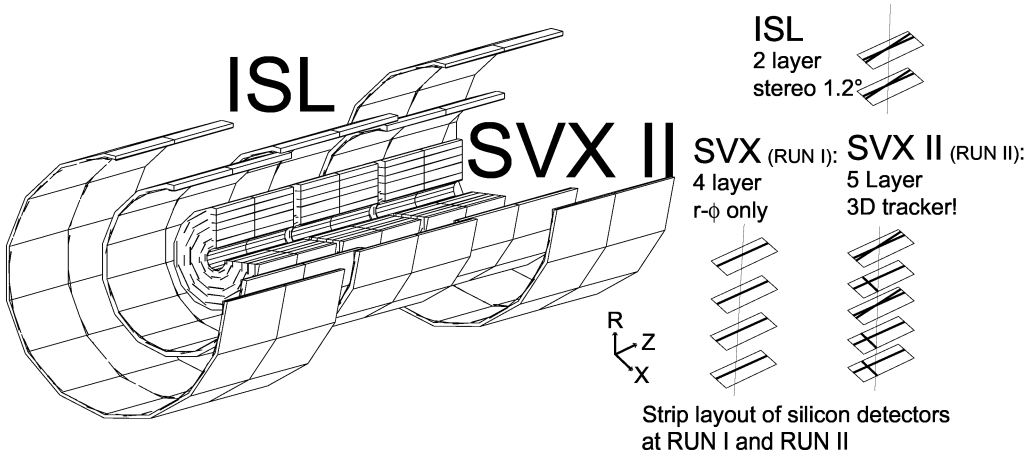


Figure 3.2: **SVX to SVX II + ISL.**
SVX was a 4 layer, 51 cm long detector in Run I providing $r\phi$ information. It will be replaced by the SVX II + ISL combination; a 5 layer, 87 cm long detector (SVX II) providing stereo information plus one additional central layer and two additional layers in the forward region (ISL), 195 cm long. All sensors are double sided with stereo readout, 4 layers with a stereo angle of 1.2^o and 3 with a 90^o stereo angle; the rectangles on the right represent the different layers and their strip layout.

3.3 Spaceframe

The spaceframe was designed with respect to weight, stiffness and material budget; this led to a carbon fiber structure. Carbon fiber rings are connected with hollow carbon fiber rods. The total weight of the structure is about 6 kg before mounting the modules. Finite element analysis predicts a maximum gravitational sag of less than 30 μm in the center. We expect the structure to be even stiffer after mounting the modules, with a final precision of 50 μm over the whole length of 2 m. It is illustrated in figure 3.3. The internal module precision is ported to the final position precision in the spaceframe by *only* connecting the hybrids, not the carbon fiber ladders. The position of each silicon sensor is measured by a Coordinate Measurement Machine (CMM). The final alignment precision will be achieved with tracks.

[3]Testbeam results showed that additional crosstalk with the conductive fiber support and additional capacitance effects can be avoided by isolating the carbon fiber ladder from the sensors and grounding the carbon fiber ladder [20].

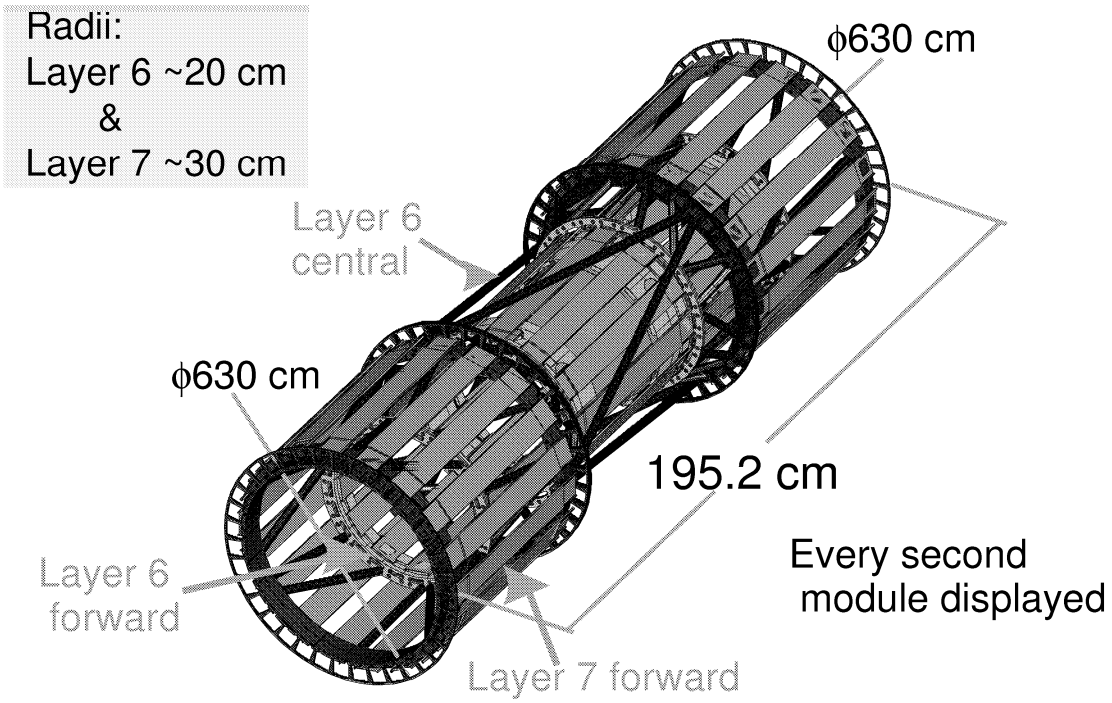


Figure 3.3: **Mechanical Design of the Carbon Spaceframe.**
The geometric concept of the single additional layer in the central region (Layer 6 central) and the two additional layers in the forward direction can be seen (Layer 6 and 7 forward).

3.4 Electrical components

In this chapter the basic electronic components will be described –the readout chip and the silicon sensors.

3.4.1 Silicon detectors [19, 24, 21]

The sensors are 7.4×5.5 cm^2 silicon microstrip detectors, 300 μm thick, AC coupled with 512 axial strips on the p-implant side and 512 stereo strips (1.2^o) on the n-implant side; both sides have a strip pitch of 112 μm. The sensors consist of high resistivity n-bulk silicon. We use a conventional design: bias is applied via polysilicon resistors, one guardring for field shaping and for the n-side a p-stop design is used. Detectors are being produced by Micron Semiconductors on 6" wafers. A slightly shorter version (6.7×5.7 cm^2) of the same detectors are being manufactured by Hamamatsu Photonics on 4" technology, with the stereo strips (1.2^o) on the p-implant side. The performance of Micron prototypes was measured in a testbeam. Using the SVX II electronics, we measured a resolution of 25 μm with an average signal/noise ratio of 21 for an average

cluster size of 1.7 strips for one detector (with no magnetic field) [20]. The prototype phase is described in chapter 7. Micron will finish production in january 2000. Each sensor is sent to Karlsruhe for quality control before the final ladder assembly in Pisa. We will discuss the quality control in chapter 8. Layout and structure are shown in chapter 9 and in appendix B.1.1 on page 120.

3.4.2 The SVX3 chip [2, 31]

The silicon sensors are read out by the SVX3 chip, a radiation hard CMOS custom integrated circuit. Each chip has 128 parallel input channels. The chip consists of two parts[4]: the front-end for the analog functions and the back-end part for the digital functions. The input amplifiers, integrators, the 46 cell pipelines needed for deadtimeless operation and the pipeline acquisition logics are located in the front-end. Up to 4 groups of cells can be queued for digitization and readout at one time. The back-end consists of an 8 bit Wilkinson ADC[5], a readout FIFO[6] and differential output drivers. The chip is able to work with positive and negative signals to handle double sided silicon detectors. It has a sparsification mode, a calibration input and is capable of pedestal subtraction at the chip level. The chip is programmable to adjust for different Tevatron running conditions, e.g bunch-spacings (132 and 396 ns). It can handle strip capacitances from 10 to 35 pF. The pipeline depth, threshold level and bandwidth limit are adjustable. The chip has been irradiated with a ^{60}Co source up to 4 Mrad and was found to perform well[7] [32]. The amplification is 15 mV/fC, which corresponds to 60 mV for a minimum ionizing particle. The chip provides deadtimeless readout with Level-1 trigger rates up to 50 kHz. The maximum delay between the Level-1 trigger decision and readout without overwriting the pipeline cell content is 5.5 μs at 132 ns between beam crossings.

3.5 The Online Alignment System and Active Alignment

The Silicon Vertex Trigger (SVT) will use impact-parameter information at trigger level to detect secondary vertices. In order to obtain impact-parameter information in the Level-2 trigger, the SVX II is read out after each Level-1 trigger. The SVT combines this data with the Level-1 tracking information from the COT, reconstructed with the XFT (eXtremely Fast Tracker) trigger [2]. The SVT computes track parameters

[4] built in a monolithic structure

[5] **A**nalog to **D**igital **C**onverter

[6] **F**irst **I**n **F**irst **O**out: Register where the data entered at the input appear in the output in the same order.

[7] During Run II the chip will be exposed to about 7×10^{13} minimum ionizing particles per cm^2 over a period of two years, corresponding to an absorbed dose of 2 Mrad at the inner layer of SVX II [39]

in the transverse plane (ϕ_0, p_T, and impact parameter) with resolution and efficiency comparable to full offline analysis. This trigger needs the beam axis to be parallel to the tracking system. Small tilts can be corrected for by adjusting the Tevatron beam. For this it is necessary to feed back the beam position to the Tevatron control room. To adjust for larger tilts an active alignment system is foreseen allowing movement of the SVX II/ISL with respect to the beam. The movement is achieved by mounting the system on rods. Micro motors (so called "inchworms", based on piezo crystals) move along the rods with high precision and vary the position of the SVX II/ISL system. The relative positions of SVX II, ISL and COT will be continuously monitored by the so called Rasnik system[8] [33] [34]. Systems of a light source, consisting of an array of 9 infrared LEDs, a distinctive pattern, a lens and a CCD[9] camera will be mounted at several places in the detector. The pattern is continuously projected on the CCD. Any relative movement of LED-array and CCD will be noticed as a shift of the pattern. A PC with pattern recognition software will calculate the movement and rotation with a precision in the sub micron range. It is also suited to detect changes due to temperature and humidity fluctuations in the whole structure. Figure 3.4 shows the positions of the Rasnik components positions in the system; relative shift of ISL to SVX II, ISL to COT, twists in the SVX II and the global tracking system to end flange position can be monitored. In appendix D we discuss studies proving the necessity for light shields in the Rasnik system, to avoid a higher leakage current, causing higher noise in the silicon system.

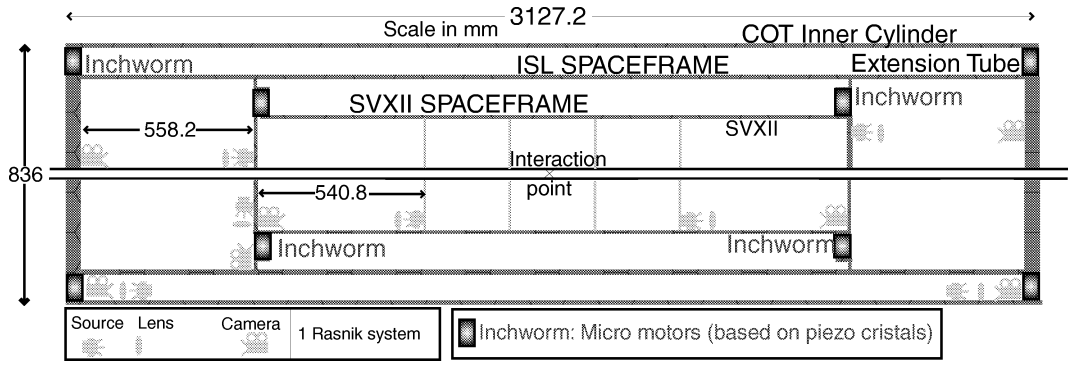


Figure 3.4: **The Online Global Alignment System.**
This picture displays the spaceframes of SVX II, ISL, COT and eight Rasnik systems. With this arrangement the relative positions of the 3 subdetectors can be monitored. One control unit consists of an array of infrared LEDs as source, a projected pattern, a lens to focus the light and the CCD as receptor. Each change of position of source or camera will be observed as a shift of the pattern.

[8] A similar system was used in the CHORUS experiment. RASNIK stands for "Relative Alignment System of NIKhef"

[9] CCD: The **C**harge-**C**oupled **D**evice is a light sensitive semiconductor pixel array, that accumulates an image by light integrating and can be read out electronically.

Chapter 4

Physics using a high precision tracking system

Lessons from Run I [2]

- The detector should have a very good acceptance for high-p_T electrons and muons from the chain $t \rightarrow W \rightarrow l\nu$:
- The detector should have large acceptance and efficiency for tagging b-jets. This is a question of geometrical coverage, efficiency, and signal-to-noise ratio, most important for secondary vertex finding but also for soft lepton identification. This is especially important for $t\bar{t}$ events, their decays have a near isotropic distribution, with two taggable b quarks and 0/2/4 jets and 0/1/2 leptons (see diagram 4.10).

Impact of Run II upgrades on Top and Bottom Physics

The CDF II upgrades significantly increase the overall top acceptance and precision at high luminosity.

- Silicon Vertex Detector (SVX II):
  The tagging of b-quarks from top quark decays will be greatly improved in the long, 5-layer, double-sided device. The region of "contained b-jets" is extended to cover the entire interaction region. With ten measurements in two views for any given track, it will be possible to make stringent track quality requirements, reducing the level of mistags, while still improving the overall track finding efficiency. A three-dimensional vertexing device will improve the b-tagging efficiency by making it possible to find bs whose displacements are predominantly in the rz direction (figure 4.1). In addition, unlike a 2D vertex, a 3D vertex is unique with even 2 tracks, again raising the possibility of reducing backgrounds while increasing the efficiency relative to the present analysis. Taking all of these factors into account, we anticipate that the SVX II will increase the efficiency for tagging at least one b-jet in a $t\bar{t}$ event to better than 65% (a 62% increase over the Run I efficiency), and will raise the double b-tag efficiency to 20% (a 200%

increase from current performance). Finally, the 3D capability of the SVX II will allow a precision measurement of primary vertex in the event, improving a variety of measurements including the E_T and p_T of the primary leptons, the E_t of the jets, and the missing transverse energy.

- Intermediate Silicon Layers (ISL):
  The ability to find unambiguous tracks pointing at the new plug calorimeter will provide clean identification of electrons from $W \rightarrow e\nu$ in the region $1.0 \leq |\eta| \leq 2.0$, improving the top quark yield in the electron channel by 33%. With the expected standalone tracking capability of the SVXII-ISL combination, b-tagging of top events will be possible out to $|\eta| = 2$, significantly improving the double-tagged top yield. The improved electron ID may also extend b-tagging with soft leptons into the plug region.

- Central Outer Tracker (COT):
  The top analysis of Run I depended crucially on the large central tracking chamber. The new COT has more robust stereo tracking. It has a lower mass and the momentum resolution is increased at the trigger level. As discussed in [2] and chapter 3, the integrated system of COT-SVXII-ISL-Layer 00 will largely increase the tracking efficiency at CDF II.

- Layer 00 (L00): To study the effect of L00 on high p_T physics analysis, $t\bar{t}$ production at 2 TeV was simulated [5]. The general results are also applicable to any similar physics signatures, including particle decays to $b\bar{b}$ (e.g. Higgs; see section 4.3). It was found that the addition of L00 to SVXII-ISL leads to a significant enhancement of single and double b-tagging efficiency. For b-jets in the SVXII layer 0 hybrid regions, the addition of L00 increases the b-tag efficiency by another 25%. In the regions without electronics, there is an enhancement in the b-tag efficiency of 7%. Overall, the SVXII-ISL detector with L00 is found to have a 9% higher single tag efficiency and a 20% higher double tag efficiency than without L00, (assuming a 30 cm luminous region).

4.1 b physics expectations for Run II with the new tracking system

Most collisions at hadron colliders are 'soft'. The formation of quark pairs in a gluon field leads to the production of mesons and baryons ($\sim$ 30 charged and $\sim$ 20 neutral particles per event) with small transverse momentum, called Minimum bias events. The enormous $b\bar{b}$ cross section with $\sigma_{b\bar{b}} = 50\ \mu b$ is large compared to other experiments (see table 4.1), but the background at hadron colliders is even larger. The $\sigma_{b\bar{b}}/\sigma_{TOT}$ ratio is around 0.001. The challenge is to extract events of interest.

	TEVATRON Run II $p\bar{p}$ $\sqrt{s}$=2.0 TeV	CESR,DORIS, SLAC e^+e^- *at* $\Upsilon(4S)$ $\sqrt{s}$=10.5 GeV	LEP,SLC e^+e^- *at* Z^0 $\sqrt{s}$=91. GeV	SLAC (PEP II) (BaBar) KEK (Belle) e^+e^- *at* $\Upsilon(4S)$ asymmetric BaBar: 9 and 3.1 GeV $\sqrt{s}$=10.5 GeV
$\sigma_{b\bar{b}}$	$> 50\ \mu b$	$\approx$ 1 nb	$\approx$ 6 nb	$\approx$ 1 nb
$\sigma_{b\bar{b}}/\sigma_{tot}$	0.001	0.28	0.22	0.28
B^0, B^+	yes	yes	yes	yes
$B_s^0, B_c^+, \Lambda_b^0$	yes	no	yes	no
Boost $< \beta\gamma >$	2-4 (trigger dependent)	0.06	6	0.54
$b\bar{b}$ production	not back-to-back	both Bs at rest	$b\bar{b}$ back-to-back	$b\bar{b}$ not back-to-back
Trigger	leptons only secondary vertex	inclusive	inclusive	

Table 4.1: **Tevatron compared to other accelerators producing b quarks,** *with respect to energy, $b\bar{b}$-cross sections, kinematics and trigger possibilities.*

The low $\sigma_{b\bar{b}}/\sigma_{TOT}$ ratio requires specialized B triggers. The SVT exploits the B lifetime to trigger on displaced vertices via the impact-parameter (see figure 4.1 and section 2.3). The new trigger is deadtimeless and the track trigger, contrary to Run I, is moved to Level-1 and a new silicon trigger is introduced at Level-2. The combination of Layer 00, SVX II and the ISL complement one another to provide best impact-parameter and momentum resolution (see figure 2.7 and 3.1).

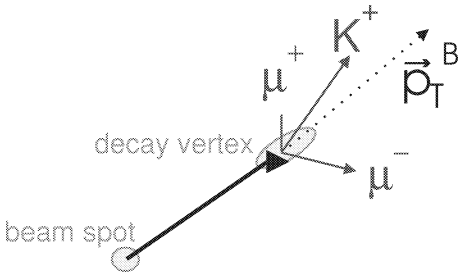


Figure 4.1: **b-tagging – looking for displaced vertices.** An example of two such secondary vertices is shown in figure 4.11.

The produced b quarks fragment into hadrons $\bar{B}^0(b\bar{d})$, $\bar{B}^0_s(b\bar{s})$, $B^-(b\bar{u})$, $\Lambda_b(bdu)$, $B^-_c(b\bar{c})$, also B^*, B^{**} etc. The lowest lying states decay via weak interaction. Studies of these decays leads to information on the CKM matrix elements: V_{cb}, V_{ub}, V_{tb}, V_{ts}, V_{td} thus tests the electroweak theory (see below). B physics is subdivided into three studies:

1. The study of Weak Decays
   Test of the CKM Mechanism: $\bar{B}^0_s$, Λ_b, $\bar{B}^-_c$.

2. New Physics from Rare Decays
   e.g. $B^0, B^0_s \longrightarrow \mu^+\mu^-$ or $e^\mp\mu^\pm$

3. Quantitative Study of QCD

   - Nonpertubative measurements: ratios of lifetimes and branching fractions, production fractions
   - Probe gluon structure function: $gg \longrightarrow b\bar{b}$

The *Cabibbo-Kobayashi-Maskawa mixing matrix* [53] (CKM matrix: V_{CKM}) describes the transformation from the eigenstates of the electroweak interaction to the mass eigenstates of the quarks. The CKM matrix and its elements is shown in formula 4.1 and the numerical values are displayed in formula 4.2. The 6 quarks and their transitions related to emission or absorptions of W-bosons are shown in figure 4.2.

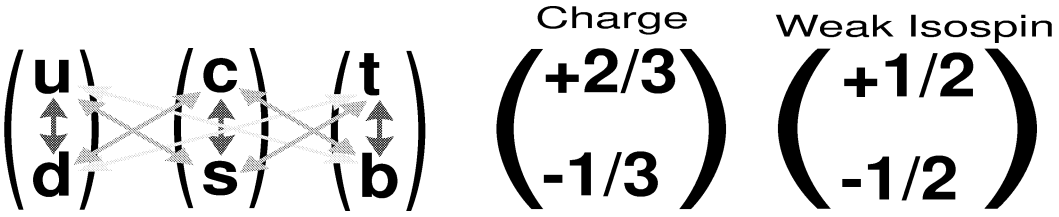


Figure 4.2: **Quarks build 3 families with two states each:**
weak Isospin Iz = +1/2, -1/2 with electric charges: +2/3, -1/3.
The transitions between Iz = +1/2 and -1/2 by emission or absorptions of W-bosons happens mainly inside one family, but transitions over one or two family borders is allowed.

By convention V_{CKM} is expressed by a 3×3 unitary matrix V operating on the charge $-e/3$ quarks:

$$\begin{pmatrix} d' \\ s' \\ b' \end{pmatrix} = \begin{pmatrix} V_{ud} & V_{us} & V_{ub} \\ V_{cd} & V_{cs} & V_{cb} \\ V_{td} & V_{ts} & V_{tb} \end{pmatrix} \begin{pmatrix} d \\ s \\ b \end{pmatrix} \tag{4.1}$$

The coupling of two quarks q_1, q_2 to a W-boson is proportional to the matrix element $V_{q_1 q_2}$, see figure 4.3. The 90% confidence limits on the magnitude of the elements of the complete matrix are [54]:

$$\begin{pmatrix} 0.9745 \text{ to } 0.9760 & 0.217 \text{ to } 0.224 & 0.0018 \text{ to } 0.0045 \\ 0.217 \text{ to } 0.224 & 0.9737 \text{ to } 0.9753 & 0.036 \text{ to } 0.042 \\ 0.004 \text{ to } 0.013 & 0.035 \text{ to } 0.042 & 0.9991 \text{ to } 0.9994 \end{pmatrix} \tag{4.2}$$

Note that these numbers assume the unitarity of the CKM matrix or the existence of three families of particles.

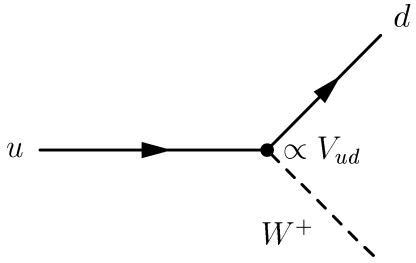


Figure 4.3: *Feynman Diagram for the coupling of an up and a down quark to a W-boson.*

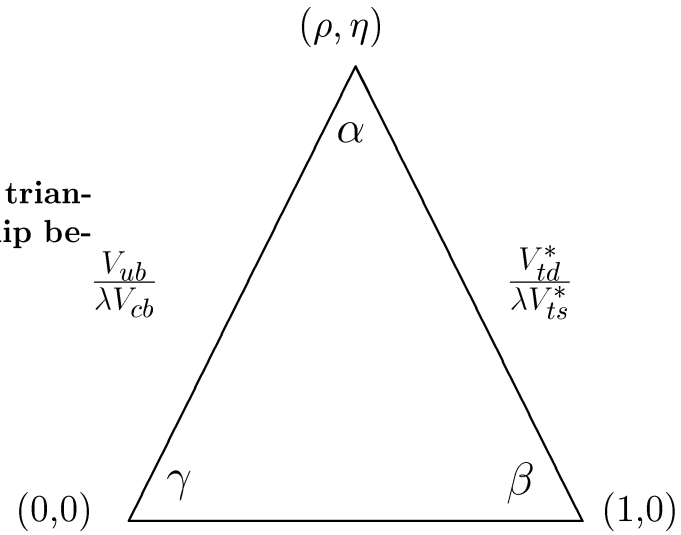


Figure 4.4: **The unitarity triangle indicating the relationship between the CKM elements.**

The Unitarity condition is: $\Rightarrow V^\dagger V = 1 \Rightarrow V_{tb}^* V_{td} + V_{cb}^* V_{cd} + V_{ub}^* V_{ud} = 0$.
The new possibility to trigger and to reconstruct high precision vertices will enable constraining the CKM matrix and therefore test the closure of the unitarity triangle (figure 4.4) by measuring [48]:

- $sin(2\beta)$ from $B^0/\bar{B}^0 \longrightarrow J/\Psi K_S^0$
- $|V_{td}/\lambda V_{ts}|$ from $B^0 - \bar{B}^0$ and $B_S^0 - \bar{B}_S^0$ flavor oscillations.

CDF II can measure **both** ($sin(2\beta)$ and $|V_{td}/\lambda V_{ts}|$). B_s physics is not possible at the B-factory machines.

$\underline{sin(2\beta)}$**:**

CP violation in the neutral B system leads to the CKM angle β.
The mixing induced type of CP violation is of the form[50]:

$$\frac{dN}{dt}(B^0 \to J/\psi K_S^0) \neq \frac{dN}{dt}(\overline{B^0} \to J/\psi K_S^0) \tag{4.3}$$

where $J/\psi K_S^0$ is a CP eigenstate: $CP|J/\psi K_S^0 >= -|J/\psi K_S^0 >$.
The mixing scheme is illustrated in figure 4.5.

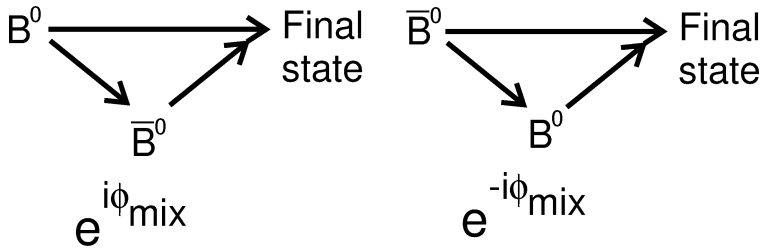


Figure 4.5: **Mixing induced CP violation in $B^0/\bar{B}^0 \longrightarrow$ final state.**
In the mixing induced case, the "direct" decay interferes with the mixed decay. For $B \to J/\psi K_S^0$ the phase ϕ_{mix} arises from the imaginary CKM element V_{td}.

In the Standard Model (SM) the CP asymmetry in this decay mode is:

$$A_{CP}(t) = \frac{\frac{dN}{dt}(\overline{B^0} \to J/\psi K_S^0) - \frac{dN}{dt}(B^0 \to J/\psi K_S^0)}{\frac{dN}{dt}(\overline{B^0} \to J/\psi K_S^0) + \frac{dN}{dt}(B^0 \to J/\psi K_S^0)} = A_{CP}(t) = \sin 2\beta \sin(\Delta m_d t) \tag{4.4}$$

and time integrated: $A_{CP} = \frac{\Delta m_d \tau_B}{1+(\Delta m_d \tau_B)^2} \cdot \sin 2\beta \simeq 0.47 \sin 2\beta$

The experimentally observed asymmetry is:

$$A_{CP}^{obs} = \mathcal{D} A_{CP} \tag{4.5}$$

with: $\mathcal{D} = (N_R - N_W)/(N_R + N_W)$ the "tagging dilution" and $N_R(N_W)$ = number of right(wrong) tags. With the "tagging efficiency"[1] ϵ, the statistical power of a tagging method can be expressed by $\epsilon\mathcal{D}^2$. For the "total tagging effectiveness" $\epsilon\mathcal{D}^2$=6.3% a

[1]Tagging efficiency: fraction of events that can be tagged

sample of 400 events, after tagging, has the statistical power of 25 'perfectly' tagged events.

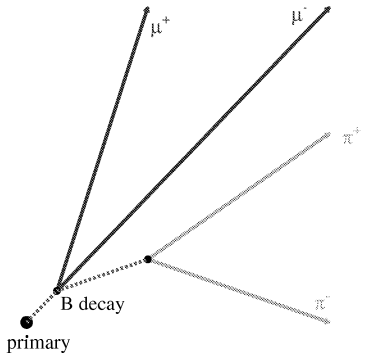
To finally measure $sin(2\beta)$:

1. A sample of $B \to J/\psi K_S^0$ decays will be collected.
   $\to$ The lifetime information helps, but is not required.
2. The flavour of the $B^0/\overline{B^0}$ must be determined at the production time.
   $\to$ This is the limiting factor, so as many methods as possible will be utilized.
3. A maximum likelihood fit to weight events will be used:
   - $\to$ in mass (peak versus sidebands)
   - $\to$ in lifetime (more analyzing power at longer lifetimes)
   - $\to$ in tagging probability (*i.e.* the probability that the tag was correct)

1.) $B \to J/\psi K_S^0$ **Event Sample**

- look for $J/\psi \to \mu^+\mu^-$
  $\Rightarrow$ central track + muon chamber track.

- look for $K_S^0 \to \pi^+\pi^-$
  $\Rightarrow$ take advantage of long lifetime to reject background: require $L_{xy}/\sigma_{L_{xy}} > 5$
- perform 4-track fit assuming $B \to J/\psi K_S^0$:
  - $\pi^+\pi^-$ constrained to PDG[2] K_S^0 mass
  - K_S^0 "points" to B (J/ψ) vertex
  - $\mu^+\mu^-$ constrained to PDG J/ψ mass
  - B candidate "points" back to the primary vertex



The main background is $c\bar{c}$ production ($\Rightarrow$ prompt $J/\psi + K_S^0$) and $b\bar{b}$ production ($\Rightarrow$ $b \to J/\psi + X$). The background has a prompt component and a long-lived component.

[2]PDG: **P**article **D**ata **G**roup.

2.) Flavor Tagging
For Run I CDF investigated three b flavour tagging methods:

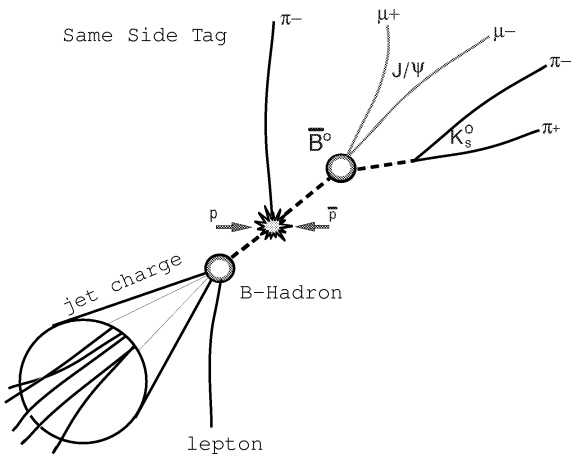


Figure 4.6: **Flavour Determination at production time [51].**

- the soft-lepton flavour tag or SLT;
- the jet-charge flavour tag or JCT;
- the same-side flavour tag or SST;

The tagging methods are illustrated in figure 4.6. The SLT and JCT are "opposite-side" flavor tagging methods, that is, they identify the flavour of the other B hadron in the event to determine the flavor of the B hadron of interest. The SLT is based on identifying the semileptonic decay of the B hadron. The charge of the lepton identifies the b flavor of the B hadron: $b \to l^-$, but $\bar{b} \to l^+$. The JCT is based on the momentum weighted sum of charges of tracks in the jet formed by the b quark and positive for a hadron containing a $\bar{b}$ antiquark.
The SST is based on the charge correlation of tracks produced in association with the hadronization of a $\bar{b}$ quark into a B meson. In particular, a π^+ (π^-) is expected to be produced in association with the formation of a B ($\bar{B}$). Figure 4.7 illustrates the fragmentation of a $\bar{b}$ quark into a B^+ or B^0 meson. To form a B^+, a $\bar{b}$ quark combines with an u quark from a $u\bar{u}$ pair, pulled from the vacuum, which leaves an $\bar{u}$ quark available for the formation of the charged hadrons π^-, K^-, p. For a B^+, all charged hadrons formed in this way have the same charge, which is opposite that of the primary $\bar{b}$ quark. Same-side tagging methods rely on identifying fragmentation tracks produced in association with a B meson and using their charge to tag the production flavour.

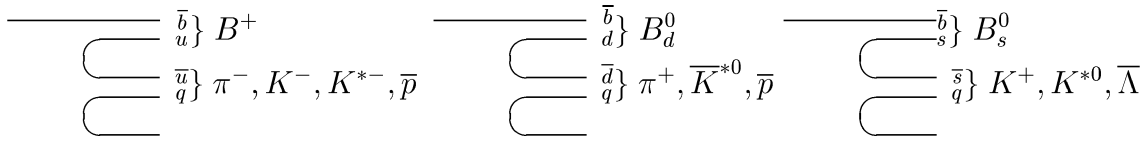


Figure 4.7: **A schematic picture of B^+, B^0 and B^0_s meson formation in $\bar{b}$ quark fragmentation.** *A B^+ is produced in association with positively charged hadrons only, while a B^0 is produced only with a positive pions, negative kaons (via $\overline{K^{*0}} \rightarrow K^-\pi^+$) and antiprotons. A K^+ is produced in association with a B^0_s.*

The tagging algorithms all have similar statistical power[50], which are displayed in table 4.2.

tagger	$\epsilon\mathcal{D}^2$
SST: same-side charge correlation	2.1 ± 0.5
JCT: momentum weighted jet charge	2.2 ± 1.3
SLT: semi-leptonic decay identification	2.2 ± 1.0

Table 4.2: **The statistical powers of the different flavour tagging strategies.**

$B^0 - \bar{B}^0$ and $B^0_S - \bar{B}^0_S$ flavor oscillations:

CDF will determine the ratio $|V^*_{td}/V^*_{ts}|$ by measuring the frequency Δm_s of $B^0_s\bar{B}^0_s$ oscillations and comparing it to the already well measured frequency Δm_d of $B^0_d\bar{B}^0_d$ oscillations (figure 4.8):

$$\frac{|V^*_{td}|}{|V^*_{ts}|} = (1.15 \pm 0.05)\sqrt{\frac{\Delta m_d \times m(B^0_s)}{\Delta m_s \times m(B^0)}} \tag{4.6}$$

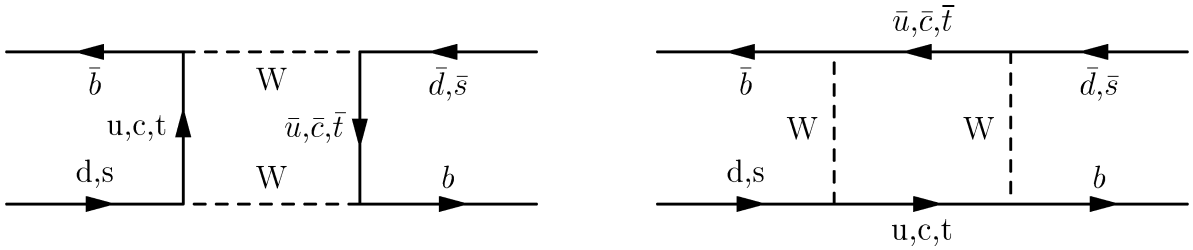


Figure 4.8: **Feyman Diagram of $B^o/\bar{B}^o$ Mixing**

$B^0, \overline{B^0}$ are the Flavor Eigenstates and B^0_H, B^0_L are the Mass Eigenstates with $\Delta m_d = m_H - m_L$ and $\Delta\Gamma = \Gamma_H - \Gamma_L$ ($\simeq 0$)

For initial state B^0:

$$P(B^0(t)) = \frac{1}{2}\Gamma e^{-\Gamma t}(\cosh(\frac{1}{2}\Delta\Gamma t) + \cos(\Delta m_d t))$$

$$P(B^0(t)) \simeq \frac{1}{2}\Gamma e^{-\Gamma t}(\quad 1 \quad + \cos(\Delta m_d t))$$

B^0 fully mixes to $\overline{B^0}$ after $\Delta m t \simeq 4.4$ lifetimes.

To measure the B_s oscillations, the proper time $t = m(B_s)\frac{L}{p}$ has to be reconstructed and the flavor of the B_s at production and at decay has to be determined, with L the oscillation length and p the momentum. The limit of $\Delta m_s > 5.8\, ps^{-1}$ at 95% confidence level is provided by the sample of $B_S \to D_s^- l\nu X$ in Run I. Ultimately the resolution depends mainly on δL and δp:

$$(\delta t)^2 \;=\; (\frac{m(B_s)}{p}\delta L)^2 \;+\; (\frac{t}{p}\delta p)^2 \tag{4.7}$$

The oscillation frequency δm_s is then given by fitting the mixing asymmetry :

$$A(t)_{mix} \;=\; \frac{N(t)_{unmixed} \;-\; N(t)_{mixed}}{N(t)_{unmixed} \;+\; N(t)_{mixed}} \tag{4.8}$$

to the function:

$$a(t) \;=\; Acos(\Delta m_s t) \;=\; Acos(\frac{x_s}{\tau}t) \tag{4.9}$$

where x_s is the decay mixing length which is inversely proportional to the proper decay time resolution. In figure 4.9 the proper lifetimes vs. the asymmetry for x_s=30 for the baseline CDF II[2] and with the additions of L00 and TOF [5] is displayed.

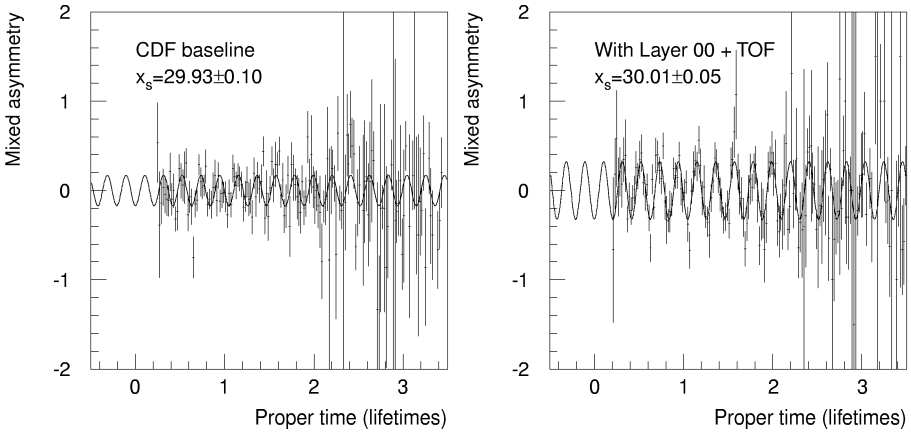


Figure 4.9: **The improvement in the asymmetry fit vs. proper time** *with the addition of L00 and TOF in comparison to the baseline CDF is illustrated.*

Additional constraints for the CKM matrix, additional B physics at Run II: The full tracking system provides real 3D Vertex and Track information which results in a factor ∼2 more acceptance. The additional silicon covering up to $|\eta| < 2$ helps finding soft bs.

- Measurement of CP asymmetry related to $sin(2\alpha)$ in $B^0/\bar{B}^0 \rightarrow \pi^+\pi^-$
  A special trigger is designed to search for $\pi^+\pi^-$ decays (the all-hadronic B decay trigger [8]). $B \rightarrow \pi^+\pi^-$ is a challenging analysis, since the branching ratio (BR) is only 10^{-5} with a large combinatorial background. The key is the ability to trigger on $\pi^+\pi^-$:
  - Level 1 (22 kHz): (XFT: Extremely Fast Trigger) The fast track processor finds 2 oppositely charged tracks ($p_t > 2\ GeV/c$).
  - Level 2 (25 Hz): Silicon (SVT) information used to require impact parameter $d_0 > 100\ \mu$m coming from the decays of heavy flavour instead of normal QCD jets with $d_0 \approx 0$.
  - Level 3: Full event information reduces the rate to 1 Hz.

  Around 10000 $B \rightarrow \pi^+\pi^-$ are expected for Run II. Particle identification of the TOF system will help to distinguish between $B \rightarrow K\pi$ and $B \rightarrow K^+K^-$. With the same effective tagging efficiency as in the $sin(2\beta)$ measurement the estimated precision is $\sigma(\sin(2\alpha)) = 0.09$ [49].
- Observe decay modes related to the CKM angle γ: $B_S^0 \rightarrow D_S^{\pm}K^{\mp}$ and $B^+ \rightarrow \bar{D}^0K^+$
- Measure CP asymmetry in $B_S^0/\bar{B}_S^0 \rightarrow J/\Psi\phi$.
- Rare Decays : Observe $B^+ \rightarrow \mu^+\mu^-K^+, B^0 \rightarrow \mu^+\mu^-K^{*0}, B_S^0 \rightarrow \mu^+\mu^-\phi$, $B_d^0(B_s^0) \rightarrow \mu^+\mu^-$, $B_d^0(B_s^0) \rightarrow e^{\pm}\mu^{\mp}$
- Study properties of the B_C^+ meson and b baryons.

Tagging Sensitivity ϵD^2	$6.3 \pm 1.1\%(Run\ I) \rightarrow \quad > 10\%(Run\ II)$
Tagging Sensitivity $\epsilon D^2(B_s)$	$3.2\%(Run\ I) \rightarrow 5.7\%(Run\ II) \rightarrow 10\ -\ 12\%(+TOF)$
Lifetimes $\frac{\tau(B^-)}{\tau(B^0)}, \frac{\tau(B_s)}{\tau(B^0)}, \frac{\tau(\Lambda_b)}{\tau(B^0)}$	Factor 4 improvement over Run I assuming same detector performance (conservative)
$\sigma(\sin 2\beta)$	0.08
$\sigma(\sin 2\alpha)$	0.09
$\sigma(\sin \gamma)$	0.25
$\sigma(A_{CP}(B_s \rightarrow J/\psi\Phi))$	$0.1 - 0.5$
Rare decay BR ($B_d \rightarrow \mu\mu$):	order 10^{-8}
Rare decay BR ($B_s \rightarrow \mu\mu$):	order 10^{-7}

Table 4.3: B **Physics Outlook at Run II.**

The aim is to overconstrain the unitary triangle by measuring sides and angles, allowing stringent tests of the standard model and perhaps evidence for new physics. The Cabibbo angle α is measured to a precision of 1%: ($\alpha = 0.2196 \pm 0.0023$)[54]. The ratio $V_{ub}/V_{cb} = 0.08 \pm 0.02$[54], determined from a combination of results from CLEO[3] and LEP[4] will be measured more precisely by adding data from the asymmetric B factories and CLEO. The angle β will be measured both by experiments on the $\Upsilon(4S)$ threshold and at hadron colliders. The ratio $|V_{td}^*/V_{ts}^*|$ will probably first be determined by measuring the frequency Δm_s of $B_s^0 \bar{B}_s^0$ oscillations, and comparing it to the already well measured frequency Δm_d of $B_d^0 \bar{B}_d^0$ oscillations. In addition $sin(2\alpha)$ and $sin(2\gamma)$ will be explored. An outlook of the expected b physics results is given in table 4.3.

4.2 $t\bar{t}$ and single top physics

The top quark (t) is produced in $p\bar{p}$ collisions mostly via $t\bar{t}$ production. Top quark pairs are produced 90% of the time via $q\bar{q}$ diagrams, the reminder via gg diagrams. Within the Standard Model (SM) top decays into $W + b \sim 100\%$ of the time.
The W decays are as follows:

$W^+ \rightarrow$	$l\nu$			$q\bar{q}$	
Branching ratio	1/3			2/3	
$W^+ \rightarrow$	$e^+\nu$	$\mu^+\nu$	$\tau^+\nu$	$u\bar{d}$	$c\bar{s}$
Branching ratio	1/9	1/9	1/9	3/9	3/9

Table 4.4: **The W decay modes and their branching ratios.**

For $t\bar{t}$ production the event topologies are:

- Dilepton channel: $l\nu l\nu b\bar{b}$; both Ws decay into $e\nu$ or $\mu\nu$.
- Lepton + jet channel: $l\nu q\bar{q}b\bar{b}$; events in which one W decays into $e\nu$ or $\mu\nu$, the other into a quark pair.
- All-hadronic channel : $q\bar{q}q\bar{q}b\bar{b}$; both Ws decay into quark pairs.

The Feynman diagram of $t\bar{t}$ production and decay is shown in figure 4.10.

[3]CLEO is the detector at the Cornell Electron-positron Storage Ring (CESR)
[4]LEP: **L**arge **E**lectron **P**ositron Collider at CERN

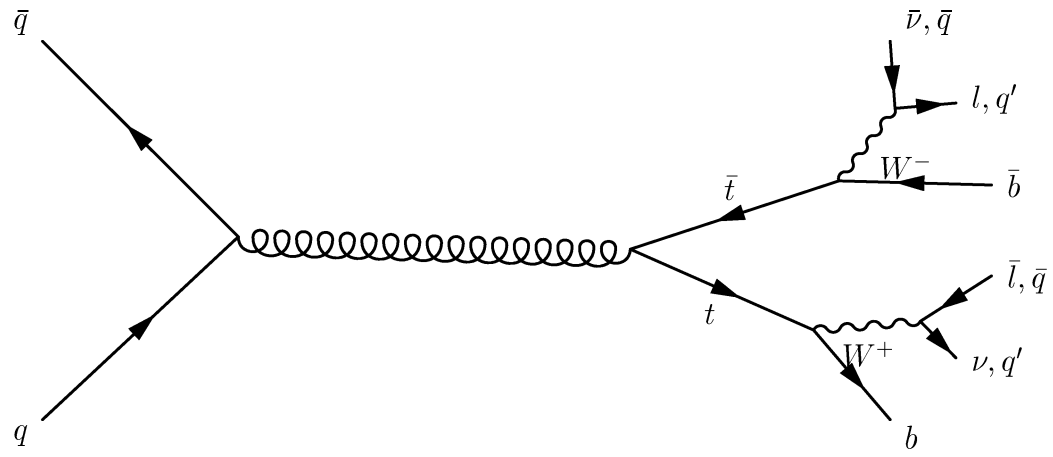


Figure 4.10: *Feyman diagram of a $t\bar{t}$ event.*

All of these channels profit from a full detector coverage for jet and lepton detection, from a good b-tagging and b-triggering. The full coverage is illustrated in figure 4.12, showing the new event display for Run II of a Monte Carlo event. An example of $t\bar{t}$ event in the all-hadronic channel with the old detector configuration of Run I is shown in figure 4.11. The cross section increases by 40%, the electron acceptance by 33% and the muon acceptance by 12% [2]. The b-tag (double b-tag) efficiency will be 60.1% (15.1%), this will largely increase the $t\bar{t}$ yield. It is expected to measure the top mass, a fundamental electroweak parameter, with a precision of approximately 3 GeV/c^2. Measurements of branching ratios, angular distributions and top production mechanisms will provide the first complete characterization of the t quark.

Top mass, new phenomena and Higgs mass

A heavy particle decaying into a $t\bar{t}$ pair could reveal itself as a visible resonance in the $M_{t\bar{t}}$ distribution. This would be an indication of new physics.
With the large number of 15 million Z bosons in the e^+e^- resonance LEP was able to fit all electroweak parameters in the framework of the SM and with that predicted the top mass to $M_t = 177 \pm 7^{+16}_{-19}\ GeV$. The second error describe the Higgs mass range form 65 GeV (-19) up to 1000 GeV (+16). The central value corresponds to $M_H = 300$ GeV. Vice versa a precision mass determination of the top quark will make a prediction of the Higgs mass possible. The fit in the framework of the SM with the combined data of Run I predicts $M_H = 141^{+140}_{-77}$ [42]. To find the resonances and make precise M_t measurements, as many $t\bar{t}$ events as possible have to be reconstructed. A double b-tag provided by the new silicon tracking system will especially improve the purity of the $t\bar{t}$ samples.

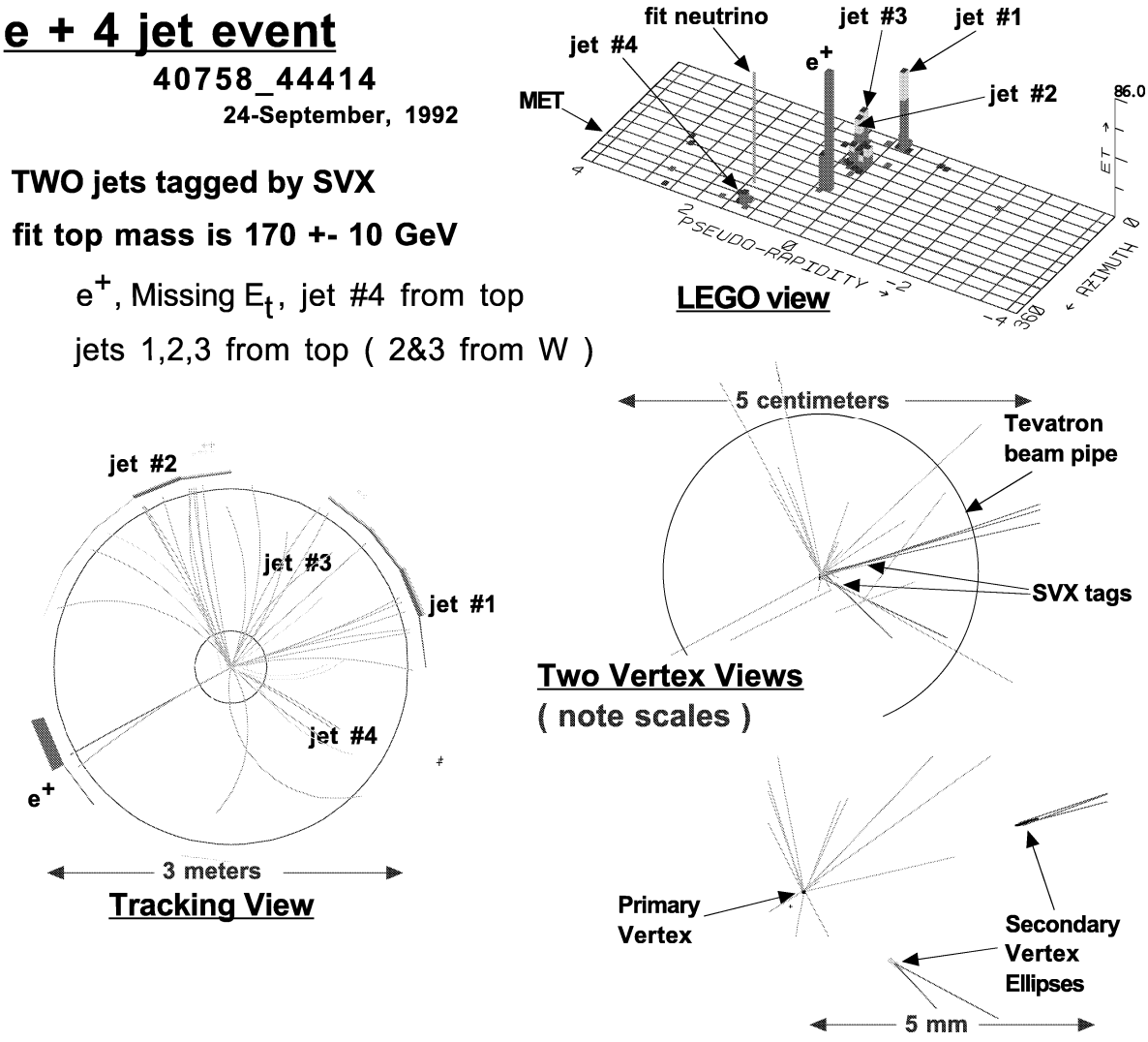


Figure 4.11: **A $t\bar{t}$ event with two jets in the final state plus two tagged b quarks.** A reconstructed $t\bar{t}$ event from Run I is displayed [3].

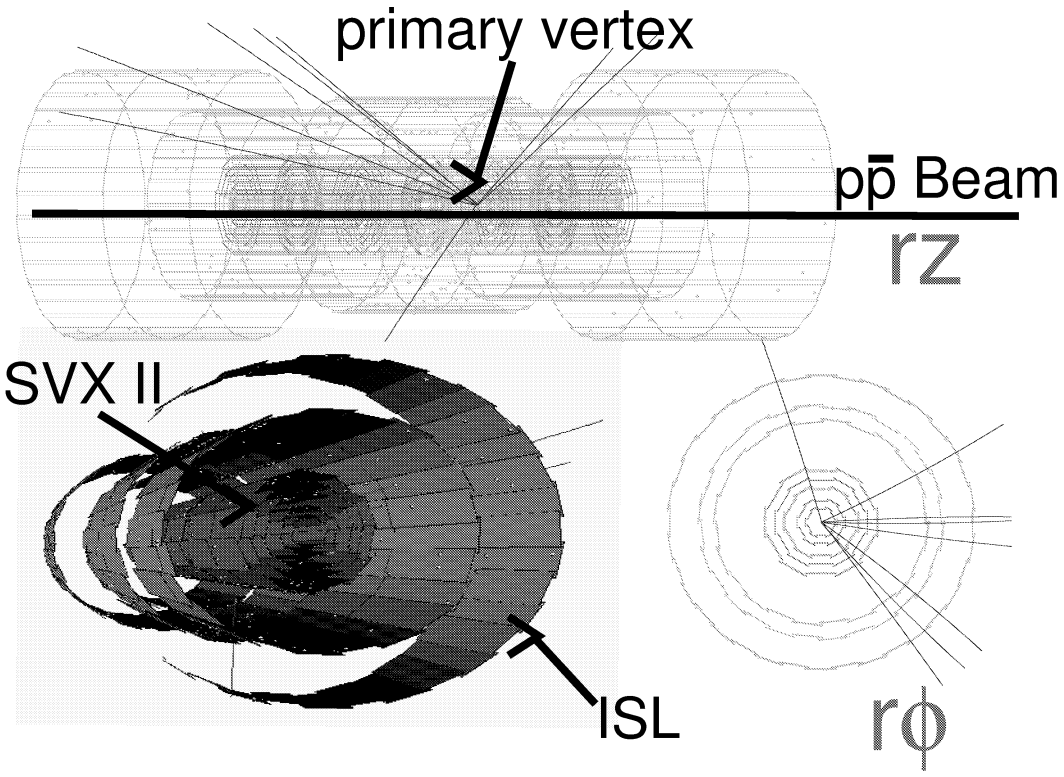


Figure 4.12: **A preliminary event display for Run II.**
The event display is rotatable and zoomable. A Monte Carlo event is displayed, taking into account the geometric structure of SVX II and the ISL. The event display was developed in Karlsruhe [61].

Single Top production

Top quarks can be produced along with a b quark through electro-weak interactions according to Standard Model predictions. Although the cross section is smaller than that for $t\bar{t}$ production, it is important to pursue this study because single top production can be used to measure the CKM matrix element V_{tb}. The process is furthermore sensitive to new physics at the $t - W - b$ vertex, like contributions from a W' or flavor changing neutral currents (FCNC). At the Tevatron two different diagrams are expected to contribute. One s-channel and one t-channel process, both with different cross sections and different methods of analysis. In the s-channel process two quarks annihilate to a highly virtual W-boson, that in its rest frame has enough energy to decay into a top quark and a down-type quark (see figure 4.13). Within the Standard Model the down-type quark is in most cases a bottom quark. In the second process, the W-gluon fusion process, a gluon splits into two down-type quarks($d\bar{d}$,$s\bar{s}$, $b\bar{b}$) while a quark emits a W-boson (see figure 4.14). This boson couples to one of the quarks of the gluon splitting and so can create a single top quark.

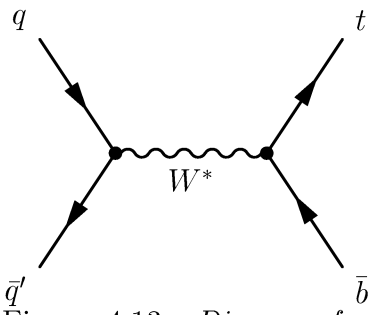


Figure 4.13: *Diagram for the s-channel process of single top quark production. Signal is* $W + b + \bar{b}$.

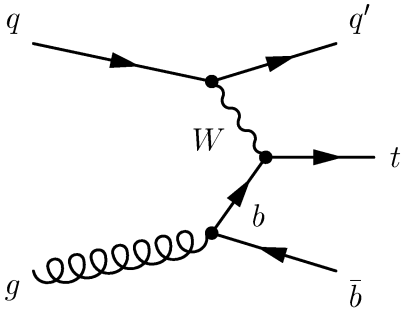


Figure 4.14: *Diagram for the* W*-gluon fusion process of single top quark production. Signal is* $W + b + q$ *(one* b *is soft and vanishes in forward direction).*

The s-channel process has the smallest theoretical uncertainties and the smallest cross section 0.73 ± 0.04 *pb* [43, 44]. To reconstruct the t quark, it is necessary to choose the corresponding b quark ($t \to Wb$), see figure 4.13. In the lepton channel of the W, the b is defined by the corresponding lepton (b with high η for l^+ and b with low η for l^-). The t quarks tend to go into the forward direction, and the $\bar{t}$ quarks tend to go backwards. This is a result of the W-boson asymmetry for $p\bar{p}$ collisions at Tevatron energies [46]. An up quark in the proton carries on average more momentum than a down quark, so the W-bosons produced in proton-antiproton collisions tend to follow the direction of the up quark: W^+-bosons tend to go along the proton direction, and W^--bosons along the antiproton direction.
The cross section for the W-gluon fusion process is 1.70 pb at $\sqrt{s} = 1.8$ TeV and 2.44 pb at $\sqrt{s} = 2.0$ TeV with an estimated uncertainty of 15% [43, 44]. The uncertainty arising from the parton distribution functions is assumed to be 10%. Other sources are the uncertainties in the top quark mass and the scale in the bottom quark distribution function and the strong coupling. For comparison, the cross section for the LHC is 245 pb. The final state of this process consists of the decay products of the $W+$ two b and one light quark jet. The bottom jet from the gluon splitting has only little transverse momentum and is in most cases not detectable. QCD background is avoided, by only using the cases, where the W decays leptonically. Reconstruction of the t quark is done by reconstruction the b and W.
In Run II one benefits from much more data and a higher detector acceptance, especially the b-tagging efficiency (new tracking system) will be of fundamental importance and a good lepton identification (plug calorimeter upgrade; muon system upgrade). The electron acceptance is increased by 33%, the muon acceptance by 12% and the efficiency for tagging at least one b-jet in an event with 2 b-jets ($t\bar{t}$) 60.1% [2].

The single top is an important probe of the Standard Model, the expected production rate is 1/3 that of $t\bar{t}$. CDF has a reasonable chance to discover the single top in Run II.

Process	cross section in pb	expected number of events for $\int \mathcal{L}dt = 2fb^{-1}$
S-Channel	0.9	1760
Wg-Fusion	2.4	4880
$t\bar{t}$	7.6	15120
$Wb\bar{b}$	13.8	27700
$Wc\bar{c}$	48.9	98000

Table 4.5: Cross sections and expected numbers for single top of events for the signal and main background processes in Run II. The number of events is the product of the cross section times the integrated luminosity, all decay modes are included. The detector acceptance is not taken into account in these numbers. [43]

4.3 Light Higgs discovery perspectives with a precision tracking system.

With the new vertex detectors, better triggering, and other improvements, the improvement to the sensitivity for the Higgs will be roughly a factor of 50 compared to the full Run I sample.

Search for Higgs in the Standard Model

The Higgs discovery will ultimately rely on optimal b-tagging, especially double b-tagging. Additionally 3D tracking is ultimately needed to deal with the different kinematics. The larger silicon coverage with the ISL will increase the chance to find a Higgs boson. Furthermore Layer 00 is largely improving the double b-tagging efficiency. Standard Higgs bosons are produced singly or with a W or Z at the Tevatron with cross sections in the range of 0.1-1.0 pb. As figure 4.15 indicates, the cross section is the largest for single Higgs production from gluon fusion, with the WH and ZH modes lower by nearly an order of magnitude. Nevertheless, the sensitivity is greater for the WH and ZH modes, since for single Higgs production the background from dijet events is too large. Higgs searches are divided in two regions below and above about 135 GeV, the mass at which the dominant Higgs decay modes change over from $b\bar{b}$ to WW. At lower masses, the decay mode of the accompanying W or Z determines the final state. The modes with the largest cross sections for masses below 135 GeV are:

- All-hadronic modes WH and ZH with W or Z decaying into $q\bar{q} \Rightarrow$ final state: $q\bar{q}b\bar{b}$.
  The main contribution supporting this modes will come from the improved $b\bar{b}$ mass resolution and the better covering, due to kinematics ; the $b\bar{b}$ pairs tend to have lower p_T.

- WH, where $W \rightarrow l\nu$ with final state: $l\nu b\bar{b}$.

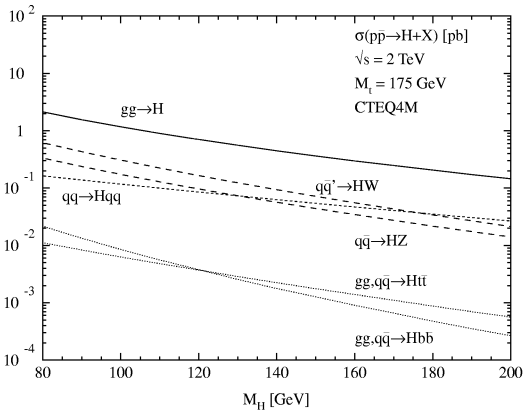


Figure 4.15: *Cross sections for the production of a Standard Model Higgs as a function of Higgs mass for various production modes. [52]*

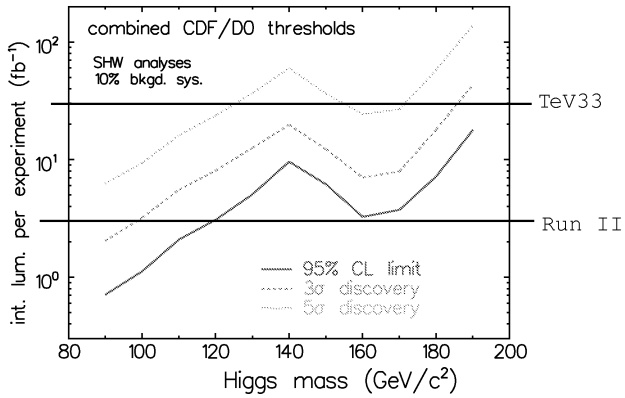


Figure 4.16: *Integrated luminosity delivered per experiment to either exclude the SM Higgs at 95% confidence level or discover it at the 3σ or 5σ levels, as a function of Higgs mass. The combined statistical power of CDF and D0 is needed. [52]*

Only at the end of Run II with high integrated luminosity collected by the CDF and D0 experiment, they will be sensitive for a possible SM Higgs discovery.

The double b-tagging efficiency with the silicon tracking system alone will be of uttermost importance. The next crucial issue is the silicon coverage to tag all bs and the $b\bar{b}$ mass resolution.

- ZH, where $Z \rightarrow l^+l^-$ with final state: $l^+l^-b\bar{b}$.
  The requirement are e^+e^- or $\mu^+\mu^-$ with an invariant mass consistent with that of the Z, recoiling against two jets with two b-tags.

- ZH, where $Z \rightarrow \nu\bar{\nu}$ with final state: $\nu\bar{\nu}b\bar{b}$.
  Exclusively two tagged bs are required and a large missing transverse energy.

For all these discovery channels, the high precision tracking system provides the needed possibility for an efficient double b-tagging.
For m_H = 120-190 GeV the mode $H \rightarrow WW$ dominates. The search channels $l^{\pm}l^{\pm}jj$, $l^{\pm}l^{\pm}\nu\bar{\nu}$ and $l^{\pm}l^{\pm}l^{\pm}$ are not so much supported by the vertex sensors, but it is still needed to provide the tracks for the leptons.
To discover the Higgs at the Tevatron the combined statistical power of CDF and D0 is needed, see figure 4.16.

4.4 Run II expected event yields

With the higher luminosities, the better covering, the improved vertexing and the new trigger scheme we expect around:

- 2000 $t\bar{t}$
- 4.3 million $W^{\pm} \rightarrow l\nu$
- 6400 di-jets with m$>$ 600 GeV
- 15000 reconstructed $B^0 \rightarrow J/\Psi K_S^0$
- 10000 $B^0 \rightarrow \pi^+\pi^-$
- 9000 $B_S \rightarrow J/\Psi\phi$

This is a conservative expectation [2].

Chapter 5

Silicon – a semiconductor

5.1 Silicon properties

Silicon comes from the Latin word silex; silicis, meaning "flint". The physical properties of silicon can be described as a hard, dark-gray solid with a bluish tinge. At ordinary temperatures, silicon is impervious to air. At high temperatures, silicon reacts with oxygen, forming a layer of silica not reacting any further. Silicon is important in plant and animal life. Diatoms in both fresh and salt water extract silica from the water to use as a component of their cell walls. Silicon does not occur in the free, elemental state, but is found in the form of silicon dioxide and complex silicates. Jöns Jacob Berzelius is generally credited with the discovery of silicon in 1824. Deville prepared crystalline silicon in 1854, a second allotropic form of the element. Sensor technology makes use of the semiconductor characteristics of silicon. The basic principles of semiconductors are described in [12] and [13]. Its properties are shown in table 5.1.

Semiconductor:
Solid matter, which isolates at low temperatures and shows a measurable conductance at higher temperatures. The specific conductance of (10^2 to $10^{-9}\Omega^{-1}\text{cm}^{-1}$) lies somewhere between metals and insulators. Since the development of Quantum Mechanics the electrical conductance can be explained with the covalent bond in the crystal lattice. Bound electrons can be excited by inducing energy above threshold energy (gap energy), e.g. energy from light, x-ray, β-ray, etc.
Band model and electric conductivity
Every solid contains electrons. The important question for electrical conductivity is how the electrons responds to an applied electric field. Electrons in crystal are arranged in energy bands[1], separated by regions in energy for which no wavelike electron orbital exist. These forbidden regions are called energy gaps, band gaps E_g or just forbidden gaps, and result from the interaction of the conduction electron waves with the ion cores of the crystal. The crystal will behave as an insulator, if the number of electrons

[1] Collections of fine split energy levels due to the electron interference in a densely packed solid.

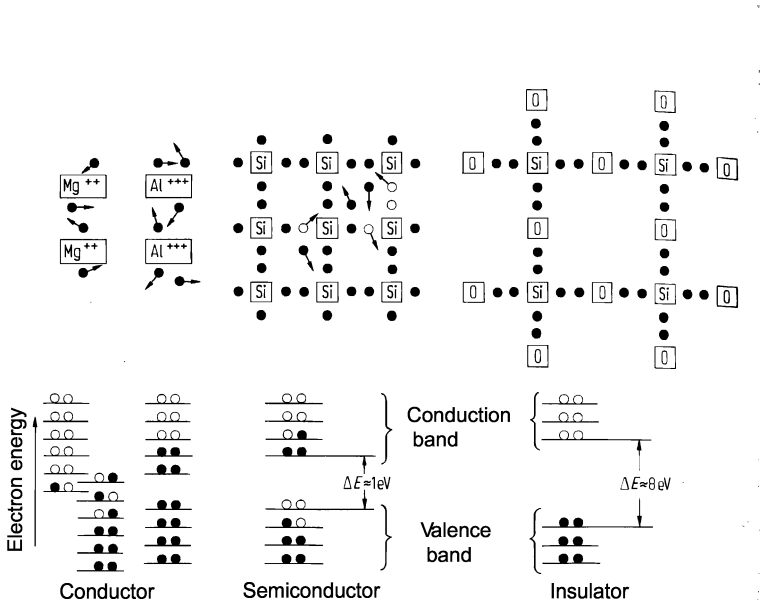


Figure 5.1: *Scheme of conductor, semiconductor, insulator.*
Upper section: electrons and holes in the crystal lattice.
Lower section: Electronic Band Scheme. (• electron, ○ hole)

is such that energy bands are either filled or empty. In this case no free electrons exist which can move in an electric field, because there is no continuous way to travel between bands. The crystal will act as a metal if one or more bands are partly filled (10% to 90%). The crystal is a semiconductor if all bands are entirely filled, except for one or two bands slightly filled or slightly empty. The partly empty band is the conduction band and the complete filled is the valence band. The electrical conductance can then be described by the gapwidth between valence and conduction band. Figure 5.1 shows schematically the band configurations for conductors, semiconductors and insulators.

Free electrons and holes - donors and acceptors
Impurities are changing the electrical properties of a semiconductor. The deliberate addition of impurities to a semiconductor is called **doping**. Pentavalent[2] impurity atoms, giving up electrons, are called **donors**. 4 electrons on the donor (e.g. P, As or Sb) form tetrahedral covalent bonds similar to silicon, and the fifth electron is available for conduction. These atoms give up an electron to the conduction band, when ionized. Vice versa trivalent[3] atoms are only able to complete their tetrahedral bonds by taking an electron from a Si-Si bond, leaving a hole in the silicon valence band. The positive hole is then available for conduction. These atoms are called **acceptors** (e.g. B, Al, Ga

[2]atom with 5 valence electrons
[3]atom with 3 valence electrons

and In), accepting electrons from the valence band, when ionized. Doping the semiconductor changes the band structure, a donor level is located just below the conduction band and acceptor levels sit just above the valence band. Therefore the gap decreases and less energy is needed for an electron to change bands. The new structure due to doping is displayed in figure 5.2. This is of practical use in semiconductor detectors, where the energy needed to produce a free electron is proportional to the resolution.

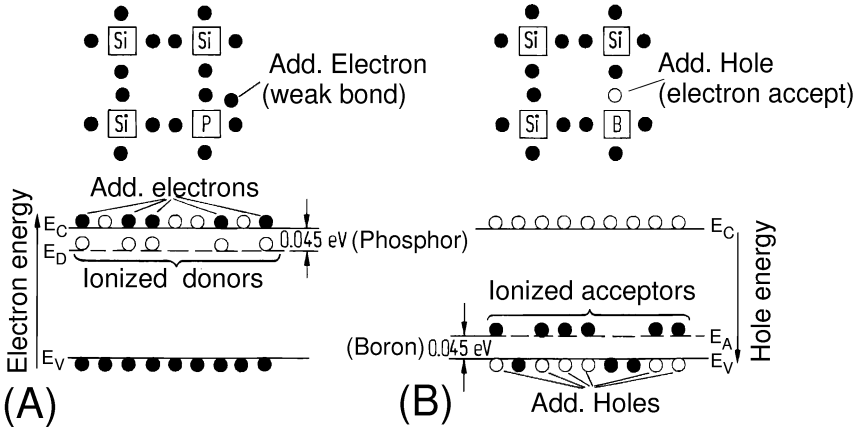


Figure 5.2: *Conductivity due to impurity states.*
A.) n-type silicon: Electrons as charge carriers. We see excess charge near the phosphorus impurity.
B.) p-type silicon: Holes as charge carriers. A positive hole can be seen, as one electron was removed from a bond to complete the tetrahedral bonds of the Boron atom.

N-type silicon is produced by neutron doping, the crystal is irradiated by slow neutrons and in the reactions:

$$^{30}Si \ + n \ \longrightarrow \ ^{31}Si + n\gamma \tag{5.1}$$

$$^{31}Si \ \longrightarrow \ ^{31}P \ + \beta^- \ + \ \bar{\nu} \tag{5.2}$$

some ^{30}Si atoms are changed into ^{31}P donor atoms. For silicon detectors n-type silicon is used to avoid problems related to the electron accumulation layer. The resistivity ρ of doped silicon material is:

$$\rho \ = \ \frac{1}{\mu_n n \ + \ \mu_h p} \tag{5.3}$$

where q is the electron charge[4], μ_n / μ_h are the mobilities of electrons and holes respec-

[4] $q = e = 1.6 \times 10^{-19}$ C

tively, with mobility $\mu = \frac{\nu}{E}$ (E the electrical field; ν the drift velocity), n and p are the densities of electrons and holes respectively (see below).
In material dominated by one type of impurity, e.g the dopant density is much larger than the intrinsic carrier concentration, one gets the following expression for the resistivity:

$$\rho = \frac{1}{q(q\mu N_d)} \tag{5.4}$$

Intrinsic silicon
We see some material properties of silicon in table 5.1. In thermal equilibrium the rate of generation of free charge carriers and recombination is equal. In intrinsic (undoped) semiconductors we have the same number of electrons and holes leading to:

$$np = n_i^2 \tag{5.5}$$

where n is the electron density and p the hole density, n_i is the intrinsic density.
Equation 5.5 is also valid for doped material. It is obvious, that an increase of electrons results in a decrease of holes and vice versa. Equation 5.5 is called the *law of mass action for charge-carrier concentration.* In thermal equilibrium the population of the allowed energetic states –taking into account the Pauli principle– is described by the Fermi-Dirac distribution function:

$$f_D(E) = \frac{1}{1 + exp[(E - E_f)/kT]} \tag{5.6}$$

with E_f=Fermi energy, k=Boltzman constant and T=temperature in Kelvin.
In lightly n–doped material, with a Fermi energy level near the conduction band $(E_C - E_f) \ll kT$ is valid and equation (5.6) is reduced to the Maxwell–Boltzmann distribution.

$$f_M(E) = exp[\frac{-(E - E_f)}{kT}] \tag{5.7}$$

The electron density in the conduction band is now given by multiplying formula (5.7) and $g(E)$, the density of the population in the conduction band, and then integrating.

$$n = \int_{E_C}^{E=\infty} f_M(E)g(E)dE \tag{5.8}$$

Some iterations and approximations [12] later we get the charge carrier density with:

$$n = N_C exp[-\frac{(E_C - E_f)}{kT}] \text{ with } N_C = 2(\frac{2\pi m_n^* kT}{h^2})^{\frac{3}{2}} \tag{5.9}$$

Analog for lightly p–doped material:

$$p = N_V exp[-\frac{(E_f - E_V)}{kT}] \text{ with } N_V = 2(\frac{2\pi m_p^* kT}{h^2})^{\frac{3}{2}} \tag{5.10}$$

With N_C for conduction band and N_V as effective state density in the valence band. E_C, E_f, and E_V are the energies of the condition band, Fermi level and valence band. The m_n^* and m_h^* stand for the effective masses of electrons and holes respectively, h is the Planck constant and the factor 2 is derived from the 2 possible spin states of the electrons.
In an intrinsic silicon substrate —the size of a standard silicon sensor used in high energy physics— we have with intrinsically $\sim 10^9$ free charge carriers but *only* $\sim 2 \times 10^4$ generated electrons induced by an ionizing particles. The resulting signal would be lost in the number of free charge carriers. We have to find a way of reducing the free charge carriers. The realization is done using p- and n-type silicon in a *reverse biased pn–junction.*

The pn junction
In thermal equilibrium directly after production of the pn–junction (see figure 5.3a) the electrons from the donors are mainly localized in the n-type region, where they neutralize the charge of the dopant ions. Vice versa the holes are in the p-type region to compensate their acceptors. According to thermic mobility the free charge carriers diffuse through the phase boundary, mix and recombine (see figure 5.3b). During that time positive donor ions are remaining in the n-type silicon and negative acceptor ions in the p-type region. Only a small fraction of free charge carriers are diffusing from the deep regions of the homogeneous semiconductor material, therefore we still have neutrality here. The main part of free charge carriers is coming from the boundaries, we have a region of uncompensated ionized extrinsic semiconductor material. At the pn–junction diffusion and recombination produces a space-charge layer which creates an electrical field $\mid E \mid$ and prevents further diffusion. A dynamic equilibrium is created: diffusion flow and field current of both charge carriers are compensating each other at the pn–junction. We start with the **Poisson–equation** describing the electrostatic potential $\phi(x)$:

$$\frac{\partial^2 \phi}{\partial x^2} = -\frac{1}{\varepsilon_{SC}\varepsilon_0}\varrho(x) \tag{5.11}$$

Assuming complete ionization the charge carrier density $\varrho(x)$ with the impurity densities N_A and N_D (acceptor and dopant respectively) is described by:

$$\varrho(x) = -q[n(x) - p(x) + N_A - N_D] \tag{5.12}$$

In the very localized contact region of n- and p-type silicon, the free charges compensate the charges of ionized and uncompensated impurities.
In figure 5.3c we see the depleted boundary layer. This leads to the **space-charge region** w[5] (Figure 5.3c):

$$w = x_p - x_n \tag{5.13}$$

[5]depleted of free charge carriers

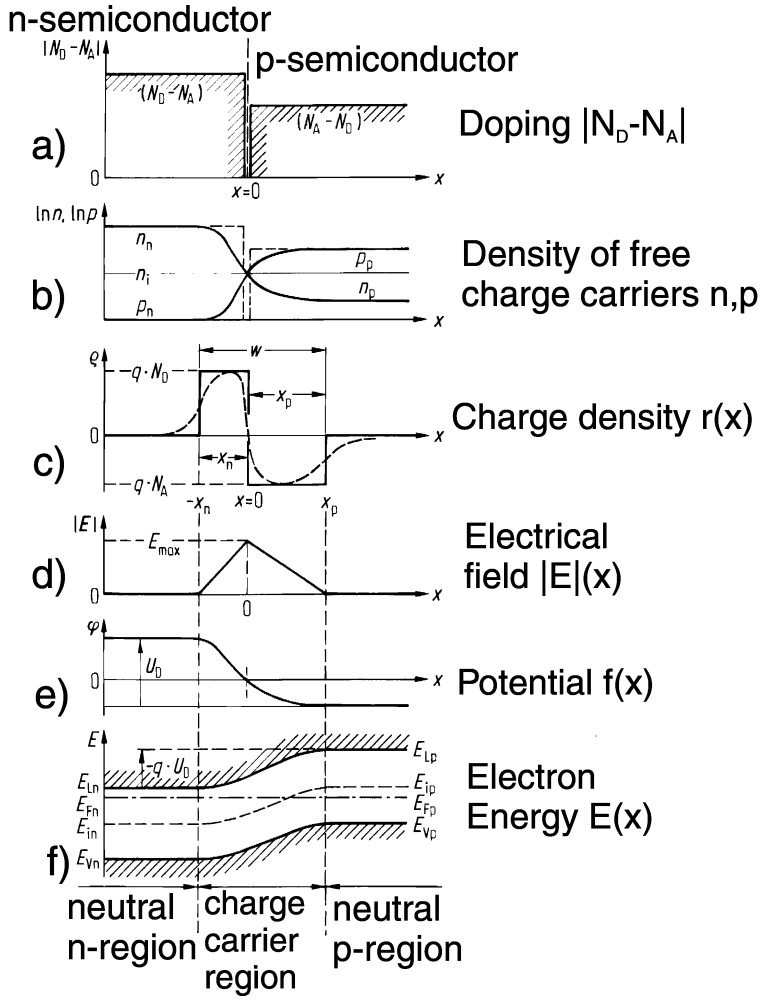


Figure 5.3: *pn–junction.*
Doping, mobile charge density, charge density, electrical field, potential, electron energy across the pn–junction at equilibrium.

Integration of the Poisson–equation including the depletion approximation[6] supplies a linear behavior of the **electrical field strength** $|E|$ (Figure. 5.3d)
N-type region $-x_n \leq x \leq 0$

$$|E_n(x)| = +\frac{qN_D}{\varepsilon_{SC}\varepsilon_0}(x + x_n) \tag{5.14}$$

P-type region $0 \leq x \leq x_p$

$$|E_p(x)| = +\frac{qN_A}{\varepsilon_{SC}\varepsilon_0}(x - x_p) \tag{5.15}$$

[6]Assuming an **'abrupt'** change of $\varrho(x)$ (see figure. 5.3c – full line)

Integrating twice leads to the parabolic behavior of the **potential** $\phi(x)$ (Fig.: 5.3e) with the boundary condition $\phi(x=0)=0$
N-type region for $-x_n \leq x \leq 0$

$$\phi_n(x) = -\frac{1}{2}|E_{max}|x_n.[(\frac{x}{x_n})^2 + 2\frac{x}{x_n}] \tag{5.16}$$

P-type region $0 \leq x \leq x_p$

$$\phi_n(x) = +\frac{1}{2}|E_{max}|x_p.[(\frac{x}{x_p})^2 - 2\frac{x}{x_p}] \tag{5.17}$$

The total difference of potential in the space-charge region gives the **diffusion voltage** $V_{diffusion}$

$$V_{diffusion} = \phi_p(+x_p) - \phi_n(-x_n) = \frac{1}{2} \mid E_{max} \mid w \tag{5.18}$$

An **external voltage** $\pm$V will disturb this equilibrium of spontaneous, generation and recombination of electrons. The external voltage increases or decreases -depending on polarity- the potential barrier of the pn–junction. Therefore we have a decrease or an increase of the depletion width (see figure 5.4a,b).

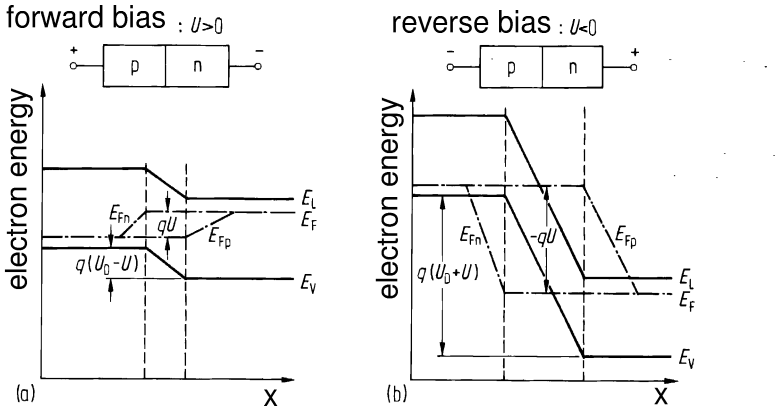


Figure 5.4: *pn-junction with forward and reverse bias.*
a) forward bias; b) reverse bias (case for silicon microstrip sensors)

The depletion zone width w is given by:

$$w \sim \sqrt{V_{diffusion} - V_{depletion}} \tag{5.19}$$

$V_{diffusion}$: diffusion voltage, $V_{depletion}$: depletion (bias) voltage.
With 5.4 the depletion zone width w can be expressed in terms of resistivity [14].

$$w = \sqrt{2\epsilon\rho\mu V_{depletion}} \tag{5.20}$$

or

$$V_{depletion} = \frac{w^2}{2\epsilon\rho\mu} \tag{5.21}$$

These equations show the necessity of using high resistivity silicon for detectors in high energy experiments, see also chapter 6.2.1. Since there is a voltage dependent charge associated with the depletion zone, we have a *junction capacitance*, defined in the following manner:

$$C_j = \frac{dQ}{dV_B} = \frac{dQ}{dw}\frac{dw}{dV_{depletion}} \tag{5.22}$$

which finally leads to

$$C_j = \sqrt{\frac{\epsilon}{2\mu\rho V_{depletion}}} \tag{5.23}$$

Parameter	Symbol	Unit	Value
Atomic number			14
Relative atomic weight			28.0855
Structure			diamond
Lattice constant	a_0	Å	5.4307
Lattice Orientation			$< 111 >$
Electron Configuration:			1s22s22p63s23p2
Density	ρ	gcm^{-3}	2.328
Melting point	T_m	°C	1412
Boiling point	T_m	°C	2355
Gap energy (300 K)/(0 K)	E_g	eV	(1.124)/(1.170)
Dielectric constant	ϵ_r		11.7
Intrinsic carrier density	n_i	cm^{-3}	1.45×10^{-10}
Mobility			
–of the electrons	μ_n	$cm^2\,[Vs]^{-1}$	1350
–of the holes	μ_p	$cm^2\,[Vs]^{-1}$	480
Effective density of states			
–of the conductance band	N_c	cm^{-3}	3.22×10^{19}
–of the valence band	N_v	cm^{-3}	1.83×10^{19}
max. electrical field	E_{max}	$V\mu m^{-1}$	30
Thermal expansion coefficient		$1/C^0$	2.5×10^{-6}
Intrinsic resistivity		$k\Omega cm$	235

Table 5.1: *Silicon properties.*

Chapter 6

Silicon Sensors and their properties

In this chapter the working principle and the basic sensor parameters of silicon-microstrip-sensors is described in general. The specifications for the ISL, named in appendix B, are based on the assumptions explained in this chapter. The main sensor faults and their detection strategies are described.

6.1 Working principle and structure

A good overview of silicon sensors can be found in [14]. The function of a silicon microstrip detector is illustrated in figure 6.1 . An ionizing particle penetrates through a fully depleted silicon n^- doped slice. The generated holes drift along the electrical field, created by the bias voltage, to the p^+ doped strips[1]. The charges collected on the doped strips are then induced, by capacitive coupling, to the aluminium (Al) readout strips, which are directly connected[2] to the charge-preamplifier of the readout chip. The final position of the penetration is then calculated by analyzing the pulseheight distribution on the affected strips (see figure 6.2).

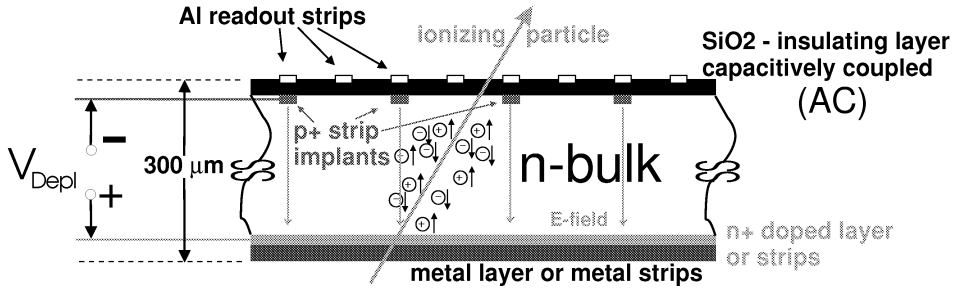


Figure 6.1: *Working principle of an AC coupled silicon micro strip detector.*

[1] on a double sided sensor the electrons drift to the n^+ doped strips, with orthogonal or stereo strip layout

[2] by wire-bonding

The strip pitch is a very important parameter in the design of the microstrip sensor. In gaseous detectors with a high charge multiplication a signal distribution over several sense wires are welcome to reconstruct the shape of the charge distribution and find the center. In silicon detectors there is no charge multiplication and small charges will be lost in the noise distribution. Therefore signal spreading over many strips would result in a loss of resolution. For single strip events the track position is given by the strip number.

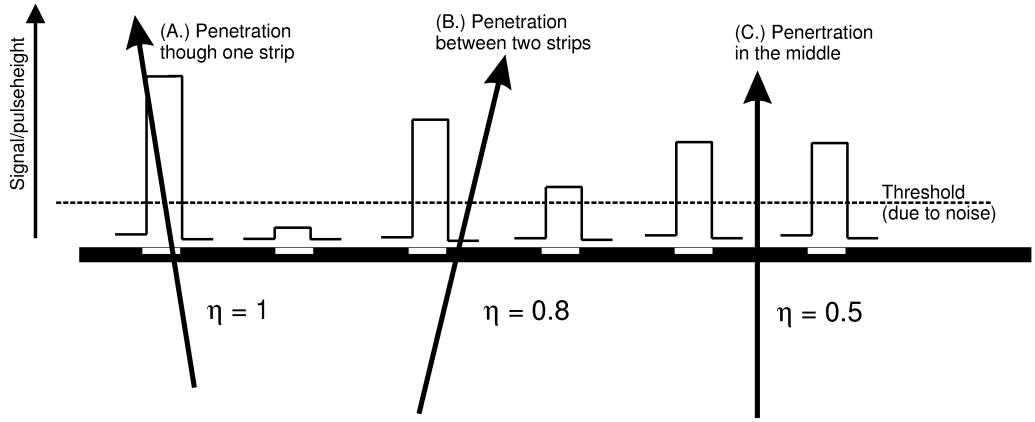


Figure 6.2: **Cluster Size depending on particle location.**
Figure (A.) shows a single strip cluster, the complete charge is collected on one strip.
Figure (B.) displays a two strip cluster the second strip signal lies just above the threshold.
In Figure (C.) clear charge distribution provides best localization precision.
The parameter η is explained in formula 6.1.

For tracks generating enough charge on two strips to exceed the threshold value, the position can be determined more precisely by either calculating the 'center of gravity'[3] or by using an algorithm, that takes into account the actual shape of the charge distribution[4] and the acceptance of the sensor. The best localization is achieved for tracks in the middle of two strips, since the charge is shared equally and the influence of noise is small. The signal for tracks near one strip have poor localization properties, because the remaining small signal on the neighbouring strips is often in the range of or below the noise level. The 'center of gravity' method makes use of the parameter η where:

$$\eta = \frac{PH_L}{PH_L + PH_R} \tag{6.1}$$

PH_L and PH_R are the pulse heights measured on the left and right strip respectively.

[3] Assuming a uniform charge distribution, a track crossing between two strips at $\frac{3}{4} \times pitch$ will store $\frac{1}{4} \times charge$ on the left strip and $\frac{3}{4} \times charge$ on the right strip.

[4] Approximately a Gaussian distribution, due to the diffusion profile.

Other determining factors for the pitch is the track occupancy[5], the number of channels the data acquisition is able to handle and simply the enormous cost of having a large number of channels.

6.2 Sensor parameters

All parameters have to be specified according to their specific need, which will be discussed in the following. Certain interdependencies must be balanced to get best results. All parameters must then be controlled during prototyping (chapter 7) and production (chapter 8). In the following we will discuss geometric structures and their effects on the functionality like bias and guard ring, implant and Al strip widths and thickness. Furthermore the fundamental electrical parameters are introduced to get the best running conditions.

Bias Ring

Main contact to apply the bias voltage. It runs around the whole sensor to ensure a single potential for all strips. It connects to all bias resistors, therefore supplying all implants with voltage, independently of whether their aluminium (Al) electrodes are connected to the readout, which is, in our case, not true for the small stereo strips.

Guard Ring

The guard ring functions to shape the field inside the sensitive area and to minimize edge effects. It drains the leakage currents from the edges of the detector. For the purpose of field shaping, an implant ring with the same type as the strip implant is located underneath the guard ring.

N-side isolation

Isolation of n^+ strips implanted on a n bulk is achieved via implantation of p^+ surrounding each strip, with a individual or "atoll" configuration. The additional p^+ implants are necessary to dissipate the electron accumulation layer at the $Si - SiO_2$ boundary. The aim is to cover as much area as possible of the gap between strips without actually contacting the strips. The yield should not be lowered by coming too close.

Aluminium strips and implant

The Al electrode should be narrower than the implant underneath [16] to reduce the electric field strength through the bulk in the vicinity of the implant strip edges, since the electrical field causes the undesirable "micro-discharge" a precursor to breakdown of the junction. This leads to a 14 μm Al electrode with a 18 μm implant for the Micron sensors and 16 μm / 22 μm for the HPK sensors.

In addition increasing the width of the strip implant increases the capacitance (mainly the interstrip capacitance) seen by the amplifier and the full depletion voltage while the Al electrode width defines with its thickness the resistivity.

The full depletion voltage of a strip array is greater than that of planar diodes. Using the strip pitch p, strip width w for p^+-strips and w' for n^+-strips, and diode thickness

[5] In the case for the ISL the occupancy is mostly determined by the large radius (see chapter 3.2).

d, the following relation is given in reference [18],

$$\frac{V_D}{V_{D0}} = 1 + \frac{2p}{d}[f_p(\frac{w}{p}) + f_n(\frac{w'}{p})] \tag{6.2}$$

where V_{D0} is the full depletion voltage for planar diodes and the functional forms f_p and f_n are given in reference [18]. Discussion about depletion voltage will follow in section 6.2.1.
The total capacitance for the p side strips can be expressed by [17]:

$$C_{p-side}[pf/cm] \sim (0.75 + 1.8\frac{w}{p}) \tag{6.3}$$

n^+ strips have larger capacitance than p^+ strips since the charge accumulated between n^+ strips makes the n^+ cathode effectively higher.

$$C_{p-side}[pf/cm] \sim 2(1.5 + \frac{w'}{p}) \tag{6.4}$$

To conclude:
The strip pitch is defined by the necessary resolution. The strip capacitance can be adapted by changing the implant width. The necessary conductivity of the Al electrode can later be achieved by modifying the thickness of the Al strip (see section 6.2.7). Balance between depletion voltage (sec.: 6.2.1) and strip capacitance (sec.: 6.2) must be achieved, but the main determining factor of the depletion voltage is nevertheless the bulk resistivity.

6.2.1 Depletion Voltage ($V_{depletion}$)

To ensure full charge collection in the detector, the silicon is depleted of free and mobile carriers around the pn junction, by applying $V_{bias} \geq V_{depletion}$ in reverse direction. To provide rapid and maximum charge-collection, the whole silicon volume should be depleted. The drift velocities and therefore the drift times and widths of the charge distribution are also affected by the bias voltage. Wider distributions lead to events where the charge is shared between two strips. For these events we can calculate the center of gravity which has an immediate positive consequence for the localization of the penetrating particle. Micro-discharge is another critical issue, which can be avoided by limiting $V_{depletion}$ safely below the micro-discharge voltage [16]. Another criteria for a large silicon vertex detector is the ability to apply one single V_{bias}, therefore $V_{depletion}$ should not vary over the individual sensors.
The depletion layer acts like a parallel plate capacitor, therefore the bulk capacitance per unit area is determined by the depth of the depletion layer d:

$$C_{bulk} = \frac{\epsilon_{Si}}{d} = \sqrt{\frac{\epsilon}{2\mu\rho V_{bias}}} \tag{6.5}$$

where ϵ_{Si} is the permeability of the bulk silicon, μ the mobility and ρ the resistivity. The thickness d is related by

$$V_{bias} = \frac{qd^2|N_{effective}|}{2\epsilon_{Si}} = \frac{d^2}{2\epsilon_{Si}\rho\mu} \tag{6.6}$$

where $N_{effective}$ is the effective charge carrier density, which is the number of donors minus the number of acceptors, and q is the absolute value of the electron charge.
After depleting the whole bulk, $d = d_{depletion} = d_{bulk}$ will remain constant. This gives a characteristic behavior C_{bulk} over V.

$$C_{bulk} = \begin{cases} \sqrt{\frac{q\epsilon_{Si}|N_{effective}|}{2V_{bias}}} & V_{bias} \leq V_{depletion} \\ \frac{\epsilon_{Si}}{d_{depletion}} & V_{bias} > V_{depletion} \end{cases} \tag{6.7}$$

The value of $V_{depletion}$ is directly observable in a CV plot, where C_{bulk} becomes constant and the curve flattens. The absolute $V_{depletion}$ mainly depends on the resistivity ρ.

6.2.2 Leakage Current ($I_{leakage}$)

A low total leakage current is one of the major criteria for the quality and functionality of a microstrip detector. Leakage current is a source of noise in a final readout system, which should be kept as low as possible. Leakage current shows up in all detectors coming from generated electron-hole pairs in the silicon in the presence of an electrical field. The leakage current is proportional to the depletion layer thickness d of the sensor which is proportional to $\sqrt{V_{depletion}}$. It should be constant after reaching $V_{depletion}$. Deviations from this rule show flaws in the detector, e.g. variations in processing. The leakage current should not exceed a certain limit, excess leakage current results in noise and hints to defects. Finding the sources of a high total leakage current could help to improve process methods. (see chapter 9.2)

6.2.3 Strip Capacitance (C_{strip})

C_{strip} includes all capacitances of a readout strip including interstrip capacitances and strip-to-back capacitance; it is the total capacitance load to the chip amplifier. This is a major noise source of a silicon detector.
In most cases it is furthermore a fine probe for strip defects as there are strip breaks, shorts between several strips and shorts to the implant[6]. A broken strip shows a lower capacitance, but the capacitances of both strip ends sum up to the nominal value. Shorted strips come in pairs or groups; the capacitance will then be N times the nominal capacitance. Pinholes have a short or a low ohmic connection to the implant, which changes the AC-coupling to DC coupling and allows a direct flow of the current into the chip amplifier; in this case the capacitance is much higher than the nominal one.

[6]known as a "pinhole" (see section 6.2.8)

The capacitance measurement of pinholes is highly frequency dependent, a quasistatic instrument must be used. By measuring the value for every single strip, we have furthermore a quality control for the uniform load of the preamplifier.

6.2.4 Bias Resistors (R_{bias})

The bias voltage to the sensor is supplied through a set of polysilicon resistors, connecting the implant strip to the bias ring, which is bonded to the biasing terminal. Noise contributions[7] from the bias resistors are proportional to $\sqrt{\frac{kT}{R}}$ where k is the Boltzman constant, T the temperature and R the bias resistor. The $\sqrt{\frac{kT}{R}}$ dependency imposes the requirement for a very high value of bias resistance. Variations of R_{bias} lead to voltage differences among individual strips and a non-uniform field. Another upper limiting factor are the associated potential differences between neighbouring strips. Reliable polysilicon resistors with very high resistivity and small deviation from the specified value are difficult to process. The specification for the ISL sensors is R_{bias} = 4.0 - 10 MΩ with ±10% variation within a single sensor. The bias resistors are determined by measuring the voltage drop δV (V_x) over the resistor, with depletion voltage supplied, and the leakage current (I_x) through the diode by shortening resistor with an ampere meter. The bias resistor is then calculated by:

$$R = \frac{V_x V_{depletion}}{(V_x - V depletion) I_x} \tag{6.8}$$

with $V_{depletion} = V_x + V_{diode}$ and $R_{diode} = \frac{V_{depletion}}{I_x}$

6.2.5 Coupling Capacitance ($C_{coupling}$)

The coupling capacitance is measured between the implant and the aluminium readout strip, which is directly bonded to the readout electronics. The coupling capacitance should be large, it is directly proportional to the signal. A large capacitance means a thin isolation layer between the implant and Al strip, which is difficult to achieve with a high reliability without creating pinholes. Shorts or ohmic connections between Al and implant would destroy the AC design, creating a DC coupling with a free bulk charge flow into the preamplifier. This limits the coupling capacitance to the manufacturing process reliability. The value 20 pF/cm was specified to allow reliable production of two-layer capacitor dielectric (SiO_2 and Si_3N_4) while preventing losses to neighbouring channels. The percentage of dead channels allowed was chosen to ensure cost effective production.

[7] thermal noise

6.2.6 Interstrip Capacitance ($C_{interstrip}$)

The interstrip capacitance is one of the major contributions to the capacitance load into the amplifier. It should have a certain value to share charge between two or more strips. Spatial resolution is increased by signals distributing charge on two or three strips, for one could calculate the 'center of gravity'. The best localization is achieved for tracks crossing in between two strips (see section 6.1). Therefore good charge sharing between direct neighbours is wanted. In order to get most of the signal into the preamplifier, the interstrip capacitance should be much smaller than the coupling capacitance. These two restrictions give the specified value 1.0 pF/cm and the ratio $\frac{C_{interstrip}}{C_{coupling}} = \frac{1.0}{20}$ for the ISL sensors. This value is mainly determined by sensor layout and stripwidth to pitch ratio.

6.2.7 Aluminum Resistivity (ρ_{Al})

There is a correlation between the resistance of the metal strip and the signal pulse shape. The resistance of the readout metal can be calculated from the width (w) and thickness (d) of the aluminum by

$$\rho_{Al} = \frac{2.824 \times 10^{-6} \Omega cm}{(d = 1.2\ \mu m)(w = 8\ \mu m)} \approx 30\ \Omega/cm \tag{6.9}$$

and thus relates to the specifications of the metal strip width and thickness. The width furthermore dependends on the coupling capacitance. This leads to a minimum value of 1.2 μm thickness.

6.2.8 Strip Faults

Pinholes

Pinholes are shorts or low ohmic connections between Al readout strip and implant. Charge can freely flow into the preamplifier, overloading the amplifiers of the main part of one whole chip (see figures 9.13, 9.14 and 9.30 and refer to [35]). These strips must be identified if not avoided in the manufacturing process, and remain disconnected from the amplifier at the cost of all aligned strips on the next sensors also being disconnected. For this reason, if possible, a detector with pinholes should be the last detector in a row on a ladder (Far from the readout).
We used the following strategy in order to find all pinholes:

- Applying 30 volts over the insulation between Al readout strip (AC pad) and the implant (DC pad). Simultaneously measuring the current will find all shorts and measure the resistance of low ohmic connections.

- Strip capacitance will increase dramatically on a pinhole strip. This measurement finds all shorts, but is strongly frequency dependent and therefore some pinholes remain undetected in some cases.
- High $C_{coupling}$ hints the presence of a pinhole. $C_{coupling}$ is also frequency dependent.

Breaks

Breaks are no danger to the readout, but will disconnect the rest of the strip and therefore all strips of the next sensors in a line. Sensors with breaks should be placed at the end of the ladder (like pinholes). We search for breaks by comparing the nominal strip capacitance with all measured strip values. Strips with lower capacitance are candidates for breaks. By measuring the capacitance from other end of these candidates one can sum up the two values $C_{left} + C_{right} = C_{nominal}$. If the sum is equal to the nominal value we have a break in the Al strip.

Shorts

A short is given by a connection of one or more neighbouring strips. This is not a crucial fault, but will result in a higher load capacitance which associated a higher noise, and also generate multistrip hits, so degrading the resolution. This kind of fault has no preferred position in the sensor row. Shorts are found by measuring C_{strip}. Capacitances which are N times the nominal capacitances should come in groups of N members. $C_{strip} = N \times C_{nominal}$ for N strips shorted together.

Leaky Strips

Strips with a high leakage current will disturb the readout by overloading the preamplifier. There are many reasons for leaky strips, e.g. defect bias resistors, inhomogeneity in the bulk silicon especially in the surface region, faulty strip implantation, non depleted regions, etc. (refer chapter 9). These strips often come in groups, which means a whole region has some defect. We measure the leakage current of every single strip at 80 V.

6.3 Uniformity of the detector

By measuring *every single* strip for C_{strip}, $C_{coupling}$, $C_{interstrip}$, R_{bias} and *leakage current* we gain a thorough knowledge of the homogeneity of the detector and the quality of the manufacturing process.
The uniformity is one of the crucial issues of a silicon sensor. Several regions with different electrical parameters will produce charge flow caused by potential difference or non-uniform depletion. This will prevent uniform gain, the SVX3 chip will not be able to do a reasonable pedestal correction and calibration will be extremely difficult to do. Often loss of signal or distortion in the readout chip and readout chain cannot be avoided.

6.4 Manufacture of Silicon Sensors at Micron

The main processes are given in table 6.1, some changes were applied during production to avoid certain repeating faults in the sensor quality (see chapter 9).

Step	Processing Description	Days	Notes
1	Silicon selection and scribing		
2	Field Oxide		Thermal at 1030 C^0; 0.9 μm dry+wet+dry, Ar/N
3	Image main implants	9	p+ on junction side, n+ on ohmic side. Deposit resist, open windows, etch in BOE[8]10 min. (should reach silicon), strip resist.
4	Reoxidation (cap oxide)	5	Thermal at 900 C^0; 0.2 μm wet+dry
5	Main implants		p+ junction side: boron 80 keV 2E15; n+ ohmic side: phosphorus 150 keV 5E15
6	Image secondary implants	8	p-stop on ohmic side (isolation), image n implant on junction side. Etch in BOE 10 min. (should reach silicon), back B+; front P+ at same time.
7	Secondary implants	2	p+ implant on junction side: boron 20 keV 5E14. n+ implant on junction side: phosphorus 40 keV 5E14.
8	Oxide partial strip	8	Remove 0.1 μm of SiO_2 in BOE sulphuric and rinse, then thin down.
9	Reoxidation		Thermal at 900 C^0; 0.1 μm wet+dry. Total time at 900 C^0; 1 h, in steam for 20 min. Three steps: Ar,O_2, H_2O.
10	Poly deposition		0.7 μm 2 h at 600 C^0.
11	Poly blanket implant	2	B+ 1.3E14, 80 keV, both sides. Boron resistivity about 30 $\frac{\Omega}{cm^2}$.
12	Silox deposition	8	0.8 μm.
13	Image silox for poly contacts		High dose implant, both sides or one at a time.
14	Poly high dose implant	4	Boron resistivity about 20-100 $\frac{\Omega}{cm^2}$ on both sides.
15	Image of poly, plasma etch.	2	Plasma etching 10 min.
16	Anneal	3	30 min. at 900 C^0; 3200 Å at most on front, 3100 Å at most on back.
17	PECVD	6	0.1 μm adjusted to have 0.3 μm over implant.
18	Contact (via) opening		Wet etching BOE about 2.5 min (significant overetching on poly).
19	Wafer cleaning		Remove about 0.01 μm of oxide.
20	Metal deposition	4	Sputtered Al_2Si.
21	Metal imaging, wet etching	4	
22	Passivation silox deposition	3	350 C^0 thickness 1 μm.
23	Passivation window opening		Wet etch that stops on metal.
24	Cutting	5	Cut and wash with DI water (no DECON90).
26	Probing		

Table 6.1: *SVXII/ISL Processing Steps. [25]*

[8]BOE stands for buffered oxide etch. It is a hydrofluoric acid (HF) with ammonium fluoride (NH4F) and water to 'buffer' the etching effect. Regular HF would etch too fast. The HF solve etches only the SiO_2, not the silicon.

Chapter 7

Evaluation of the Silicon Prototypes

The prototype silicon sensors delivered by Micron Semiconductors [28], Seiko Instruments [30] and Hamamatsu Photonics [29] were evaluated by measuring each important and specified parameter for each single strip [19]. Comparison with the specification and vendor information was done. Special attention has since been paid to uniformity and the number of bad strips per side. We realized that in principle all companies were able to process the sensors within the specification. Uniformity was still an issue and some work has been spent to realize consistency of parameters over the full area of the sensors after these evaluations.
At the same time we used these measurements to decide and define a reasonable quality control procedure to ensure functionality in the final operation condition with a large safety factor (see chapter 8). We also took the opportunity to tune all test routines with respect to speed and handling.

7.1 Micron Semiconductor prototypes

Micron Semiconductor is producing it's sensors on 6" high resistivity wafers. This is worldwide the first time that 6" technology has been used for silicon microstrip sensors in high energy physics. The problems and solutions which are correlated with this new approach will already be noticeable in these prototype studies, but further discussion both for and against will be presented in chapter 9. A complete geometric and electrical specifications can be found in appendix B.1 on page 120ff.
The first prototype of Micron arrived with the following data at Karlsruhe: total leakage current: 4140 nA @ $V_{bias} = 40$ V; 5000 nA @ $V_{bias} = 60$ V; 6080 nA @ $V_{bias} = 80$ V. 10 shorts (pinholes) @ strip: -242, -180, -156, -141, -119, -94, -62, -46, -4, 8.
In this starting up phase, Micron only tested the total leakage current, depletion voltage, individual strip coupling capacitance to detect pinholes, shorts between strips and breaks; no individual leakage current measurements were done. Over the later measurement and production period they increased more and more their measurement efforts.
All ISL sensors are aligned starting in the middle of the detector. The strip counting

starts at -256 and goes up to strip 256 skipping 0. Therefore all parameter scans over all strips will have the value 0 at bin 0. A complete geometric layout can be found in figure B.1 on page 124. According to the total capacitance versus bias voltage scan,

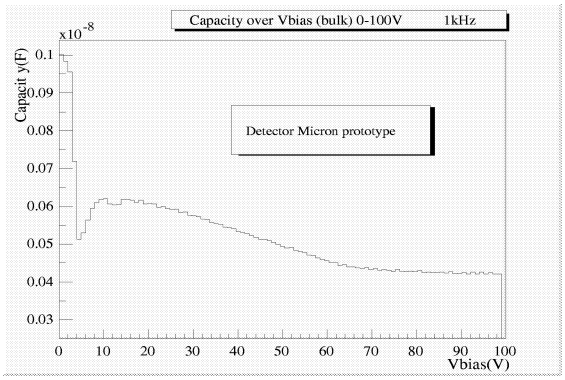


Figure 7.1: **Capacity vs. bias voltage** *of the MICRON prototype detector to determine the depletion voltage. The detector depletes at* $\approx 65\ V$.

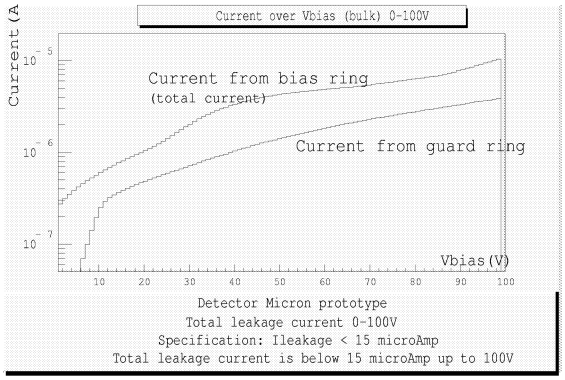


Figure 7.2: **Total leakage current** *of the MICRON prototype detector with a leakage current of 10* μA *@ 95 V. Bias ring and guard ring current are measured and displayed separately.*

displayed in figure 7.1 the sensor depletes around 65 V. The depletion is reached when the capacitance plateaus at a constant value. With 5.4 μA at 70 V the sensors' total leakage is completely within its specified limit of 15 μA at $V_{Depletion}$ + 15 V (see figure 7.2).

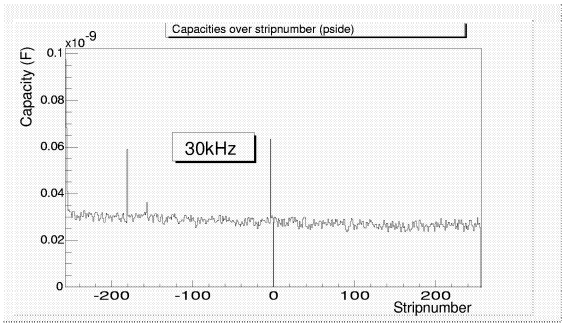


Figure 7.3: C_{strip} **measured @ 30 kHz – p-side**
We find a flat C_{strip} *distribution.*
Only 3 pinholes at strip -180, -156 and -4 were found. All confirmed with the current measurement AC-DC pad (figure 7.5) and indicated by MICRON.

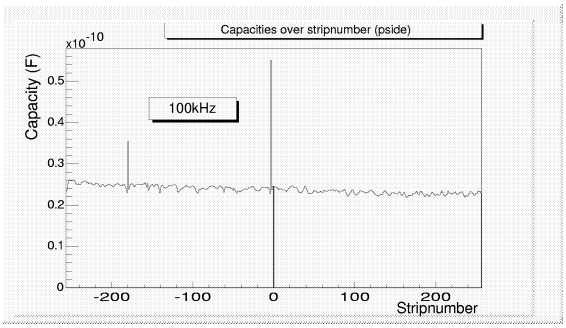


Figure 7.4: C_{strip} **measured @ 100 kHz – p-side**
Capacitance measurement at 100 kHz finds only 2 pinholes of the strips found with 30 kHz (strip -180 and -4; figure 7.3).

To find pinholes, shorts and breaks we measure the total individual strip capacitance across the whole sensor. Since our instrument is only capable of measuring at fixed frequencies instead of quasistatic, not all pinholes were found. This shows the strong frequency dependence of this type of measurement. ν 100 Hz, 120 Hz, 500 Hz found only 1 pinhole, 5 kHz found 2, 30 kHz and 100 kHz found 3 pinholes. Figures 7.3 and 7.4 illustrate the 30 kHz and 100 kHz measurement. Since a pinhole is a critical sensor fault we changed from a capacitance measurement to a current measurement. Applying 30 V[1] over the coupling capacitor (AC and DC pad), while measuring the current, finds all pinholes. In figure 7.5 we see currents 5 orders of magnitude higher than normal. This test at the same time gives us the resistances of the SiO_2. A measurement scheme is shown in figure 9.23 on page 99.
In addition all C_{strip} measurements were done on both ends of the sensor, to look for breaks and shorts between neighbouring strips. Since both ends showed the same C_{strip} value for all strips we conclude not to have any breaks, at the same time we found no occurrence with $n \times C_{strip}$, which is an indication for no shorts.

Comparing the number of pinholes which were found at Karlsruhe and Micron we see a discrepancy of two. Even double checking strips -242 and 8 and their neighbours with an IV scan of 0-40 V over the coupling capacitor showed no pinhole (see figure 7.6). A current of 40 pA @ 40 V is a good indicator of insulation. In addition all other

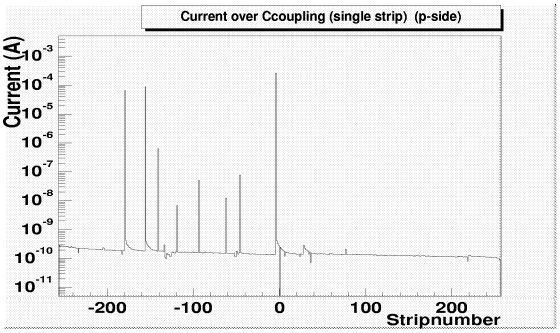


Figure 7.5: **Current over the coupling capacitor @ 30 V – p-side**
To find all shorts[2] between the Al readout strip and the p+ implant, we applied a voltage of 30 V over the isolation. A current $2.5*10^{-10}$ *A* $\pm$ $0.5*10^{-10}$ *A is nominal. 8 strips are indicating pinholes, showing currents up to* $2.65 * 10^{-4}$ *A. Strips -180, -156, -141, -119, -94, -62, -46 and -4 are pinholes; all indicated by MICRON.*

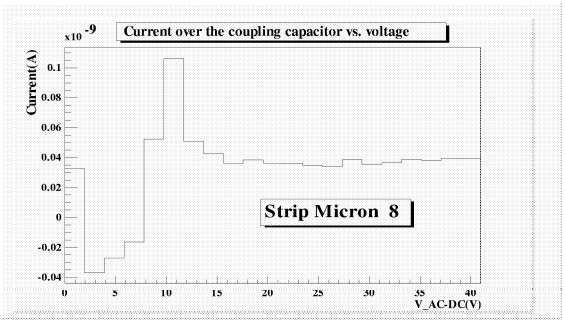


Figure 7.6: **Current over coupling Capacitor vs voltage**
To ensure the absence of a pinhole found at Micron we additionally measured the current over the insulator vs voltage. In case of a pinhole, the current would be rising steeply and with currents up to 1 mA. The same measurement was done for strip -242 with the same result.

[1] changed later to 60 V
[2] pinholes

parameters for these strip were nominal, e.g. C_{strip}, $C_{coupling}$, $I_{leakage}$ and $C_{interstrip}$. This was the first and only occurrence of such a pinhole count mismatch between Karlsruhe and Micron test data.

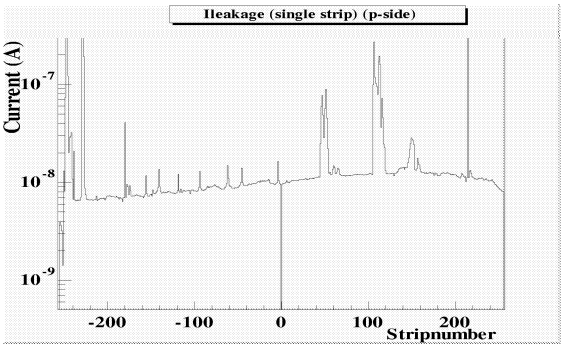


Figure 7.7: **Leakage current** *over strip number @ V_{bias} = 95 V*
This plot shows three non-uniform sensor regions and 13 leaky strips peaking with high leakage currents above 100 nA.

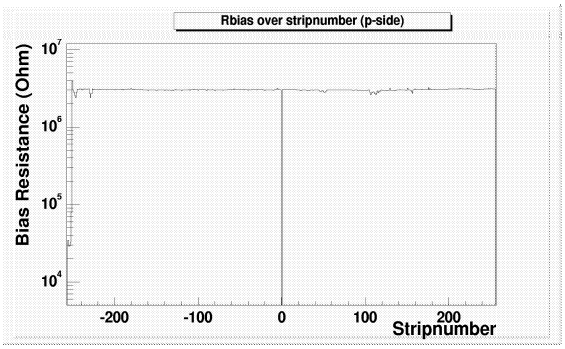


Figure 7.8: **Bias Resistors**
Flat distribution of bias resistors R_{bias} at 3 $M\Omega$. The two regions with the high leakage current have slightly lower bias resistors ($\sim$ 2.6 $M\Omega$)

The average single individual strip leakage current of about 3.2 nA was acceptable low. Some regions with currents up to 40 nA were still within the specified limit but nevertheless quite high. 13 strips have a leakage current above the specification of 100 nA. 7 of these were still below 300 nA, which the SVX3 chip is able to handle. Two were even above 1 μA which more or less represents most of the total leakage current.
Later the cause for finding regions about 15 strips in a row with high leakage current was found and is explained in chapter 9.2.2. Figure 7.8 shows a perfect flat bias resistor distribution. Additionally this is a sign for a homogeneous interstrip resistance $R_{interstrip}$ distribution. The relationship between of R_{bias} and $R_{interstrip}$ will be explained in chapter 8.

Figure 7.9 illustrates the coupling capacities for each individual strip. We observe a slope starting from 130 pF down to 100 pF. With a specification of $\sim$120 pF we have about half 'good' and half 'bad' strips. The 'bad' strips are still near the specification and in chapter 9.4 on page 89 we will illustrate the reason for this decrease to one sensor end and show the changes in the production to eliminate this effect for the final production sensors.
The same observation was made for $C_{interstrip}$ values of the strips at the sensor end. We have a uniform distribution of $\sim$ 4.5 pF across the senor but a steep decrease at the sides. The measurement was taken against one neighbour strip. To get the full value we have to multiply this value with $\sim$1.6 [3].

The n-side is even better than the p-side. We found no pinhole, break or short. The

[3] according to literature and some sample measurements.

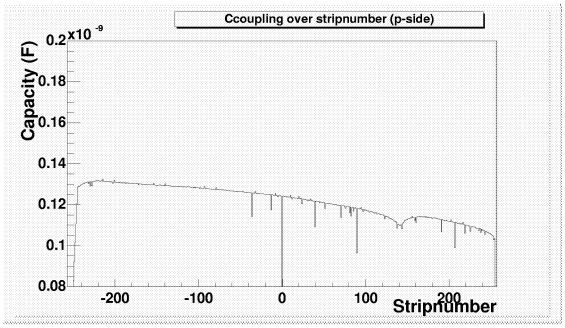


Figure 7.9: **Coupling capacity – 1 kHz – p-side**
Uniform decreasing of $C_{coupling}$ to higher strip numbers with a mean value of ∼120 pF.

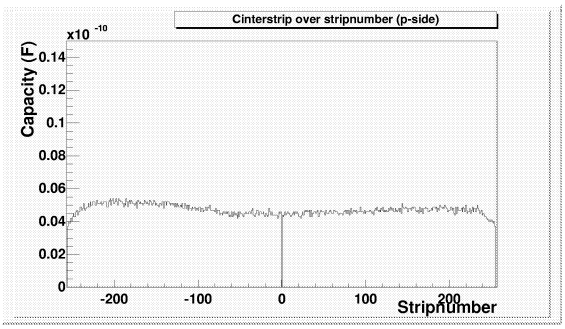


Figure 7.10: **Interstrip capacitance (AC and DC) – 100 kHz – p-side**
$C_{interstrip}$ is measured only against one neighbour. We have ∼4.5 pF with lower values at the edges.

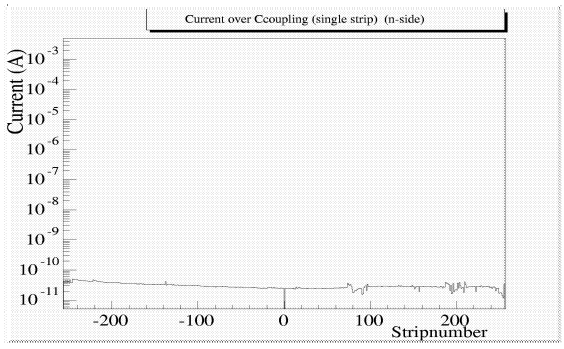


Figure 7.11: **Pinhole scan – n-side**
No Pinhole was detected, The current mean value was 20-40 pA.

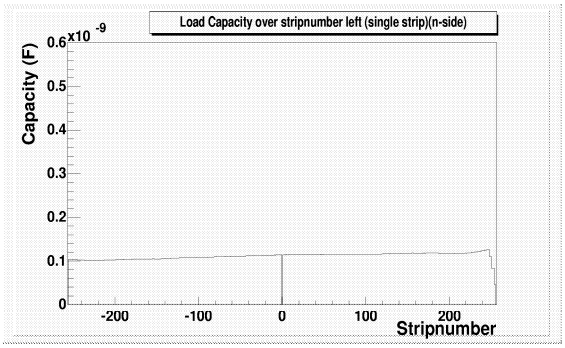


Figure 7.12: **Load capacitance – 100 kHz – n-side**
C_{strip} measurement is showing a homogeneous behavior. The low values at the right end exhibit the smaller end strips of the stereo side, which do not span the whole sensor length.

current over the SiO_2 indicates no defects and shows a good homogeneous distribution. At the end starting at strip 246 the values even decrease because of the shorter striplength due to the stereo layout.
The C_{strip} values are slightly decreasing to lower strip numbers. The capacitance measurement starting at strip 246 illustrates again the decreasing length of the stereo strips.

The lower values of the coupling capacitances to lower strip values are showing the same effect as on the p-side. Since strip 256 on the p-side corresponds to strip -256 on the n-side, we see the effect on the same side of the sensor (see chapter 9.4 on page 89). The interstrip capacitance distribution is homogeneous and around 5 pF slightly higher

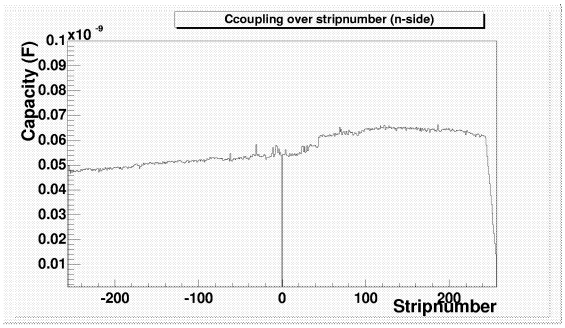


Figure 7.13: **Coupling capacity – Micron Semiconductor – 1 kHz – n-side** *Shorter strips at the right end have lower coupling capacitances. The values slopes to the left.*

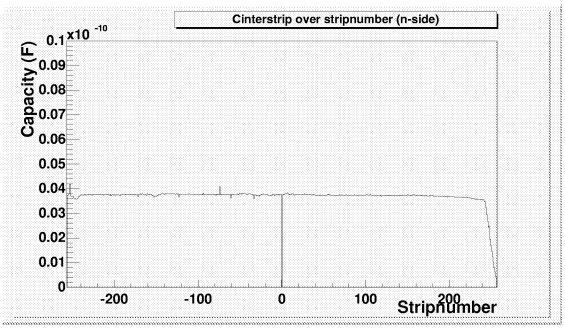


Figure 7.14: **Interstrip capacitance (AC and DC) – 100 kHz – n-side** *The shorter strips at the right end have lower interstrip capacitances.*

than 4.5 pF on the p-side as required in the specification (See figure 7.14).
The Micron prototype sensors tend to have some regions of high leakage currents, whereas the average level is fine. The number of pinholes is reasonable and will decrease for the production sensors. The $C_{coupling}$ distribution should not decrease to one sensor end. In chapter 9.4 this problem and its solution is discussed.

Sensor	# pinholes n-side	# pinholes p-side	# leaky strips n-side	#leaky strips p-side
MICRON prototype	0	8	-[4]	13
Almost production 1599-19-1	4	35	8	3
Almost production 1599-19-2	1	2	4	15

Table 7.1: **Number of Micron sensor faults** – *leaky strips and pinholes.*

In table 7.1 many leaky strips are noticeable. The reason for these high number of leakage strips on the p-side of sensor 1599-19-1 will be explained in chapter 9.2. Plots can be regarded in figure 9.10. Visually the fault can be seen in figure 9.9 on page 86.

[4]no leakage current measurement done for the n-side

7.2 Hamamatsu Photonics prototypes, first production sensors

Hamamatsu Photonics (HPK) and Seiko Instruments are using standard well established 4" technology with high resistivity silicon. Double sided processing 6" is not available at HPK and Seiko Instruments for mainly fragility of the wafers and handling procedure problems. For technical reason HPK and Seiko are making r-ϕ and r-z (stereo) side by implanting n^+ and p^+ on the n bulk, respectively. The n^+ implanting is used for the r-ϕ side, because the drawing of the n^+ side requires additional p-stop isolation and implantation. This is easier without the stereo angle. Complete geometric and electrical specifications can be found in appendix B.2 on page 122ff.

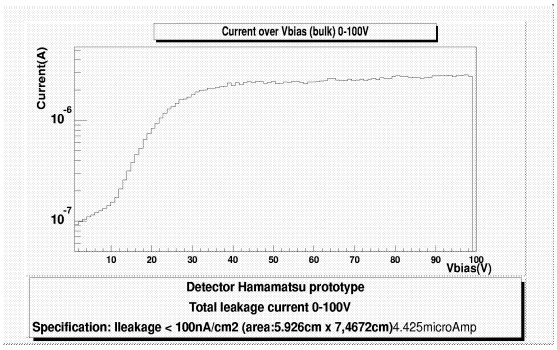


Figure 7.15: **Total leakage current – HPK.** *The prototype has a total leakage current of 2.6 μA @ V_{bias} = 95 V.*

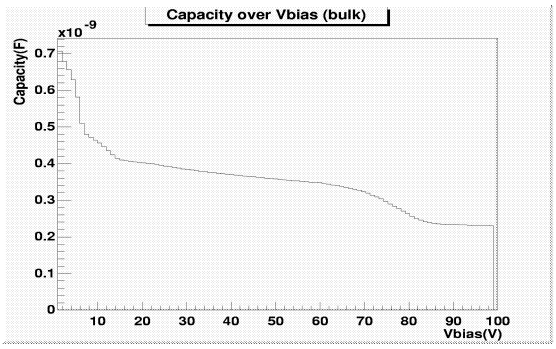


Figure 7.16: **Capacity vs. bias voltage – HPK.** *The detector depletes at $\approx$ 85 V.*

Figure 7.15 shows the bulk current of the Hamamatsu prototype saturating at ∼50-60 V with a total current of $\sim$ 2.6 μA, including bias and guard ring, perfectly within specification. According to specification, $V_{depletion}$ should be between 40 V and 80 V. The prototype of Hamamatsu depletes at $\approx$ 85 V. Since the leakage currents are still quite small at these voltages and above, the specification regarding $V_{depletion}$ was increased to 40-100 V. In figure 7.30 we see a large improvement with respect to $V_{depletion}$ of the first production wafer compared to the prototypes. HKP0001 depletes around 38 V. The total leakage current is also lower in the production sensors (fig.: 7.29) compared to the prototype.

There are only 3 strip defects on the p-side of the Hamamatsu sensor; 2 pinholes which can be noticed in figure 7.17 and 7.18. There is an additional non-uniform region concerning the strip insulators. These defects are candidates for breakthroughs after bonding, but the average level is still reasonably low, we therefore do not expect any post failures. Additional scans at higher voltages created no new pinholes. The C_{strip} distribution (fig. 7.18) is nicely flat and therefore promises a uniform preamplifier input and gain.

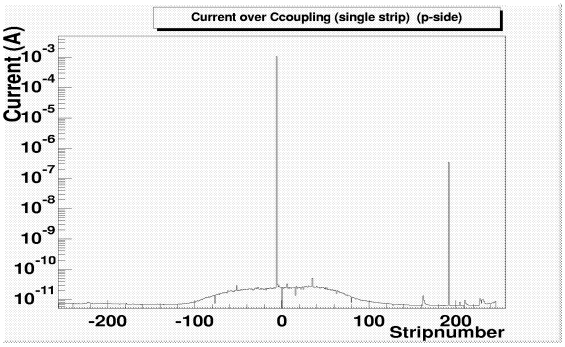


Figure 7.17: **Pinhole scan – p-side.**
We observe 2 pinholes at strips: -6; 192. A non-uniform but probably non critical behavior is seen from strip -100 to 100. We presume an insulator defect over a large area.

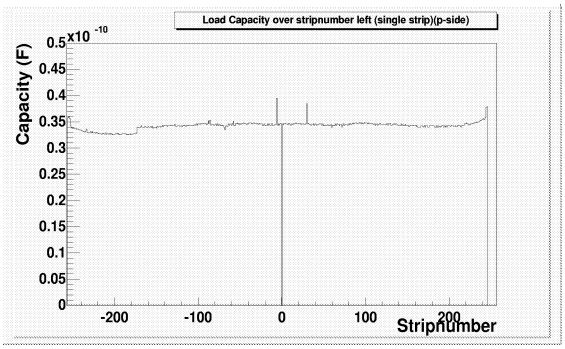


Figure 7.18: **Load capacity of individual strips – p-side.**
Pinholes(see figure 7.17), were confirmed with the C_{strip} measurement.

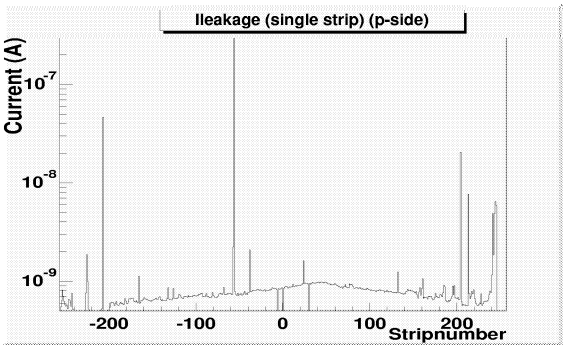


Figure 7.19: **Leakage currents – p-side.**
Nominal values are 0.6 to 0.9 nA. Only 4 strips above 1 nA were found, but only strip -51 with 971.85 nA is above 100 nA, which is defined 'bad'.

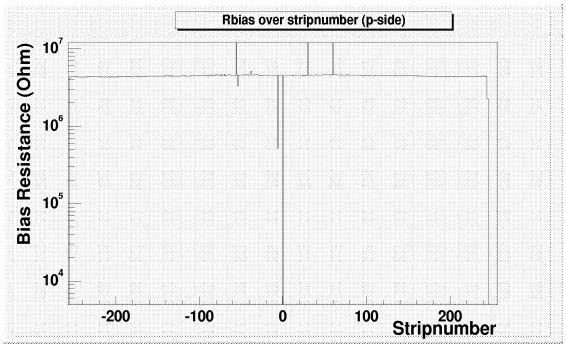


Figure 7.20: **Bias resistors of individual strips – p-side.**
The average level is 4.3 MΩ, the low value of strip -6 coincides with the pinhole, strip -56 with high R_{bias} is the only leaky strip.

Bias resistors and leakage currents are distributed homogeneously. The average low leakage current (fig.: 7.19) level mirrors the low total leakage current and is perfectly suited for readout with a low noise level. The mean bias resistance value was 4.3 $M\Omega$, which is well within specification (fig.: 7.20). All individual $C_{coupling}$ (fig.: 7.21/7.27 n-side) and $C_{interstrip}$ (fig.: 7.22/7.28) for all strips meet the specification with 140 pF/140 pF $C_{coupling}$ and 3 pF/5 pF $C_{interstrip}$ for p-side/n-side respectively. Some strips on p-side and n-side have a much lower coupling capacitance than the rest and a much higher conductivity between implant and Al strip. This is related to the shorts of the capacitor – the pinholes. The higher $C_{interstrip}$ on average on the n-side

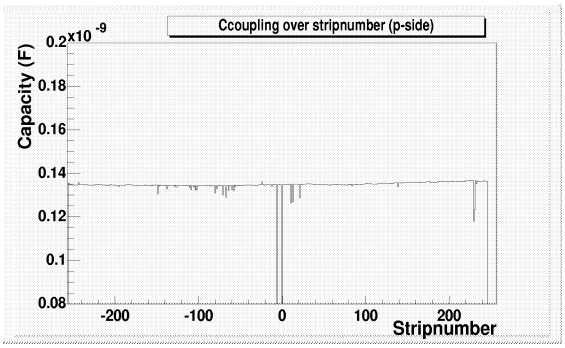


Figure 7.21: **Coupling capacity – p-side.**
We measure a homogeneous distribution at 140 pF. The pinhole at strip -6 is obvious.

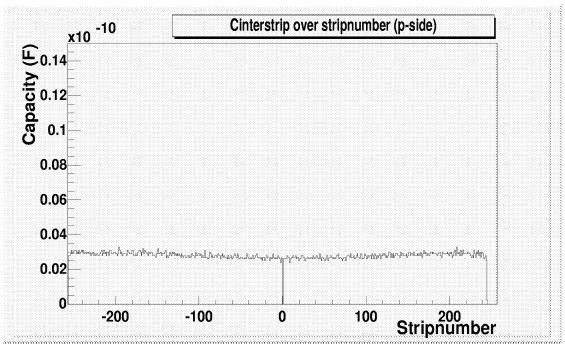


Figure 7.22: **Interstrip capacity of individual strips – p-side.**
A mean value of 3 pF gives a $\frac{C_{coupling}}{C_{interstrip}} = \frac{140}{3}$ *which is excellent for good charge collection.*

was expected (see equations 6.3/6.4 on page 54). Only the end region of the n-side shows low $C_{coupling}$, which corresponds to a region with 3 pinholes. As for the other

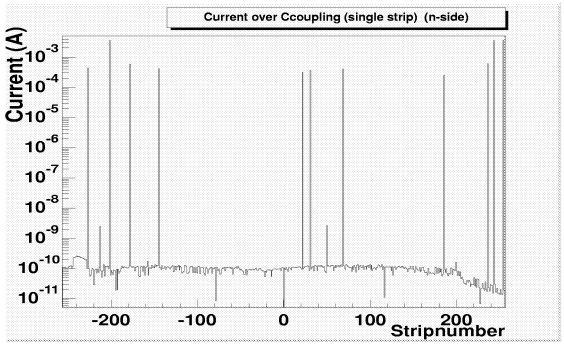


Figure 7.23: **Pinhole scan – n-side.**
The n-side shows 11 pinholes. We confirmed all 11 with an additional IV scan over the coupling capacitor; V starting from 0 - 30 V.

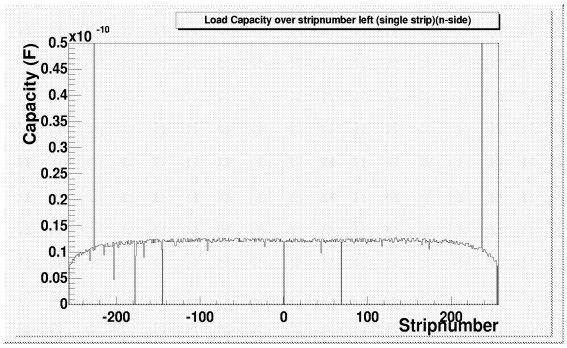


Figure 7.24: **Load capacity of individual strips – n-side.**
We confirm 6 pinholes, and find one break at strip -202.
The capacitances of the left and right strip end of strip -202 sum up to 10 pF nominal value:
$C_{right} + C_{left} = C_{nominal}$*; 4.7 pF + 5.6 pF = 10.3 pF*

prototypes and for all production wafers, we applied a voltage between implant and Al electrode and evaluated the produced current, which is $\sim 100\,pA$ for a non pinhole strip and 0.4 mA to 3 mA for a pinhole strip. All pinholes on the n-side were confirmed by the $C_{coupling}$ and $C_{interstrip}$ measurements but only 6 were found with the C_{strip} method.

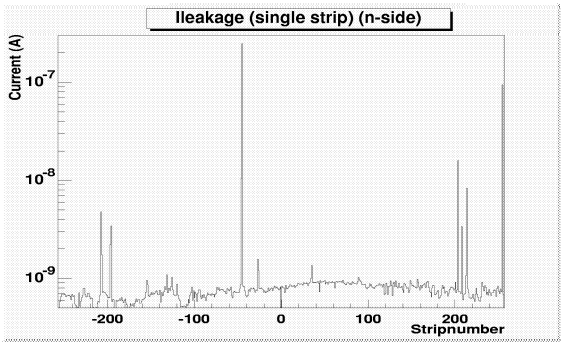


Figure 7.25: **Leakage currents – n-side.** *The mean value of the leakage current is at 500 pA. Only one strip reaches above 100 nA.*

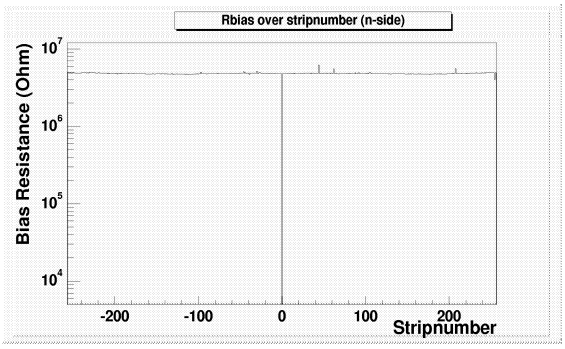


Figure 7.26: **Bias resistors of individual strips – n-side.** *We see a perfect flat distribution without any deviations.*

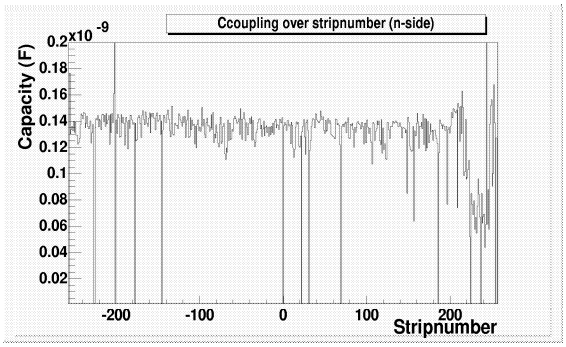


Figure 7.27: **Coupling capacity – n-side.** *All 11 pinholes can be identified but not as well as with the current method. There's a low $C_{coupling}$ region at the end of the sensor.*

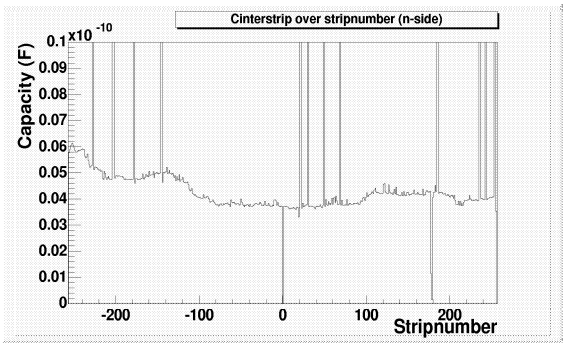


Figure 7.28: **Interstrip capacity – n-side.** *A mean value of 5 pF gives a $\frac{C_{coupling}}{C_{interstrip}} = \frac{140}{5}$ which is perfect for good charge collection. The measurement confirms the pinholes and the break.*

The Hamamatsu sensors have amazingly low leakage currents on average and in addition a very small number of leaky strips. Since the number of pinholes is quite high, especially on the ohmic side[5], the total number of strip defects is high, but still within specification. Table 7.2 shows the defect distribution per sensor and side.

[5]n-side: ohmic side, p-side: junction side

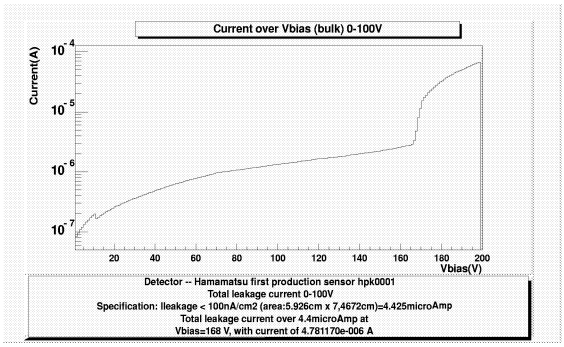


Figure 7.29: **Total leakage current** *of the first Hamamatsu production wafer detector with a leakage current of 1.2 μA @95 V.*

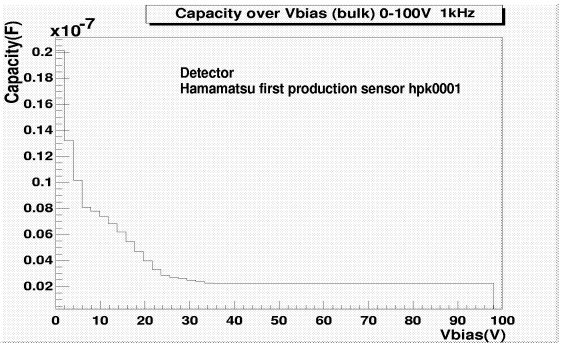


Figure 7.30: **Capacity vs. bias voltage** *of the first Hamamatsu production wafer shows the depletion voltage of $\approx 35\ V$.*

Sensor	# pinholes n-side	# pinholes p-side	# leaky strips n-side	#leaky strips p-side
HPK prototype 1	11	2	1	1
HPK prototype 2	8	4	0	0
HPK0001	4	6	1	3
HPK0002	5	3	2	0
HPK0006	11	8	3	0

Table 7.2: **Number of HPK sensor faults** – *leaky strips and pinholes.*

7.3 Seiko Instruments prototypes

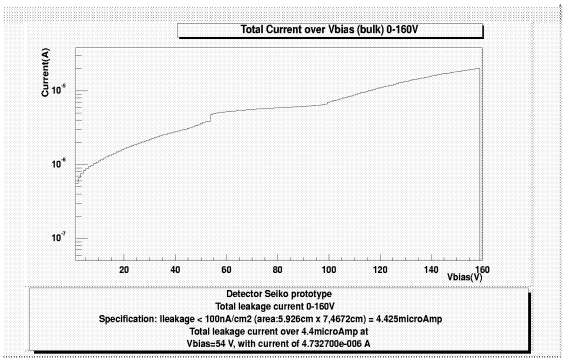


Figure 7.31: **The total leakage current** *about 4.4 μA @ V_{bias} = 54 V and 20 μA@ 150 V is above the breakdown current. But the steep rise of leakage currents only begins at 100 V, which is already above the depletion voltage. The current measurement includes bias and guard ring.*

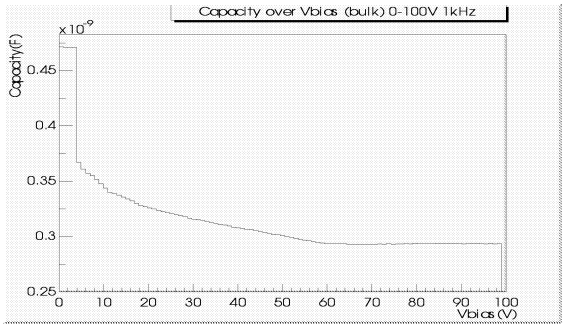


Figure 7.32: **Capacity vs. bias voltage** *of the MICRON prototype detector to determine the depletion voltage. Detector depletes at ≈ 65 V.*

The Seiko prototype shows a high total leakage current (fig.: 7.31) and many individual strips with very high leakage currents (fig.: 7.33). The depletion voltage around 65 V is well within specification(fig.: 7.32). Figures 7.33 to 7.37 indicates low interstrip resistance. Without the clear plateau of the total capacitance vs. bias voltage these results could be explained by the sensor not being fully depleted (In chapter 9.6 a case of low interstrip resistance, resulting from a not fully depleted sensor is described.). However, scans at higher bias voltages gave the same results. The average individual leakage currents with 10 to 20 nA are already quite high compared to specification, but there are some strips with a steep increase in $I_{leakage}$ at voltages below operating condition (fig.: 7.41). These individual strips are also responsible for the high total leakage current. Disregarding the *'bad'* region with low interstrip resistance, the capacitance values are quite promising with an average of 2.3 pF for $C_{interstrip}$ and 170 pF for $C_{coupling}$ we get a ratio of $\frac{C_{coupling}}{C_{interstrip}} = \frac{170}{2.3}$ which is perfect for charge collection.
Very promising is the insulation between implant and Al strip. The distribution for the current between AC and DC pad with 30 V applied is very flat with an average of 120 pA and only one pinhole on the p-side (fig.: 7.38). We get a similar picture of the n-side with only 2 pinholes found by evaluating the strip capacitances.
The C_{strip} values are uniform on both strip ends and for p- and n-side (see figures 7.39 and 7.40). This is a perfect scenario for the input of the preamplifier of the readout chip. Only one Al strip break is detected but it disrupts a strip which has a pinhole, too (see figure 7.39).

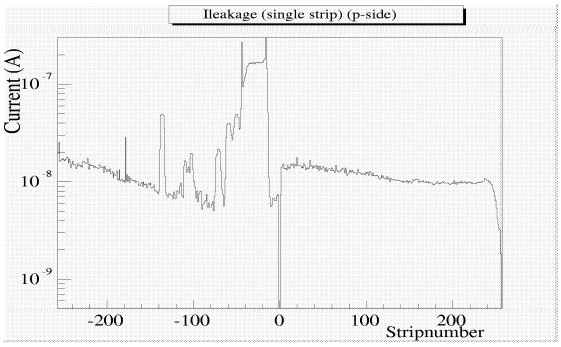


Figure 7.33: **Individual leakage current per strip (p-side)** *is on average 10 to 20 nA, disregarding the high current region from strip -60 to -5.*

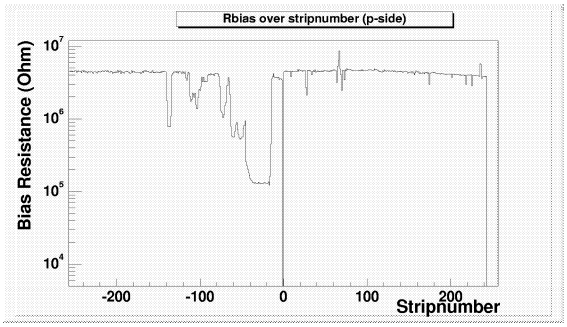


Figure 7.34: **Bias resistors over strip number – p-side.** *We measure a mean value of* 4.5 $M\Omega$. *The same region with the high leakage currents has low bias resistors.*

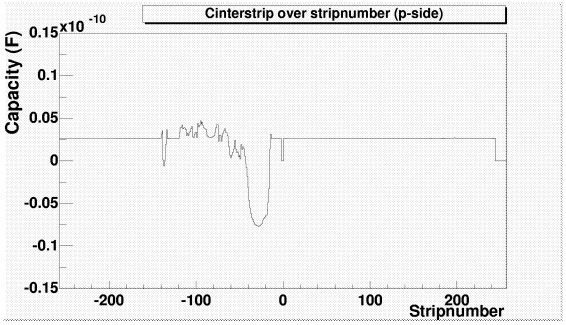


Figure 7.35: **Interstrip Capacity – p-side.** $C_{interstrip}$ *has a constant value of 2.3 pF, perfect for an interstrip capacitance. There is one region with negative values!* $C_{interstrip}$ *was measured against one neighbour.*

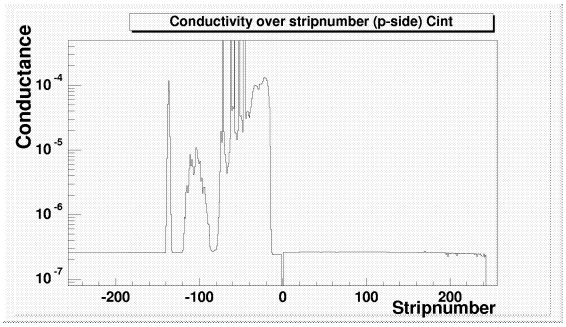


Figure 7.36: **Conductivity between 2 neighbouring strips.** *This measurement is done in parallel to the interstrip capacitance. We detect two strip regions with strips almost shorted to each other.*

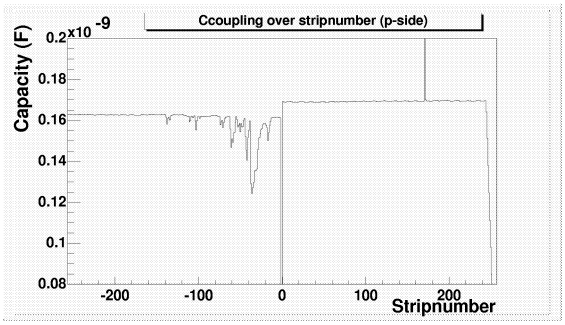


Figure 7.37: **Coupling capacity (individual strips p-side (left))** *This measurements shows a pinhole at strip 171 as expected and a region of low $C_{coupling}$. The values for the end strips are decreasing due to the shorter strips, coming from the stereo layout. The mean value is about 170 pF.*

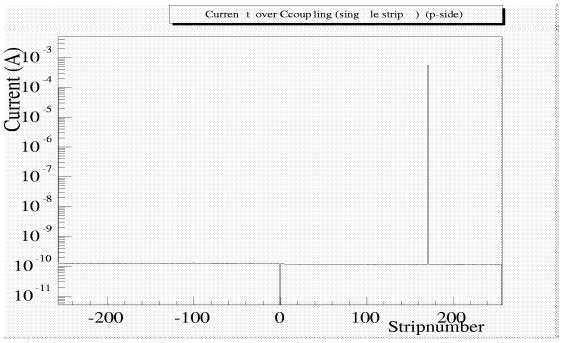
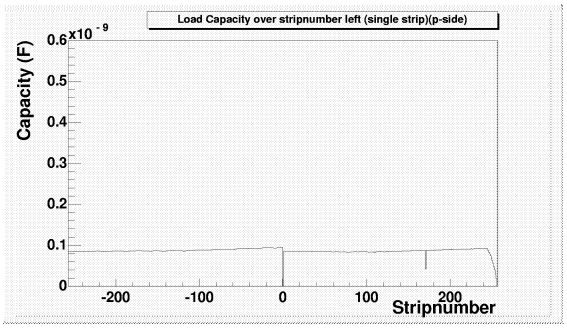


Figure 7.38: **Pinholes.**
The pinhole strip 171 with a current of 0.56 mA is clearly detectable under a homogeneous distribution of 120 pA.



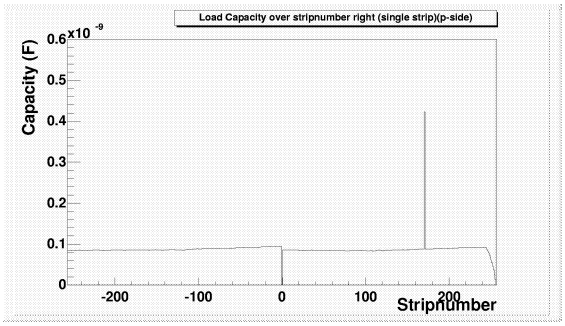


Figure 7.39: **Load Capacity (individual strips p-side (right and left))**
The load capacitances for all strip and both strip ends are distributed homogeneously. Regarding the left side of the sensor we see smaller value than average hinting for a Al strip break. The right side shows a much higher value which indicates a pinhole, also found with the current method. This is a rare case of a pinhole strip with a break.

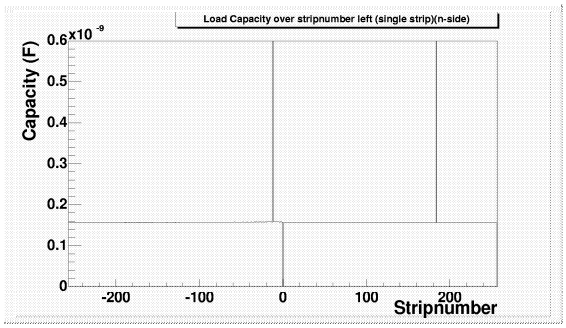


Figure 7.40: **Load Capacity (individual strips n-side (left))**
There are 2 pinholes and no breaks or shorts on the n-side.

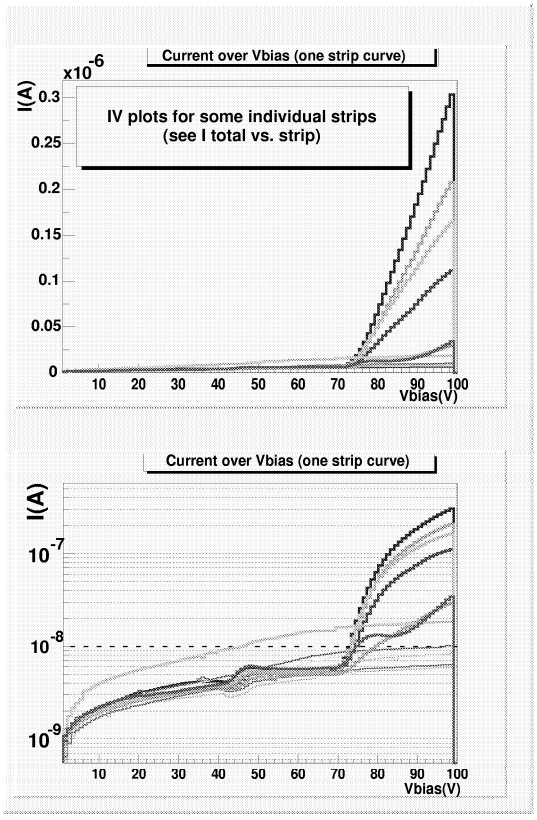


Figure 7.41: **Leakage currents of individual strips vs. voltage.**
The average current is already quite high, but in addition there are some strips with a low current breakdown voltage leading to high currents at operation voltage.

7.4 Summary and Comparison

All measured mean values of all detectors were compared with the specifications.

Parameter	MICRON	SEIKO	HAMAMATSU
Depletion Voltage	Specification met.	Specification met.	$V_{depletion}$ with 85 V above specs. Leakage current saturates at lower level.
Total leakage Current	Specification met.	Specification met.	Individual strips produces a high $I_{leakage}$ above 100 V.
Bias Resistors	Specification met apart some individual strips.	region on p-side with very low R_{bias} indicates a process error.	Specification met except some individual strips.
Interstrip Capacitance	All detectors show a good $C_{interstrip}$, except some individual strips.		
Coupling Capacitance	All detectors show a good $C_{coupling}$, except some individual strips.		
Strip Faults			
Pinholes	8 pinholes[6] p-side	2 n-side, 1 p-side	2 p-side, 12 n-side
Breaks (Al)	no breaks	one break	one break on n-side
Shorts[7]	No shorts	No shorts	No shorts
Leaky Strips	All have many individual leaky strips.		
Average leakage current	MICRON and SEIKO prototypes show regions with a very high $I_{leakage}$		very low single strip leakage current.
Additionally Seiko has a large region with low interstrip resistance on the p-side. This affects all values of $I_{leakage}$, $C_{interstrip}$, R_{bias}, $C_{coupling}$ in this region.			

Table 7.3: *Summary of the Silicon prototype sensor results from Micron, Hamamatsu and Seiko.*

7.5 Conclusion

The electrical parameters of three prototype sensors, supplied by Micron Semiconductor, Hamamatsu Photonics and Seiko Instruments were measured. All three detectors were still in the prototype phase, additional *R&D* has since been spent on the processing, to avoid defects, which only showed up in isolated regions. All measurements

[7] 10 strips were indicated as pinholes by MICRON, only 8 could be confirmed. The other two showed no unusual behavior, including additional testing of the AL-implant insulator and individual strip leakage current measurements. All pinholes are on the p-side

[8] Short between two readout strips.

clearly show, that the companies were able to largely meet the specifications, but problems remained to meeting the specifications over the whole sensor, Specifically:
The SEIKO prototype detector had a too high leakage current and a region of low interstrip resistance.
The MICRON sensor showed some regions of high leakage current.
The HAMAMATSU detector had many individual strip faults, most of them from problems with implant – Al isolation.
This led to the conclusion, that all companies still had some deficiencies in the production process at this stage, e.g. mask defects. These problems were corrected before producing production-grade sensors.

7.5.1 Vendor decisions

The prospect of larger 6" wafers with the possibility of processing two sensors at once and the resulting lower cost, led to the decision to buy sensors at Micron Semiconductor – the only supplier of sensors out of 6" wafers. The evaluation of the prototype sensors did not contradict this decision. Still it was decided to split the order between two vendors to ensure the production of all wafers in the short time available. The measurements of the prototypes of Hamamatsu and Seiko and the reputation of Hamamatsu provided Hamamatsu with the order. Finally it was decided to buy about half of the sensors from MICRON (460 sensors ISL — 380 sensors SVX II) and half from Hamamatsu (500 sensors ISL — 380 sensors SVX II)[9].

7.5.2 Know How from experience for the quality control

During these extensive measurements, we established a reliable way to check for quality over a large sample of 444 detectors (+spares) for the ISL. We measure the total leakage current and the C_{bulk} over V_{bias} behavior. We search for pinholes, measure single strip leakage current both sides for all sensors and in addition $R_{interstrip}$ for as many sensors as possible. Finally we check some detectors per batch, as we checked the prototypes. Since we see a strong frequency dependence in the C_{strip} measurement intended to be used to search for pinholes, we decided to look for pinholes via the current method[10]. At the same time we confirm the breakdown of the coupling capacitor to be higher than the set voltage. Applying a voltage of 60 - 80 V corresponds to a bias voltage of 120 - 160 V[11], therefore we have a safety factor of $\sim$2.

[9] Later 190 single sided 4" sensors were ordered from Hamamatsu for Layer 00
[10] It would be possible to use an instrument with quasistatic frequency settings
[11] We will use a split bias scheme.

Chapter 8

Quality Control

8.1 Performed measurements

To evaluate the quality and performance of a silicon microstrip detector, it is important to check the following parameters (table 8.1) and compare them with mean and specified values. Micron is producing and checking all the 6" sensors. In the beginning all sensors were once again and more thoroughly checked for quality in Karlsruhe. In the ongoing production Micron increased their testing effort, and measurements formerly exclusively done in Karlsruhe are now implemented in the general testing scheme of Micron. This made it possible to check only a fraction of processed wafers in Karlsruhe, namely average and not classifiable sensors.

This is a list of the standard electrical measurements on the full automatic.

1. IV scan (0-100 V) (sometimes up to 160 V)
2. CV scan (0-100 V)
3. Leakage current of each strip @ 80 V (to determine noisy, leaky strips)
4. Bias resistance of each strip
5. Current over Al-implant insulator @ 60 V for each strip (to determine pinholes, bad insulation layer)
6. Measurements of C_{strip} for each strip (two sides)
   $\rightarrow C1, C2, C_{mean}$ (to determine faulty strips)
   pinhole: $C1 = C2 >> C_{mean}$
   short: $C1 = C2 = n * C_{mean}$
   break: $C1 + C2 = C_{mean}$
7. Interstrip resistance
8. Coupling capacitance of each strip
9. Interstrip capacitance of each strip (between strip and one neighbour)
10. IV scan for individual strips (Additional test and homogeneity check)

Table 8.1: *The list includes all measurements done during the prototype phase and for sensors difficult to classify. Measurements 1 to 5 were done for each sensor on both sides. The location of breaks, shorts and pinholes can be seen in figure 8.1.*
C1 and C2 are the strip capacitances on both ends of a strip.

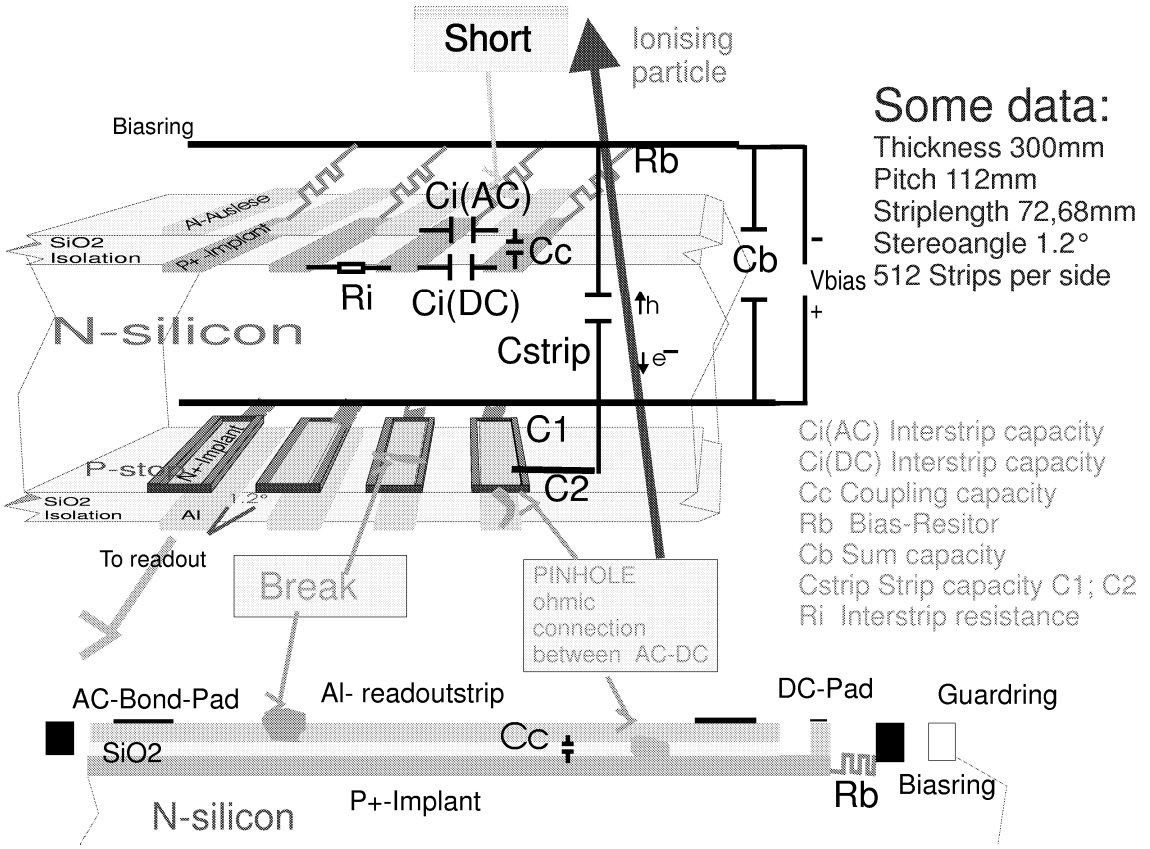


Figure 8.1: **Scheme of an ISL sensor including measured parameters and faults**

In general all measurements of Karlsruhe and Micron are in agreement.

8.2 Probestation

The wafer rests on an x,y stage on conductive rubber or fastened in a special test frame. Micro probes are placed either on the x,y-stage with the wafer or on sidearms of a z-stage. The manipulating area is 200 mm (x), 300 mm (y), 100 mm (z).
The system is able to automatically contact to 40 $\times$ 40 μm^2 (DC) and 60 $\times$ 200 μm^2 (AC) Al pads applying probe needle with a 2 μm tip. The minimal stepping of the x,y stages are 0.250 μm and 0.5 μm for the two different probestations. This flexible arrangement allows fast switching between different measurements. Some measurements are done in one run, by switching measurement options with coaxial relays. Therefore the number of probepad contacts is minimized.
The system is controlled by a standard PC with a GPIB[1] board and a DC-motor-

[1]GPIB: **G**eneral **P**urpose **I**nterface **B**us representing the standard IEEE-488 also known as HPIB (from Hewlett Packard)

controller board with I/O capabilities to switch the relays. We use the 4274A Multi-Frequency LCR Meter from Hewlett Packard [36] and 2 electrometer from Keithley: model 617 and 6517 [37]. The bias voltage is provided by a Hewlett Packard standard voltage supply, especially chosen for high stability with respect to currents.

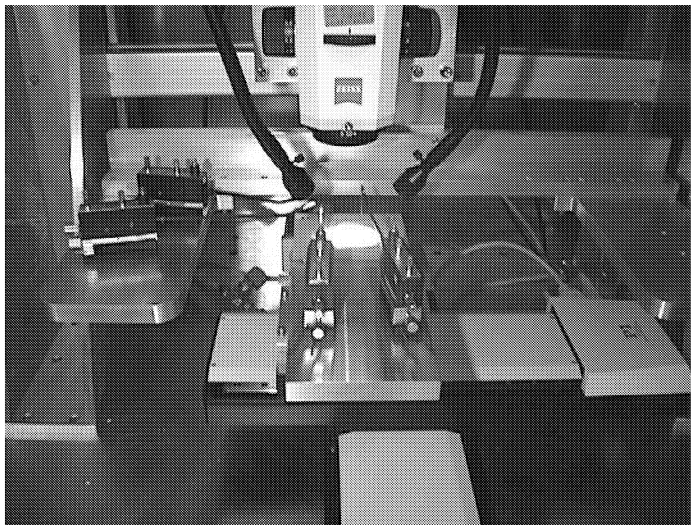


Figure 8.2: **The probestation.**

To ensure the capability to handle 2 to 4 sensors per day we use 2 fully automatic probestations (figure 8.2) of the described type and a manual one for visual scans and mounting. The main time constraints are the waiting times between the measurements. One has to wait for the currents to settle after a new contact or changes in the voltages. The motor stepping is no time issue.
The time optimized measurement sequence is:

1. mount one sensor (p-side up) in the mounting station,
2. place into probestation,
3. measure IV and CV,
4. align sensor, probes and start the automatic measurement,
5. do step 1 - 4 for the second sensor,
6. mount a third sensor and fourth sensor,
7. wait for first sensor to be processed,
8. change it with one already mounted,
9. do step 3 - 4 with third sensor,
10. turn over the first sensor (p-side to n-side),
11. do step 7 to 10 for sensor two and four.

The procedure makes optimal use of the equipment with respect to time. The testing person has to record[2] all the data about the measurements being done and compares the measured data with the Micron results. All measurements are controlled by a single Labview[3] program (refer appendix C) which saves all data in one file. Finally plots are created using the ROOT software package [59] and put on the *WORLD WIDE WEB* at [27]. This makes all data and plots immediately available to the whole collaboration.

8.3 Results

For most of the sensors received for quality control we have a fundamental agreement in the data between our results and the Micron measurements. The pinhole match is 100% perfect on both n- and p-side even though Karlsruhe is using a completely different testing method to find the pinholes. Micron measures the strip capacitance with a quasistatic frequency, while Karlsruhe measures the current over the SiO_2 insulator (@ 60 V). The current value is highly dependent on the processing. We get values starting from 5 pA to 5 nA for different sensors; this will be explained in chapter 9.8. Still, we have a 100% efficiency in finding all pinholes having currents between 10 μA and 1 mA. The exact level of leakage current tends to be a little different in Karlsruhe than at Micron which is normal, when using different probestations. Very leaky strips and leaky regions are usually highly correlated between the two measurements.
Karlsruhe is the only place measuring individual strip leakage currents on the n–side for all detectors. In some cases the quality control proved to be essential, since sensors, classified A-Grade at Micron were measured to have different properties in Karlsruhe. These dis-functionalities will be thoroughly discussed in chapter 9. Whenever defects were found, this information was fed back to the collaboration and to Micron to improve processing. To avoid further mismatches, Micron increased more and more their initial quality control, with the help of the CDF collaboration, e.g. interstrip resistance measurement is now part of the standard quality control at Micron and depletion voltage is now measured on the devices themselves instead of one measurement on the test structures surrounding the sensors on the wafer. This work is on-going. Efforts are made not to copy the exact testing procedures at Micron. The comparison of all individual measurements for all sensors would go beyond the scope of this thesis. All data and plots can be found at [27], but all data is under permanent scrutiny by the collaboration and Micron for feed back. The main program used to measure all standard parameters is shown in figure C.1 on page 125.

[2]there are special test sheets and a general logbook
[3]Labview is a graphical high-level programming language from National Instruments.

Chapter 9

Design, problems and solutions with 6" sensors

This chapter will give a description of the sensor design and layout in detail. The problems, resulting from the larger wafer size are illustrated. Some of these problems were already detected during the prototype phase, see chapter 7.

9.1 Design

The fabrication of microstrip detectors on 4" high resistivity wafers, allowing a maximum workable area up to 42 cm^2 has been established. The workable area using 6" wafers increases up to 100 cm^2. Since this is twice the area of a 4" wafer a larger number of sensors can be processed at the same time on the same wafer resulting in significant reduction of cost. Figures 9.1 and 9.2 show the mask layout of the 6" wafers for ISL and SVX II sensors respectively. In the case of the ISL wafer both sensors are identical in size. In the SVX II wafer, the sensors are produced for layers at different radii and hence have different geometry. The ISL sensors on 6" design are 5.75 mm longer than their counterpart in 4" design. Figure 9.3 shows the different electrical structures of an ISL sensor. Figure 9.4 shows a photo of a full wafer in original size.

Type	Width (mm)	Length (mm)	Diagonal (mm)	Pitch p-side(μm)	Pitch p-side(μm
SVX II L2	40.30	74.30	84.53	60	60
SVX II L4	60.17	74.30	95.61	65	65
ISL (6")	59.26	74.77	95.41	112	112
ISL (4")	59.26	69.02	90.97	112	112

Table 9.1: **Sensor dimensions for SVX II and ISL.**

Mask layout of the 6" design. Two sensors fit on one wafer.

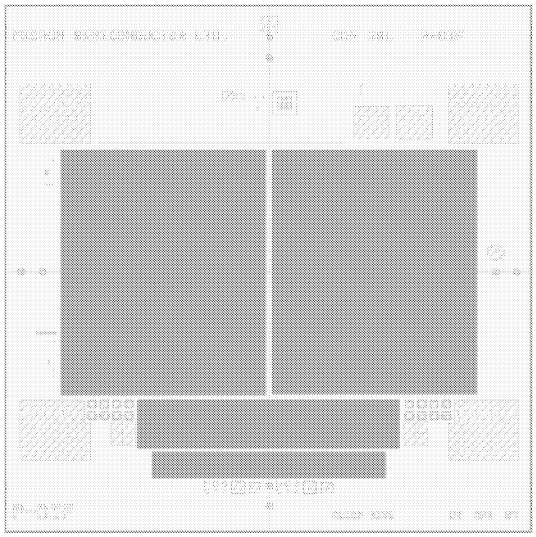


Figure 9.1: **Mask layout of an ISL wafer** *including some small test structures and 2 small test sensors.*

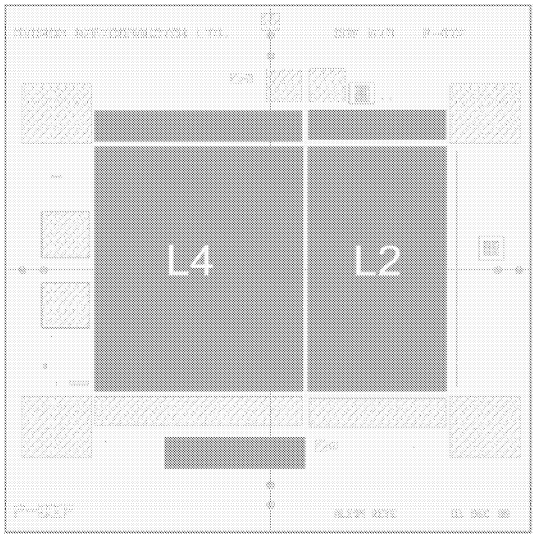


Figure 9.2: **Mask layout of a SVX II wafer** *with a layer 2 (L2) and a layer 4 sensor (L4).*

Layout of the 6" design.

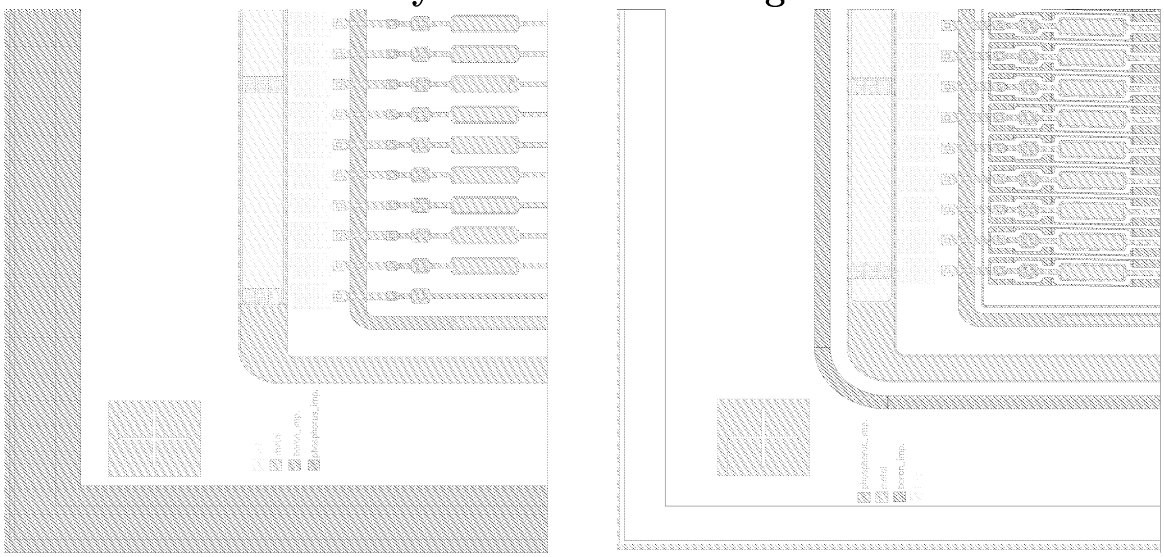


Figure 9.3: **Structure of an ISL sensor – p-side (left) and n-side (right).** *All 6" sensors for ISL and SVX II are 300 μm thick on* $< 100 >$ *oriented silicon. The sensors are double sided, single metal, AC coupled, polysilicon biased, with a common p-stop structure on the ohmic side for SVX II and isolated p-stops structure for ISL to provide interstrip isolation. A 3D scheme is displayed in figure 8.1.*

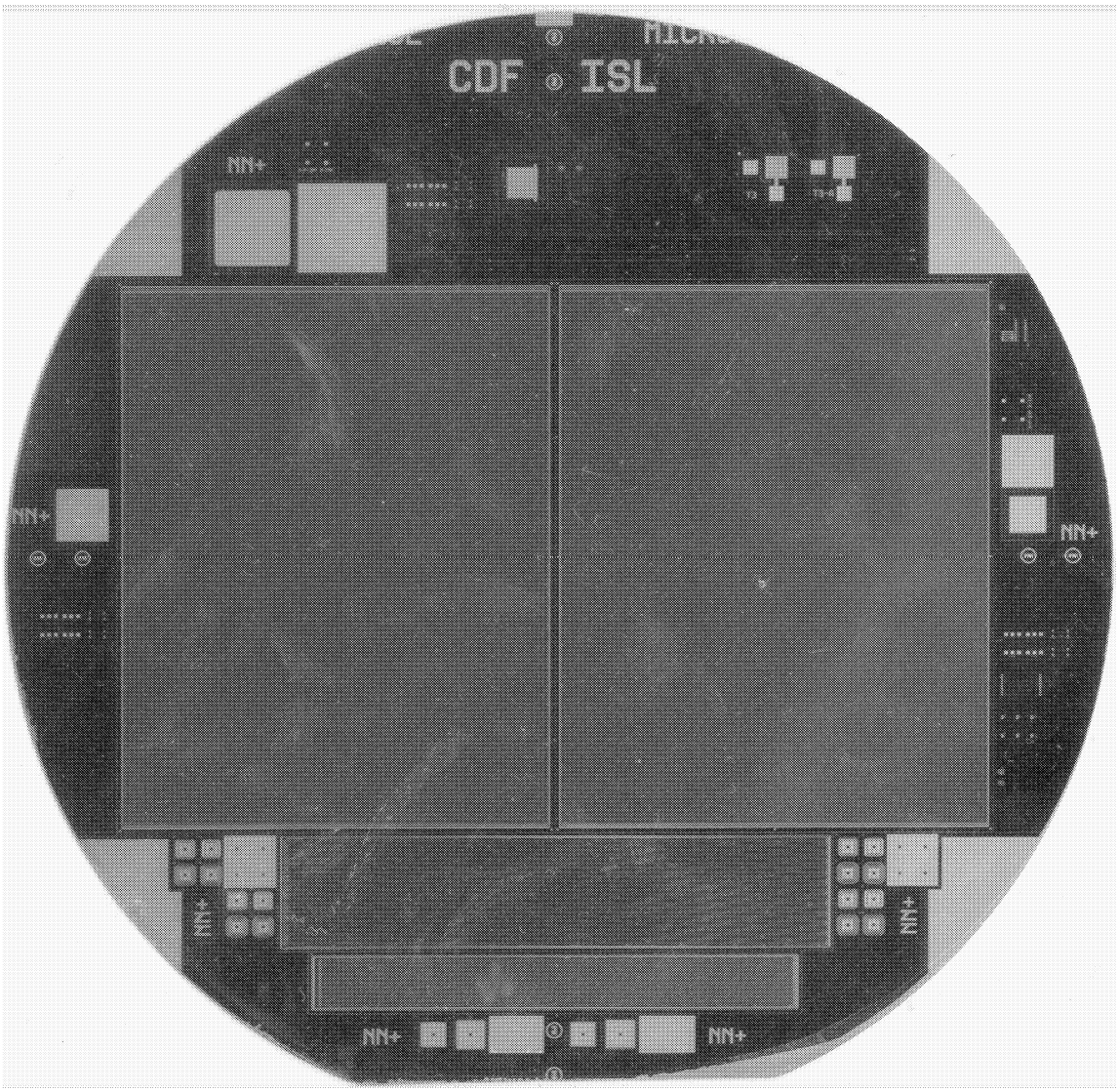


Figure 9.4: **Photo of a full 6" ISL wafer in original size.**
Two ISL sensors plus two smaller study sensors and many small test structures, like diodes, resistors can be seen. The four rounded triangles at the perimeter are for handling purposes.

9.2 Leakage current

As discussed in chapter 6.2.2 leakage currents are one of the main concerns in a microstrip detector. One problem is the associated increase in noise. Another is the possibility of a total distortion of the readout (see figure 9.30). A small number of single *isolated* strips is no crucial problem, since these strips can be disconnected from the readout. Large clusters and patches of leaky strips pose a serious problem. It could lead to an insensitive region, large enough to affect the complete track reconstruction. Sensors with this type of defect are beyond the specification and are rejected. Figure 9.5 illustrates an example of different strip behavior under bias voltage. The steep rise of the leakage current starts at different voltages. The operating condition is depletion voltage plus ∼15 V, hence only high currents below this voltage region and slightly above[1] are problematic.

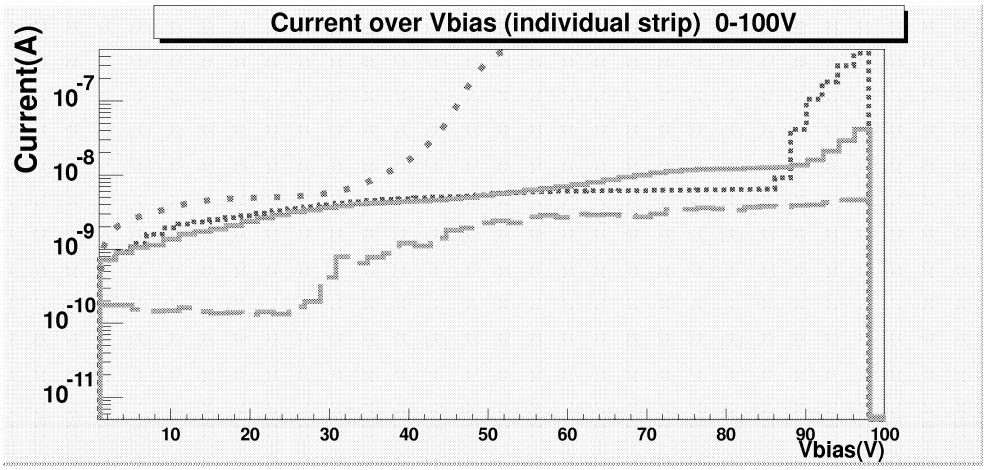


Figure 9.5: **Leakage current vs. depletion voltage of individual strips.**

9.2.1 Isolated high leakage current strips

Sensors with a few single individual *'high'* leaky strips have a major contribution to the total leakage current but are nevertheless not really critical. Charge is flowing along electrical field lines, therefore it is not surprising, that high currents concentrate at high field concentrations, which normally happens at sharp edges. In figure 9.6 and 9.7 exactly these conditions are realized - naturally not on purpose. These inhomogeneities result from processing errors and end in high fields and therefore high current concentrations of 1 μA are often found. With an infrared camera small hot spots can be seen.

[1]The depletion voltage will increase with radiation damage.

Strip defects which leads to a high leakage current.

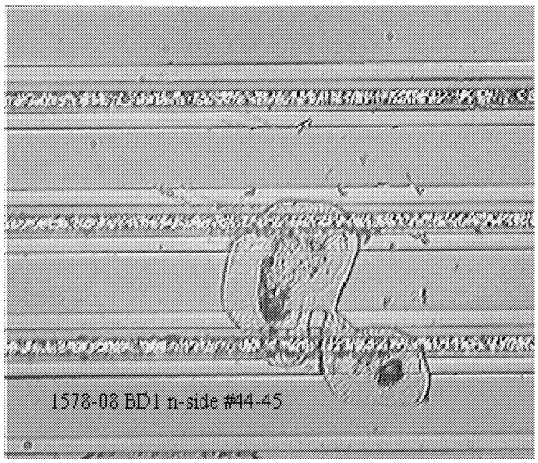


Figure 9.6: **Unregularities between implants, leading to a field distortion.**
Dirt causes breakdown at junction edges. The higher leakage current comes from large charge collection at edges.

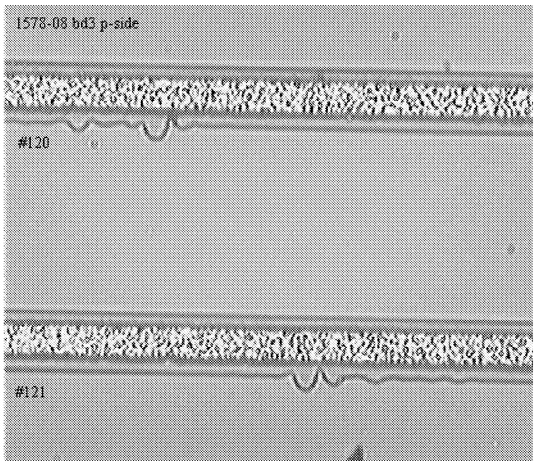


Figure 9.7: **Faulty strip with a nodge.**
Here we see a strip with a nodge at the side with a pointy edge. This will maximize the electrical field at that point, which leads to a very high leakage current on that strip. This is an individual strip fault.

The same type of error is present on the n-side, but in addition to the strip implant deviations, irregularities in the p-stop may cause the same problem. The missing half circle (mouse bite) in figure 9.8 for example caused a leakage current above 1 μA in one single strip. Another cause for these defects is bad handling and bad cutting. Scratches have sometimes pointy edges too, and cutting may cause small microscopic breaks in the edges leading to field distortions at the sensor edges. Often these irregular edge fields can be reshaped with the guard ring, saving the side strips from any irregularities. It is well known that end strips are often more leaky than the rest. This problem is mostly solved by an overlap of neighbour detectors, with 'good' side strip quality.

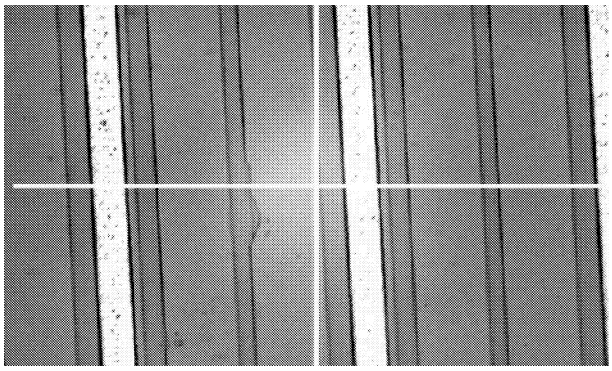


Figure 9.8: **Mouse bite in a p-stop**.
Defect shown causes a high field detoriation leading to an individual current above 1 μA.

9.2.2 Cluster of high leakage currents on the p-side

The double sided devices of Micron quite often showed large clusters of high leakage currents on the p-side. Always 15 strips in a row were affected. This is exactly the number of strips geometrically corresponding to one n-side strip, due to the stereo layout. In fact the real defect happened on the n-side. One n^+-implant is shorted to the p-stop. The n^+-implant is therefore at the same potential as the bias voltage, instead of being biased through the bias resistor. Figure 9.9 shows an example picture of these connections. They are located in the SiO_2 layer and not removable after processing. The main source is dust while processing, another factor are scratches connecting p-stop and implant. The leakage current can be seen in figure 9.10 for both p- and n-side. The matching is perfectly observable. This was the second sensor delivered by Micron after the first prototype. This explains the large number of leaky strips reported in table 7.1. After classifying the defect, improved procedures eliminated this fault for the majority of sensor, especially improvements in the clean rooms are responsible for the correction. But this is still the major defect responsible for a large number of leaky strips on the p-side.

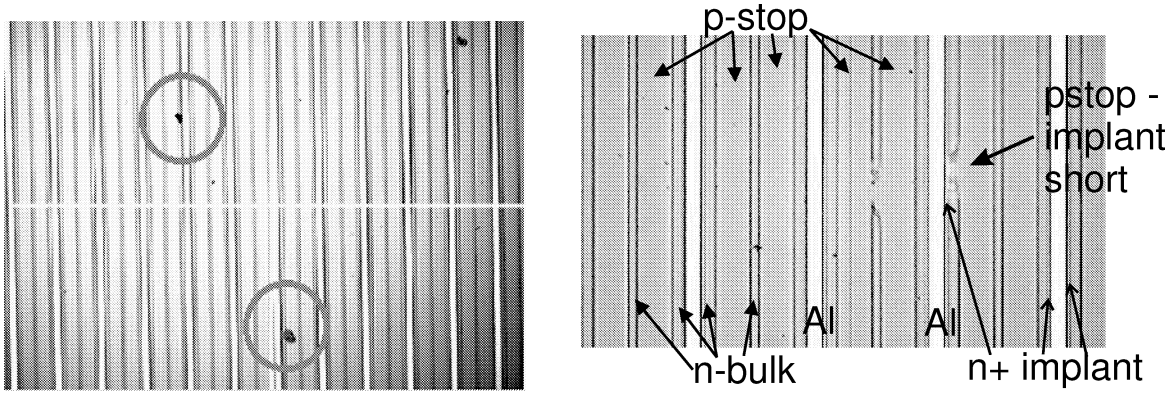


Figure 9.9: **Electrical short between implant and p-stop on the n-side.**
The short between n+ implant and the p-stop increases the implant voltage to V_{bias}, which strongly distorts the field over the whole silicon volume around the strip and therefore affects the leakage current of the faulty strip and in addition all geometrically overlapping strips on the p-side. Since we have a stereo angle strip layout on ohmic-side single strip will affect up to 15 strips on the junction side (see figure 9.10).
These shorts are happening due to miss-implanting or dust shortening. On the left picture you see shorts due to dust and on the right due to p-stop implantation overlapping the n-bulk, hence contacting the n^+-implant.

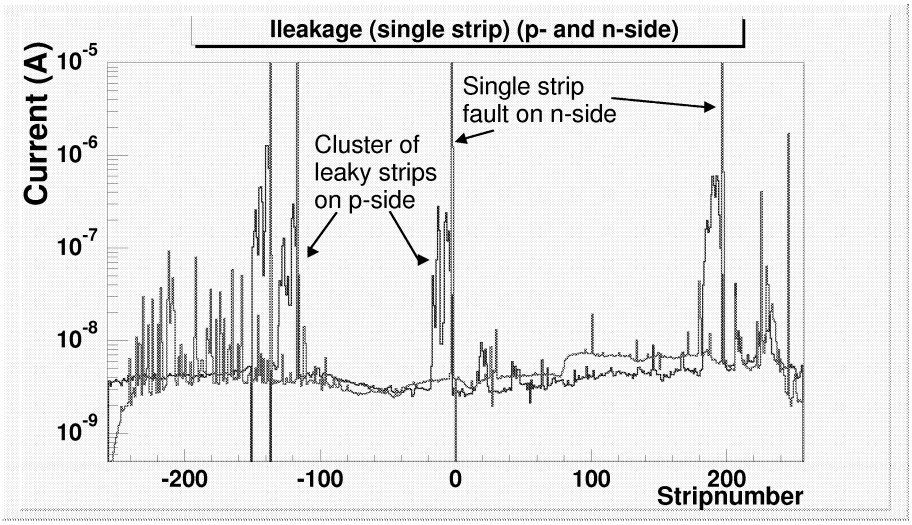


Figure 9.10: **Individual strip leakage currents on p- and n-side with a p-stop to implant short.**
One fault on the n-side causes a cluster of strip faults on the p-side.

9.3 Pinholes and pinhole candidates

Pinholes are essentially serious sensor faults, which will distort a row of channels in the final readout (see figure 9.30). Since all readout channels are capacitively coupled to the readout electronics, using charge instead of current pre-amplifying, it is not designed to be capable to take high currents. Plot 9.11 shows the current distribution over the coupling capacitor. Values between around 50-80 pA are measured[2] for a good capacitor. Pinholes are showing currents of the order of 0.1 - 10 mA for voltage values of 10 to 80 V. We will use split bias in the final readout in the detector of about 60 to 80 V. This bias scheme will imply 30 to 40 V over the coupling capacitors on both sides[3], since the pre-amplifier is on virtual ground. In addition these Al strips then have the same potential as the implant, which effectively connects chip input to the implant. The current is no more driven by the silicon but by the bias circuit. These potential differences are then affecting neighbour readout channels (see figure 9.13 for the junction side and 9.14 for the ohmic side). Figure 9.30 displays the resulting impact on the readout for the pinhole strip and its neighbours. Applying a voltage of 60 V over the insulator ensures the insulator quality very efficiently. First pinholes are detected very efficiently and secondly we ensure that no further breakdown will happen up to a depletion voltage of 120 V. The average level of current is primarily defined by the real resistivity of the SiO_2 layer but in addition the 'via'-contacts from DC pad to implant

[2] 5 pA to 5 nA is the average for different sensors; this large range will be explained in section 9.8
[3] Non-split bias would have one side with 0 V and the other side with 60 to 80 V

have to be fully conductive (see section 9.8). Therefore current deviation from detector to detector are not unexpected and not critical, because in case of a pinhole currents are much higher than the baseline currents. But figure 9.12 shows different levels in one single sensor. This hints at different levels of insulator quality. This is no real problem unless a breakdown of the insulator occurs and results in a pinhole. crucial fault.

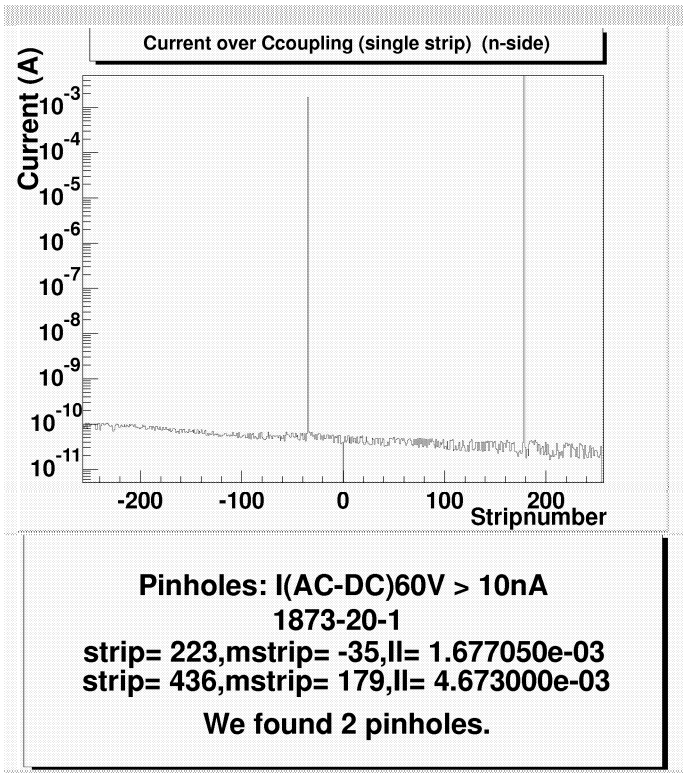


Figure 9.11: **Current over the SiO_2 insulator @ 60 V – standard measurement.** *Two pinholes were found on the n-side of this sensor. The standard quality control output displays our strip counting and the Micron strip counting scheme plus the currents flowing through the pinhole.*

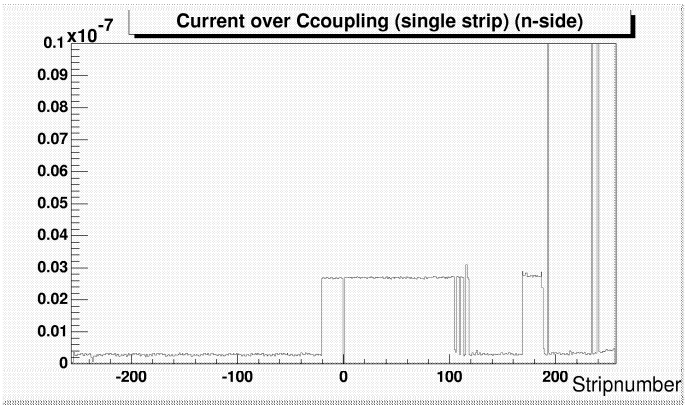


Figure 9.12: **Current over the SiO_2 insulator @ 60 V — different current levels.**
There are two different current values over one detector side. There are two explanations for the different levels, either there is another problem with bad via-hole contact (refer section 9.8), but that would show itself in the leakage currents. The other possibility would hint for different quality levels in the SiO_2 insulator.

Pinhole – Impact on neighbour strips.[24]

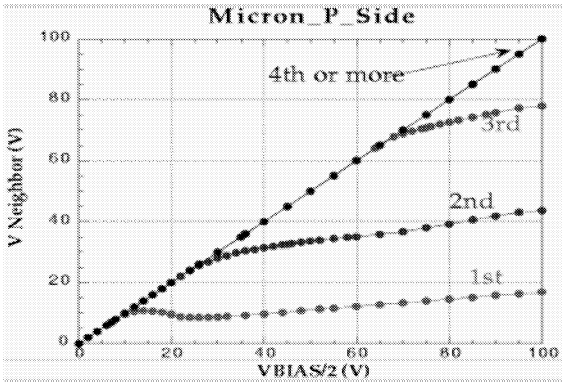


Figure 9.13: *Up to* **3** *neighbour strips are affected on both sides– p-side.*

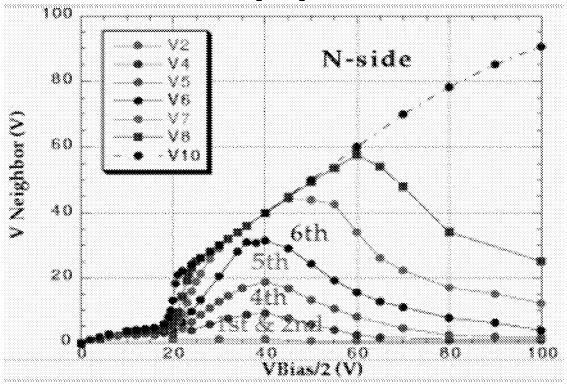


Figure 9.14: *Up to* **8** *neighbour strips are affected on both sides – n-side.*

9.4 Coupling capacity

Prototypes were delivered with a certain pattern of $C_{coupling}$. In the middle of the wafer they were within specification, but dropped down to values below specification at the sides. Primarily this would lead to bad charge coupling to the readout Al layer (see section 6.2.5). Much charge would be lost. And secondly this would result in a non-uniform gain in the final readout system across the sensor, which would make effective cluster analysis impossible. An example distribution over a complete wafer is shown in

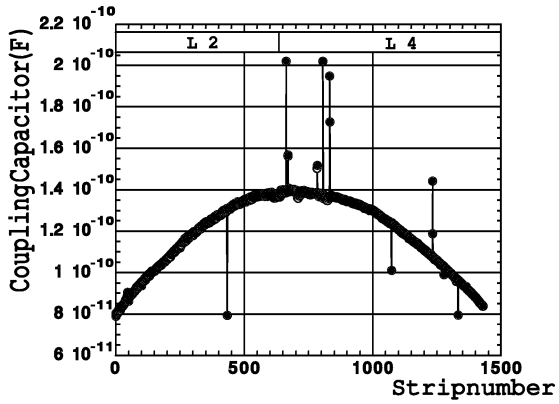


Figure 9.15: **Low $C_{coupling}$ at the edges of the wafer.**

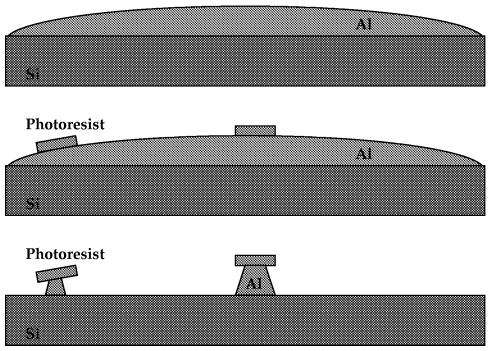


Figure 9.16: **Uneven metal deposition and underetching,** *due to sputtering problems.*

figure 9.15. Another example can be seen in figure 7.9 on page 64 and in figure 7.13 on page 65. These two examples show an existing effect on both faces of the sensor. This is a problem specific to 6" wafer technology. The Al sputterer was calibrated for 4" silicon. The new definition of a larger area is non-trivial. It is not just a question of enlarging the sputtering area but also to do it in a homogeneous way. Uneven metal deposition due to sputtering led to underetching below the photoresist. Thinning the Al strips, this led to decreasing $C_{coupling}$ values up to the sides of the wafer. The effect is visualized in picture 9.16. On a single sensor, this is observable by decreasing values from one side to the other. This problem was eliminated by a better calibration of the sputterer.

9.5 Low interstrip resistances

During production we encountered three different types of interstrip resistance problems, described below:

9.5.1 Ionic contaminant

The first occurrence was detected at Micron. An ionic contaminant, located either on the surface, in passivation layers, or at the $Si - SiO_2$ interface provided conductive paths between the strips. Tracking down and eliminating the source of the problem was done by a group of Micron and Fermilab people. The field oxide is grown by both 'wet' and 'dry' methods [12]. A 'wet' process forming the majority of the field oxide and is accomplished by burning ultra-pure H_2 and O_2 in an oven (1000 C^o) and is chosen for

fast growing times (pyrogenic oxidation). A 'dry' oxide begins and ends the processing, and forms a denser but slower-growing oxide (Si(solid) + O^2(gas) $\rightarrow$ SiO^2(solid) no H_2: 'dry'). An inert gas annealing (either N_2 or Ar) is used to reduce the trapped charge density at the $Si - SiO_2$ interface, after the oxide is grown. The annealing is crucial to maintaining good leakage current properties and proper strip isolation in the sensor. A capacitance versus voltage plot (the 'flatband' voltage), together with a nanospec (laser interferometry) measurement of the thickness, provide a measurement of the quality of the oxide and the density of interface charge traps (the flatband mainly depends on the thickness and *interface traps*). It was this flatband information that revealed that the 1671-1672 serial numbers had problems. Micron had some problems during the first run, and tried to etch off the oxide and regrow it. Problems come at the annealing step; if the gas is not ultra-pure, contaminants can be introduced. Micron had been using the house N_2 system for the annealing gas (pure bottles are expensive, and they use several). A problem was already suspected and the process switched to an argon annealing in July [26]. But still there was another unexpected source of contaminants. It had to do with the plate the wafers sat on during passivation. The silox passivation machine (Applied Materials mode 1000) burns silane to produce a protective oxide layer (of a quality only suitable for a protective layer). This is a simple device, which holds the wafers flat on a tray and heats it to 350 C^0 while running. In summer the old aluminum tray was exchanged for a new stainless steel tray. The exchange from Al to stainless steel was the main problem, since parts of the steel diffused into the SiO_2 After commissioning a new Al plate the interstrip resistance problem was fixed. Only two of these devices arrived at Karlsruhe and showed regions with high leakage currents and low bias resistances.

9.5.2 Charge up

The second type was much more severe, because it was not detected at Micron. Without the quality control at Karlsruhe, these devices would have been classified A-grade and be put into the experiment. Since they went unnoticed through the whole chain of quality control at Micron, it was clearly a problem at the very latest step, even after probing these devices. These problems with interstrip resistance seem to be unrelated to ionic contaminants, and rather due to a static charge up of the wafers. Because of the number of sensors affected (essentially all of them) and the possibility of the problem recurring while in use in the main collision hall, this problem needed to be fully understood and solved. If, for example, this was happening because the sensors were more susceptible to charge up, then it could indeed be related to an ionic contaminant in the surface layers. If this was rather due to a thinner passivation layer, this also would need to be fixed by changing the process. Figure 9.17 shows the first sensor found, having this problem. We first assumed a dark current flowing into our measurement circuit, since we were not measuring interstrip resistances at this time. But regions with nominal behavior convinced us of having low interstrip resistances for all sensors sent.

One sensor with high leakage current, low bias resistances
and
two regions with nominal measurement values.

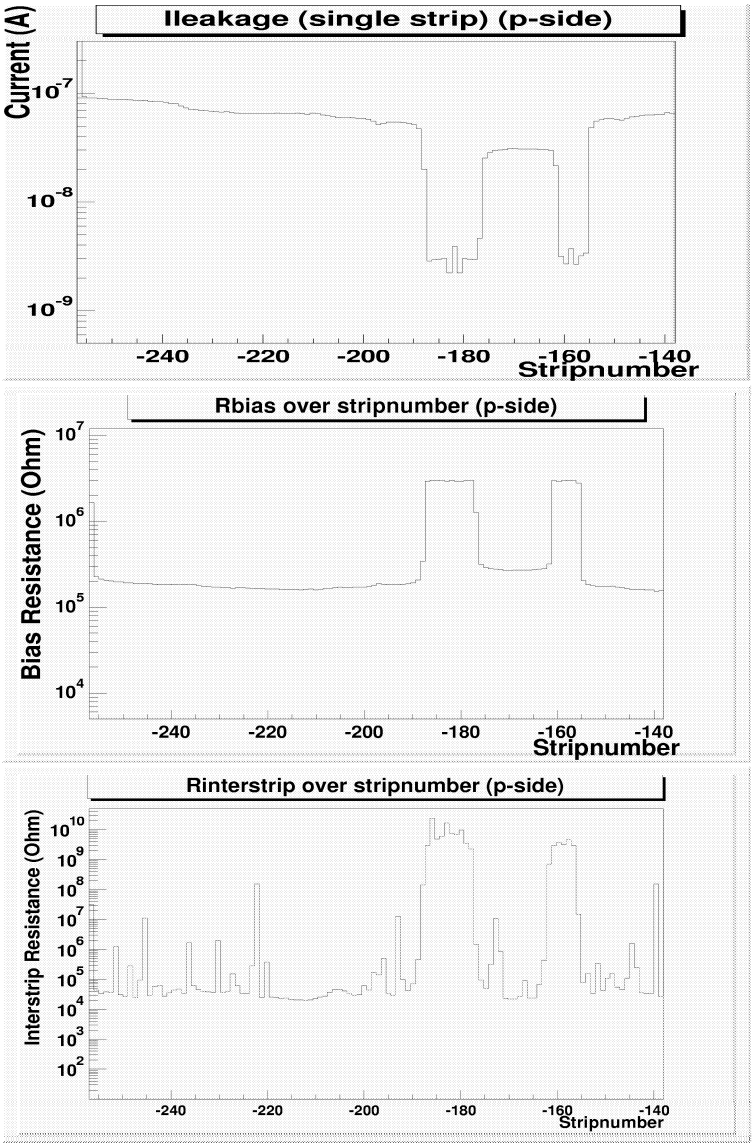
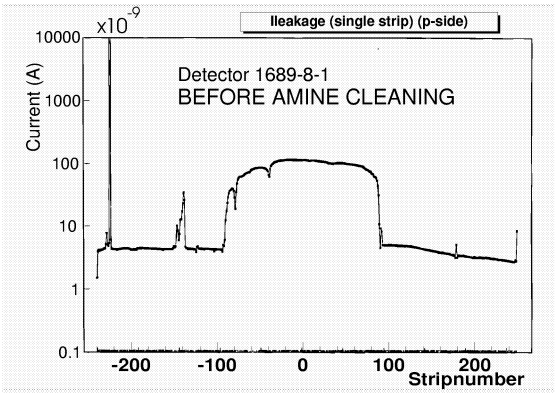


Figure 9.17:
$I_{leakage}$, R_{bias} **and** $R_{interstrip}$ **of a sensor charged up between strips.**
In all these plots two regions with nominal measurement values can be seen: $I_{leakage}$ = 3 nA, R_{bias} = 3 MΩ and $R_{interstrip}$ = 3-4 GΩ
The possibility of having a not fully depleted detector is ruled out, by continually checking for total leakage current, before, during and after the measurement.
This detector was perfect at the first check at Micron and charged up later between strips, resulting in low interstrip resistance. High leakage currents are the result of single strips drawing current from all neighbour strips, and low resistance comes from the parallel network formed by the 'shorts' between strips.

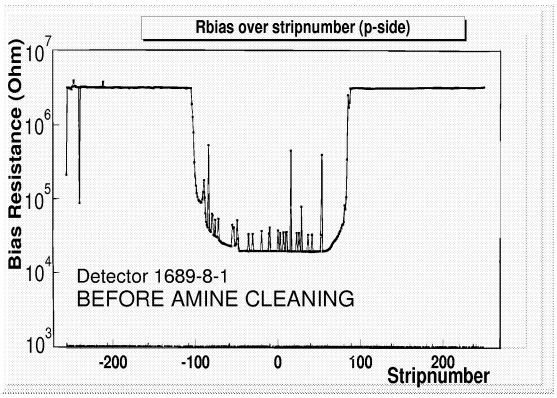
We therefore inserted a fully automatic procedure for measuring $R_{interstrip}$ into our current measurement scheme. It was found that the problem could be eliminated by cleaning the sensors in de-ionized water or amine (see figure 9.18). All sensors were recovered. This was the first hint that some charging up happens to the SiO_2 layer. The likely candidates producing the problem are the handling, cutting, testing, and final packaging stages, since the problem only appeared at the very last stage at Micron. Finally two problems were isolated. In one factory at Micron there is no static control implemented and humidity levels varied from 25 % to 65 %. Therefore the likely problem

is just one of static buildup. Micron employees were made aware about the dangers of electrostatic discharge (ESD) damage to circuitry. Additionally the packaging was changed to ESD protective boxes. An interim step has been implemented whereby the old boxes are used, but with aluminum foil. There has been a significant reduction in the problem now that awareness has been increased. The main reason for the charge up was discovered later. The storing and packaging material changed from lint-free paper to another material. Obviously this was the problem, since when Micron changed back to the previous brand/type of lint-free, together with increased awareness and the removal of teflon boards for temporary storage of diced wafers, this dismissed the problem. During the upgrade of the silicon detector for the Delphi experiment at LEP, a similar problem was encountered. Plastic packaging introduced pinholes during shipping from SIntef in Oslo to CERN [35].

Leakage current and bias resistor values of a low interstrip resistance sensor *BEFORE* cleaning with amine.

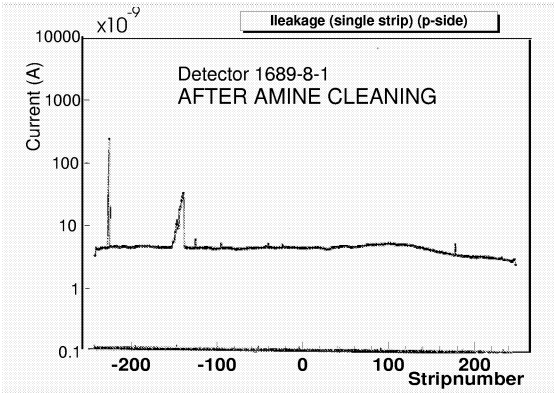


A.) $I_{leakage}$ **of a low interstrip sensor.**

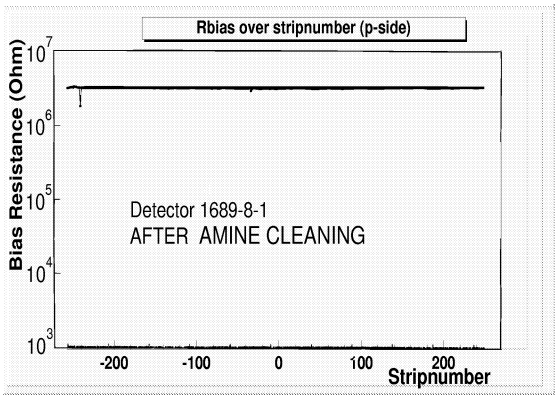


B.) R_{bias} **of a low interstrip sensor.**

Leakage current and bias resistor values of a low interstrip resistance sensor *AFTER* cleaning with amine.



C.) $I_{leakage}$ **of a low interstrip sensor.**



D.) R_{bias} **of a low interstrip sensor.**

Figure 9.18: **Amine cleaning recovers sensors with low** $R_{interstrip}$**.**

9.5.3 Low interstrip resistance in a regular pattern

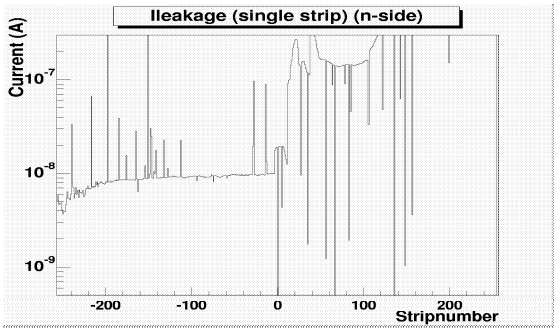
A new temporarily low interstrip problem came up. Low $R_{interstrip}$ values seemed to be localized and regular, affecting only a few strips and in a regular pattern. This pattern seems to be consistent with the PECVD[4] gas outlets. In addition this pattern is occasionally visible on wafers (which are then failed). Assuming the problems were at dicing, experiments with changes to the cutting, contact with the blue film, and contact with lint-free tissue were conducted. It was found that by eliminating contact with the lint-free tissue on the p-side, low interstrip resistance no longer appeared at testing. Pushing the p-side of the wafer down on the even lint-free tissue prior to cutting (or possibly brushing afterwards) causes certain charge-up susceptible strips to fail. This is a temporary condition that has been largely corrected by an elaborate cleaning of the charge from the surface. Though not the ultimate cause of the charge up, the PECVD machine is causing certain strips to be more susceptible to charging up and shorting out. These layers are used to give a final protective SiO_2 coating, and sometimes to make capacitive oxides.

9.6 High depletion voltage

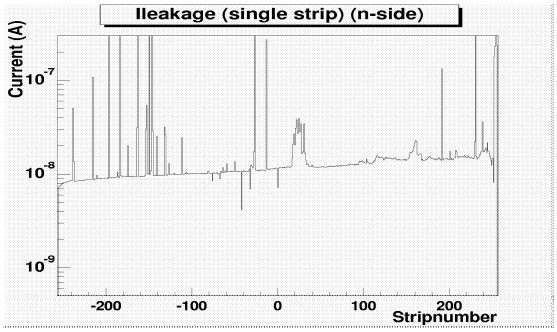
Sensors with very high depletion voltages were detected at Karlsruhe. Discrepancies from an expected $V_{depletion} = 40$ V up to $V_{depletion} > 160\ V$ were measured. Sometimes two sensors out of the same wafer showed different depletion behavior. As shown in chapter 6.2.1 $V_{depletion}$ is mainly dependent on the sheet resistivity of the bulk silicon, which should be homogeneous over the whole 6" wafer. At Micron $V_{depletion}$ is measured on the test structure diode at the sides of the wafer (see figure 9.1 on page 82). Therefore only a *'local'* image of the bulk resistivity is measured. Discrepancies on the 2 sensors are only detectable by measuring the bulk capacitance for each sensor.
Since the junction side is still working fine with a voltage below $V_{depletion}$, these problematic devices were not detected at Micron. The behavior of the n-side is a totally different one, something only noticed at Karlsruhe. We find *'regions'* with nominal values and some *'regions'* with the characteristics of low interstrip resistance (see section 9.5), which is something not expected for the n-side, since the interstrip resistance is completely defined by the p-stop implants between the strips (see figure 9.19). This phenomenon of high $I_{leakage}$, low R_{bias} and low $R_{interstrip}$ is only explicable by a region not being fully depleted. Operating below depletion voltage results in a huge amount of free charge carriers at the borders of the sensors. Enough to supply efficient conduction between strips even beneath the p-stop barriers. The electrical fields are not fully built up to define separate electrical entities for the individual strips. Our measurements showed, that in these cases $V_{depletion}$ on the ohmic side is only reached at a higher voltage than on the p-side.

[4]PECVD is plasma-enhanced chemical vapor deposition.

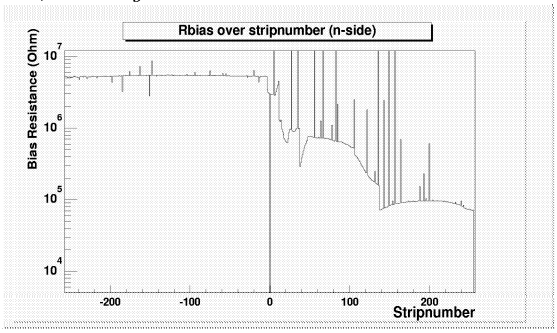
Leakage current, bias resistor and interstrip resistances below and above $V_{Depletion}$. Sensor depletes above 80 V.



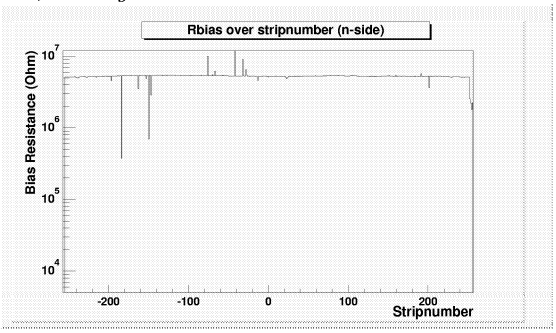
A.) $I_{leakage}$ **at** $V_{bias} = 80\ V$**.**



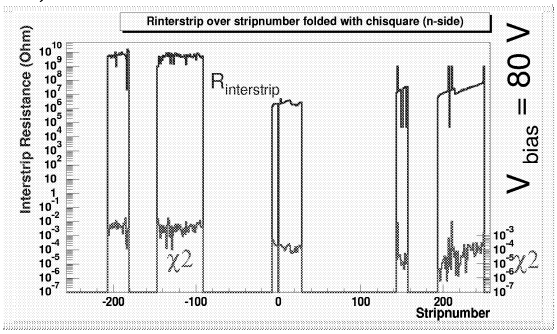
B.)$I_{leakage}$ **at** $V_{bias} = 100\ V$**..**



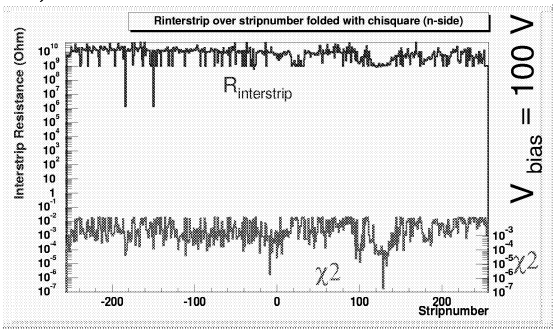
C.) R_{bias} **at** $V_{bias} = 80\ V$**.**



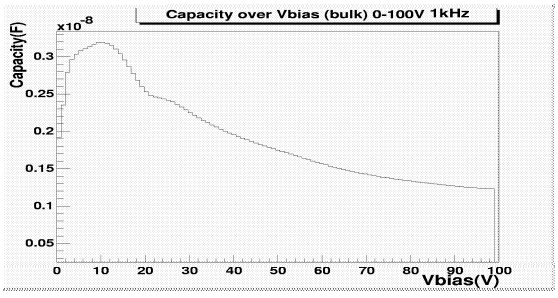
D.) R_{bias} **at** $V_{bias} = 100\ V$**.**



E.) $R_{interstrip}$ **at** $V_{bias} = 80\ V$**.**
Avoiding overprobing, we scanned only representative regions. Low $R_{interstrip}$ **was directly obvious after some strips.**



F.) $R_{interstrip}$ **at** $V_{bias} = 100\ V$**.**
We scanned the complete sensor to ensure nominal $R_{interstrip}$ **over the whole sensor.**



G.) Total capacitance vs. $V_{Depletion}$**.**
The capacitance is still decreasing above 80 V.

Figure 9.19: **Effect of operating with a voltage below** $V_{Depletion}$**.**
Strips are almost shorted, each strips draws the leakage current of all neighbours combined, and the bias resistors are forming a parallel network.

The *'local'* appearance of high depletion voltage regions hints at inhomogeneous resistivity bulk silicon. Another explanation could be strip width differences of the implants (see chapter 6.2 on page 53). However the overall structure: abrupt rising and always covering *continuous* areas favors the theory of low local sheet resistivity.
Sensors delivered by Micron indicating high $V_{depletion}$ on the test sheets tend to deplete at even higher voltages. These sensor should be grouped together to have a special group with a higher depletion or should not at all be put into the experiment. From the point of coupling capacitor breakdown, we have no problem since we are using split bias and have still some safety factor with respect to breakdown (see section 9.14). Later, resistivity measurements on different wafers of the silicon proved the inhomogeneities in the silicon (figure 9.20).

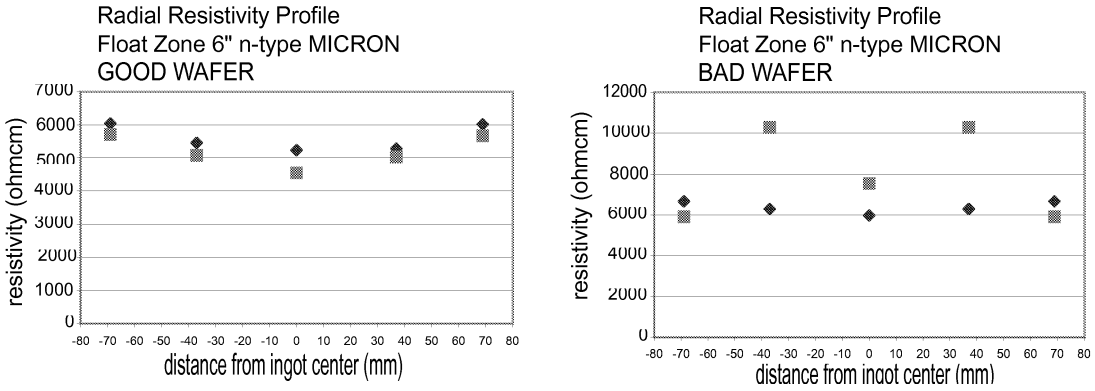


Figure 9.20: **Resistivity measurements across two wafers from different silicon ingots** *[26].*
The resistivity of the finished ingot was measured along its length to determine the usable region. The specification is 3-7 kΩcm. Wafers are then cut from the usable region only. The two plots contain each resistivity measurements across two wafers from different ingots. The two wafers are the "first" and "last" wafers taken from the same ingot, and the location of each is noted in cm. The first wafer (diamond symbol) is from the seed crystal side and will be more pure (higher resistivity) by virtue of the float-zone growth. The last wafer used (square symbol) is from the end, will be less pure and have lower resistivity. Variation of resistivity radially for the left case is about 20%. On the right plot regions with a resistivity of 10 kΩcm and more can be seen.

The sensors delivered in a period from january 1999 to november 1999 were reclassified and all sensors not passing the $V_{depletion}$+20 V specification on the junction and the ohmic side were rejected. The production of 50 additional sensors was initiated.

9.7 Humidity effects

During summer 1999 a sensitivity to humidity was detected. The quality control was transferred to another bigger laboratory with an air condition system. Suddenly a large increase in total leakage current was detected (figure 9.21).

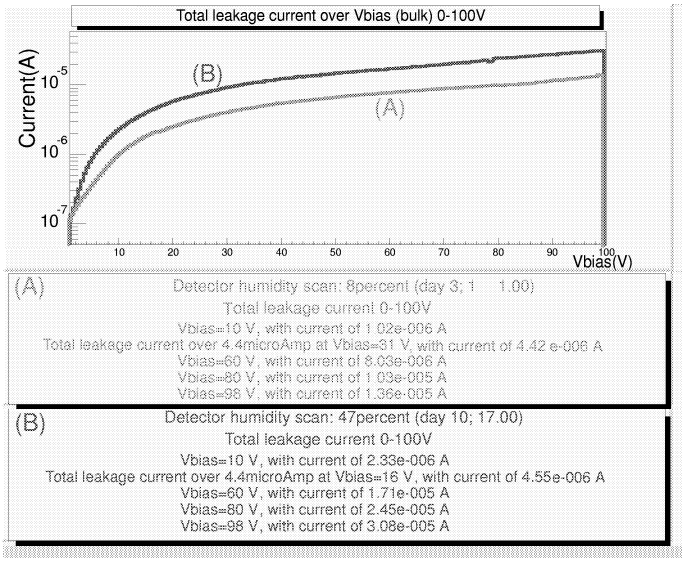


Figure 9.21: *Two different current behaviors for one single sensor at different humidity levels are displayed. We noticed that above humidity of 40 % and a certain amount of time ∼ 1.5 h the currents are increasing dramatically. A humidity of ≈ 40 % acts like a due point. To evaluate the effect along the whole range from 0 to 100 V we used a logarithmic scale for the currents. Some current values for certain different voltage values are written in the lower part. In figure 9.22 a decrease in R_{bias} is visible.*

The measurement of a total leakage current of ∼ 50 μA initiated thorough checking and testing of our test equipment with no result. Only flooding the probestations with dry clean air made sensible measurement possible. Total leakage current dropped down again to ∼ 7 μA. We immediately introduced dry and clean storages for the sensors, which solved the problem. No problem is expected in the final experiment, since all sensors recovered perfectly and the final assembly will be flooded with dry nitrogen. Further investigation indicated the dew point at a humidity of ∼ 40%. Furthermore we noticed a certain amount of time is needed to produce the effect. Figure 9.22 shows a sensor, behaving perfectly normally, directly out of the dry box. There is however an increase of leakage current after staying in a humid environment for ∼ 1.5 h (over lunch). Immediate remeasurement of a former 'good' region showed the expected increase in current. Further flooding of storage cabinets and test boxes with dry clean air eliminated the problem completely.

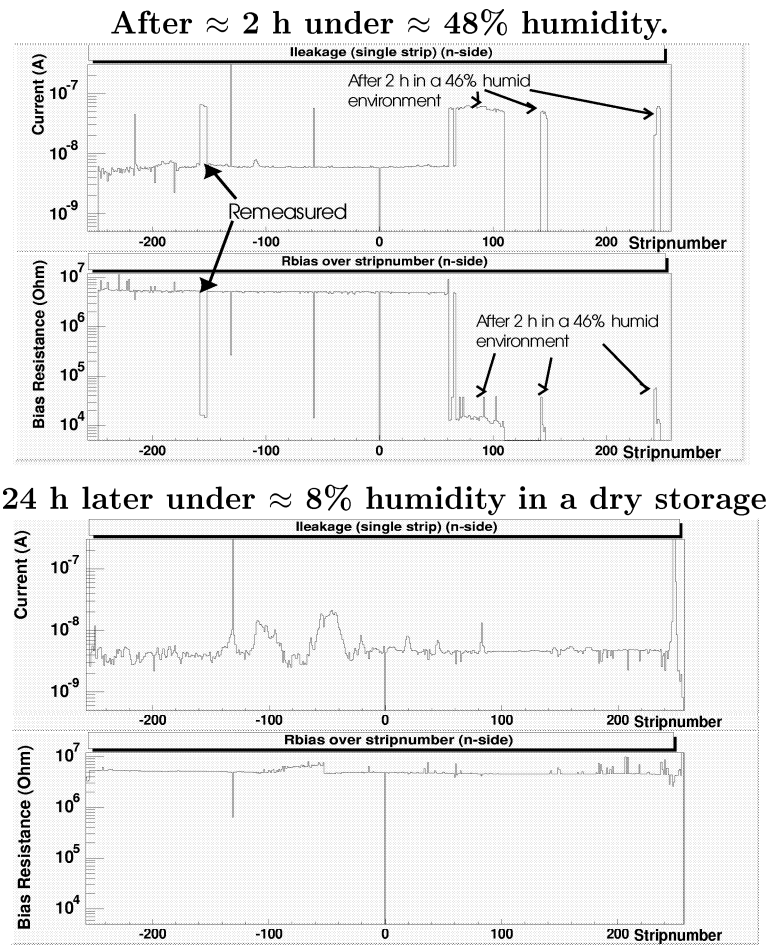


Figure 9.22: **Increase of leakage current after a period in humid environment.**
The change in the base leakage current and bias resistance level is quite obvious. Strips -160 to -140 were remeasured. Therefore the increase is caused by decrease of inter-strip resistance.

9.8 Via-holes and adapting the understanding of measurement levels.

To qualify and classify the detector we have to measure individual strip leakage currents and look for pinholes. To accomplish these measurements, we have to access the strip implant directly, something impossible without proper sensor design, due to the fact that the implant is decoupled from the rest of the sensor surface by a SiO_2 insulator layer. Therefore an extra conductive connection to the implant via the via-hole is made for probing issues. It ends on an Al pad –the DC-pad. An example scheme of the pinhole measurement and the location of the via-hole is shown in figure 9.23; the pinhole method is explained in chapter 7. Differences in these contacts leading to differences in the average level of the current, since with different levels of isolation to the implant we collect currents from other sensor areas than from the implant only. During quality control we encountered different levels of current over the coupling capacitor (section 9.3). Another problem arose when measuring leakage currents and R_{bias}; we often had values hinting at 'no contact', but even re-adjustment gave no improvement.

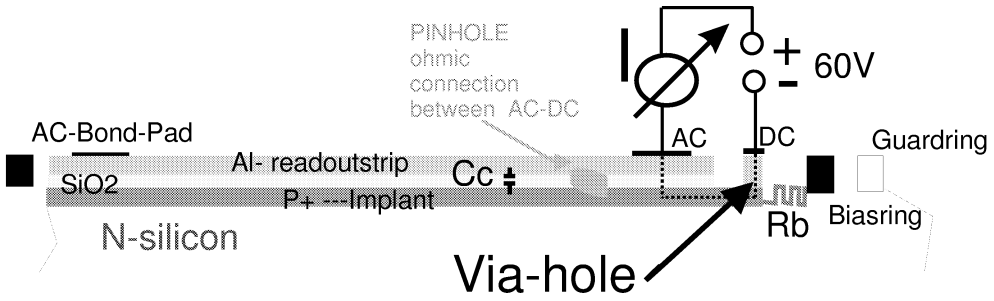


Figure 9.23: **Via holes and pinhole measurement scheme.**
The via-hole is the contact channel between implant and DC-Pad and is designed for testing purposes only.

Two examples are displayed in figure 9.25. These devices are then not classifiable. Figure 9.24 shows resulting detector damage, because the 'no contact' signature led to additional probing.

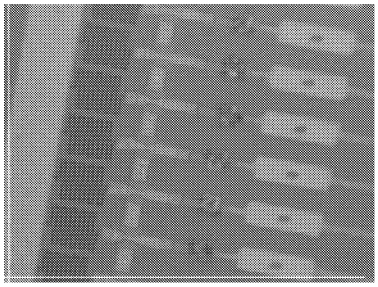


Figure 9.24: **Overprobed DC pads.**
Since the via-holes are not fully opened, the measurements of pinholes and especially leakage currents are giving strange results. Measurement results hinting for bad contact, encourages testing personal to overprobe the pads. In this case it almost results in the contacting of DC pads to AC pads.

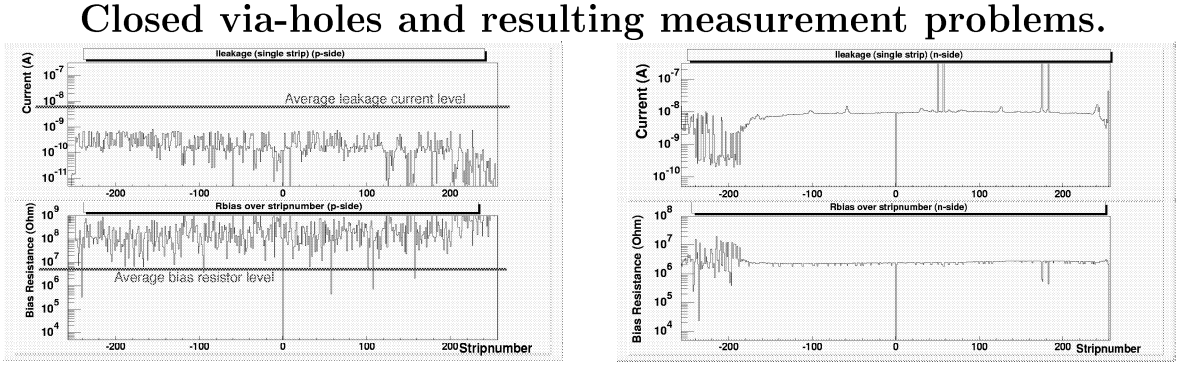


Figure 9.25: *On the left you see a sensor with almost closed via-holes for all channels. A reasonable measurement is impossible. All results look like bad contact. The right plot shows the same problem but only for a small region at the start.*

9.9 High bias resistors

There were problems of silicon oil contamination and scratches at IBS[5] in France. Micron recovered a fraction of wafers by removing the oil with the plasma etching method. Etching was done while the polysilicon layer was exposed, hence thinning the bias resistors and leading to a number of sensors with high bias resistance of $\sim$ 9-11 $M\Omega$ (see figure 9.26).

Low bias resistors after improper polysilicon implantation.
High bias resistors due to additional plasma etching.

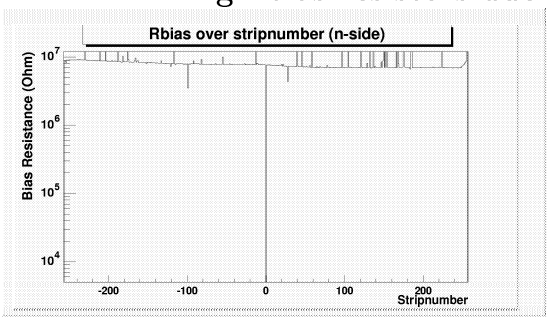


Figure 9.26: **High bias resistors** *caused by additional plasma etching to remove oil contaminant from IBS. This additional etching thinned the polysilicon resistors, leading to higher resistance*

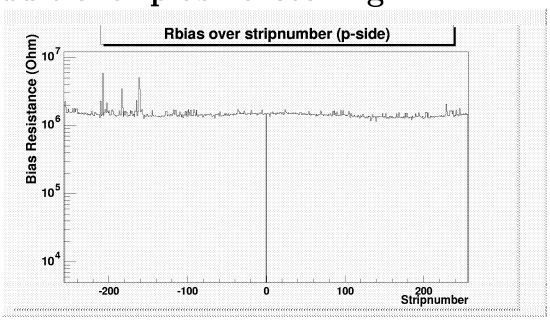


Figure 9.27: *Faulty polysilicon implanting results in too* **low bias resistance**, *which would result in higher noise (see section 6.2.4). The correlation with the process is obvious, since the defect appears only on one side. Later bad environment conditions would have caused the defect to happen on both sides.*

9.10 Low bias resistors

In may 1998 two batches of implants were not correctly processed. It is not known if the polysilicon was over-implanted, or if the polysilicon was etched too thin. However the results of this are obvious, bias resistors had resistances between 0.9 and 1 MΩ (see figure 9.27 left), which is much too low. All were rejected.

[5]IBS is doing the implant to p-stop bridges

9.11 Bad handling

Careless handling of sensors is a sure way to decrease yield. Silicon is very fragile material and the microscopic structures on silicon microstrip sensors are especially sensitive to damage. Keeping testing and production areas clean is of uttermost importance. Figure 9.28 shows scratches on a silicon sensor, probably damaged at IBS. This is still a lucky case, where the scratches concentrated on the bias ring without interrupting it. Despite the strip to strip short this sensor is still usable (figure 9.28 right side). Because of these faults, for some time the overall yield decreased significantly. The contact persons of Fermilab struggled to make the staff of Micron and IBS aware of the problem. After a period of increasing the awareness of employees and improving cleanliness, the problem disappeared and the yield increased significantly. In addition new procedures were introduced in collaboration with the employees. This is another example of problems directly related to the size of these devices. The handling of devices this size needs more experience, in particular new handling procedures. Only enlarging the direct processing apparatus is not enough. Special storages and even packaging must be provided. For shipping and transfer the traditional 4" boxes are used. The slightly larger length of 5.75 mm requires more precise placement in these boxes. Each sensor placement goes in line with the danger of crushing the sensor edges.

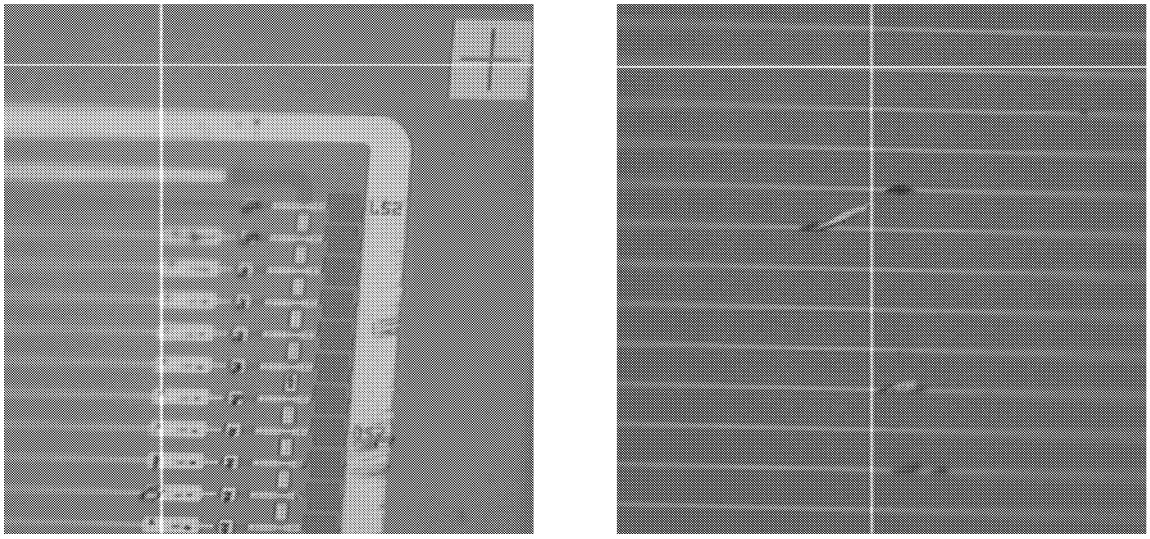


Figure 9.28: **Scratches due to bad handling at IBS and Micron.**

9.12 Problems with the silox machine

Problems appeared at the SiO_2 layer growing stage. The "Silox" apparatus had to be rearranged and cleaned. Wafers at the passivation stage came out with both color variations and 'shadows' from flecks that fell down on the wafers during passivation (figure 9.29). Taking it apart and cleaning it improved things. Some of these devices even went through the quality control at Micron and arrived at Karlsruhe. After finding these strange patches, these devices were tested more thoroughly and additional capacitance tests were done and several areas were re-tested. Nevertheless, since these devices showed nominal electrical behavior and were accepted.

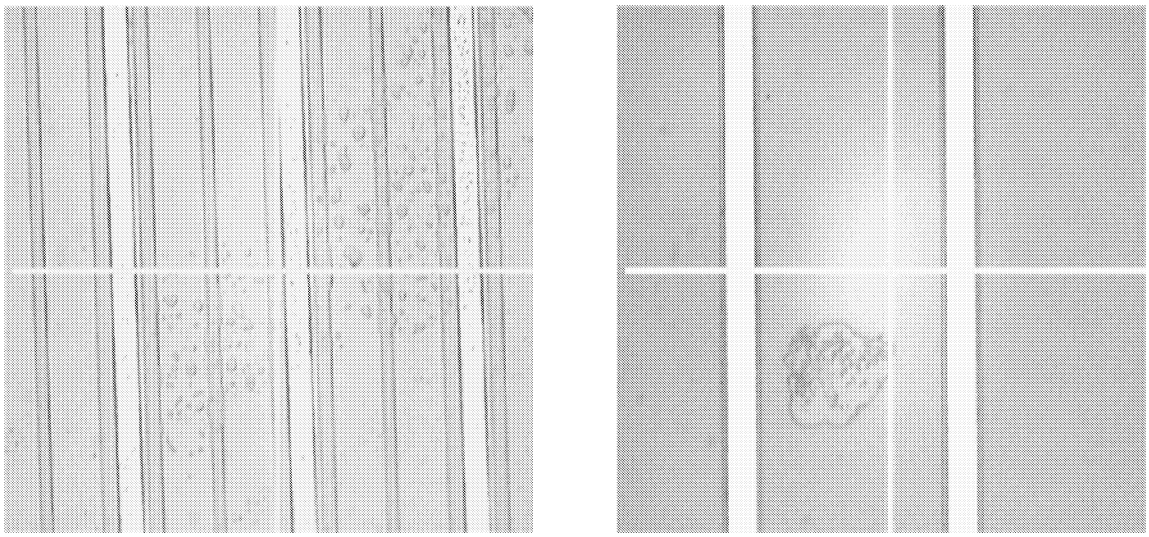


Figure 9.29: **Surface contaminants on the sensors coming from a dirty silox machine.**

9.13 Strip defects – impact on readout

Finally all electrical defects classified have certain impact on the readout. Figure 9.30 illustrates the consequences of the different defects. All connected channels have a higher noise than unconnected channels, caused mainly by the capacitive load, the dark current and the resistance noise. Channels with a high leakage current (*leaky*) have a much higher noise, they will not be used in the final data acquisition. Shorted strips (*short*) have double the nominal capacitance, hence a slightly higher noise, however the strip short connects the electronic channels too, and the reset signal of one channel disturbs the other. One of these channels will be disconnected from the readout. Breaks in the Al strip (*open*) decrease the capacitance connected to the readout, the noise is slightly lower. However, only part of the strip will be read out, in addition the signal of the strips following on the connected sensors is not available. The current through

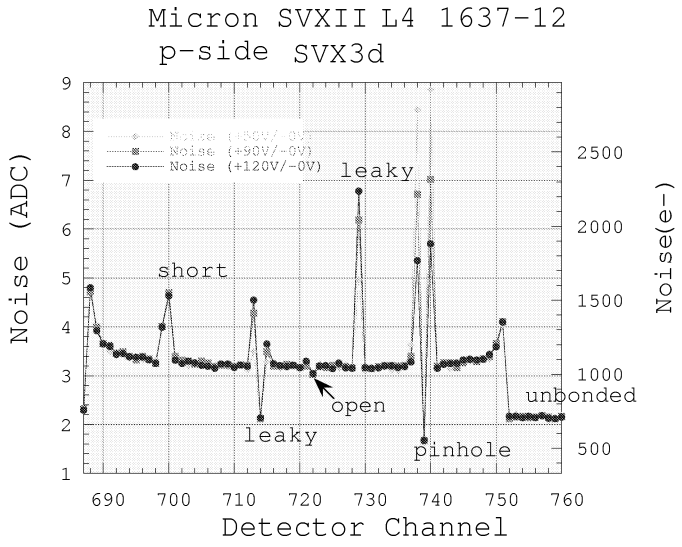


Figure 9.30: **Effect of sensor faults on the readout of the SVX3** *[22].*

an Al-readoutstrip — implant short (*pinhole*) is driven by the bias circuit. This defect effects many neighbouring strips and may even damage the preamplifier. A pinhole must be disconnected from the readout.

9.14 Breakdown voltage - Tuning of bonding procedure

Wire bonding is always a critical issue. In the past bonding procedures, not especially tuned to the sensors, led to a decrease in the breakdown voltage of the coupling capacitor or in the worst case to pinholes in the sensors. These pinholes will be connected to the readout electronics, at this stage they are 'unknown', because they were only created during the wire bonding phase[6]. The free flowing currents through the shorted insulator will distort the readout or may even damage the pre-amplifier, (figure 9.30). Learning from past experience [35] the bonding parameters were checked on one b-grade sensor. One sensor without any pinholes or known coupling capacitor anomalies was used to measure the breakdown voltage on 5 strips. This should give an estimate of the average breakdown voltage of the sensor without having any lasting effect on each coupling capacitor. The sensor was bonded with standard bonding parameters to ensure the usability of these parameters. Figure 9.31 shows that there is still some tuning needed.

[6]Bonding is done after quality control and construction (gluing). The construction sequence is illustrated in chapter 10.2.

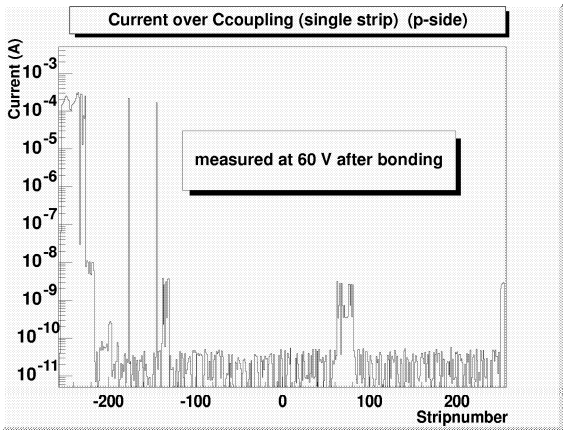
Stripnumber	Breakdown voltage [V]
-236	205
-234	189
-230	158
-216	181
-176	172

Table 9.2: **Breakdown voltages of some individual strips.**
Only some individual strips were measured manually to learn about and understand the breakdown signatures. The first sensor was bonded without previous probing on all strips for breakdown to have real production condition without any previous possible effects due to probing. All breakdown voltages are within the specification of 120 V.

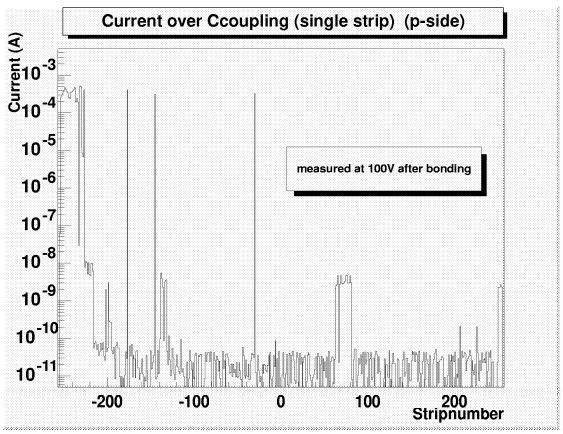
Many pinholes were created and some regions showed anomalous behavior according to the current through the insulation, e.g. strip -140 to -130 and 60 to 90. The conclusion was to test more sensors to find the 'right' parameters and finally apply theses parameters to a full detector side to confirm them. Table 9.2 shows the breakdown voltages ($V_{breakdown}$) of the measured strips. This confirms the initial quality of the region, mostly affected by the bonding.
The coupling capacitor breakdown voltages of three more sensors were measured, two sensors for tuning purposes and the last one to test the resulting optimized parameters. The measurements were done in Karlsruhe, while the bonding was done in Pisa, where the final ladder and module construction is done (see chapter 10.2). Multiple bonding parameter sets of TIME (bonding arm resting on the pad), STRENGTH (pressure on the pad) and POWER (power of the ultrasonic wave) were applied.

Measurement

The measurement is similar to the normal pinhole measurement. A voltage ramp instead of a single constant voltage was applied over the coupling capacitor. Testing the breakdown voltage before and after bonding requires a non-destructive measurement. The very delicate balance of not damaging the capacitor while exploring the voltage up to the breakdown voltage was difficult to maintain. It was decided to explore the current behavior right at the edge of the breakdown. The measurement program was changed to increase the voltage in defined intervals and in a fixed timing. The measurement 'break' was then done manually. These manual tests led to a reasonable but still sensitive 'break condition'. All voltages and currents were saved including the values at breakdown. The second step was to efficiently study the breakdown in a minimum of time, with the best possible accuracy and with a minimum of real breakdowns. The process was automated to cope with the need of measuring the breakdown voltage for all strips on 3 sensors. We refrained from defining a fixed value of current to stop the measurement, to cope with different current levels of individual strips. We started a



Pinhole test after bonding (60 V). *Many pinholes were created at the start of the sensor. The coupling capacitors in some other regions were damaged too, visible due to a high increase in the average current level. Strip 60 to 90 showed a high increase in the currents.*



Pinhole test after bonding (100 V). *Increasing of the average current levels is expected, but the increase is higher than anticipated for an insulator. An additional pinhole was created at 100 V. With a minimum breakdown voltage of 120 V, measuring at 100 V should have no effect at all.*

Figure 9.31: **Pinhole measurement after bonding.** There were zero initial pinholes prior to bonding.

voltage ramp at 60 V up to 120 V with a 1 V step. This provided the mean current value with $mean = \sum_{V=60}^{V=120} I(V)/60$. To avoid a breakdown, the voltage stepping was changed to 0.1 V above 120 V. Already existing pinholes where detected with a current above 1 μA at the starting voltage of 60 V. The 'break condition' is displayed in formula 9.1:

$$Break\ condition = \begin{cases} I(V) \geq n \times \sum_{V=60}^{V=120} I(V)/60\ for\ V \geq 120\ V \\ I(V) \geq 1\mu A \\ V \geq 200\ V \end{cases} \tag{9.1}$$

where n proved to be efficient between 5 and 12.
Still all these precautions did not enable us to save all the strips, quite a fraction of coupling capacitors were damaged. The problems associated with defining a 'good break condition' is demonstrated in figure 9.32 and 9.33. The immediate increase from 4.2 pA to 1.07 mA caused a real breakdown before any 'break condition' could be applied. The whole procedure was tuned to save as many strips as possible for future measurement after bonding.

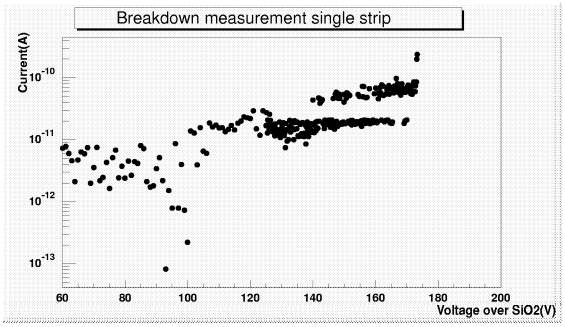


Figure 9.32: **Non-destructive breakdown measurement (one single strip).**
According to an insulator, there is no real slope visible. An increase is observable and two significantly higher values are observable at the end. The increase is 'slow' enough for the program to stop before a real breakdown happens.

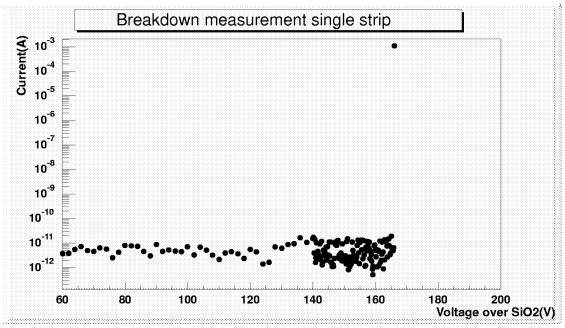


Figure 9.33: **Real breakdown of the coupling capacitor. (IV-scan)**
The current level is almost constant. Even with the automated procedure and a stepping of 0.1 V, the breakdown is unavoidable. The current steps from 4.2 pA to 1.07 mA. The SiO_2 insulates until the last point before unrecoverable damage happens to the capacitor. (In this measurement the mean was taken after 140 V.)

Results

The effect of bonding can be accessed when looking at the breakdown voltage differences between the unbonded and bonded sensors. On each sensor several sets of parameters were applied in different regions and the effect can directly be observed in figure 9.34and 9.36. The bonding time and power was gradually increased starting from strip 256 down to -256. The breakdown voltages on the second half (strip 1 to 256) were around 190 V before and after bonding. Figure 9.36 shows $V_{breakdown}$ and breakdown currents $I_{breakdown}$ before and after bonding, figure 9.34 displays the differences of $V_{breakdown\ -\ before\ bonding}$ and $V_{breakdown\ -\ after\ bonding}$. Differences of 20 to 40 V appear either due to bonding, or more probably due to a combination of bonding and initial breakdown testing, which already stresses the capacitor. The values of -70 V are artificial, this is the voltage defined for a pinhole created at the initial measurement of the unbonded sensor, therefore useless for any comparison. Good areas appear with voltage differences around zero. Values of difference at about 100 to 120 V are indications of pinholes created during the bonding phase. For the breakdown test after bonding, the pinholes are flagged, using the signature of a high breakdown current ($I_{breakdown} \geq 1\ \mu$A). The difference between the initial breakdown voltage value of $\sim$ 160 to 180 V and the starting voltage of 60 V results in 100 to 120 V characteristic of a pinhole. On the second half of the sensor more destructive bonding parameter were chosen to show and explore the possible damage due to bad bonding. Nearly every coupling capacitor was stressed due to bonding and permanently effected. Many pinholes

were produced. The measurement was done for a p-side. The bonding parameters for the different detector regions are shown in table 9.3. Naturally all bonding parameters are additionally constrained to supply full electrical contact and to endure a force of about 10 g.

Pads	Parameter:			
	F: Strength	T: Time	PW: Power	
256	15	85	90	
255 .. 207	15	20	85	
206 .. 167	15	20	95	
166 .. 106	15	25	100	
105 .. 001	15	25	120	
-001 .. 100	15	30	120	
-101 .. 152	15	30	120	(no bonding wire)
-153 .. 256	15	20	80	

Table 9.3: **Differently treated regions of the sensor 1685-15-1**

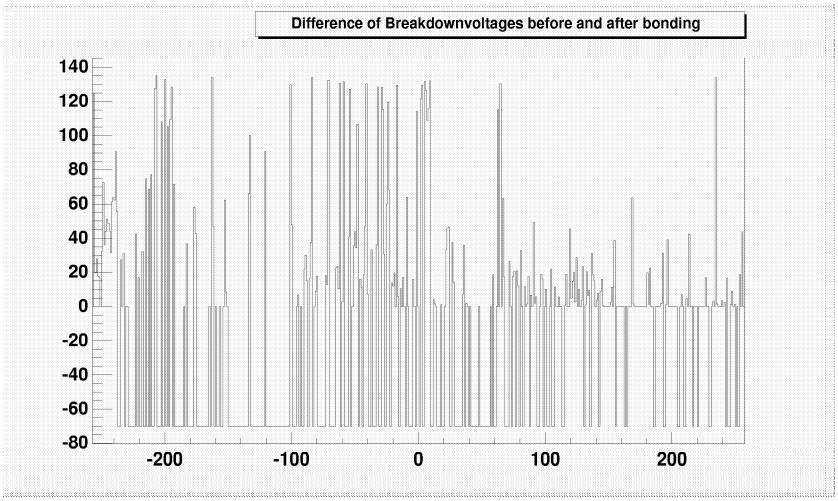


Figure 9.34: **Difference in the breakdown voltage before and after bonding.** *Several regions have been treated differently, as can be seen at higher voltage differences. Starting from very destructive sets of parameters (strips -256 to -1) passing strip one the parameter sets proved to be more and more usable. Sensor 1685-15-1*

On another detector $V_{breakdown}$ values of the n-side strips were measured to have a second sample to confirm the first result. This is also important to confirm the ability to use one set of parameters on both sides. All results can be seen in [27]. A smaller number of real breakdowns happened on this sensor, and the results confirmed the first

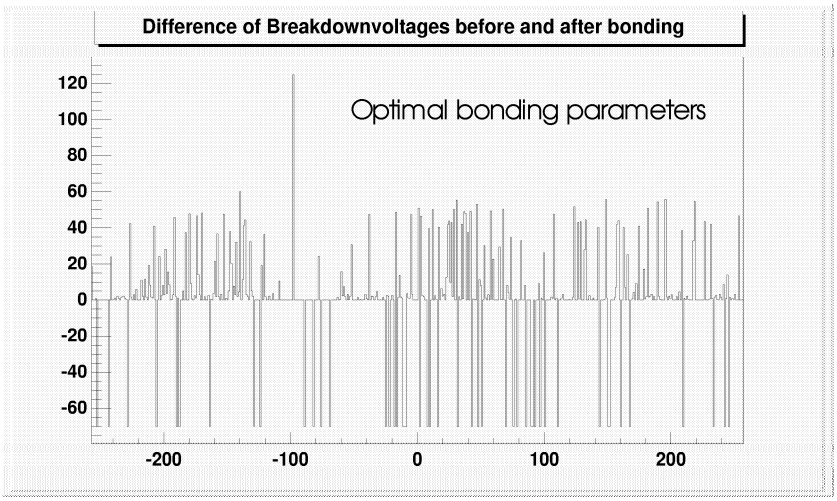


Figure 9.35: **The difference in the breakdown voltage before and after bonding.**
This sensor has been treated with optimal bonding parameters. Only one pinhole was created. This is of no concern, since the initial stress is always effecting the coupling capacitor.

measurement on the p-side. The resulting optimized bonding parameter sets are displayed in table 9.4 . The optimized bonding parameters were tested on 1686-9-1 (figure 9.35 and 9.37). Obviously the chosen parameter set should ensure mass production without the risk of some additional pinhole creation.

Parameter:			
F: Strenght	T: Time	PW: Power	Result
15	20	80	Good
15	18	78	Good
15	20	85	Good
15	20	90	Still Good
15	20	100	Fair
15	25	100	Fair
15	25	110	Bad
15	30	110	Very bad

Table 9.4: **Different bonding parameters and their effects on the coupling capacitors.** *The results of all measured sensors were taken into account.*

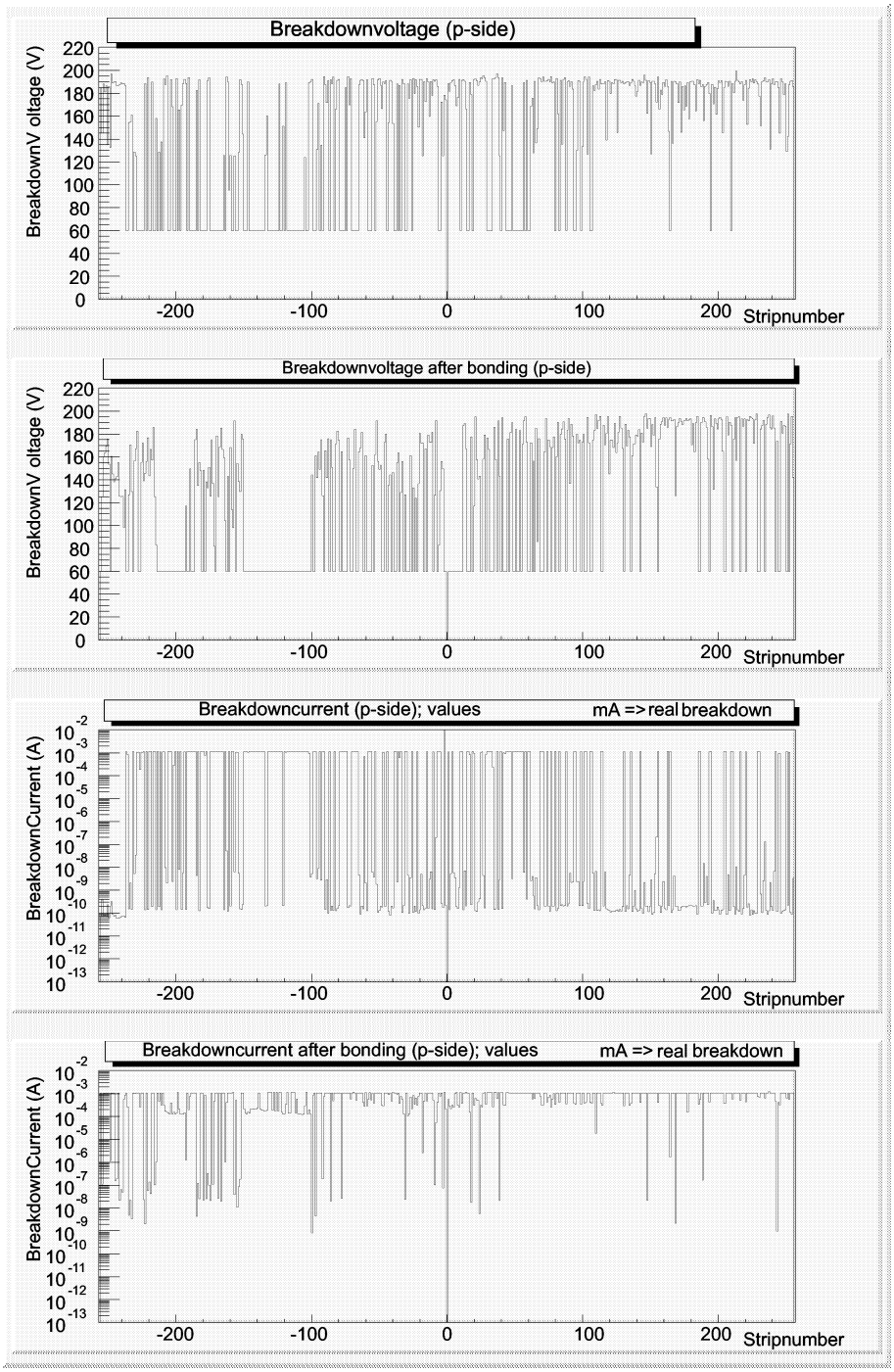


Figure 9.36: **Breakdown voltage and breakdown current, before and after bonding (different parameters).**
Several regions have been treated differently, as can be seen at higher voltage differences. The measurement starts at 60 V, therefore breakdown voltages of 60 V indicate already existing pinholes.

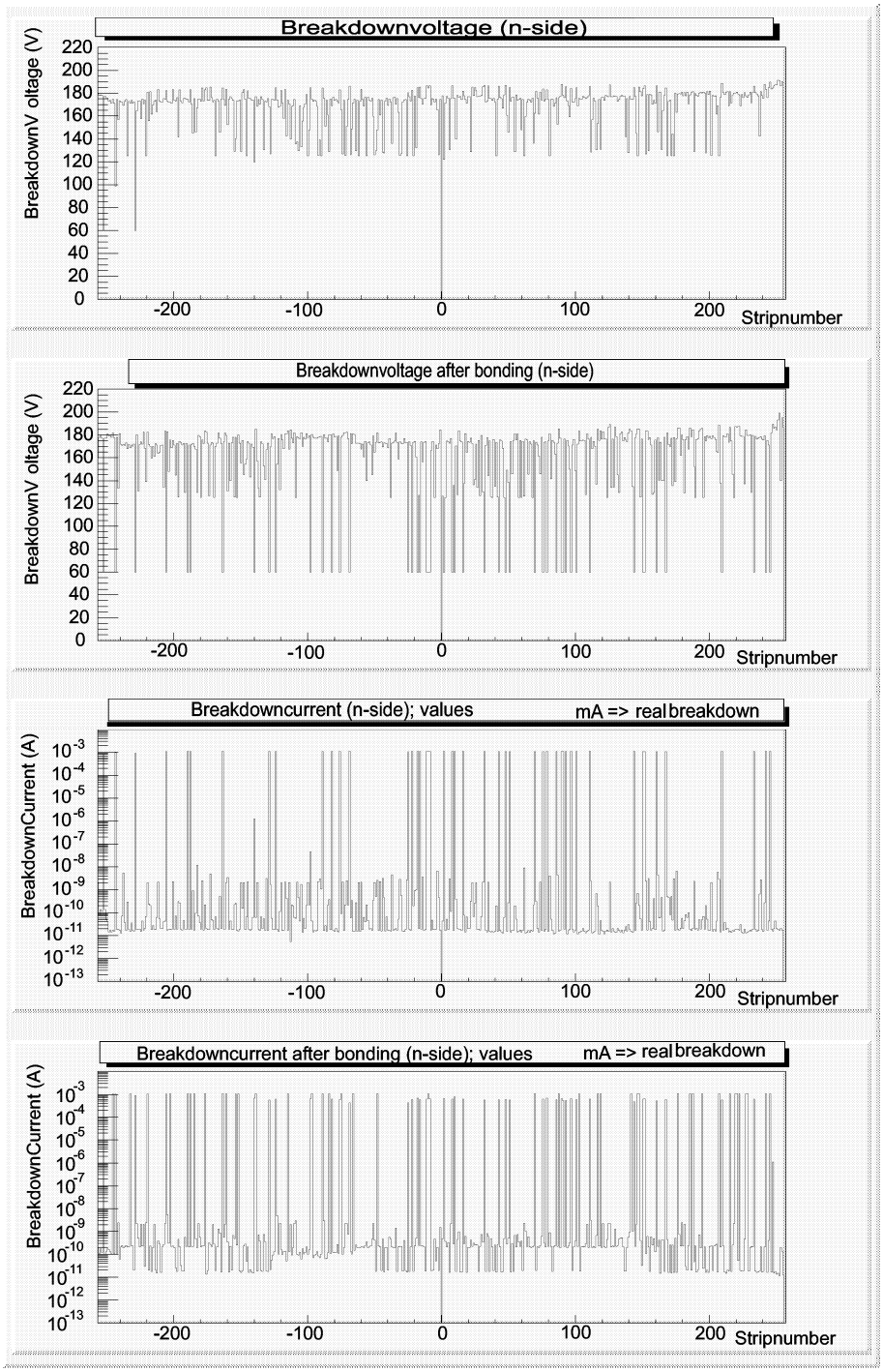


Figure 9.37: **Breakdown voltage and breakdown current, before and after bonding.**
All strips were bonded with the optimized parameters. There are almost no changes according to the breakdown voltages, only real breakdowns (pinholes) created at the initial measurement can be observed.

Chapter 10

Mechanical Mounting of Silicon Sensors

10.1 Ladders and Modules

The most crucial aspect of the construction is the exact alignment of the individual silicon sensors inside the support spaceframe. The internal alignment of a ladder has to be much better than the intrinsic hit resolution of 25 μm (see section 3.4.1). During construction and gluing we achieve this high precision with one rotating stage, holding the hybrid, and a row of 3 X-,Y-,rotating-stages, holding the sensors (Figure 10.2). The hybrid and the 3 sensors are held in position by applying a vacuum. The teflon surfaces of the vacuum chucks on top of the towers have an accuracy in planarity of ± 5 μm. The carbon fiber support is placed on a metal bridge underneath the teflon vacuum chucks, led by high precision bearings to provide good planarity. The mounting is done on a coordinate measurement machine (CMM) with a precision along the strips of about ± 1 μm. The hybrid is mounted first, rotated with respect to the carbon fiber ladder, the 3 silicon sensors are then positioned with respect *only* to the precision hole on the hybrid. The glue-laden ladder is then elevated to the sensors. The structure is released when the glue has fully settled. This procedure ensures an internal module precision only depending on the CMM precision for construction. It ensures an internal precision independent of the carbon fiber ladder. The wire bonding to connect the sensors is done after mounting, therefore the bonding areas have to be fully accessible after gluing (Figure 10.1). Finally the two ladders are glued together on a similar mounting fixture to form a module (figure 10.3). The precision is controlled by a 3D coordinate measurement machine (CMM). The complete procedure with all details is described in section 10.2.

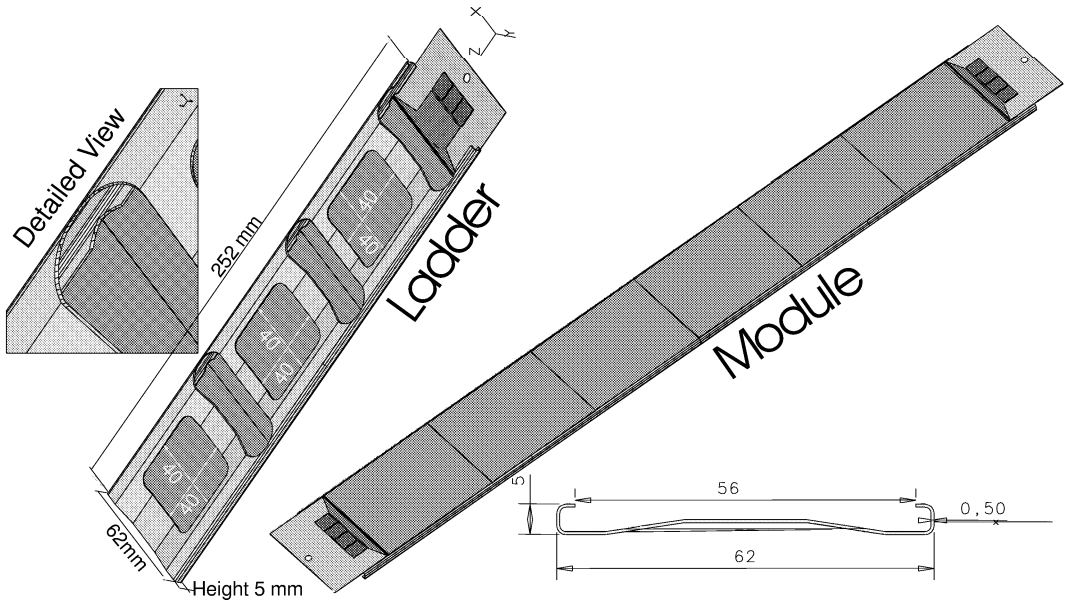


Figure 10.1: *ISL Carbon Fiber Ladder and Module Design.*
The picture shows the design of an ISL ladder and a module; the expanded view shows the cut-out designed for easy access for microbonding. On the right one sees the wedge shape, which is mainly adding to the rigidity of the carbon fiber frame.

10.2 Mounting the silicon sensors

The sensors are assembled into ladders, each consisting of three sensors. Two ladders are glued together, making a full ladder. The assembly is performed at Fermilab and Pisa, using mounting fixtures designed and constructed by the Karlsruhe group. There

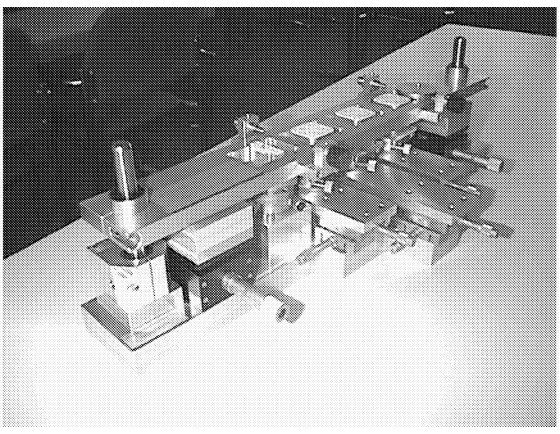


Figure 10.2: *A ladder mounting fixture.*

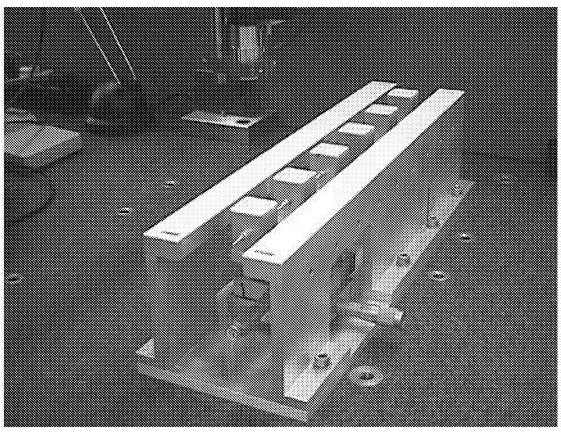


Figure 10.3: *A module mounting fixture.*

are two gluing fixtures for ladders (fig.: 10.2) at Fermilab and Pisa. The assembly takes less than two hours with a curing time of 24 hours for the glue. The bonding will take another one to two hours per side, therefore 2 ladders per side per day can be done. There is one module mounting jig (fig.: 10.3) at Fermilab and Pisa, with the same restriction of a 24 hour curing time, one module per site can be achieved per day.
The assembly procedure is outlined below. A picture of a full mounted ladder can be seen in figure 10.4.

1. Ladder frame.
   Three sensors and a hybrid are glued onto a ladder frame (see figure 10.4). The frame body is made of carbon fiber bars with Rohacel foam (see figure 10.1). Since carbon is electrically conductive, sensors are glued on Rohacel bars next to the long carbon fiber bars. This part of Rohacel bar is reinforced by having a structure of stacking Rohacel bars and carbon fiber bars.

2. Sensor alignment and mounting fixture. (see figure 10.2)
   The main parts are three stages for sensors and one smaller stage for the hybrid with teflon surface and a vacuum-chuck system. The stages can be individually positioned in X-Y (horizontal plane) and rotated. The hybrid can be rotated. In addition the jig has two sets of linear bearings at the ends, restraining a long metal plate in horizontal position. Resting on this support the ladder frame can be positioned vertically.

3. Ladder frame placement.
   The metal support is placed using linear bearings. On this support a ladder frame is positioned (temporarily) with spring-loaded pins at the four sides.

4. Hybrid placement.
   The teflon stage face is resting higher than the frame face so that sensors and hybrid can be placed without touching the frame. The hybrid is positioned about a dowel pin, with the hybrid edge aligned along the coordinate of the measurement system.

5. Measure the dowel pin position.
   Measure the position of the dowel hole made in the hybrid. The hole center is calculated from 8 measurements around the hole. The coordinate system is thus defined, and the fiducials will be positioned (see below) according to the design. The ladder frame is re-positioned at this stage.

6. Place the 1st sensor.
   The 1st sensor is placed. The r-ϕ strip side (n-side) is faced up. In all "alignment" steps there is "NO" contact to the carbon fiber ladder frame. The only position dependence is due to placing the sensors.

7. Place the 2nd sensor.
   The 2nd sensor has been placed. Like for the 1st sensor, the two fiducials along the median line are positioned. The TV monitor shows one of the fiducial and cross-hair of the measurement system. Typically precision of $\pm$ 1 μm is achievable. The 3rd sensor is similarly positioned (Figure 10.4).

8. Apply the glue.
   Epoxy glue (Hexcel 5313 with DEH24 hardener) is applied on Rohacel foam using a syringe.

9. Adjust the frame z position (height).
   The metal support with the ladder frame is lifted up by two z linear motion stages positioned underneath near the linear bearings. The sensors and hybrid are to be faced to the frame. At this stage, the sensor positions are re-adjusted to correct for any shifts during the assembly process. Wait for 24 hours until the glue is completely cured. The vacuum is released and the position of each sensor is surveyed at the four fiducials at the corners.

10. Bonding.
    Wire-bonding between the sensors and to the electronics takes typically 1.5 - 2 hours per side. The ladder frame is designed such that the head of wirebonder is not impeded.

11. Two ladders form one module.
    Two such ladders are mated on a stage (Figure 10.3 displays the fixture) and epoxied together using L-shaped carbon fiber pieces. The silicon sensors of one ladder rest fixed on one tower structure. The silicon sensors of the second ladder rest on a tower, movable in X-Y (horizontal plane) and rotatable. The design ensure total position dependence on the sensors. The carbon fiber frames have only a supporting function.

12. Set on the spaceframe.
    The ladders are placed on the spaceframe. Figure 10.5 shows the final spaceframe. Beryllium (BE) plates glued on the spaceframe to define the positions of the ladders. Aluminum (Al) cooling pipes run underneath the Be plates.

13. Insertion.
    Figure 10.6 shows the final assembly to insert the SVX II into the ISL and the complete structure into the COT.

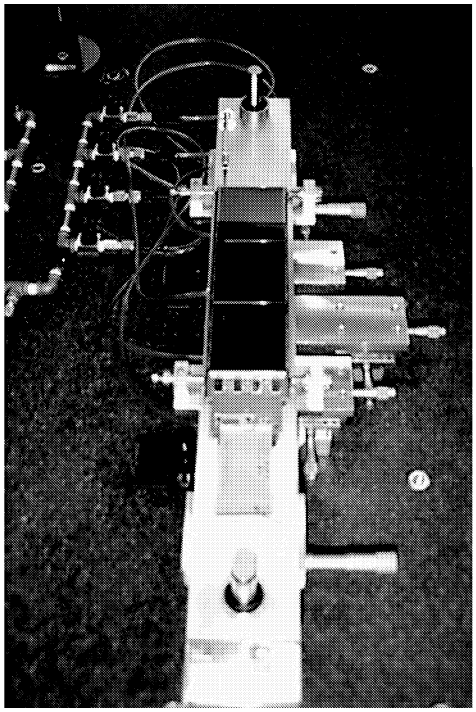


Figure 10.4: *Full mounted ladder including readout hybrid resting to cure for 24 hours. The silicon sensors are held by vacuum during the full curing time. The hybrid is held by a screw in the precision hole of the fixture which corresponds to the precision hole in the spaceframe. On the upper left side the vacuum pipes for the vacuum chucks can be seen. To reach maximum precision the whole mounting fixture rest on a coordinate measurement machine.*

10.3 Mounting the Modules in the space frame

The spaceframe was designed with respect to weight, stiffness and material budget, which led to a carbon fiber structure. Carbon fiber rings are connected with hollow carbon fiber rods. The total weight of the structure is about 6 kg before mounting the modules. Finite element analysis predicts a maximum gravitational sag of less than 30 μm in the center. We expect the structure to be even stiffer after mounting the modules, with a final precision of 50 μm over the whole length of 2 m. The internal module precision is ported to the final position precision in the spaceframe by only connecting the hybrids, not the carbon fiber ladders. The position of each silicon sensor is measured by a CMM. The final alignment precision will be achieved with tracks.

10.4 Assembly

The spaceframe was designed in Pisa, and carbon fiber parts are laminated by Monfrini S.R.L. (Italy). The gluing of single parts into the whole structure will be done in Pisa under a CMM using precision gluing masks to obtain the needed accuracy. Struts are custom-made by Reglass S.p.A. (Italy). The spaceframe is designed in such a way that it can be disassembled into 3 parts and shipped to Fermilab. The SVX II and the ISL will be assembled together on the adapted rail system, previously used to install the SVX' in Run I. We make use of one single CMM by placing one granite table on both

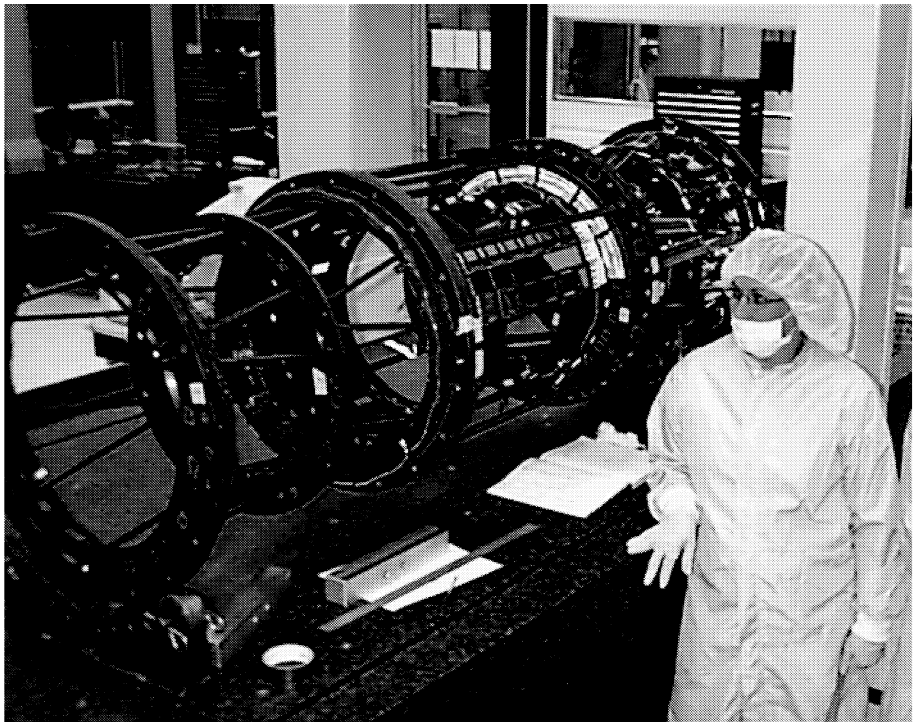


Figure 10.5: *Picture of the final carbon fiber spaceframe.*

ends. SVX II and ISL will then be placed on the rail system, resting on this set of granite tables (see Figure 10.6). We will begin to assemble the SVX II on the CMM, then move it to one side to make room for the ISL. After assembly both detectors, we will mount the SVX II in the ISL. The same rail system will also be used to insert the ISL and SVX II into the COT. All parts rest on the same rail from the beginning of assembly until final insertion into CDF II.

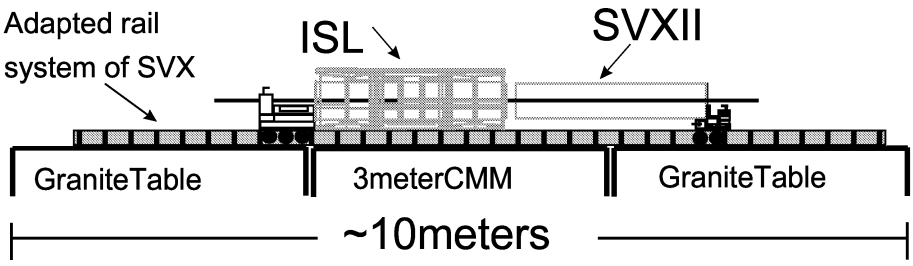


Figure 10.6: *Assembly of the SVX II and the ISL on one CMM.*
We use 3 granite tables, with a CMM on the inner one to support a rail system supporting both ISL and SVX II. Everything will be assembled on a rail system, which itself will be used to insert both detectors into the COT.

Chapter 11

Conclusion —— Outlook

A new silicon sensor technology was developed and explored for the realization of the vertex detector for CDF in the upcoming Run II in collaboration with silicon experts from CDF. The mayor step from 4" to 6" wafer size was undertaken with all advantages and all corresponding problems. CDF is the first collider experiment using a significant number of double sided silicon microstrip sensors. My main contributions were the evaluation of the silicon prototypes from the three potential suppliers; the design, manufacture and control of the mounting fixtures, including the development of the final construction scheme, the proposal of light shields for the Rasnik alignment system (working with an array of LEDs) and finally the permanent quality control of the 6" production sensors for the ISL coming from Micron. The last part included the classification of sensor defects related to failures in the production process. Several critical sensor faults were detected, for example:

- Low interstrip resistances, caused by ionic contaminants and charge up (new packaging material contained lint).
- A non-uniform depletion voltage across the sensors was detected, related to non-uniform base silicon material with respect to resistivity.
- Low coupling capacitors at the wafer edges, caused by uneven metal deposition and underetching.
- Shorts between a p-stop and an implant on the n-side, causing regions of high leakage currents on the p-side, because of field distortions.
- Increase in leakage current with the increase in humidity for some sensors.
- Differences in bias resistor values, (over-implantation or additional etching).
- Missing contacts to the implant, resulting in miss-measurement and miss-classification.

Four ladder mounting fixtures and two module fixtures were designed, built, evaluated and shipped to Pisa and Fermilab. The parameters for the wire bonding in Pisa, were tuned with the help of the breakdown voltage tests at Karlsruhe. This will improve the quality and pinhole creation will be avoided.
With a detector surface of ~ 7.5 m^2 the CDF inner tracking system will remain the largest silicon vertex detector until the realization of CMS with ~ 270 m^2 and ATLAS

at the Large Hadron Collider (LHC). Some of the lessons learned will be valuable in the development of the CMS detector at the LHC.
Vertex detectors are far more complicated to design and build than normal tracking detectors, their design must accommodate for cabling and cooling in a very tight mechanical environment. The module design has to be as simple as possible to enable automatic mounting, gluing and bonding. All wirebonds should be accessible after mounting the sensors on module frames. The switch from manual to automatic bonding should only be taken after very thorough tuning of the bonding parameters to avoid damaging the detectors at a late step in the production sequence. The switching from 4" to 6" is feasible, however the organization and calibration of the processing should be quite carefully adapted at the supplier for the larger size. Silicon base material should be carefully checked, especially with respect to sheet resistivity. Another issue is the manufacture of double sided silicon sensors in large quantities. All vendors had problem with double sided silicon with respect to technical throughput and yield problems. Layer 00, consisting of single sided sensors was the last order placed and the first order completed. A full test of pinholes, leaky strips for each sensor is mandatory. At least for every third or fourth strip to prevent sensors with large defect regions to come into the system, using double sided sensors both sides have to be tested. A WWW accessible database must be maintained, to enable every responsible person in the production sequence to have access to informations of parts at any given time [58]. In addition, the schedule has to accommodate delays, caused by missing parts.
Extrapolating from CDF ISL, CMS can expect to build 10 000 to 20 000 single sided-equivalent modules in a reasonable amount of time and on schedule with:

- single-sided silicon
- simple module design
- automation
- many fully equipped clean rooms with CMM and wirebonding facilities

The following table represent the latest schedule (12/1999):

ISL ready to accept SVXII	7/26/2000
SVX II ready to install in ISL	9/19/2000
(SVXII and ISL) are ready for installation	11/13/2000
Central detector ready for insertion	1/8/2001
CDF Ready for Collisions	3/1/2001
LHC	2005

The aim of this work to support the upgrade of the Collider Detector at Fermilab (CDF), by co-developing the Intermediate Silicon Layers Detector (ISL) and writing a substantial part of the Consumer Online Monitoring Software package, has been accomplished.

Appendix A

Cross section and event rates at hadron colliders

The important cross sections for the Tevatron and LHC are displayed in figure A.1.

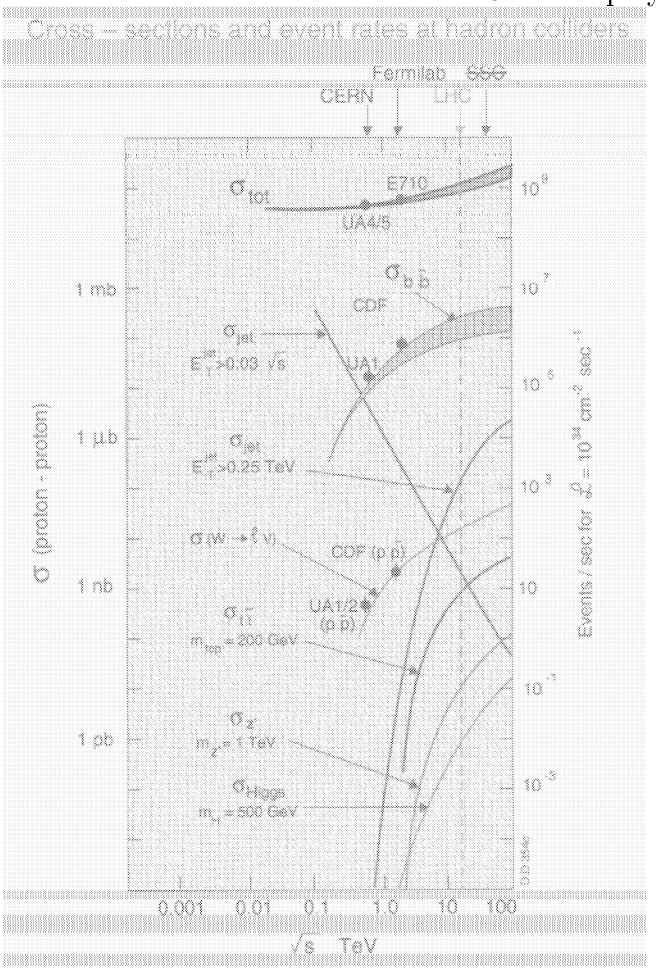


Figure A.1: **Cross section and event rates at hadron colliders.**

Appendix B

Sensor Specification

To get the best performance out of the detector, the ISL group defines the detector parameters, to suit the purpose as a very large silicon vertex tracker in the outer region. The occupancy at larger radii is smaller, therefore one could decrease the number of readout channels by increasing the strip pitch. Critical issues are fast and efficient charge collection, low leakage current, a good uniformity of $V_{depletion}$ and a small number of strip faults.

B.1 MICRON detector specification

We present the specification of the MICRON sensors which were defined by the ISL group. [22]

B.1.1 Geometrical specifications

dimension	
sensitive area:	5.926 cm x 7,4672 cm
sensor type:	double-sided, both sides AC-coupled
	n-side stereo at 1.2^o
strip pitch:	p-side: 112 μm
	n-side: 112 μm
number of strips:	p-side: 512 readout and 2 dummies
	n-side: 512 readout and 1 dummy
bonding pads:	60 μm x 200 μm
	one row of pads per strip at each end
strip dimension :	16 μm wide
thickness:	300 $\pm$ 20μm

B.1.2 Specification on electric properties

depletion voltage.	40-80 V
bulk resistivity:	$4 - 8$ $k\Omega$m
biasing scheme:	poly resistors on one end (some on edges)
passivation thickness:	SiO_2 $0.3 - 0.5$ μm
implant strip width:	18 μm
width of Al strips:	14 μm
thickness of Al strips:	> 1 μm
p-stop width (layer 2):	32 μm
p-stop implant density:	$> 1 * 10^{14} ions/cm^2$
gap between p-stops and n-strips:	10 μm
standard operation:	full depletion +15 V
	at 25 ^{o}C, relative humidity $< 50\%$
total detector current (guard excluded):	max 100 nA/cm^2
(in standard operation)	< 1 $\mu A/cm^2$ after 1 Mrad of photons (^{60}Co)
total detector current (with guard)[1]:	< 15 μA
(in standard operation)	
single strip current:	< 100 nA
(in standard operation)	
uniformity of $V_{depletion}$:	$< 20\%$ over detector area
junction breakdown:	> 150 V
micro breakdown:	> 150 V
$C_{coupling}$ capacitor breakdown[2]:	> 120 V
$C_{coupling}$ capacitor value:	> 20 pF/cm
$C_{coupling}$ capacitor leakage:	< 10 nA at 100 V
$R_{interstrip}$ (DC):	> 1 $G\Omega$
(in standard operation)	
> 100 $M\Omega$ after 1 Mrad of photons (^{60}Co)	
poly resistor value:	$4.0 - 10$ $M\Omega$ wafer to wafer
	$< 10\%$ variation on single wafer
resistivity of implant:	< 150 $k\Omega/cm$
resistivity of Al strips:	< 30 Ω/cm
total interstrip capacitance[3]:	1.0 pF/cm (< 1.2 pF/cm on ohmic side)
	variation $< 20\%$ after 1 Mrad photons (^{60}Co)
bad strips:	$< 2\%$ both sides
	$< 3\%$ for each side

Bad Strip definition: a strip is defined as bad if any of the following conditions occurs:

[1]The total detector current must remain stable ±20% over a 24 hour burn-in test.
[2]The capacitor breakdown voltage is defined as the voltage, permanently damaging the detector.
[3]defined as the capacitance of the strip to BOTH adjacent strips.

1. Strip isolation: A strip with less than 1 $G\Omega$ resistance relative to the two neighboring strips is defined as BAD.
2. Strip coupling: Any strip coupling capacitor drawing more than 10 nA at 100 V implies, that the corresponding strip is defined as BAD.
3. Single strip current: Any strip drawing more than 100 nA in standard condition is defined as BAD.

B.2 SEIKO and HAMAMATSU detector specification

We present the specification of the SEIKO and HAMAMATSU sensors which were defined by the ISL group. [21]

B.2.1 Geometrical specifications

sensor type:	double-sided, both sides AC-coupled p-side stereo at 1.207^o
bulk:	
type:	n-type
thickness:	300 ± 15 μm
flatness:	< 60 μm (any detector shall fit between two parallel plates which are separated by 375 μm)
biasing method (both sides)	poly-silicon resistors
n-side strip direction:	strips run along the long edge
p-side strip direction:	strips run at 1.207^o with respect to the n-strip
n-side isolation method:	p+ stop channel surrounding n-strip
passivation:	thickness: $0.5 \sim 1.0$ μm
p-stop implant density:	$\geq 1 * 10^{14}$ borons/cm^2
implant+diffusion depth:	~ 1 (1.5 preferable) μm for p and n-strips, and p+ stop
dead channels, p and n-side each:	$< 2\%$ dead channels per detector and $< 3\%$ per side
dimension	
sensitive area:	5.723 cm x 6.750 cm
outer size:	5.926 cm x 6.902 cm
number of strips:	p-side: 512 readout and 1+13 dummy n-side: 512 readout and 1+1 dummy
strip pitch:	p-side: 112 μm n-side: 112 μm
implant strip width:	p-side: 22 μm n-side: 22 μm
Al electrode, n and p-sides:	16 μm
bonding pads:	60 x 200 μm one row of pads per strip at each end

B.2.2 Specification on electric properties

initial full depletion voltage (V_F):	$40\ V\ < V_F < V_F^{max}$ with $V_F^{max} < 80\ V$ **after initial prototype testing**[4] $V_F^{max} < 100\ V$ no strange behavior for $V > V_F^{max} + 50\ V$. including $I_{strip} < 100\ nA$ (breakdown)
initial leakage current: (bulk, surface and edge contribution):	$< 100\ nA/cm^2, 50\ nA/cm^2$ typical $=2\ \mu A$/detector **changed** to $4\ \mu A$/detector **after initial prototype testing**[5] at $Vb = V_F^{max} + 10\ V$ and $T = 20 - 25\ C^o$
junction breakdown[6] with open readout electrodes:	$> V_F^{max} + 100\ V$
dark current slope (dI/dV) in $[nA/cm^2/V]$:	$dI/dV < 0.2$ at Vb from V_F to $V_F^{max} + 80\ V$ ($Vb = 2\ V_o$ when p and n sides are $\pm V_o$)[7]
breakdown voltage of coupling capacitor n-/p-side:	$> 100\ V$ (200 V typical)
interstrip resistance:	$> 2\ G\Omega$
poly-silicon resistor value mean value: variation within one detector:	$4\ \pm 1.5 M\Omega$ $\pm 10\%$
resistance of Al electrode, n-/p-side:	$< 20\ \Omega/cm$
capacitance of coupling capacitor, n-/p-side:	$> 14\ pF/cm$ / 20 pF/cm typical)
interstrip capacitance (full length)[8] p-side: n-side:	$< 10\ pF$ $< 12\ pF$ (10 pF typical)

[4]refer chapter 7.2: Evaluation of the HPK prototypes.
[5]refer chapter 7.3: Evaluation of the Seiko prototypes.
[6]junction breakdown voltage is defined as $I_{break} > 10\ I_{leak}(V_F + 10\ V)$
[7]p and n side balanced bias, both side readout electrodes grounded.
[8]the interstrip capacitance is measured at Vb of 1.2 V_F with both neighbour strips

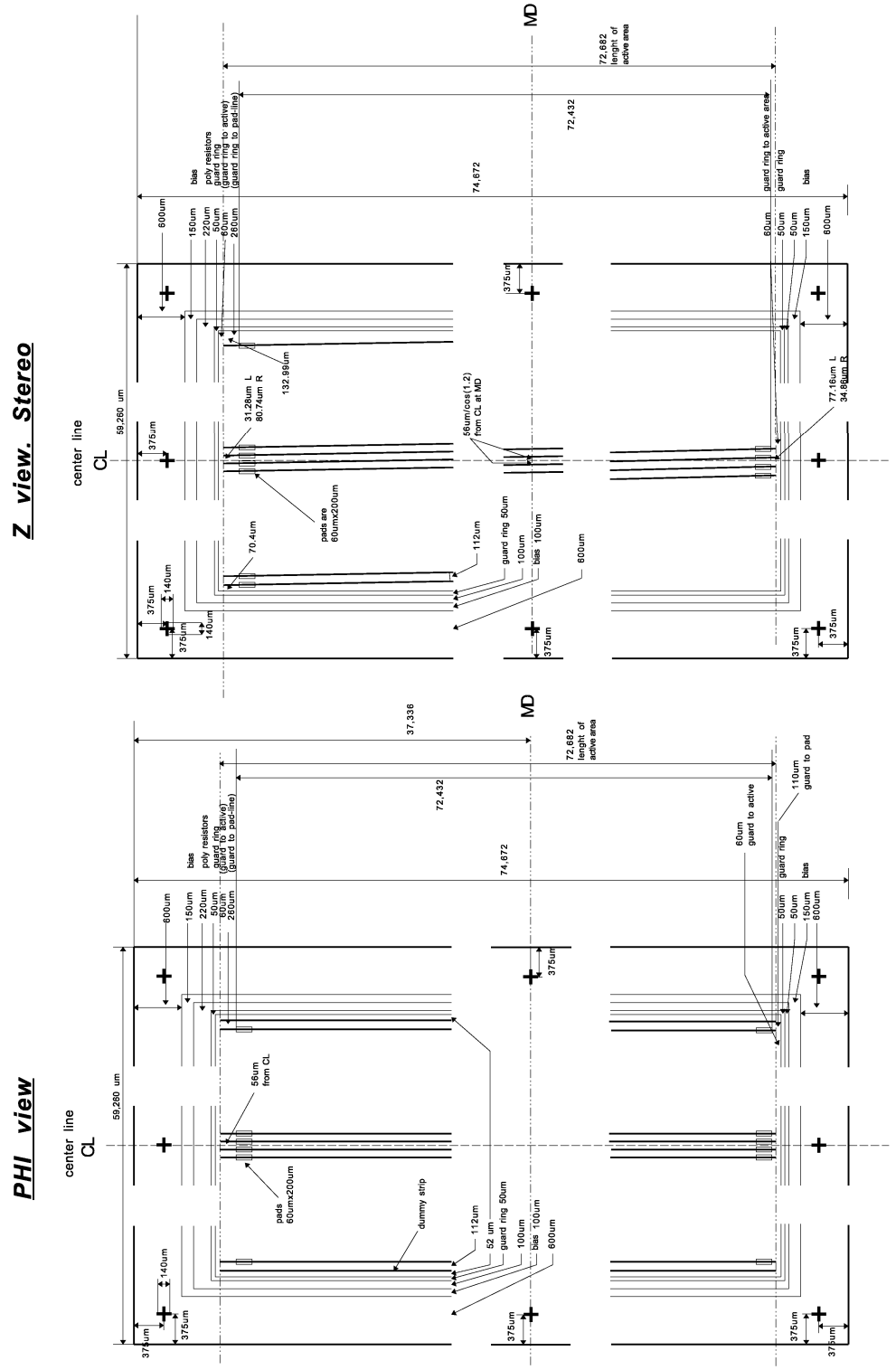


Figure B.1: **Geometrical layout of a Micron sensor.** *ϕ- and z-side (stereo) are displayed. Strip numbering starts at -257 up to 256 skipping 0; center-zero lies in the middle between strip -1 and 1. Since the strip counting starts from the leftmost strip on both sides, strip -256 one p-side corresponds to 256 on the n-side and strip -1 corresponds to 1. The definition of zero at the center in the masks eliminated shifts to the right or left side of the sensor.*

Appendix C

Software for the Quality Control

All online programs of the quality control are done in Labview graphical programming language, which is perfectly suited for instrumentation and measurement. One single virtual instrument[1] controls all measurements and instruments; the motor controller and some relays; it calculates, displays and analyses the data.

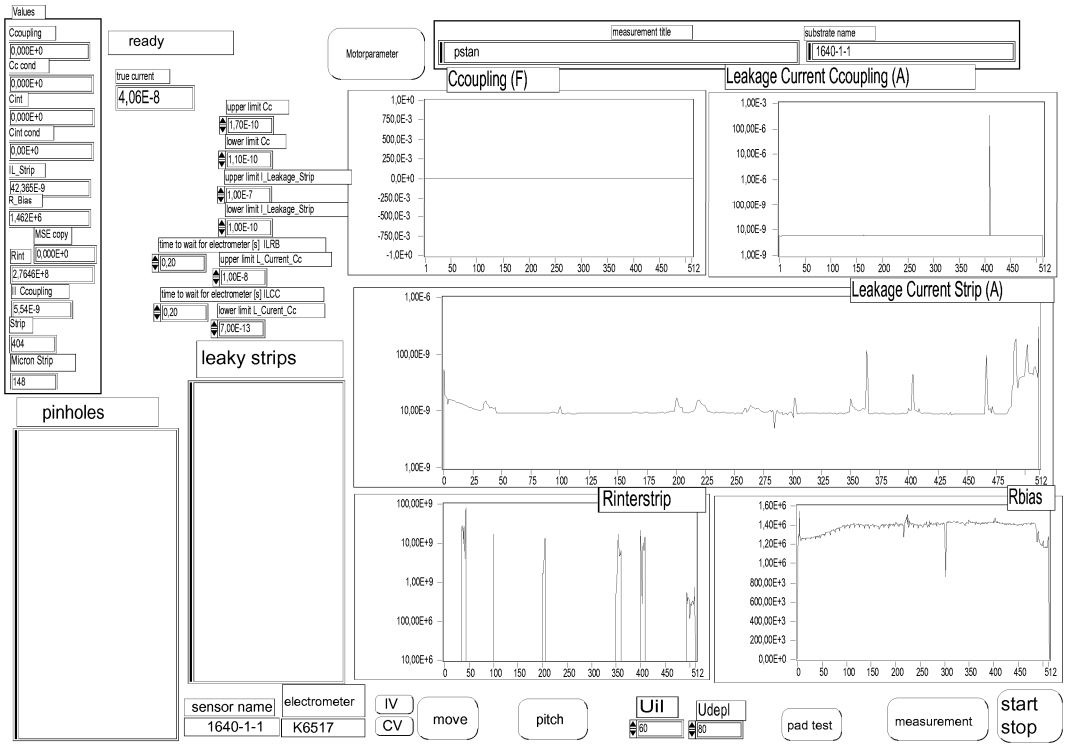


Figure C.1: **Graphical interface of the quality control software.**
Main virtual instrument to measure the standard parameters.

[1]We speak here of virtual instrument instead of program. On can refer to the program as a single "virtual" measurement instrument.

On the lower part of figure C.1 you see the measurement sequence:

1. Mount sensor on the fixture and place needles on bias rings on both sides.
2. Specify sensor name.
   It will appear in all saved files and screen pictures.
3. Measure total leakage current and capacitance.
4. Align sensor:
   First and last DC pad position is used to define pitch and direction.
5. Calculate pitch:
   The program compares spec with obtained value; to avoid bad alignment.
6. Specify pinhole probing voltage and $V_{depletion}$.
7. Align needle and test needle contact: Pad test.
   (a) Place probes on the pads.
   (b) Do single steps with light[2] on and re-adjust probes if needed.
8. Choose one or more measurements.
   Changing of measurement cabling will be done by a matrix of relays.

Table C.1: Quality control – how to minimize testing time.

Emphasis was taken on evaluating sensors online. This enables us to immediately compare our results with the Micron measurements, bad probe contacts can be remeasured directly. Pinholes and leaky strips are flagged on the fly. Thresholds for flagging and lower thresholds for remeasuring can be adapted during measurement. Subprograms are responsible for measuring total leakage current and total capacitance. All windows can be adjusted to show only different regions of the sensor and y-scaling is possible too. This enables the testing person to investigate single strips or some regions closer.
Measuring one side of a sensor takes about two hours[3], this totals in four hours for one detector plus time evaluating the data with a ROOT macro and publishing the data on the web. Sometimes we like to transfer results immediately. The graphical windows is printable into a postscript file, hence fast distribution of all data and plots needed for evaluation is possible.

[2]No voltage supply.
[3]including mounting of the sensors

Appendix D

Rasnik system without light shields

The "Relative Alignment System of NIKhef" (Rasnik) was first installed in the CHORUS [33] experiment. It was used in the fiber tracking system which is not effected by infrared light, on the contrary to a silicon tracking system.
To keep the system as light, with the least amount of material as possible, the first design did not foresee any light shielding. We did some calculations and measurements about the influence of the Rasnik system on surrounding silicon sensors, because silicon is quite sensitive to infrared light. Wavelengths up to 1107 nm [1] are affecting the silicon.

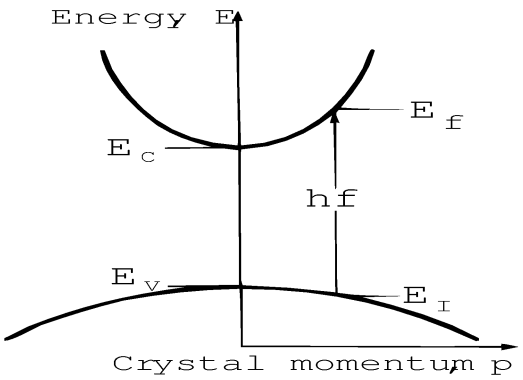


Figure D.1: **Direct band-gap crossing.**
Absorption of a photon by excitation of an electron from the valence to the conduction band.
Energy and momentum is conserved by a single photon.

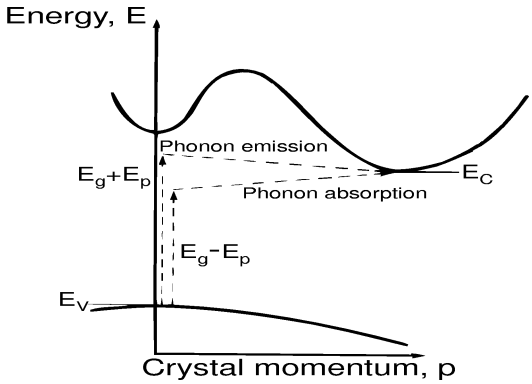


Figure D.2: **Indirect band-gap crossing.**
Absorption of photons by a two step process, involving phonon emission or absorption.
Phonon is needed to conserve momentum.

[1] 1107 nm corresponds to the bandgap energy of 1.12 eV

Calculations

In an optical absorption, the direct absorption process (figure D.1), a photon is absorbed by the crystal with the creation of an electron and a hole. In silicon this happens at 3.62 eV, which is significantly higher than the bandgap energy of 1.12 eV. In an indirect absorption process (figure D.2) the minimum energy of the band structure involves electron and holes separated by a substantial waveband vector k_C. Here a direct photon transition at the energy of the minimum gap cannot satisfy the requirement of conservation of wavevector, because photon wavevectors are negligible in comparison with k_C at the energy range ($\sim$ 1 eV) of interest. But if a phonon with wavevector K and frequency ν is created in the process, then we can have:

$$k(photon) = k_C + K \cong 0, \qquad \hbar\omega = E_g + h\nu, \tag{D.1}$$

as required by the conservation law. The phonon energies $h\nu$ will generally be much less than E_g, characteristically ~ 0.01 to $0.03\ eV$.
This leads to the fact, that photons $\geq\ E_g$ are able to generate electron hole pairs with the help of phonons, generated earlier by photons. The total absorbed energy is still 3.62 eV. Another factor, which must be taken into account is the transparency of silicon for photons with different energies. The absorption coefficients for different wavelengths are illustrated in figure D.3, they are correlated by

$$E = \hbar\nu = \frac{\hbar c}{\lambda} \longrightarrow \lambda_{MAX} = \frac{\hbar c}{E_G} \tag{D.2}$$

to the photon energies. Calculating the intensity remaining in the silicon wafer with

$$I(x) = I(x_0)\exp -\alpha(x - x_0) \tag{D.3}$$

and

$$\frac{I_0 - I(x)}{I_0} = \frac{I_0 - I(300\ \mu m)}{I_0} = \frac{I_0(1 - \begin{array}{c}3.7e-11\\3.05e-7\end{array})}{I_0} = 1 \tag{D.4}$$

leads to an absorption factor of 1 at a 300 μm thick silicon wafer, for the given energies of the proposed diodes. Therefore no light can penetrate through the sensors, only the surrounding material is affected.
Knowing the energy needed to generate an electron hole pair we can with the different powers of the infrared diodes and

$$nE_0 = Pt \longrightarrow n = \frac{Pt}{E_0} \tag{D.5}$$

calculate how many electrons the expect in the sensor. Finally these calculations lead to table D.1. To know the resulting impact on individual strips the incident angle (divide 300 μm by $sin(\Theta)$ for other angles) and the distance ($P \times \frac{1}{r^2}$) from diode to strip have to be taken into account. Remember all values correspond to 1 LED (the RASNIK system uses an array of 9 LEDs).

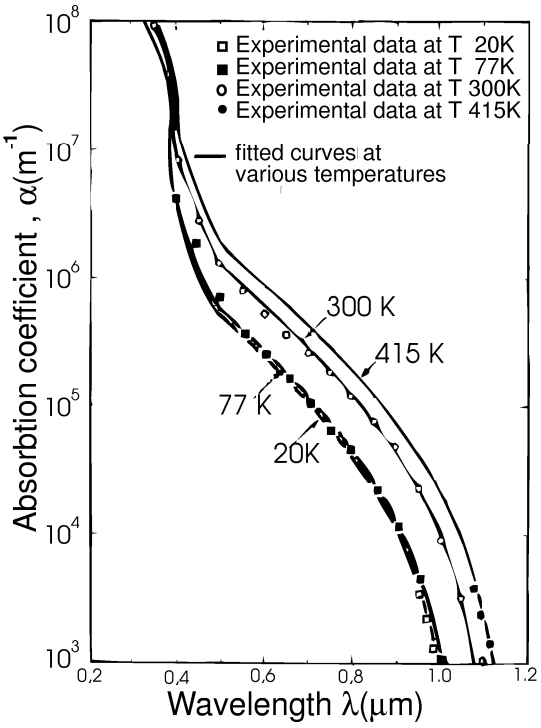


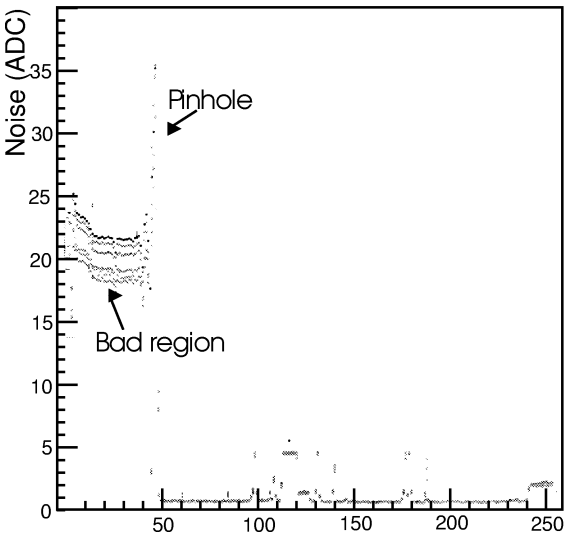
Figure D.3: **Absorption coefficient of silicon as a function of wavelength of light at different temperatures.** *[13]*
The two proposed diodes have absorption coefficients α of 8e4 and 5e4 m^{-1} at λ = 880 and 940 nm respectively at room temperature.

	energy [eV]	λ [nm]	absorption coefficient α [1/m] Si (approx)	power [mW]	photons per 100 ns [x 10^9]
Eg (300 K) indirect bandgap crossing	1.12	1107	1e3		
direct band gap crossing	3.62	344	1e9		
LED type 1	1.41	880	8e4		
				24	10.62
				12	5.31
				9	3.98
				0.24	0.1
LED type 2	1.32	940	5e4		
				8	3.78
				1.5	0.7
				0.075	0.035
				0.015	0.007

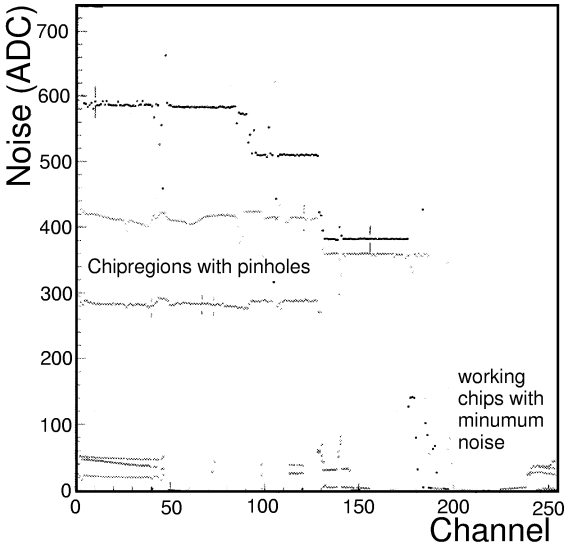
Table D.1: *The corresponding absorption coefficient α were displayed for direct, indirect bandgap energies and for different proposed LEDs for the Rasnik system. The last column shows the number of photon emitted for different powers of the LEDs. The time interval of 100 ns corresponds to the integration time of the SVX3 chip.*

Measurements

The huge increase in noise, displayed in figure D.4 and D.5 show the necessity of light shields in the system. Even readout during duty cycles would effect the readout, since the total leakage currents (figure D.6) are increasing enormously, a permanent defect is very likely to happen. The components of the tracking system are very densely packed. Therefore the next components will be at most 2.5 cm away, the plots prove that even the next devices at larger distances are highly affected.



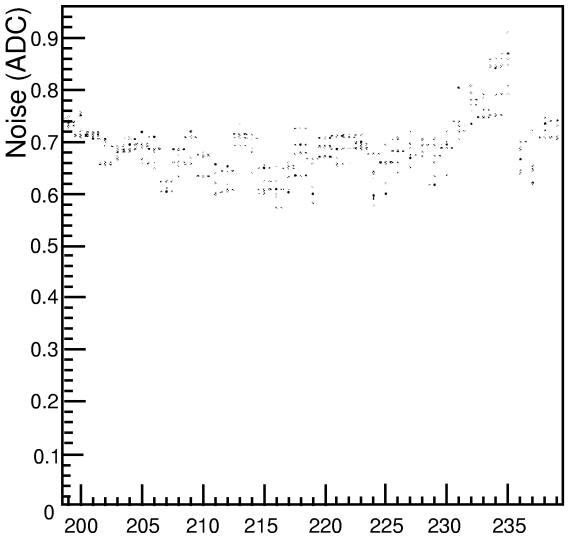
A.) Strip noise with diodes ON but light shields applied. This displays the average noise level of the sensor. Noisy strips (120-140)are much more affected by the light than average strips. See right.



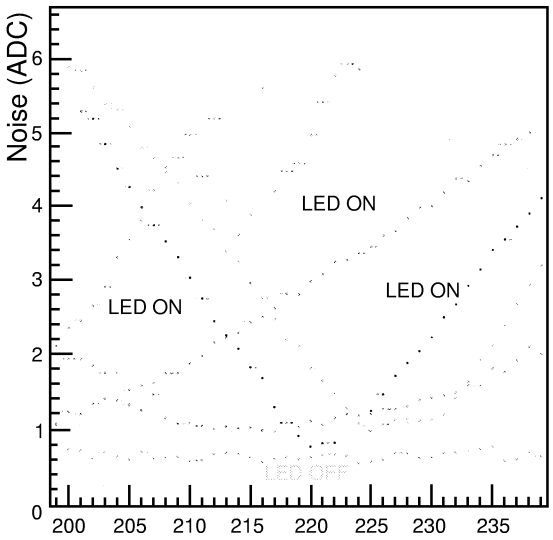
B.) Strip noise with diodes of different power (ON). The different diodes are held in a distance of $\sim$ 5 cm over the sensor. Obviously single defect strips are affecting large regions.

Figure D.4: *The average impact on nominal strips, which can be seen in figure D.5, is quantitatively small compared to the effect on defect strips. Large regions of the detector are completely out of scope. The different lines stand for the different diodes shown in table D.1. Different distances are additionally changing the baseline of all different data points.*

The studies led to the conclusion, that shielding is absolutely necessary for all types of proposed diodes. The arguments and measurements hold for all usable types of diodes, since the CCDs –needed to read out the infrared light– are made out of silicon, too. Using the Rasnik system is only possible while using 100% perfect light shielding.



A.) There is a light shield between sensors and LED array, the diodes are shining in the opposite direction. Since one of the lines was measured with all diodes OFF, these lines corresponds to the base noise level of the sensor.



B.) The LED array is shining directly from a distance of $\sim$ 2.5 cm onto the sensors, the slopes are due to the different positions of the different diodes over the detector.

Figure D.5: *This is an expanded view of channel 200 to 240 of figure D.4*

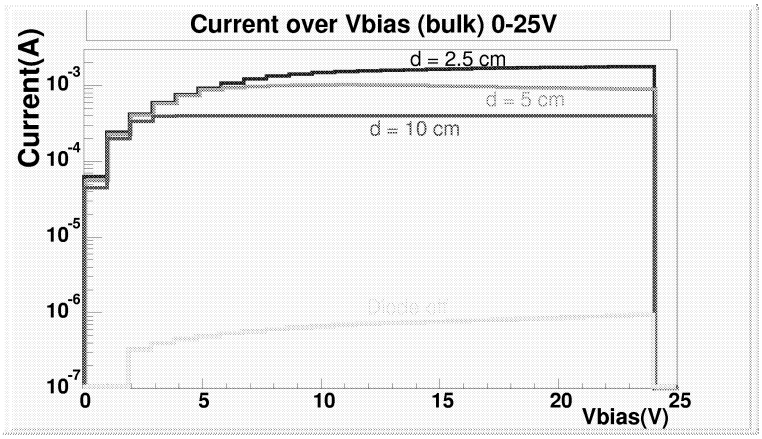


Figure D.6: **Total leakage current with infrared LEDs at different distances.** *This test test was done for all proposed diodes with the same result. This plot shows leakage currents induced by a 880 nm diode with a power of 9 mW. The detector depletes around 15 V.*

Appendix E

Data Acquisition – Consumer Online Monitor Server

CDF will start Run II with a significantly different detector, trigger system, data format and software environment. Therefore, the programs which served to monitor the data stream (YMON, LUMON, TRIGMON, etc.) during Run I have to be rewritten. For this purpose we are realizing a framework based on the ROOT package. Part of this project was realized during my time as a Ph.D. student. We concentrated mainly on the server and the Displayclient –a full functional GUI[1]. The whole sequence

1. Producing the items, e.g. histograms, tables, canvases
2. Writing to shared memory
3. Reading from shared memory
4. Sending everything via a socket connection
5. Receiving and displaying the information

was tested and realized. The project is still ongoing, but the main parts and many details are already realized. The schemes are illustrated in figures E.1 and E.2.

E.1 Why do we want to use ROOT?

Root has been developed with high energy physics in mind. It provides a complete framework and can be regarded as a C++ replacement for PAW, Cernlibs, ZEBRA and more. What makes ROOT so interesting for online monitoring purposes is the fact that classes dealing with shared memory, socket connections etc. are provided together with examples explaining how to use them. The shared memory is implemented for different architectures. So far, we worked only in the Linux/Unix environment. The ROOT

[1]GUI: **G**raphical **U**ser **I**nterface

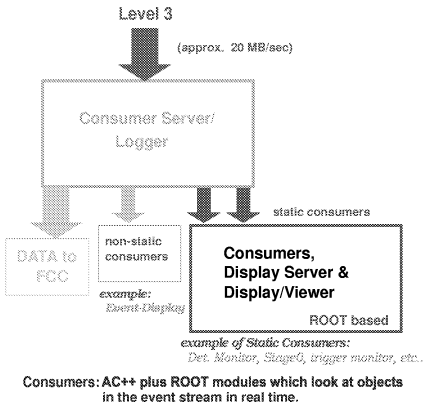


Figure E.1: *Data from Level 3 to the Consumer and Display.*

TMapFile class utilizes the UNIX mmap system call. The classes know about ROOT objects so you can send histograms or root trees with a single command. Creating a data driven client server architecture is relatively easy with ROOT. Some other experiments in high energy physics have already done it and we can build on their experience. Overall the root user community is growing and whenever one has a problem one can just post it to the root mailing list and usually within hours or a day one gets an answer. The root team was really responsive to questions and suggestions. Since the source code is available it is possible to change it to suit your application and to feed back the code to the root team. Other aspects interesting for online purposes are the fact that a rootd daemon is provided which allows to send root objects over the net. There is also a plugin for the Apache webserver which makes the server root aware and allows to access root files via a web browser like netscape. We have tested all this components and found them to work well and easy to use. The CINT interpreter and its debugging capabilities allow fast prototyping to some extend. One just has to be aware of the fact that the interpreter has its limitations and allows a few things which a C++ compiler doesn't allow. But in principle it is not difficult to write programs which can be used as a root macro and can also be compiled to form stand alone programs.

E.2 Consumers in CDF II

Consumer Interactions with Databases (DB) The consumer processes monitoring the data stream will have frequent interactions with the database. It is possible that many of the consumers will write their results to the database. Some examples of consumers and possible read and write access to the database are (using their Run I names):

- Calibration : Monitors datastream during calibration run.
  Writes to the Calibration DB.

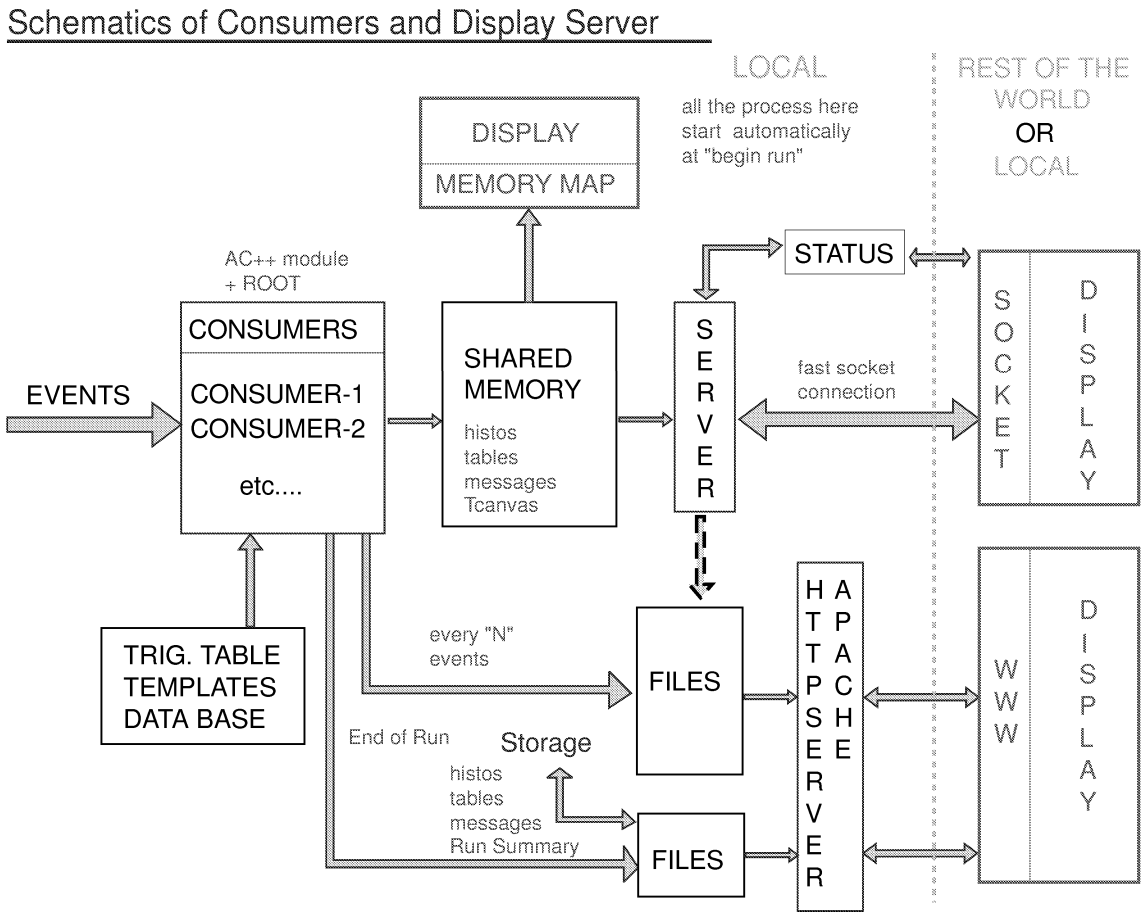


Figure E.2: *Consumer, Display Server, the Internet and Display Client.*

- YMON : Monitors detector response.
  Reads the database for online calibrations and histograms (templates of valid detector response). Writes histograms and results to the Run Conditions DB.

- TRIGMON : Monitors trigger performance.
  Reads the Trigger Table and Calibration DB (trigger calibrations to simulate the trigger). Writes results to the Run Conditions DB.

- LUMMON : Monitors luminosities and cross sections per trigger.

- PHYSMON : Monitors physics plots.
  Reads the database for online calibrations and histograms (templates of valid physics plots). Writes plots and results to the Run Conditions DB.

- Event Display : Displays of events during run.

- SVX: Monitors the occupancies of the silison tracking system (see example in figure E.6).
- Other monitors like SPY (Level 3 physics), Beam, Luminosity, etc.
  Reads the database for calibrations. Writes plots and results to either CDF Conditions or Run Conditions DB.

The consumers will need to access the calibration DB "Used Sets" of calibrations actually used for the online hardware, and for level 3 (possibly different "Used Sets"), but will not need to create their own "Used Sets" of calibrations.

E.3 Display Server

The Display Server (figure E.3) is a ROOT based program that allows the display/viewers programs (Display Clients) to connect to it as a client and to access the information in the shared memory in real time. Since the Display Server needs access to shared memory it has to run on the same machine as the consumers. One server program is able to handle more than one consumer. Each consumer is writing its data to one shared memory area, which can be accessed by all sub-processes of the server program. Multiple display/viewer programs can connect from anywhere in the world without having any effect on the consumer itself. The server will handle the requests (of course the processes which are looked at by a shift crew will be given the priority). To handle many display/viewer programs at once, the server spawns a new child process to handle all requests. In reality it spawns a child- and a grandchild-process to decouple dependencies between main server and sub-processes. This cancels the need to permanently send information between the processes to control aliveness of the child and parent process. An improved command fork2() is used instead of Unix command fork(). With fork2() the new process is immediately orphaned (it won't leave a zombie when it exits). It returns 1 to the parent, not any meaningful process ID (pid). Therefore the parent cannot wait()[2] for the new process (it's unrelated). This enables the display/viewer programs to shut down the child processes without creating "zombie"[3] processes. These sub-process are then independently and individually handling the shared memory reading and the socket connections. Furthermore the server is capable of parsing a status webpage with all informations of the different consumers. This includes location (IP number), shared memory file, run number,process events, event number and status. According to the given informations and a status change request via a socket connection the server will change the information and write a new HTML webpage and copies it via secure copy onto the corresponding webserver. An miniature

[2]fork() and wait() are basic Unix commands, handling multiprocess environment.

[3]Zombies are processes still having a process ID without doing anything, but can not easily be dispatched. In addition there is a limit on the number of processes each user can run, which is smaller than the system's limit. With many clients disconnecting this number will run out fast.

example of such a status page is given in figure E.5. In the future this feature will be moved into a individual observer program (the Watchdog see figure E.4).

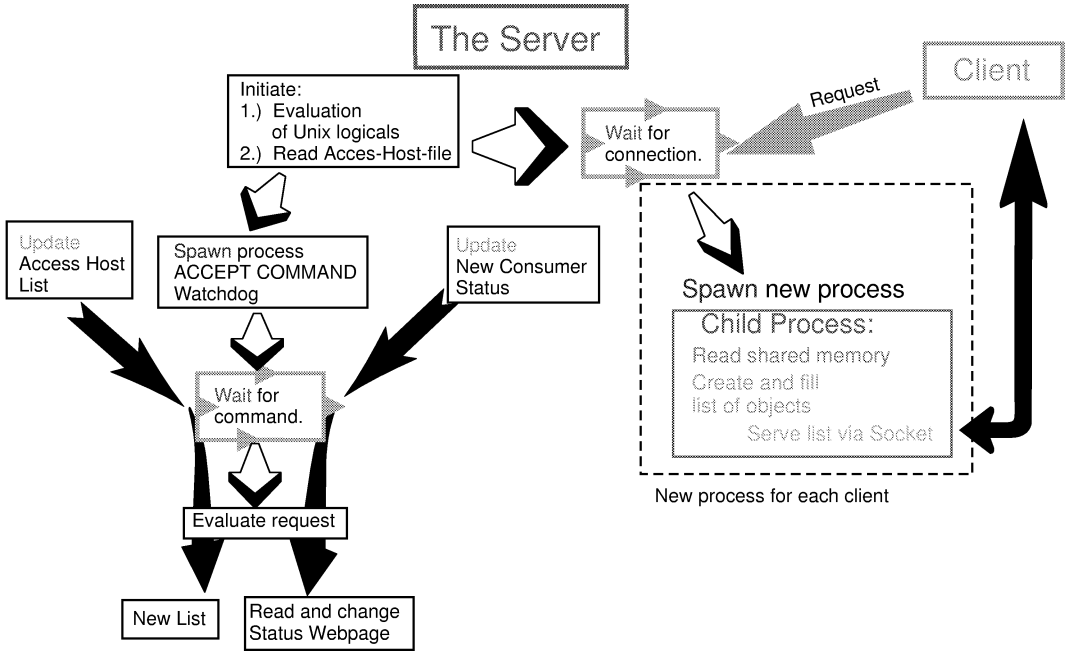


Figure E.3: **Scheme of the Server program and its functionality.**

E.4 Displayclient

The display is a ROOT based program that can run on the same or on a different machine with various ways to connect:

- Access shared memory directly when running on the same machine.
  This option is planned to be used for debugging purposes only.
- Connect to the Display Server via a socket connection.
  This should be the default way to access the information. Preferably from a remote machine so that all the CPU-load associated with displaying graphics is transferred to the remote machine.
- Connect via the world wide web.
  A plugin for the Apache webserver exists, which makes the server root aware and allows to access root files via a web browser like netscape.
- Access data via the the rootd demon which can serve root file via the net.

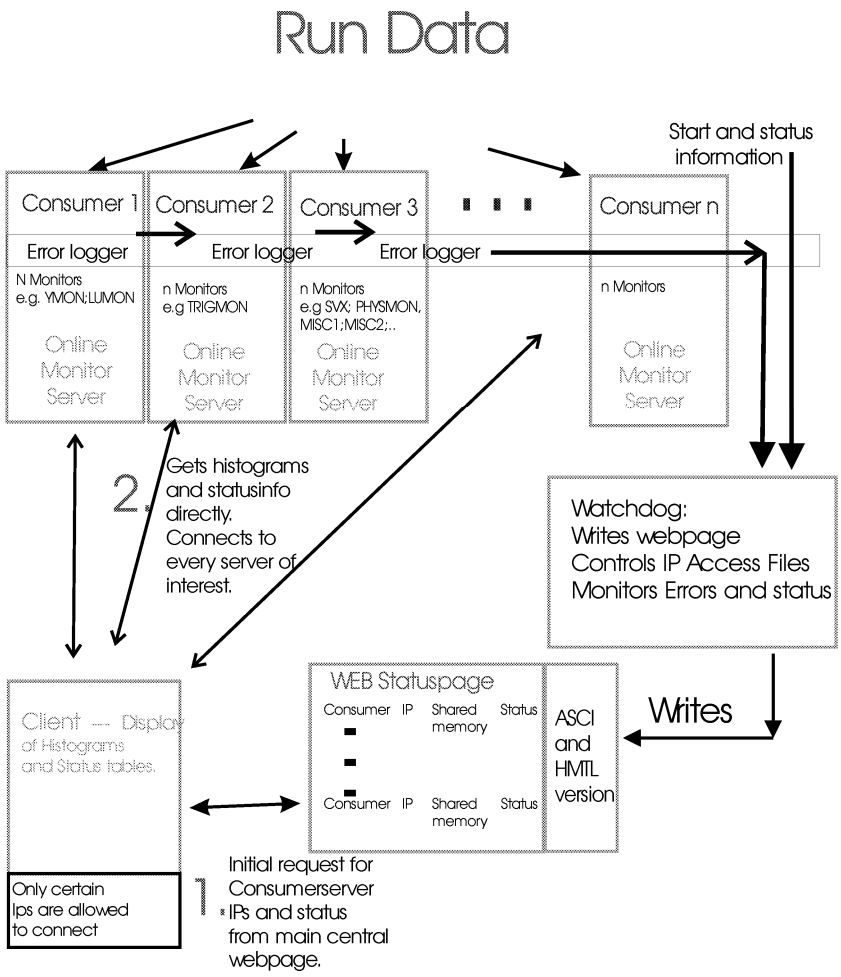


Figure E.4: *Connection of a Display Client to the needed Display Server.*

Through the socket connections, we can access the monitoring results in real time (see the entries of a histogram grow). Through the web, we access the root files which is closed. We definitely close the files at the end of each run. But we could also think of closing the files occasionally during a run, so that we can see relatively up-to-date monitored results via WWW.

With this scheme we realize the idea of relieving one computer to do all tasks, since the display is transferred to a remote machine. Serving many clients is only possible, because we are sending only small objects via the net. The whole scheme would be impossible with the transfer of graphical objects. The realization of graphical display on the remote machine makes it possible to adjust views and amount and type of data displayed to the need of the user. Realizing all this with the traditional 'round command

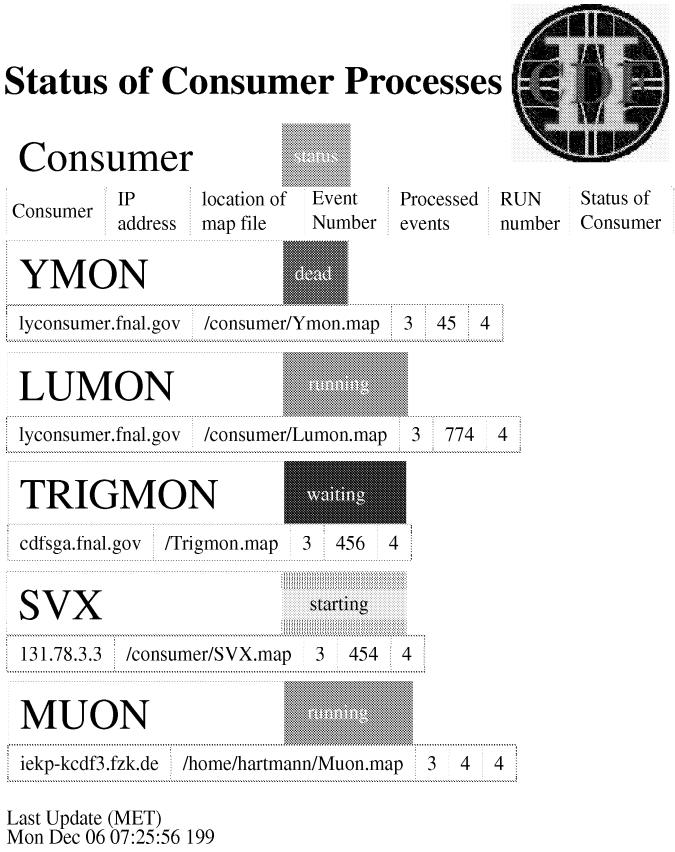


Figure E.5: **Example of a Consumer Status Webpage.**

scheme' would completely swamp the system, and therefore be impossible.

E.5 Future implementations

Several additional implementations are planed for the future:

- The display/viewer programs receive only parts (requested) data. To reduce network traffic and avoidance of useless data travel. The status webpage will tell the Display Client the available information. The user can mark the needed information via checkboxes.
- Priority checking for different Display Clients. The client is able to request a continuous update of the data or just a request-on-button. The shift crew will naturally continuously monitor the data, while a desk computer somewhere should not be able to continuously request for data.

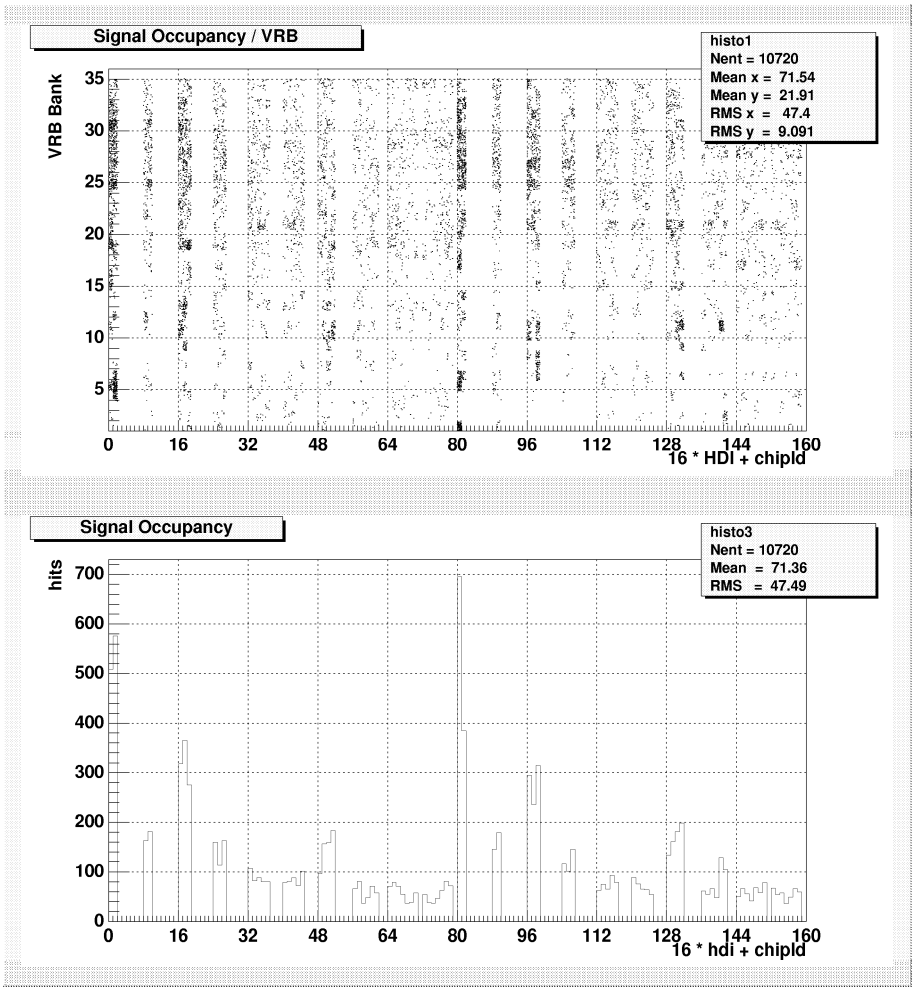


Figure E.6: *Example of the SVX Consumer Monitor output [60].*
The occupancies of the individual chips of the silicon system are shown. The plots are showing Monte Carlo data. The Online Monitor Software package allows all collaboration members to online observe changes or notice 'dead' chips. HDI stands for 'High Density Interconnect', the connection between hybrid and the DAQ.

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