

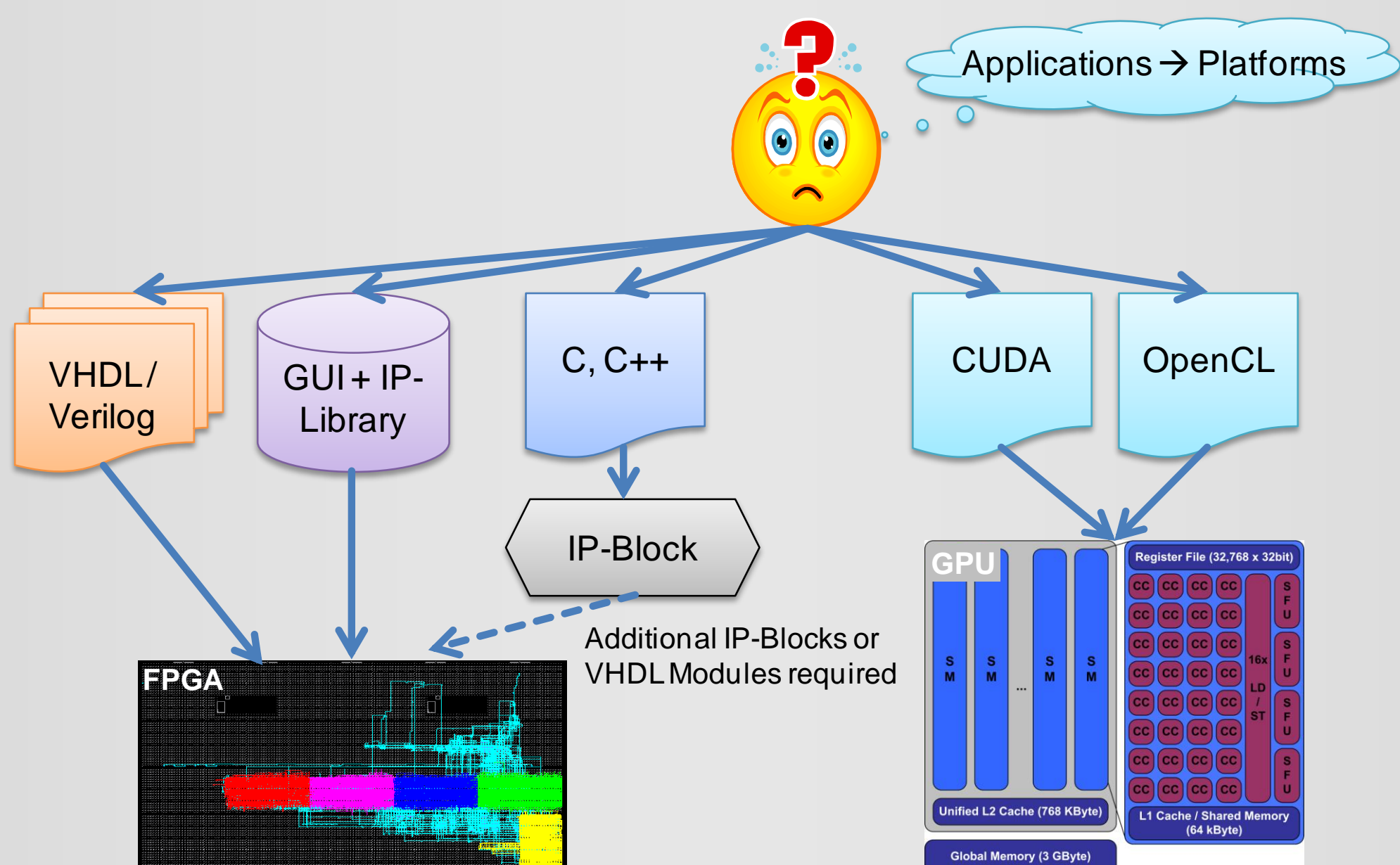
High-Level Design for FPGA-based Multiprocessor Accelerators

Diana Göhringer¹, Matthias Birk², Michael Hübner², Jürgen Becker²

¹Fraunhofer-Institute for Optronics, System Technologies and Image Exploitation IOSB, Germany
²Karlsruhe Institute of Technology (KIT), Germany,
diana.goehring@iosb.fraunhofer.de, {matthias.birk, michael.huebner, becker}@kit.edu

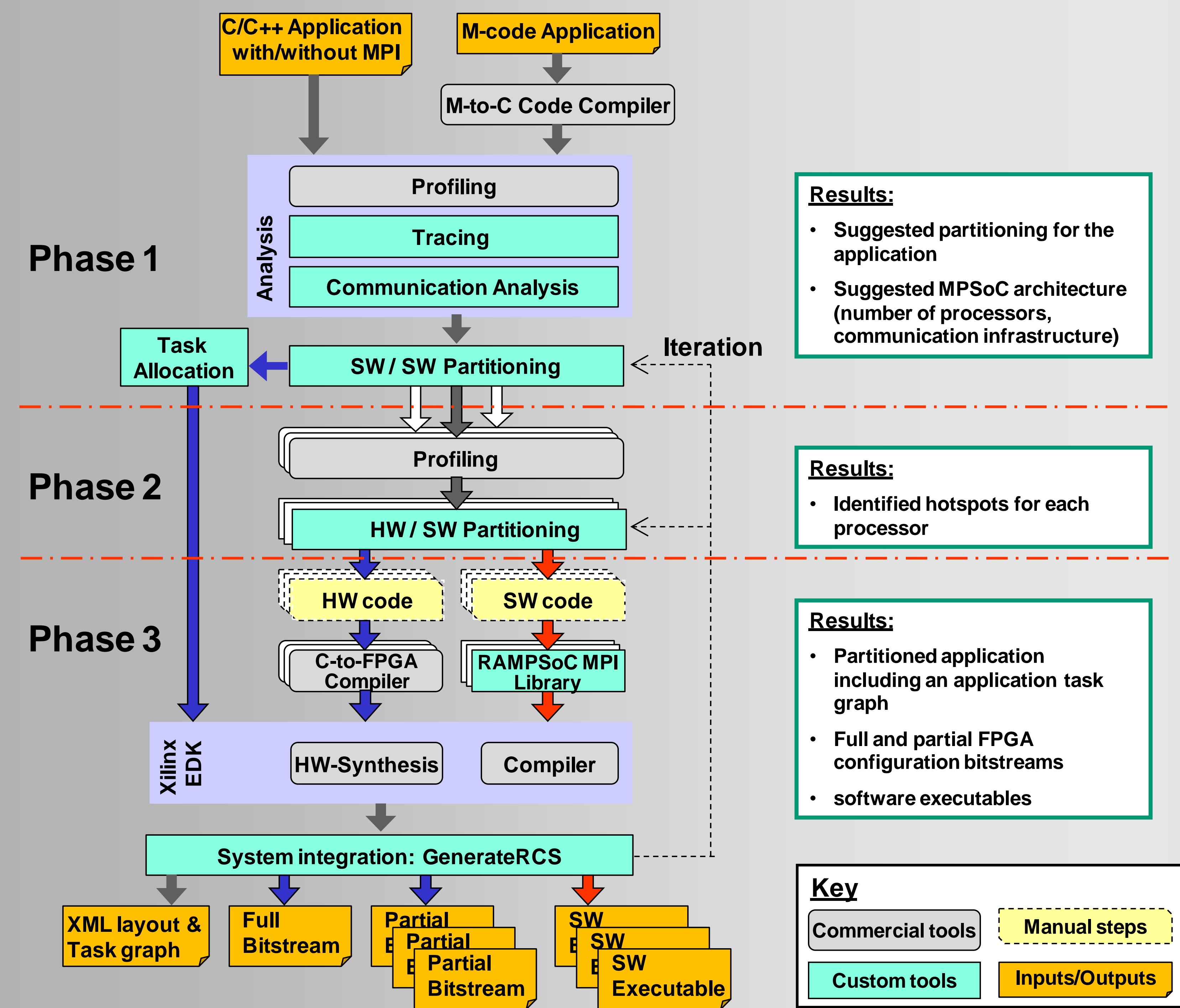
1. Introduction: FPGA versus GPU Programming

Application Description	Advantages	Disadvantages
VHDL, Verilog	Optimized Designs, Full control over the design	Low level, Difficult to debug, seldom used by application engineers
Graphical Tools (e.g. MATLAB HDL-Coder, System Generator)	High level, Easy to use: Drag and Drop	Restricted to a specific IP library
C, C++ (e.g. CatapultC, Autopilot)	Fast design space exploration, automatic generation of IP-blocks	Special C, C++ coding style required for good results, generates only IP blocks not full FPGA designs

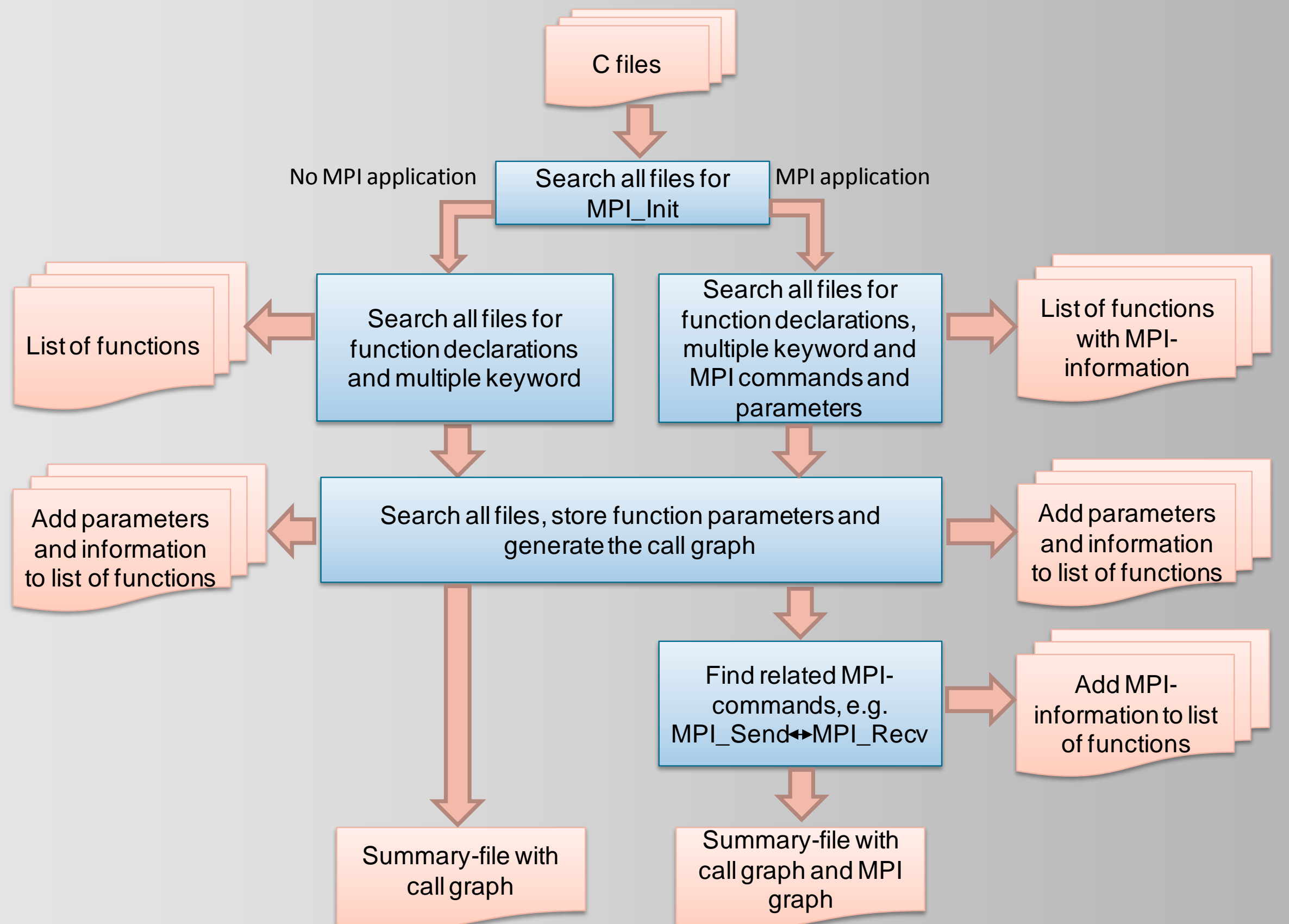


Characteristic	Description	Consequence
Programming Language	Programmed in C-like languages such as NVIDIA's CUDA or OpenCL	Easier and faster design flow than for FPGAs, because more familiar to application developers
Programming Model	Based on an implicit data-parallel programming model (single instruction, multiple threads)	Write scalar code and execute on thousands of threads / data elements, no support for task-parallelism
Communication & Synchronization	Limited and costly inter-thread communication and synchronization mechanisms	Most efficient if no global communication between threads and independent on order of processing

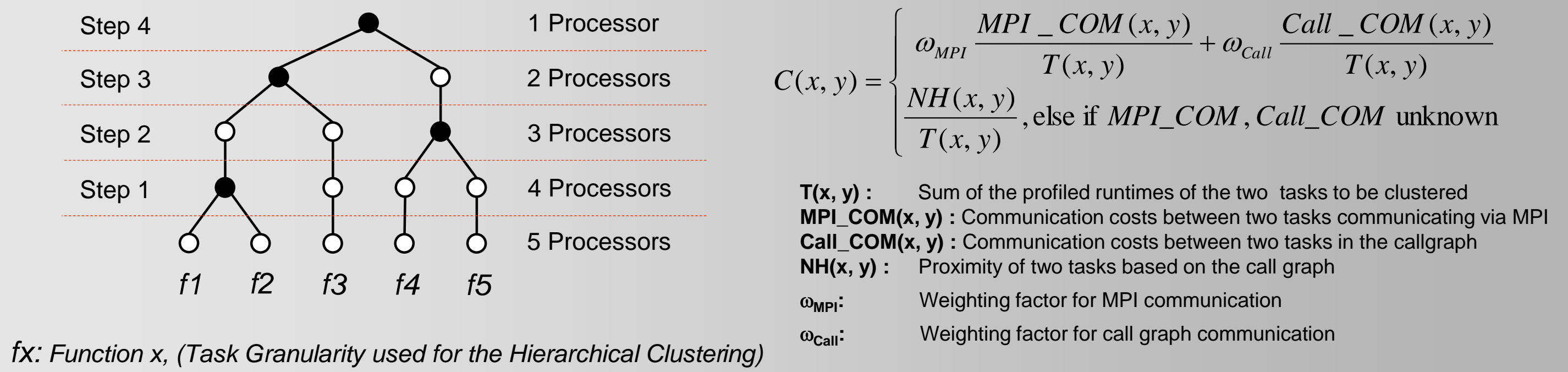
2. Design Methodology for FPGA-based Multiprocessor Accelerators



a) Communication Analysis

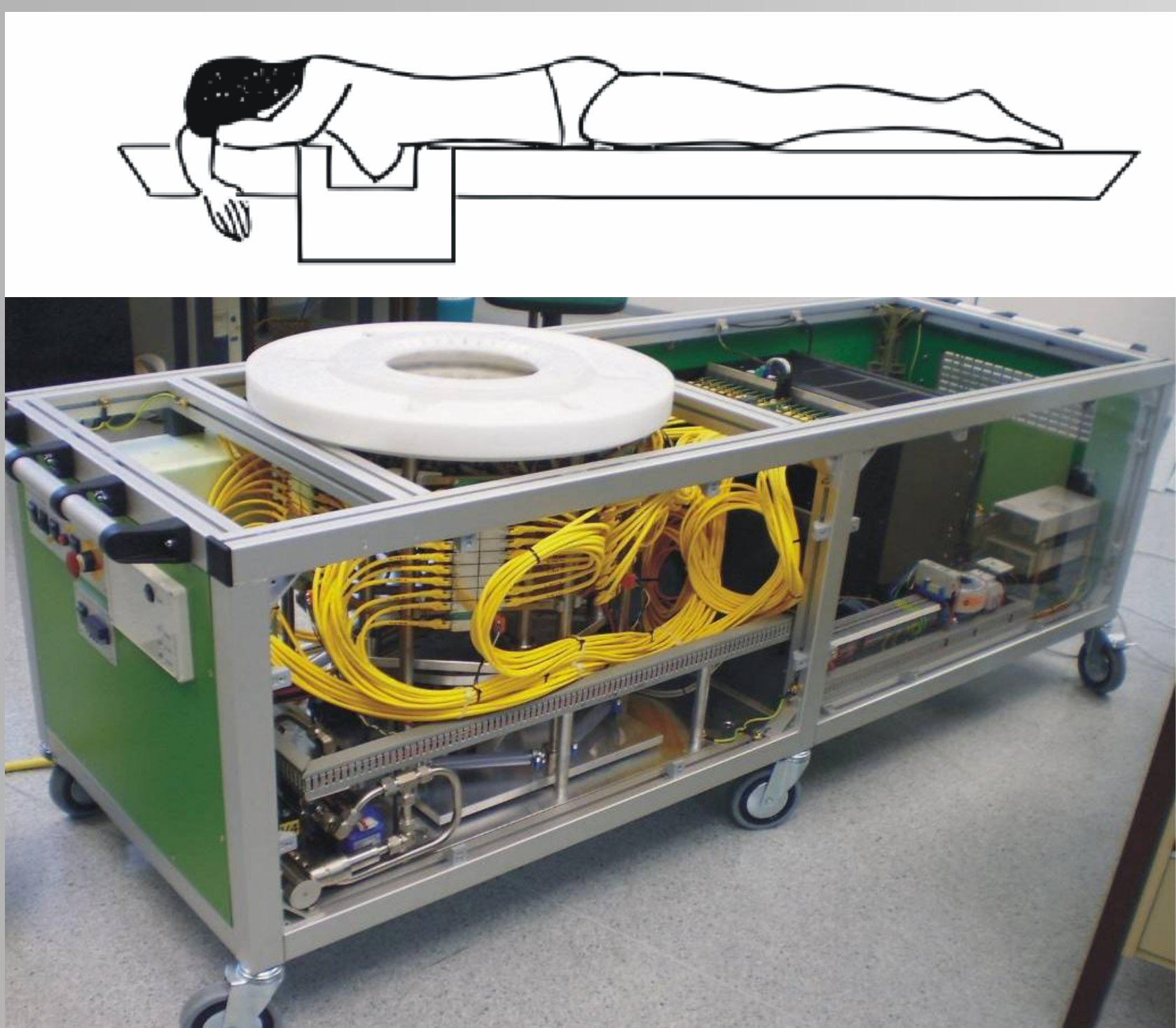


b) SW/SW Partitioning

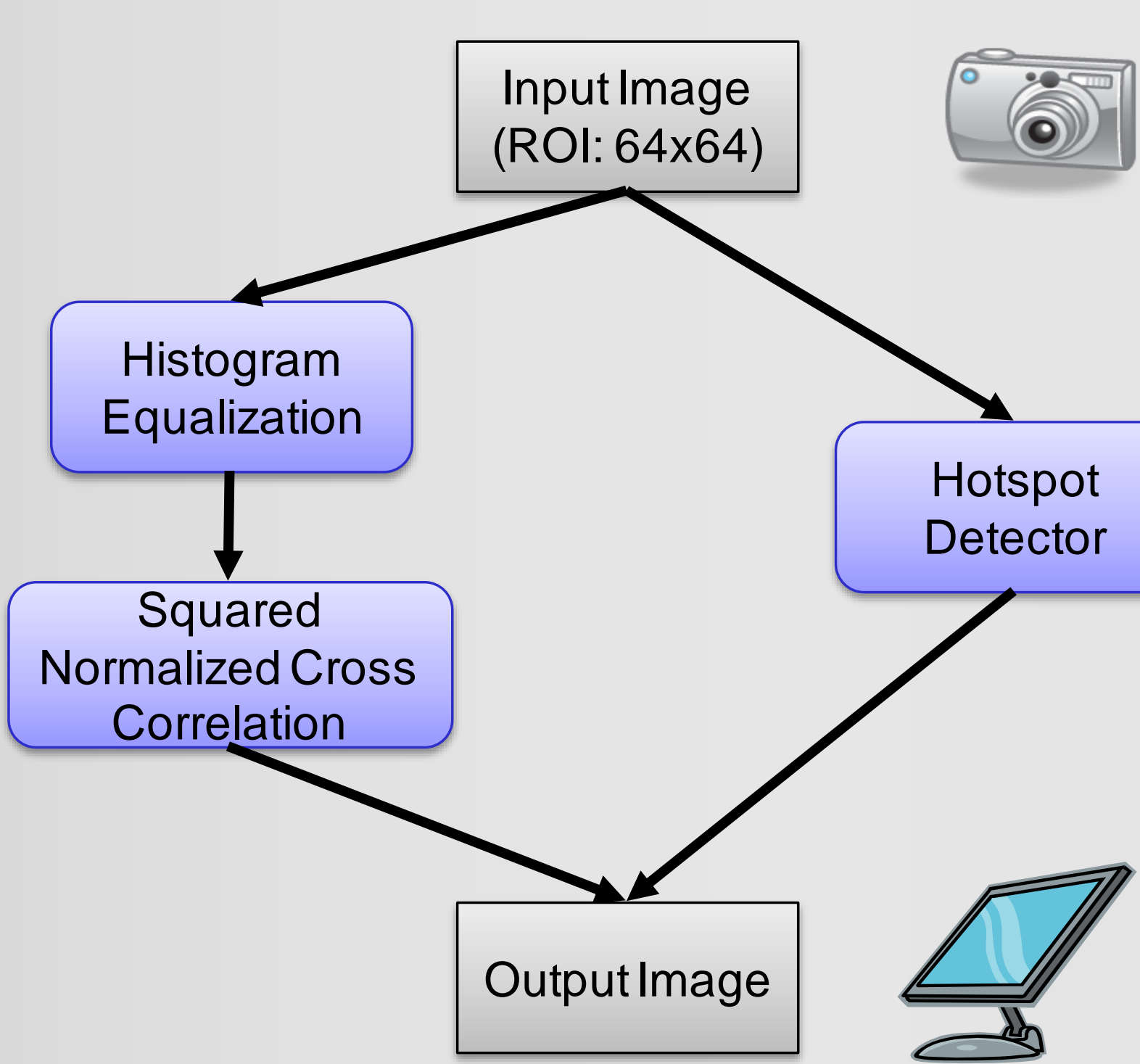


3. Application Exploration

a) 3D Ultrasound computer Tomography

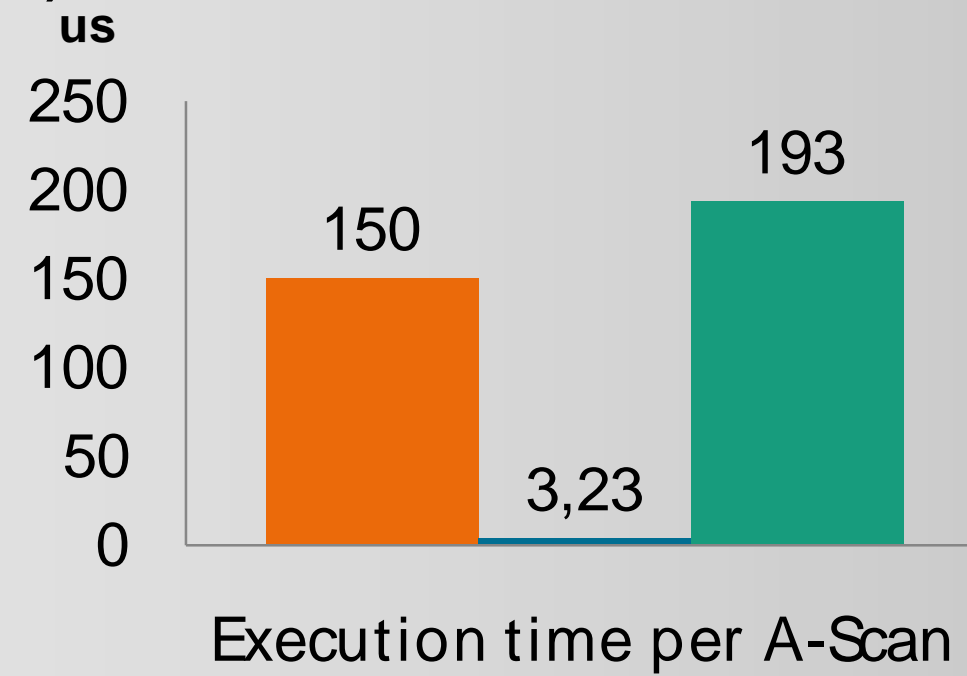


b) Object Recognition



4. Results

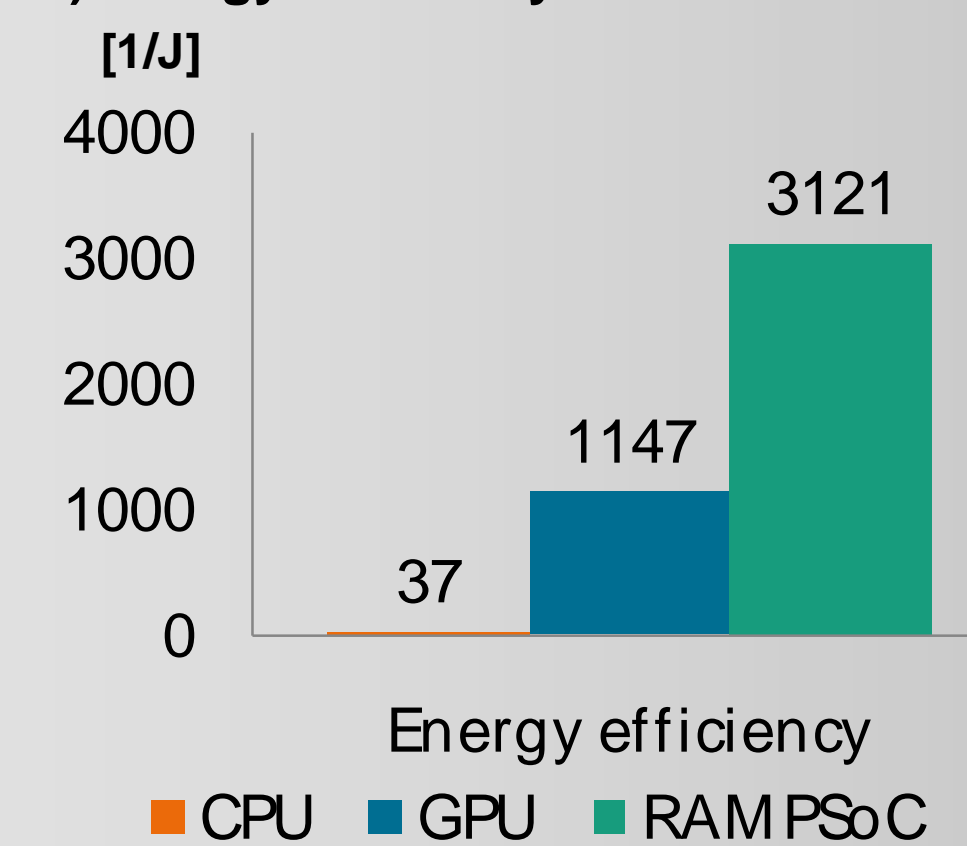
a) Performance 3D USCT



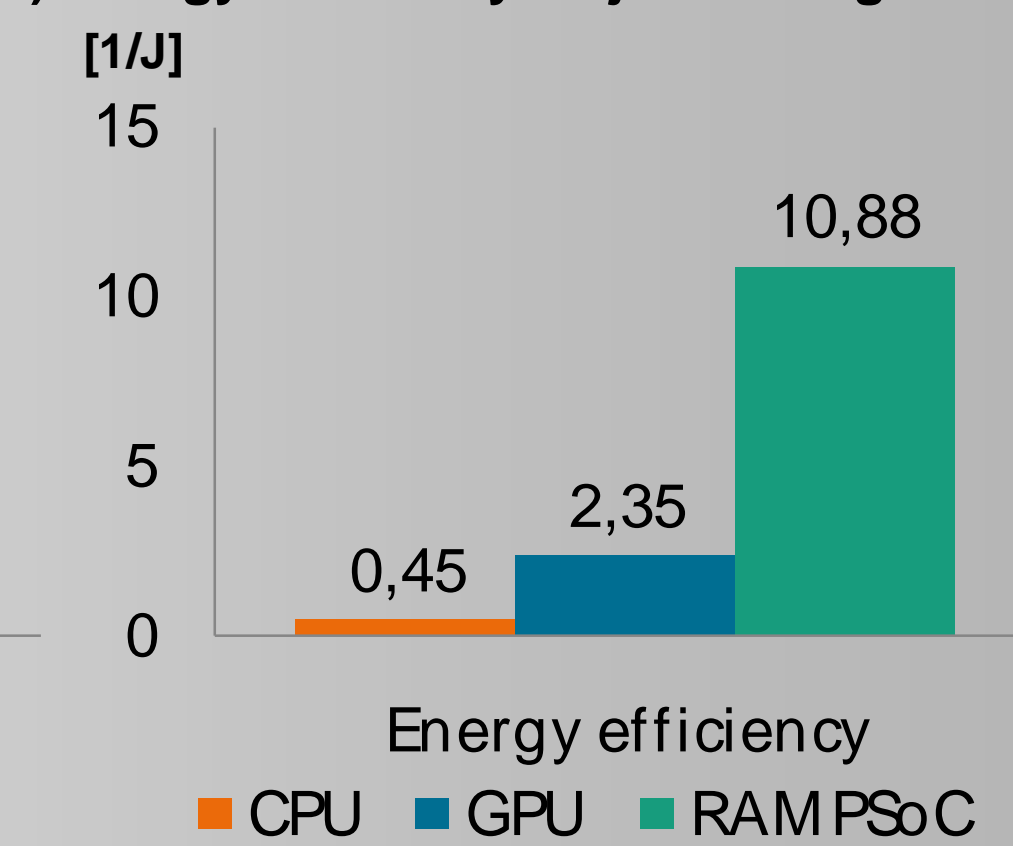
b) Performance Object Recognition



c) Energy Efficiency 3D USCT



d) Energy Efficiency Object Recognition



5. References

- (1) D. Göhringer, M. Hübner, J. Becker, "Adaptive Multiprocessor System-on-Chip Architecture: New Degrees of Freedom in System Design and Runtime Support," in Multiprocessor System-on-Chip: Hardware Design and Tool Integration, M. Hübner and J. Becker, Ed. Springer, 2010, pp.125-149.
- (2) H. Gemmeke, N.V. Ruiters, "3D ultrasound computer tomography for medical imaging," Nuclear Instruments and Methods in Physics Research Section A, vol. 580, no. 2, pp.1057-1065, 2007.

