RIVER Architecture
Reconfigurable Pre-Synthesized-Streaming Architecture for Signal Processing on FPGAs
Christian Brugger, Dominic Hillenbrand, Matthias Balzer

Performance
- 8-core DSE: 250 GMACs
- 4-core TI TM320C6670: 154 GMACs
- Tensilica ConnX BBE64: 128 GMACs
- Tesla C2050 (Fermi): 589 GMACs

Frequency
- 145 MHz (8-Core DSE)
- 300 MHz (individual cores)

Area
- 51% of a Virtex 7 (XCV7000T)

Bandwidth
- 10 GB/s

Dynamic-Streaming-Engine (DSE)

2D - Convolution Filter
Input matrix × Coefficients 3x3 → Output matrix

Example: Mapping 3x3 filters to DSEs

Design Flow

8-core DSE

HiPEAC 2012, 23 January 2012, Paris, France

www.kit.edu