Ultra-fast Data Acquisition System for Coherent Synchrotron Radiation with Terahertz Detectors


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Fast detector systems with picosecond time resolution

Ultra-fast FPGA digitizer board for ANKA

Hardware: 1st prototype (one channel sampling board)

The first prototype contains a single sampling channel operating at 500 MS/s. The track-and-hold amplifier receives the analog pulse and acquires one sample in the peaking time region of each THz pulse (resp. CSR bunch emission).

The time characterization has been achieved by a sequential equivalent time sampling method where one sample per pulse is taken after a very short but well-defined delay.

First results at the ANKA

At the synchrotron light source, ANKA, up to 184 RF buckets can be filled with electrons with the distance between two adjacent buckets of 2 ns corresponding to the 500 MHz frequency of the RF system.

This shows the typical filling pattern of the ANKA storage ring, consisting of three trains separated by a several ns gap. The prototype system is able to resolve single bunch fluctuation in a multi-bunch filling pattern.

Summary and Outlook:

- Measurements using 1st prototype of FPGA board successful
- Open up new possibilities in the CSR diagnostics
- Test beam with the 4-channel board scheduled for October 2013
- Final aim: studies of correlations on the bursting pattern and interactions of very short pulses in the synchrotron storage rings

Design goals

- Simultaneous monitoring of all 184 buckets
- Turn-by-turn acquisition
- Continuous acquisition up to ~3 10⁶ turns
- Fixed reference bucket for all measurements
- Online analysis on FPGA/GPU
- Control system Graphic User Interface
- Real time data analysis

Four sampling channels board

1. A clean jitter phase locked loop (PLL) used to generate a clock signal with high temporal accuracy.
2. Clock is distributed to the picoseconds delay chips by a low skew and jitter clock fanout.
3. The track-and-hold receives a time controlled sampling signals synchronized with the ANKA RF-clock (resp. bunches time distribution).
4. Each delay chip is individually programmable from 3 to 100 ps.
5. 12 bits ADC resolution

Four sampling channels board

1. A high data throughput readout based on a bus master DMA architecture connected to PCI Express. Data throughput of up 4 GByte/s.
2. The HEB detector system
   - Joint development of IMS (Karlsruhe) & DLR (Berlin)
   - SC niobium nitride detector
   - Response time < 165 ps
   - Spectral range: 150 GHz - 1 THz
   - Study of single and multiple bunches

YBCO-THz Detector System

- Yttrium-Barium-Copper-Oxid detector
- Based on YBa2Cu3O7−δ T SC
- Response time: down to 1 ps
- Spectral range: depends on antenna

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