

# High frequency technologies for high-data rate DAQ systems

M. Caselle, S. Cilingaryan, T. Dritschler, A. Kopmann, L. Rota, U. Stevanovic, M. Weber



# Outline

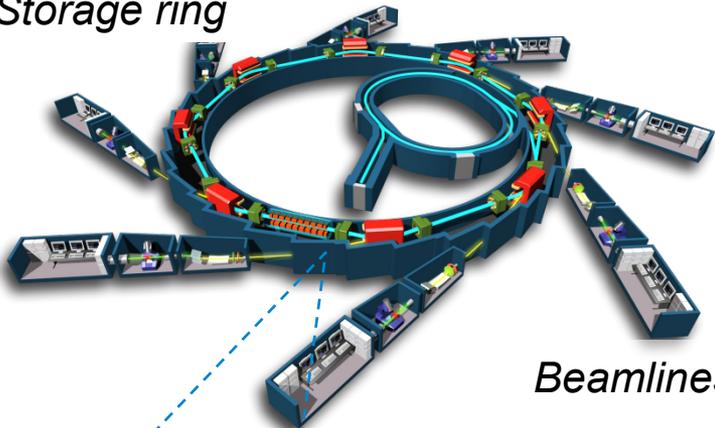
- ❑ Introduction to ANKA terahertz Coherent Synchrotron Radiation (CSR)
- ❑ Cryogenic terahertz detectors technologies
- ❑ High-bandwidth front-end
- ❑ Picosecond pulse sampling “KAPTURE” system and beam test results
- ❑ New DMA-PCIe Readout compatible with GPU Direct access
- ❑ Conclusions

ARD  $\longleftrightarrow$  DTS

Pico / Femto second  
Beam diagnostic, detectors and DAQ system

# Terahertz Coherent Synchrotron Radiation at ANKA

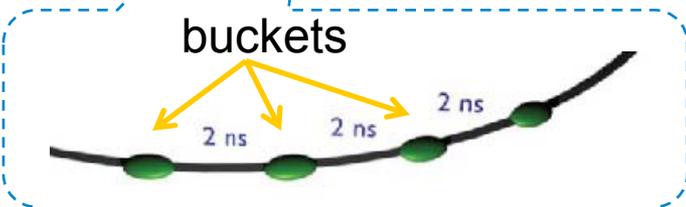
Storage ring



Beamlines

**ANKA** is the Synchrotron Radiation Facility at the Karlsruhe Institute of Technology (KIT)

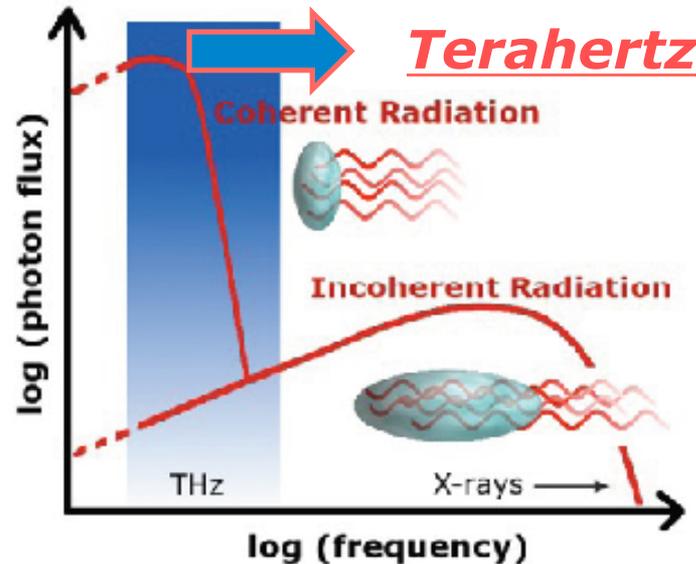
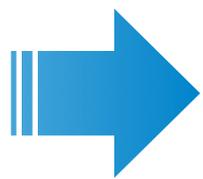
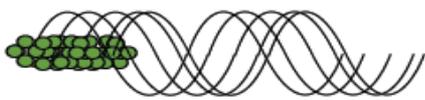
- ❖ Circumference: **110.4 m**
- ❖ RF-system: **500 MHz**
- ❖ Harmonic number: **184**



*Low alpha mode*



*Normal mode*



Reference:  
**A.-S. Müller, et al.** Observation of Coherent THz Radiation from the ANKA and MLS Storage Electron Bolometer. (TU5RFP027), 2009. 23rd Particle Accelerator Conference PAC09 Vancouver, Canada.



# Ultra-fast THz Detectors

To detect and study of the emission characteristics of CSR in the THz range →  
high time accuracy detector, spectrum of hundred GHz -> Terahertz

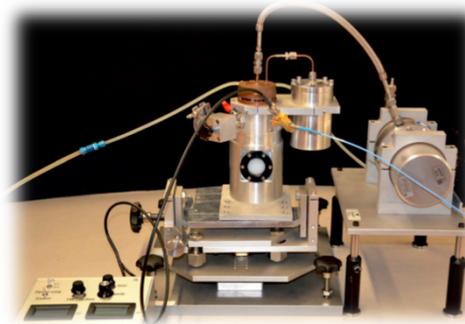
## Hot-Electron-Bolometer (NbN)



- Response time < 165 ps
- Liquid He cooling
- Developed at DLR

[1]

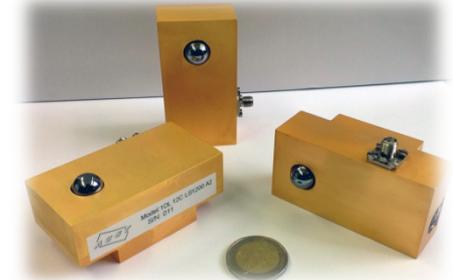
## YBCO-Detector



- Response time < 15 ps
- Liquid N<sub>2</sub> cooling
- Developed at KIT-IMS

[2]

## Quasi-Optical Broadband Detector (Schottky diodes)



- Response time < 200 ps
- No cooling required
- Commercially available (ACST, VDI)

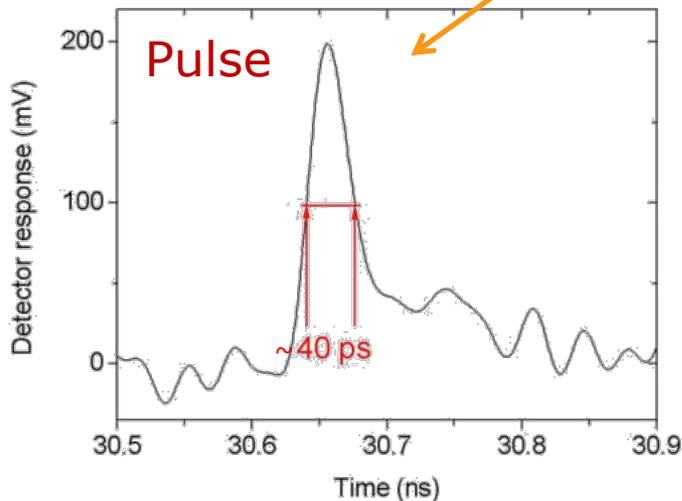
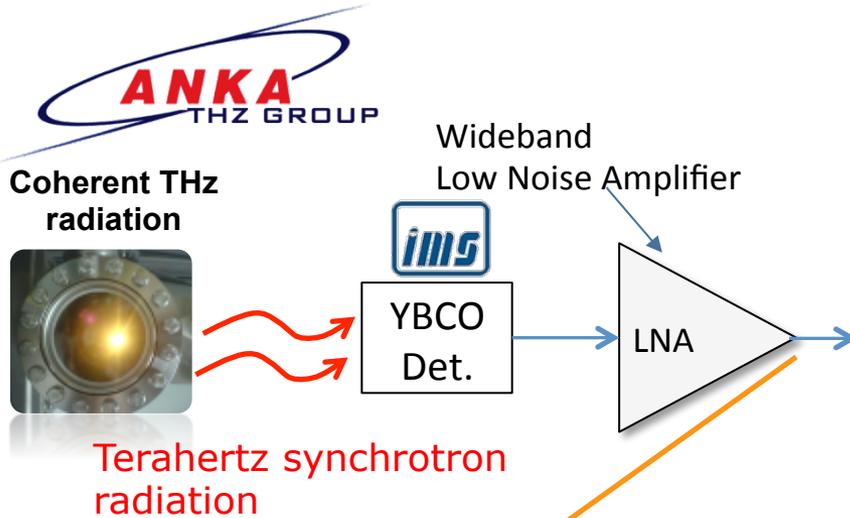
[3]

[1] A.D. Semenov, et al., IEEE Transactions on Microwave Theory and Techniques 55 (2007) 239

[2] P. Thoma, J. Raasch, et al., IEEE Trans. Appl. Supercond., Vol. 23, No 3, pp2400206, June 2013

[3] A. Semenov, et al., IEEE Electron Device Letters 31, (674) 2010

# Picosecond pulse sampling requirements

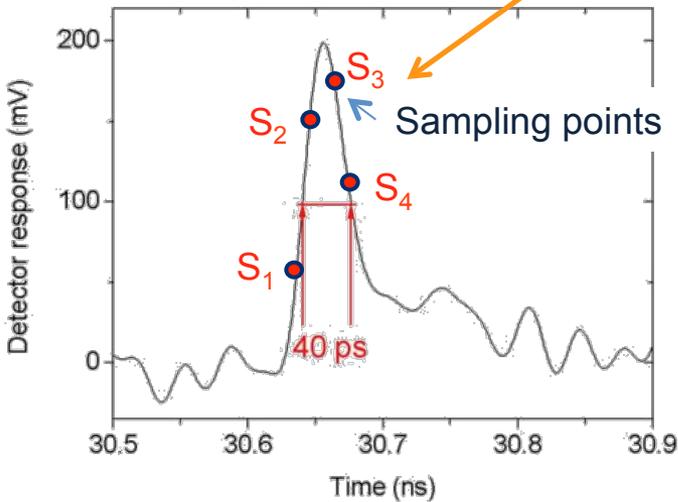
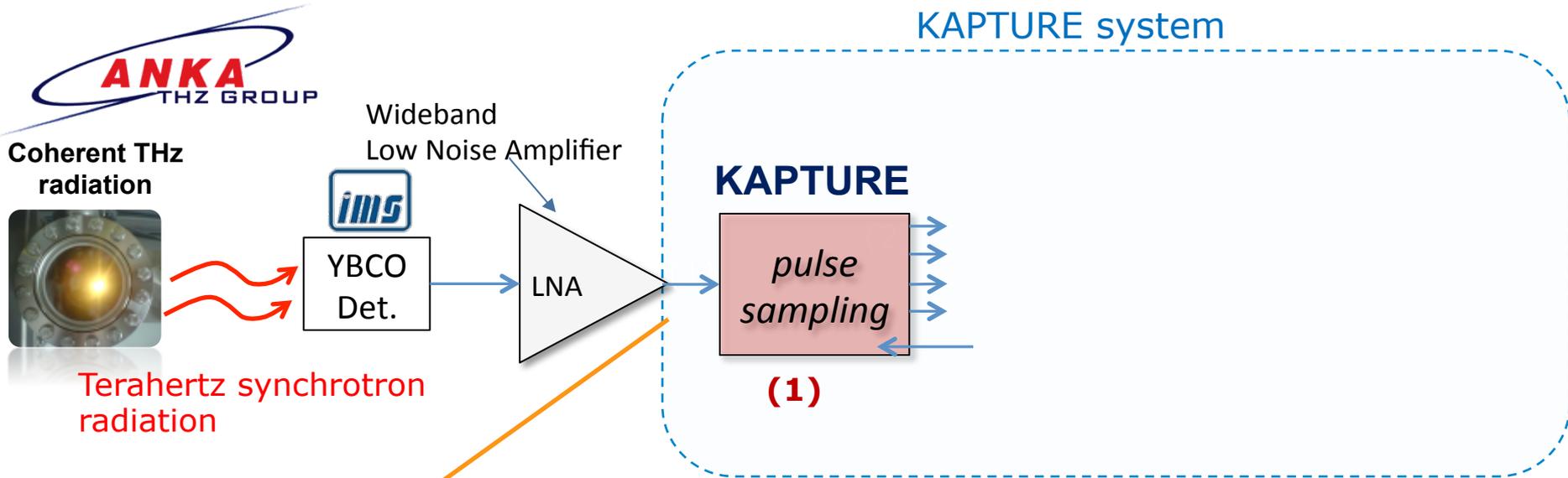


Pulse measured with a real-time oscilloscope (bandwidth 60GHz)

## Requirements:

- 1. DAQ for THz detectors:** YBCO, Schottky Diodes, HEB, ..
- 2. Pulse repetition rate: 500 MHz**
- 3. Continuous acquisition for long observation time:** seconds, minutes...
- 4. Wideband circuitries, bandwidth: DC-60GHz**

# Picosecond pulse sampling requirements



*Pulse with repetition rate 500 MHz*

- 1. Sampling:** each pulse sampled with 4 samples by **KAPTURE** system , minimum sampling time of 3 ps.

# Picosecond pulse sampling requirements

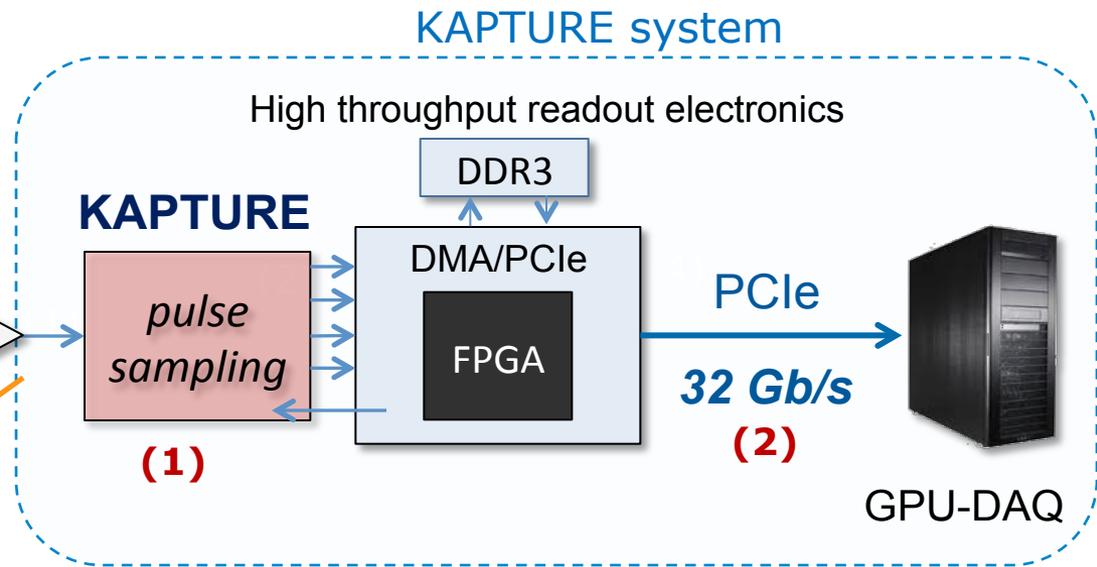
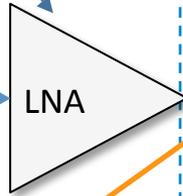
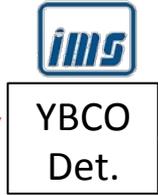


Coherent THz radiation

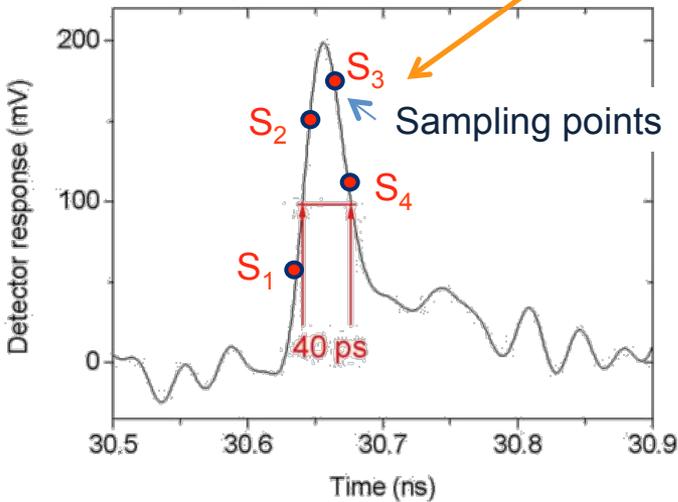


Terahertz synchrotron radiation

Wideband Low Noise Amplifier



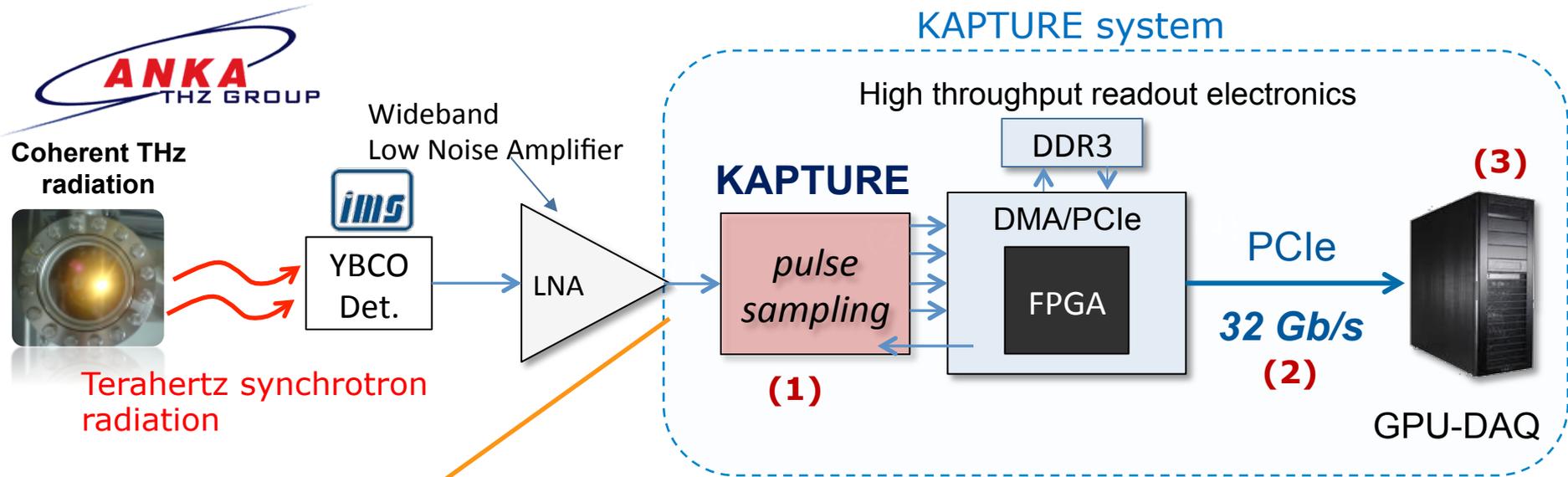
Continuously data streaming



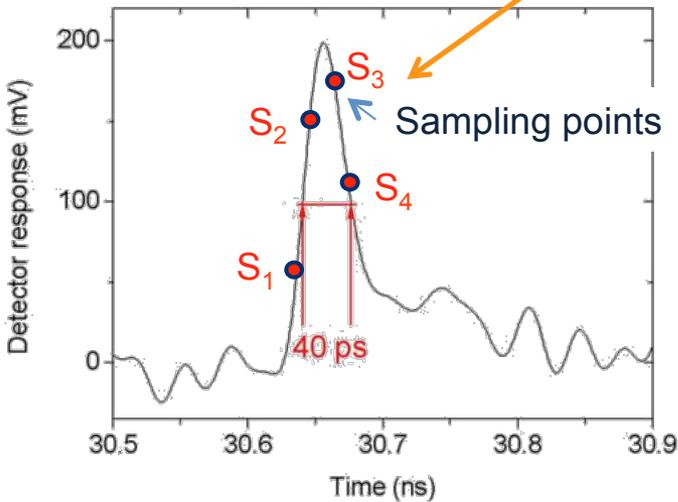
Pulse with repetition rate 500 MHz

- 1. Sampling:** each pulse sampled with 4 samples by **KAPTURE** system , minimum sampling time of 3 ps.
- 2. Data transfer:** digital samples transferred to high-end GPU (Graphics Processing Units) by a PCIe-DMA architecture

# Picosecond pulse sampling requirements



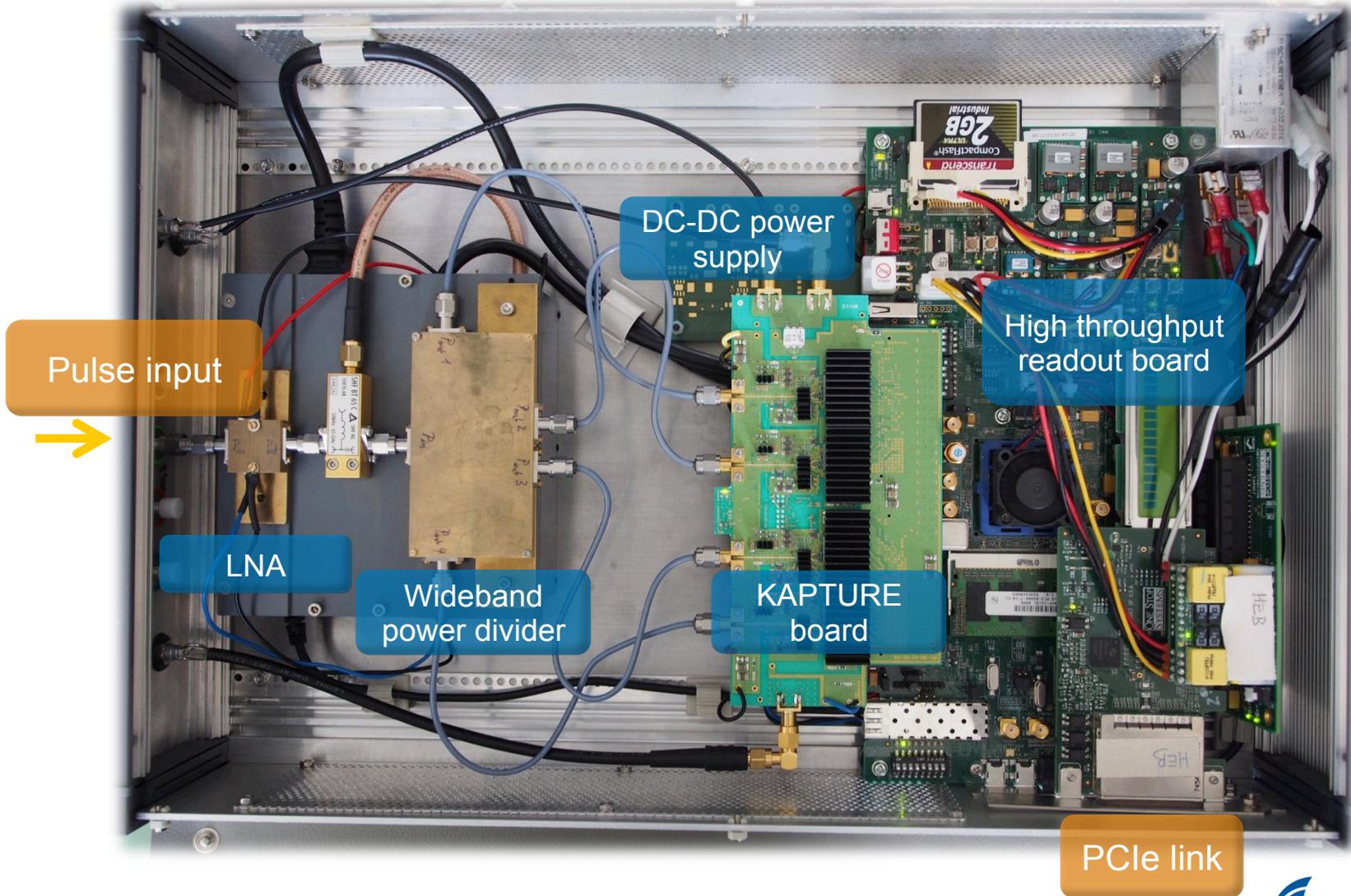
Terahertz synchrotron radiation



Pulse with repetition rate 500 MHz

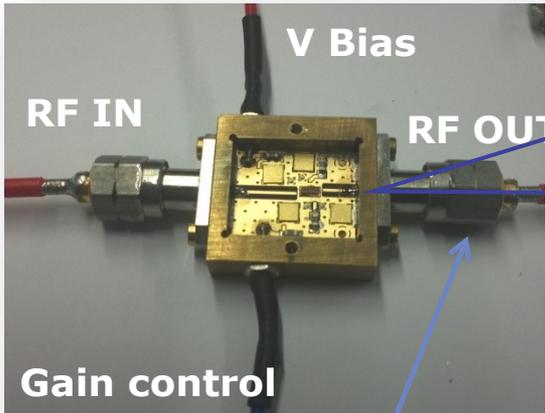
- 1. Sampling:** each pulse sampled with 4 samples by **KAPTURE** system , minimum sampling time of 3 ps.
- 2. Data transfer:** digital samples transferred to high-end GPU (Graphics Processing Units) by a PCIe-DMA architecture
- 3. Real-time GPU data elaboration:** pulses reconstruct, amplitude and peaking time respectively with “mV” “picosecond” accuracy are evaluated

# KAPTURE - system

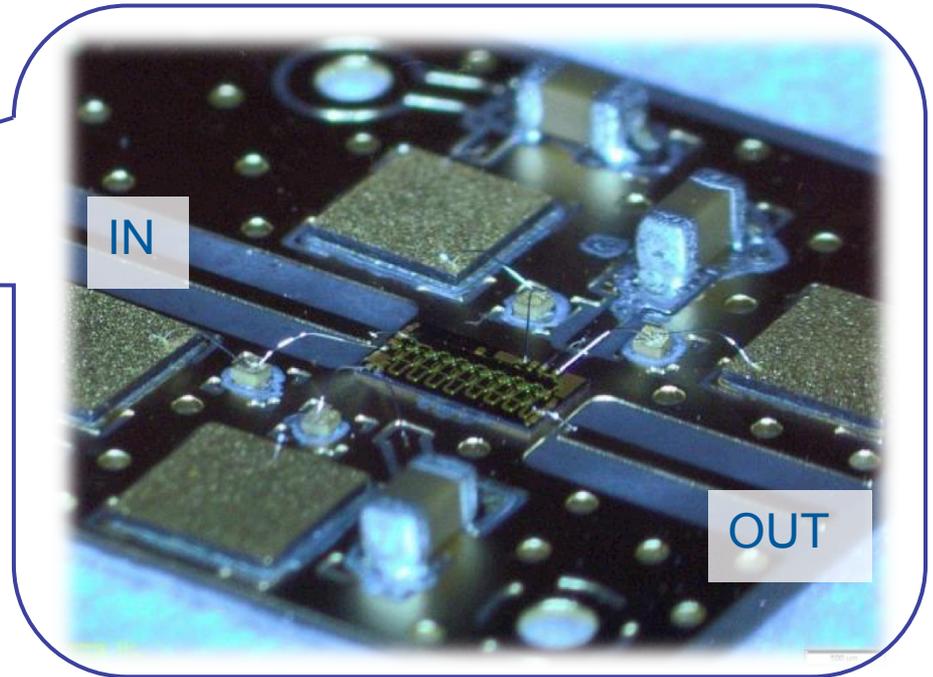


# Low Noise Amplifier (LNA)

## Wideband Low Noise Amplifier



High-freq.  
V-connectors

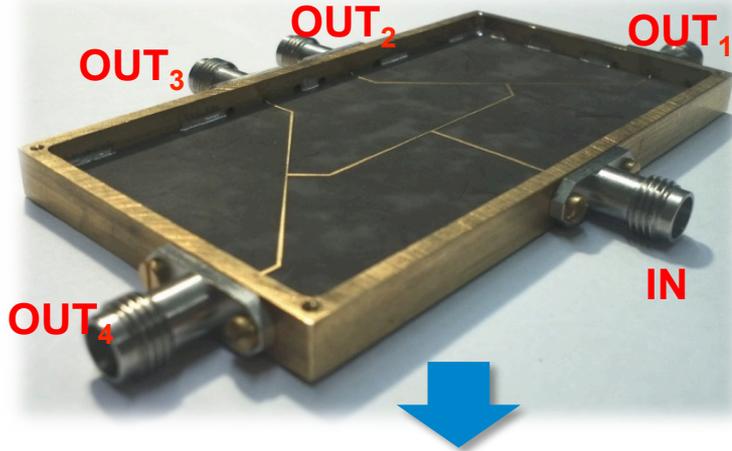


- ❑ MCM-D technology with new PCB materials for Microwave/RF design
- ❑ MMIC based on GaAs technology
- ❑ Bandwidth DC- 55 GHz and Flat gain : **12 dB up to 48 GHz**
- ❑ Under development → new LNA with bandwidth: **0.5 – 65 GHz, gain = 10 dB**

# Wide-Band power divider

Components not available on the market

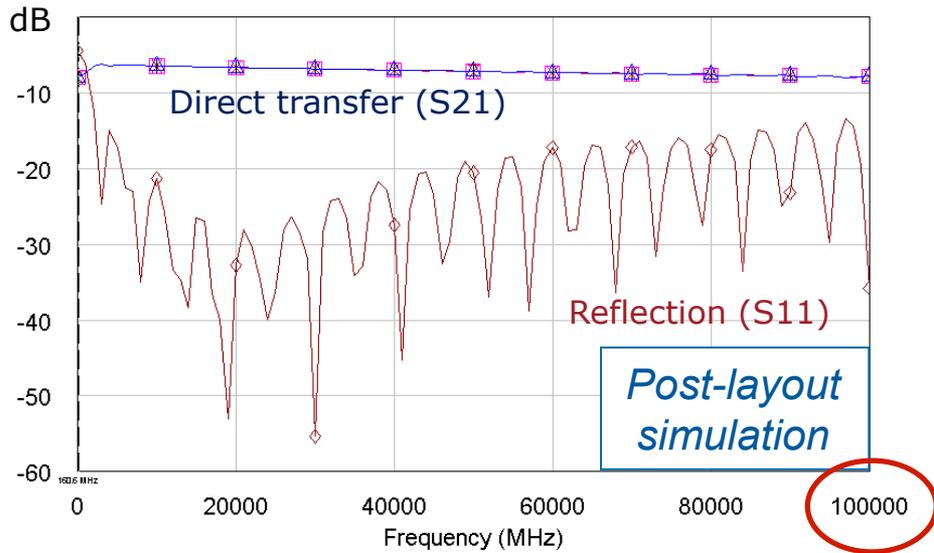
Power divider 1:4 outputs



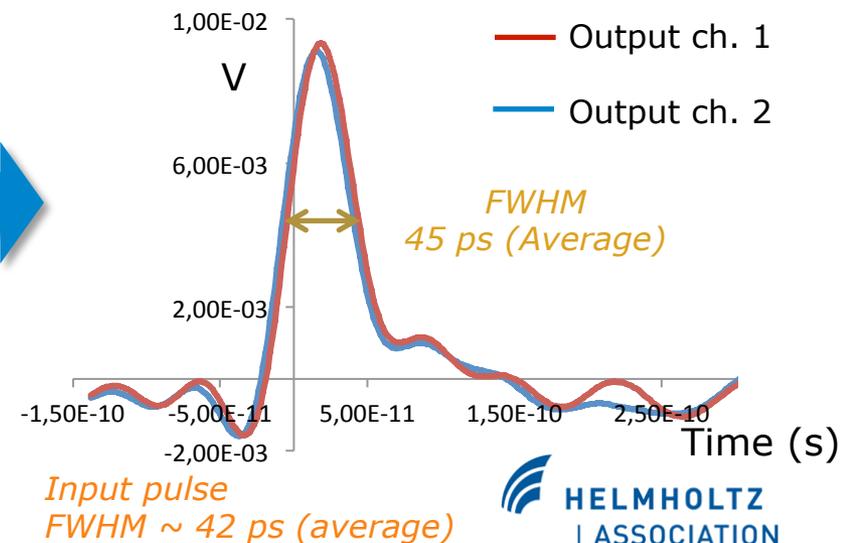
Power divider 1:2 outputs



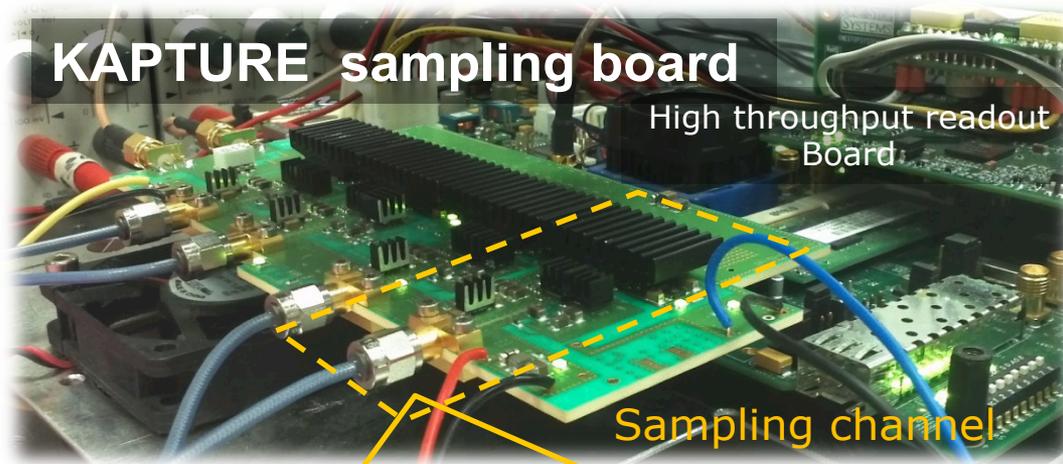
KIT power splitter 1:4 (S parameters)



Outputs channels (time)

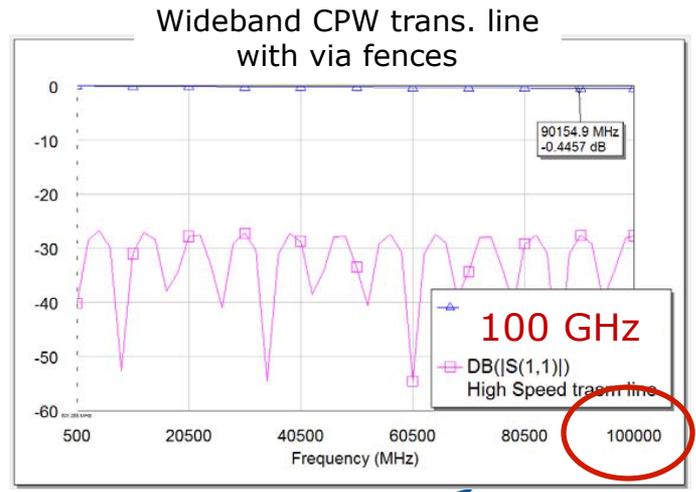
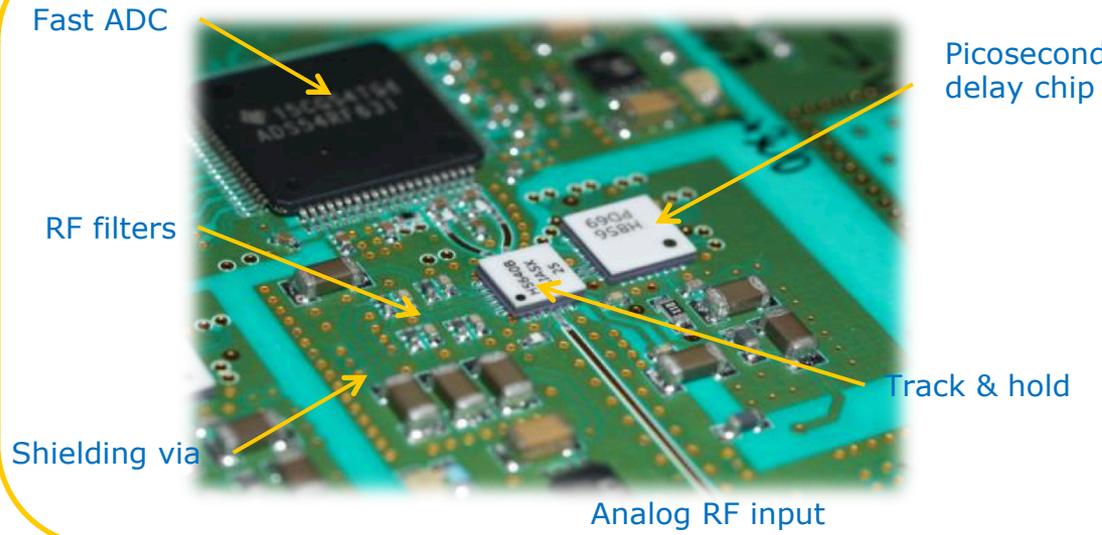


# KAPTURE sampling board

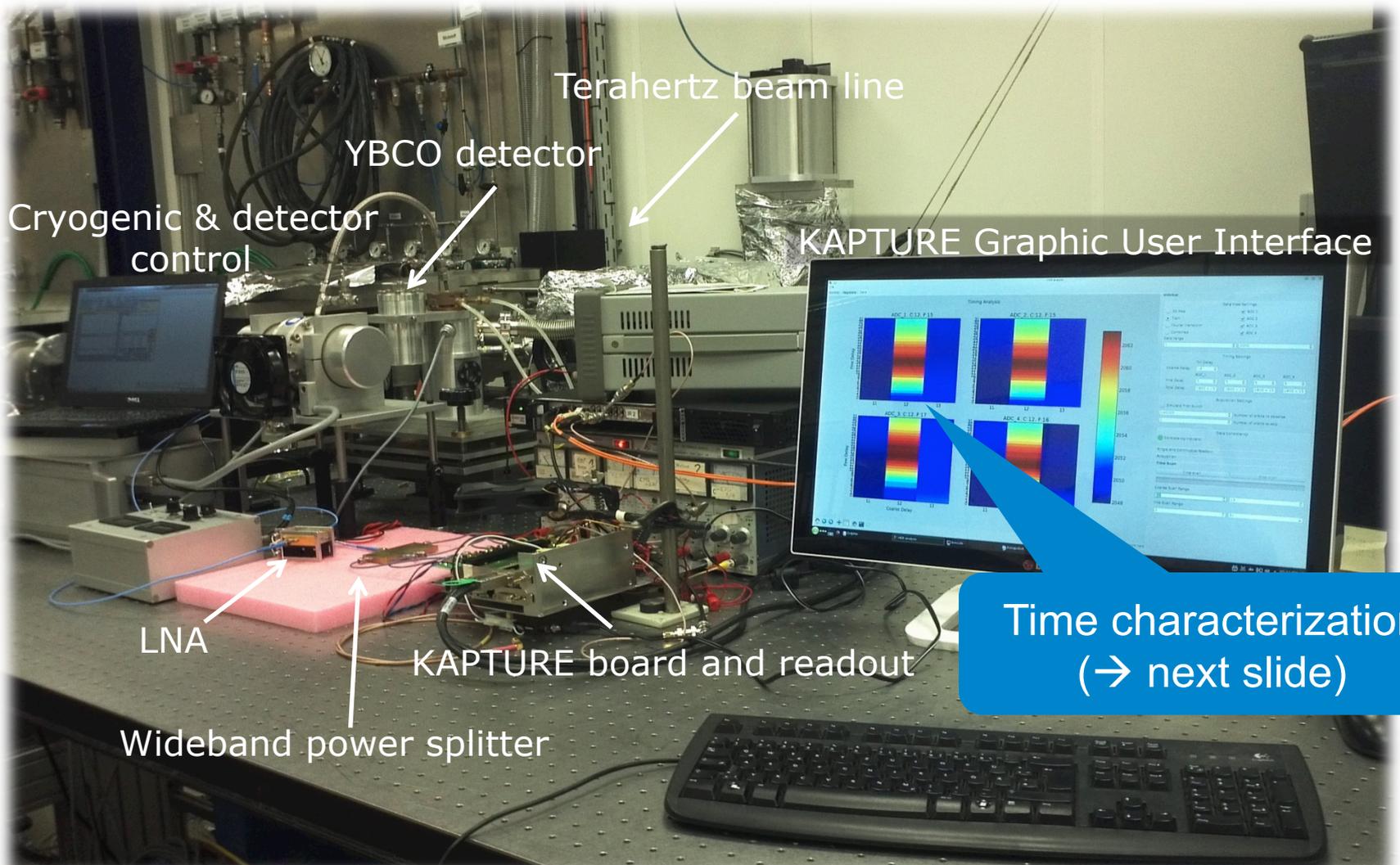


- ✓ Minimum sampling time: 3 psec → >300GS/s (equivalent sampling mode)
- ✓ 12 bit ADC resolution
- ✓ Configurable for the readout of up to 4 ultra-fast detectors in parallel

## Sampling stage



# First beam test setup / May 2014



Terahertz beam line

YBCO detector

Cryogenic & detector control

KAPTURE Graphic User Interface

LNA

Wideband power splitter

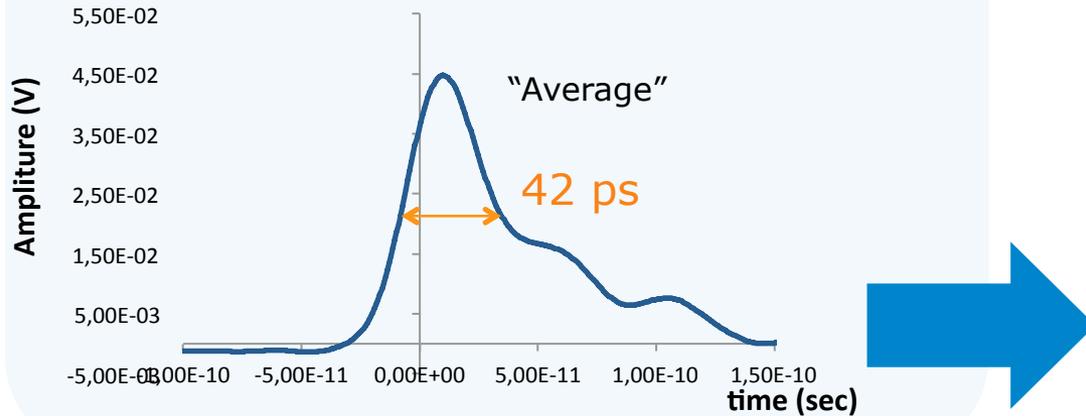
KAPTURE board and readout

Time characterization (→ next slide)

# Time characterization with YBCO detector pulse

- YBCO detector pulse acquired using equivalent sampling method by KAPTURE: minimum sampling time **3 ps**, pulse repetition rate **500 MHz**

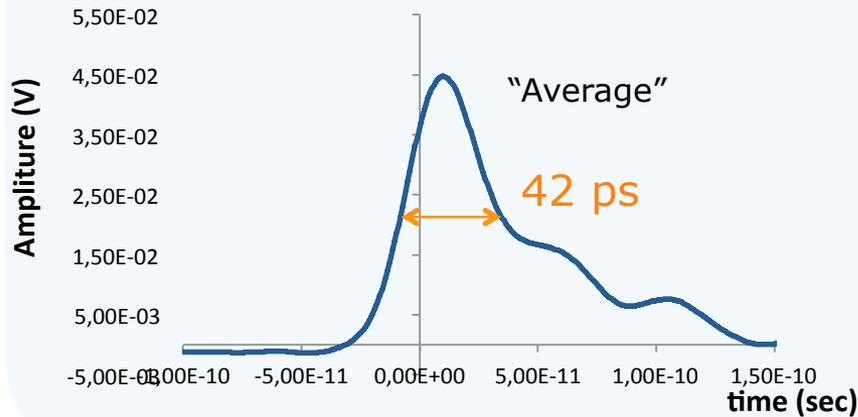
Pulse measured by real-time oscilloscope (bandwidth 60GHz)



# Time characterization with YBCO detector pulse

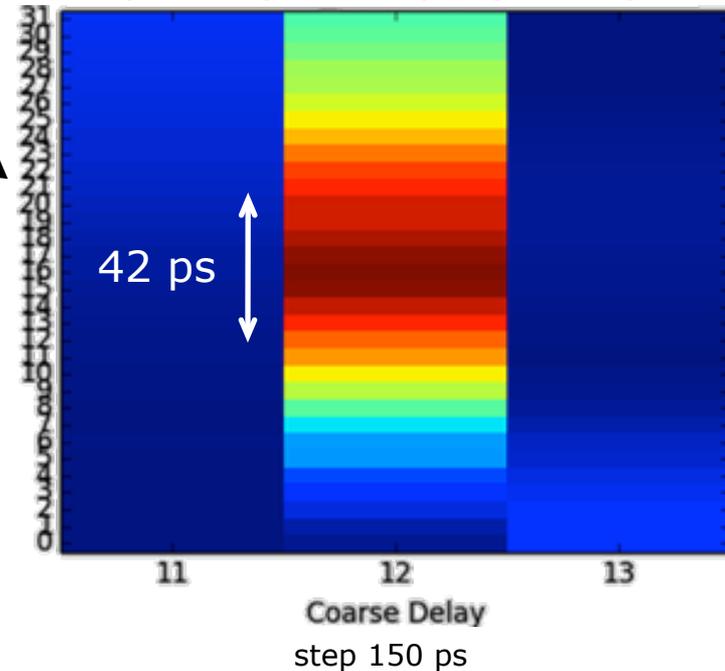
- YBCO detector pulse acquired using equivalent sampling method by KAPTURE: sampling time **3 ps**, pulse repetition rate **500 MHz**

Pulse measured by real-time oscilloscope (bandwidth 60GHz)



Pulse measured by KAPTURE, operating in sampling timing

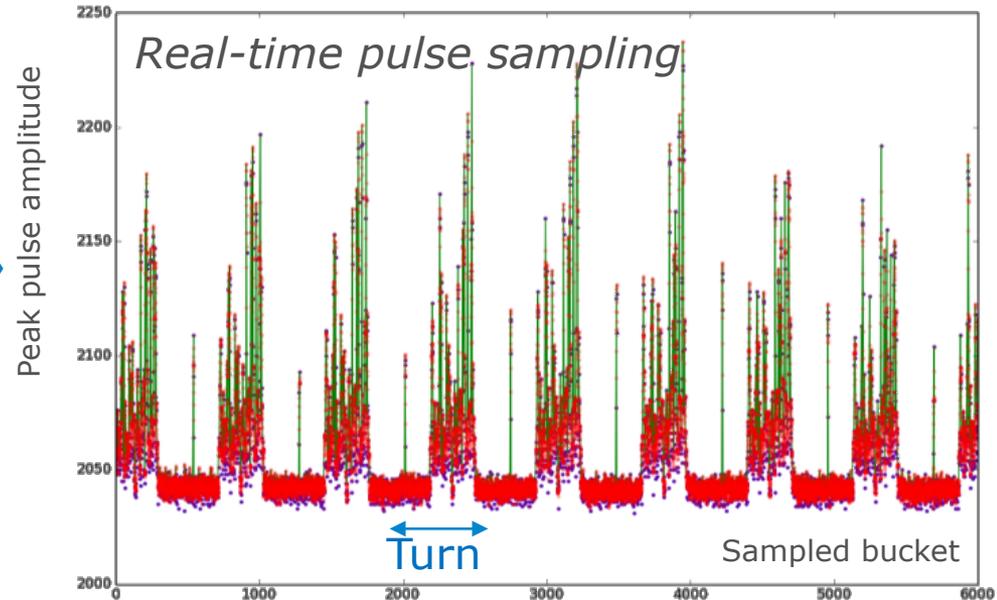
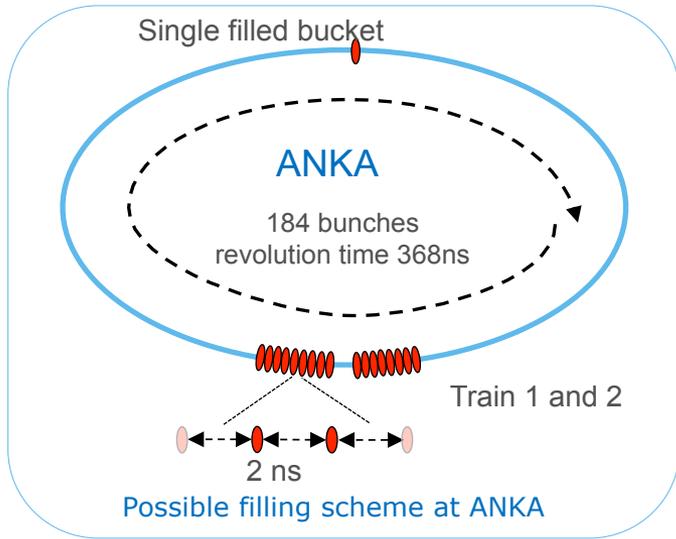
Fine delay (step 3 ps)



## Results:

The pulse width (FWHM) measured by KAPTURE is 42 ps in agreement with the measurement by fast real-time oscilloscope

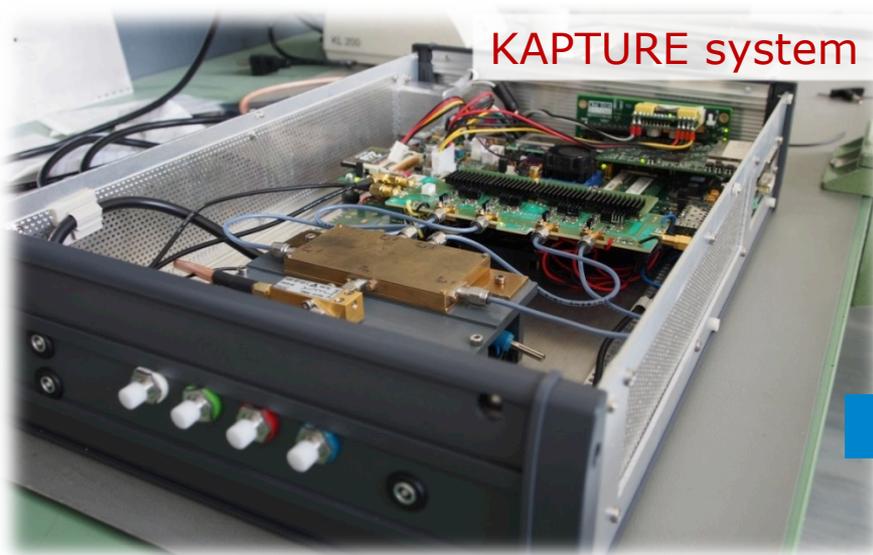
# Beam test with YBCO detector and KAPTURE



## Performance real-time mode:

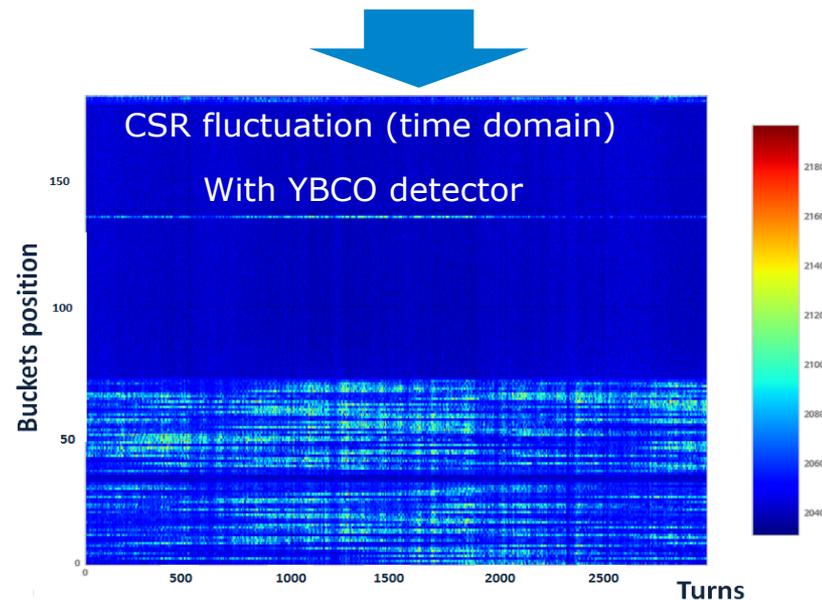
- ❖ Each pulse acquired by 4 samples
- ❖ Pulse repetition rate of 500 MHz
- ❖ Pulse reconstruction (GPU) and measurements of:
  - ❖ Pulse amplitude (mV)
  - ❖ Peaking time (ps)
  - ❖ Pulse width (ps)
- ❖ Fast Fourier Transform (GPU)

# An Ultra-fast Picosecond Digitizer for Coherent Synchrotron Radiation

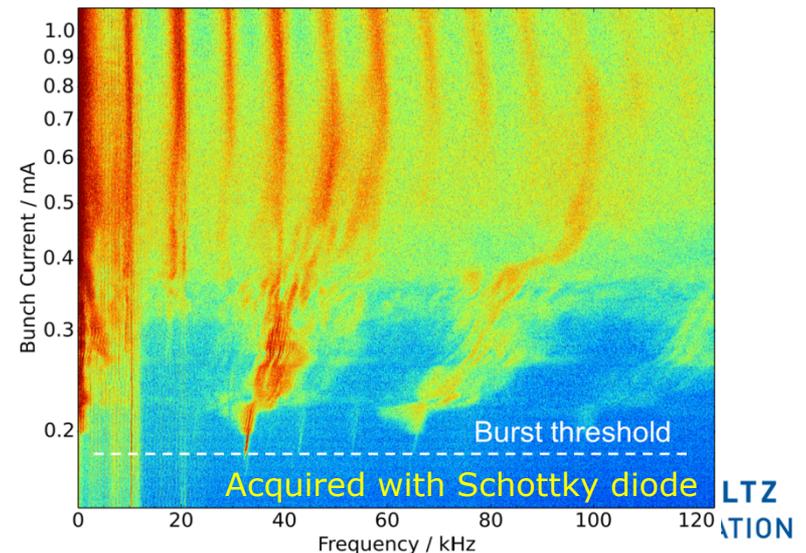


- ✓ Simultaneous monitor of CSR fluctuation of all buckets. (multi-bunch mode)
- ✓ Continuous turn-by-turn acquisition
- ✓ Studies of CSR fluctuation at different bunch current regimes

Opens up new diagnostic possibilities such as instantaneous measurement of bursting threshold and longitudinal particle dynamics



Frequency behaviour of CSR @ different bunch current

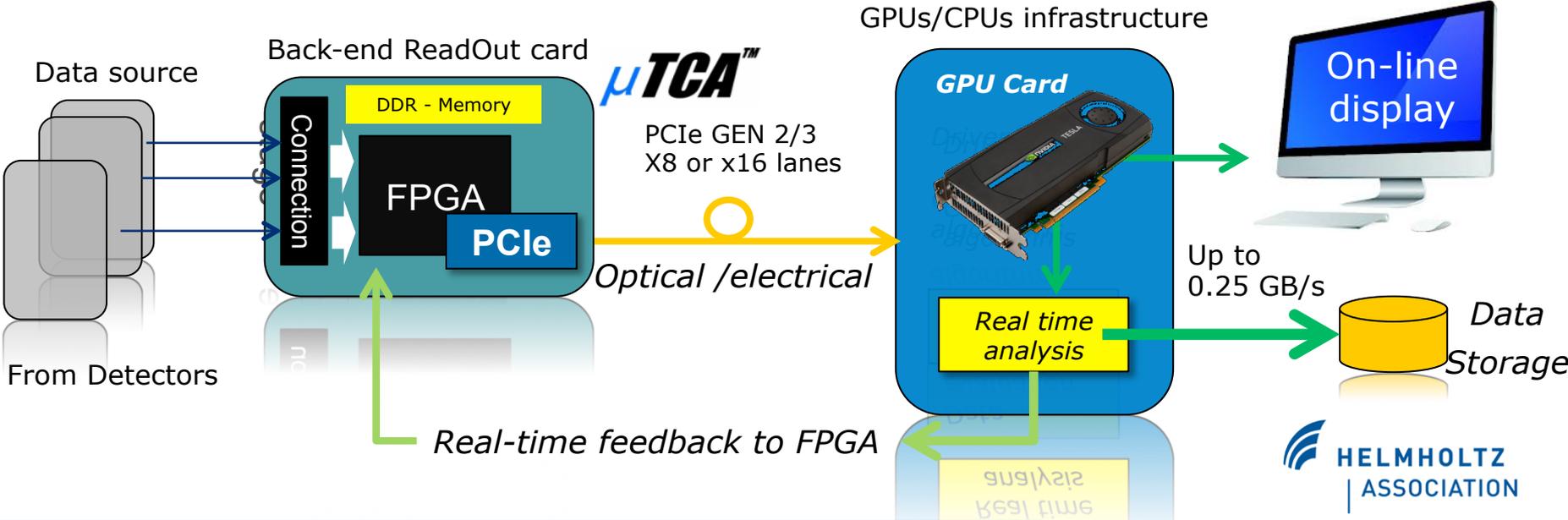


# High-speed DAQ architecture and real-time elaboration

- ❑ High flexibility readout card → based on **FPGA**
- ❑ Fast data throughput → based on last generation of “commercial” data link **PCIe/InfiniBand**
- ❑ High-flexibility real-time elaboration → based on **GPU**

## Point – to – point DAQ architecture

- Very-fast data link → to move data from data-source to real-time elaboration
- Real-time elaboration → by Graphics Processing Unit (GPU)

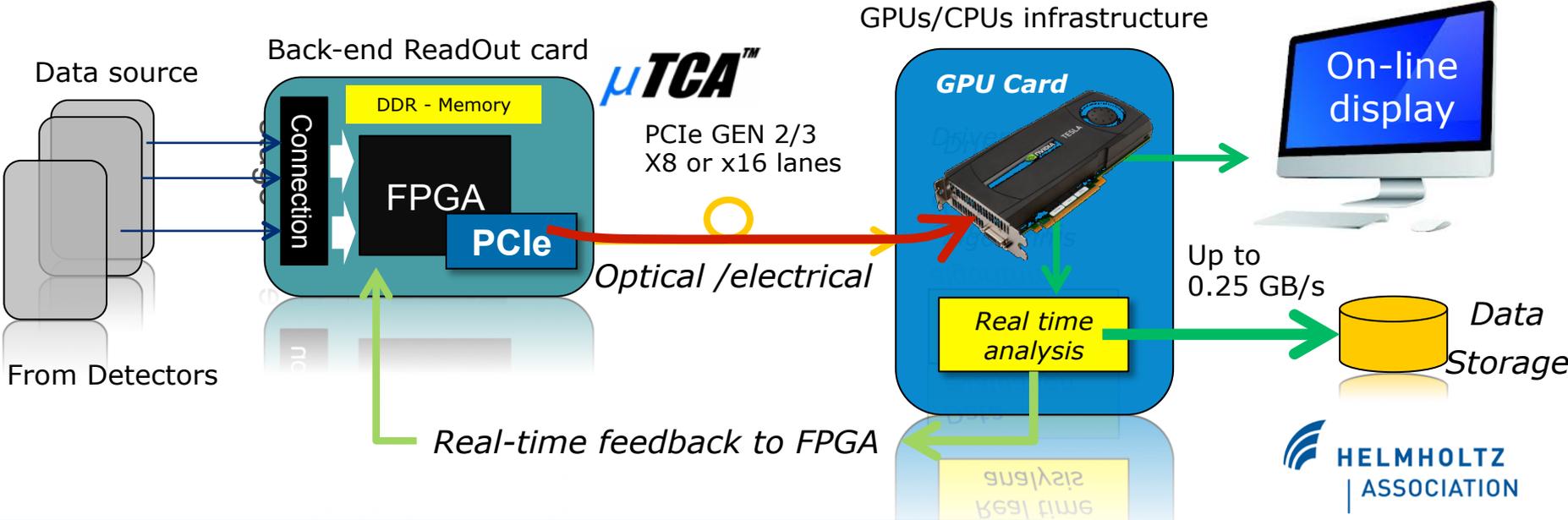


# High-speed DAQ architecture and real-time elaboration

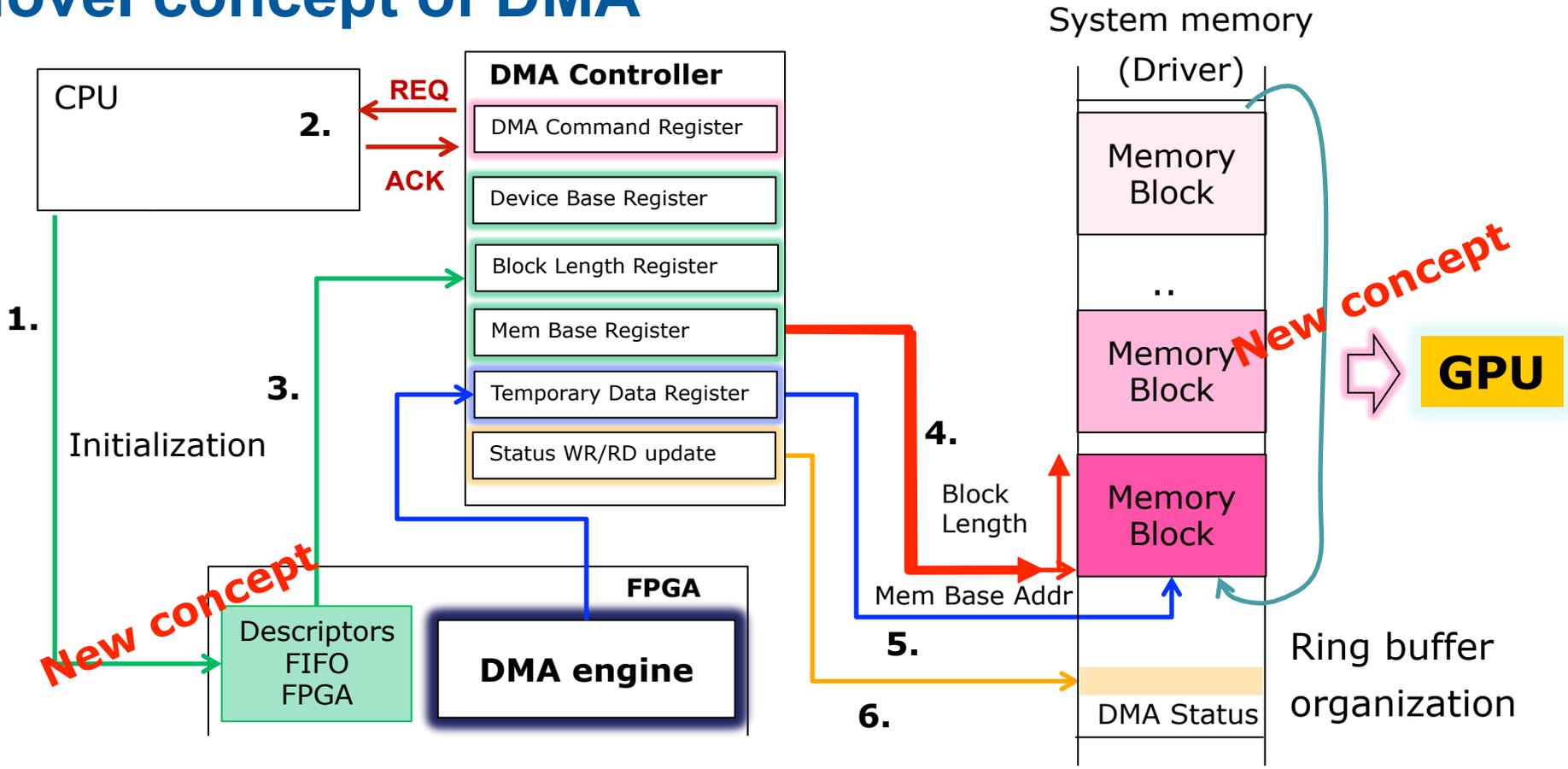
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## Point – to – point DAQ architecture

- *Very-fast data link → to move data from data-source to real-time elaboration*
- *Real-time elaboration → by Graphics Processing Unit (GPU)*
- *GPUDirect data access → data write into GDDR5 Memory and not in the system memory*



# Novel concept of DMA

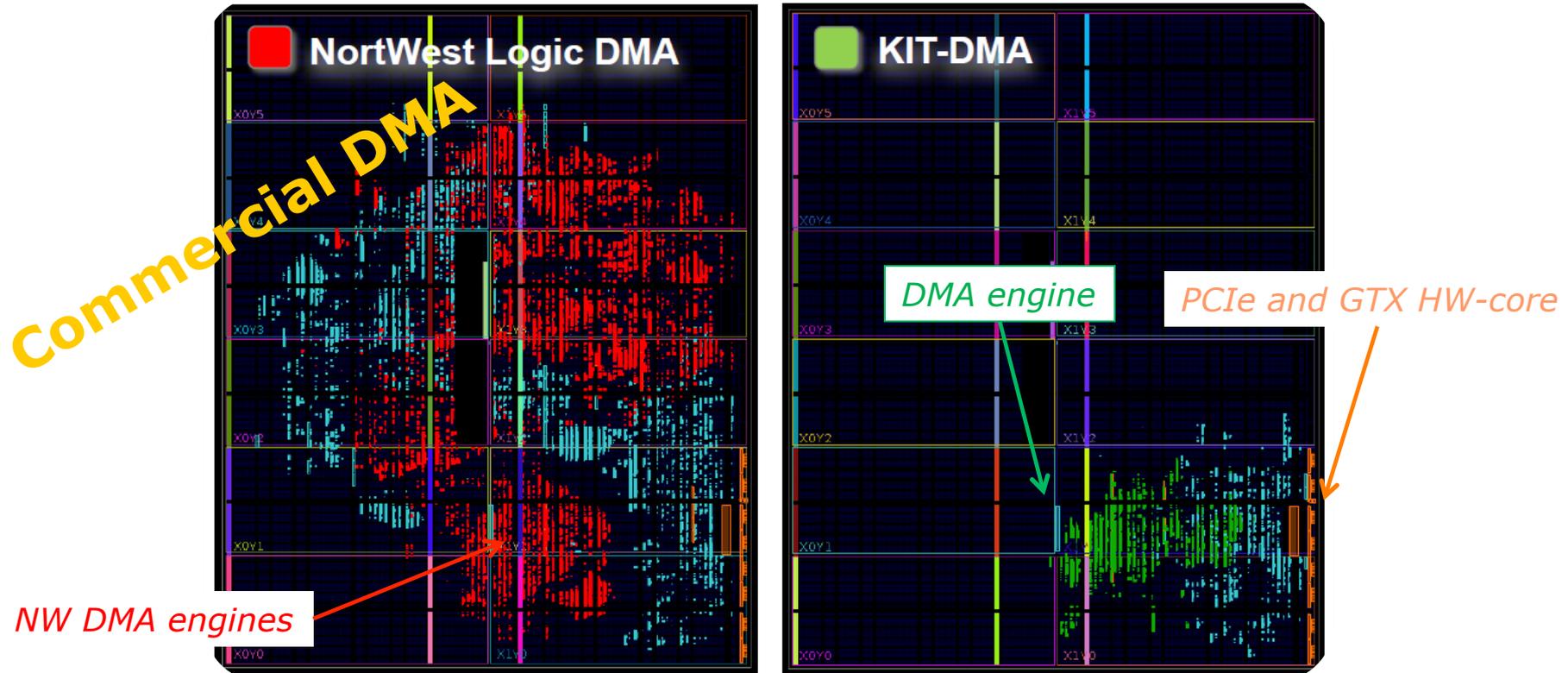


## Operations:

1. Driver write the command and Descriptors in the FPGA and memory blocks allocation (Initialization)
2. DMA – Start by REQuests to CPU and waiting the ACKnowledge signal
3. DMA load the descriptor from the FIFO and fetch the DATA
4. Initiated the Memory Block and 5. Data transfer from I/O → to Block Memory
6. Update the Status → number of blocks written, address, status ..

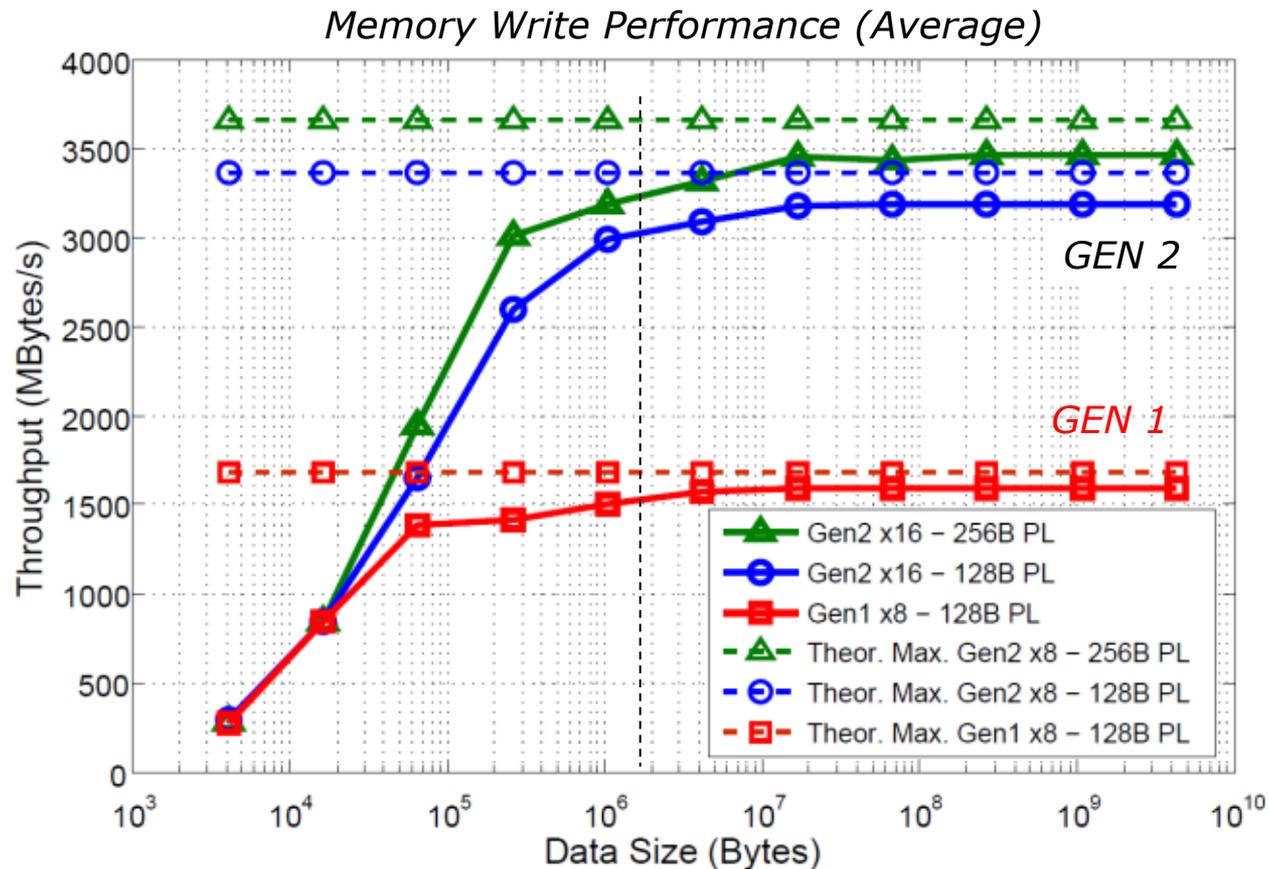
# Comparison with commercial PCIe-DMA architecture

Virtex 6 -> XC6VLX240-2 FF1759



*Same logic functions*

# PCIe-DMA architecture - performance



L. Rota & M. Caselle "High-throughput PCIe DMA architecture for Gigabyte Data Transmission". *IEEE-Transactions on Nuclear Science. Real Time Conference 2014*

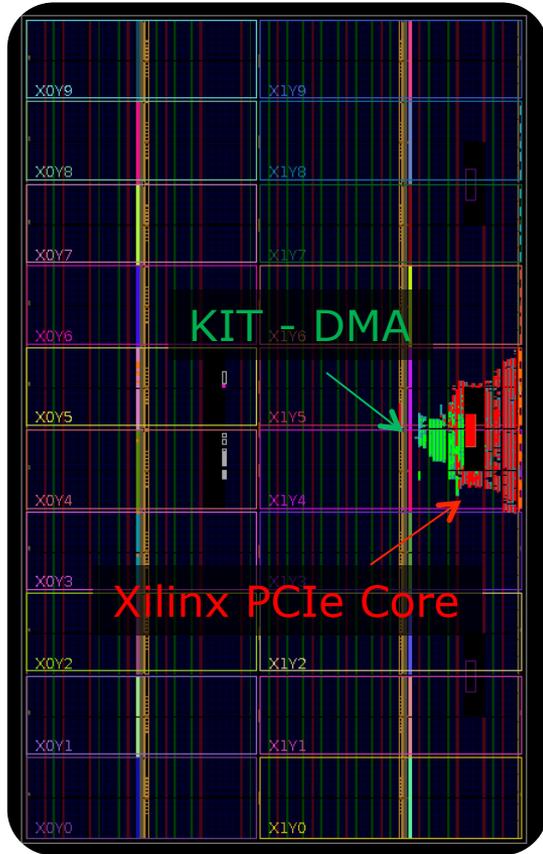
✓ Average data throughput of **3.5 GB/s** (DMA max data transfer @ 4 GB/s).

✓ No bit errors observed (tested up to several TB of data exchanged)

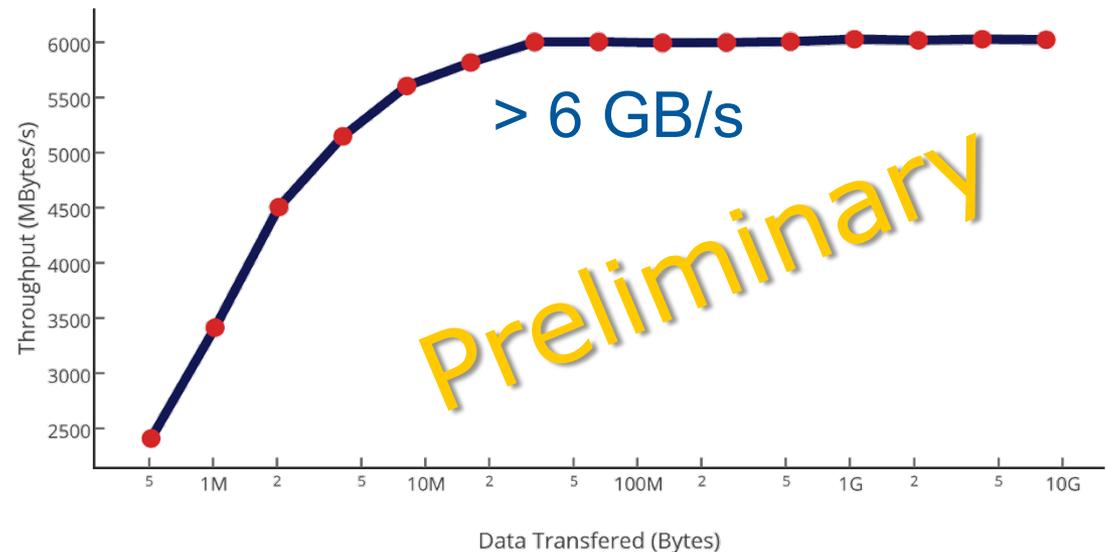
# PCIe-DMA for generation 3

Preliminary results of a DMA – PCIe based on **GEN 3 x8 lanes**

Virtex 7 -> XC7VX690T -2



IPE-DMA for PCIe Gen3 - Memory Write Performance



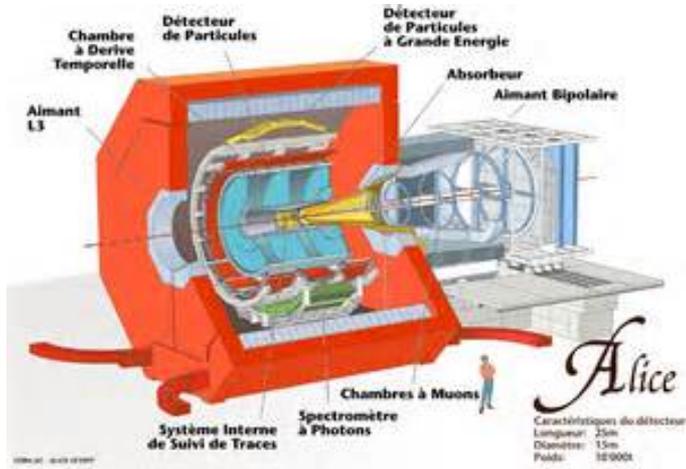
No optimized firmware and driver

Low occupancy

NO errors → detected during the data transferred

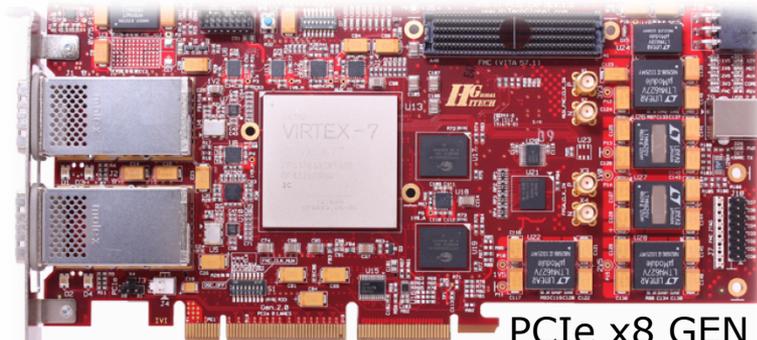
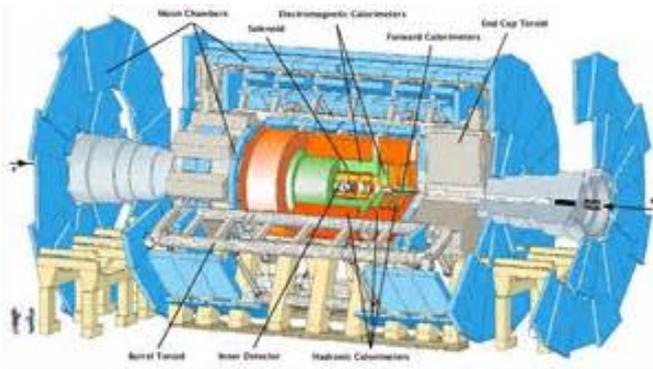
# KIT-DMA for High Energy Physics DAQ

## Alice DAQ



ALICE C-RORC → RobinNP

## ATLAS DAQ



ATLAS – FELIX (FE Link eXchange)

*Are interested in KIT-DMA for HL-LHC upgrade*

# Conclusions

- ❑ Kapture → proper instrumentation for picosecond diagnostic beam and CSR studies.
  - ❑ Thanks to Kapture → published more than 20 scientific papers on CSR studies for future accelerators
  - ❑ Synchrotron community is interested in Kapture
- ❑ New DMA-PCIe Readout compatible with GPU Direct access
  - ❑ HEB community interested at KIT-DMA logic
- ❑ Future Kapture → based on SiGe or different monolithic integrated circuits

*Thank you for your attention*