Prototype active silicon sensor in LFoundry 150nm HV/HR-CMOS technology for ATLAS Inner Detector Upgrade

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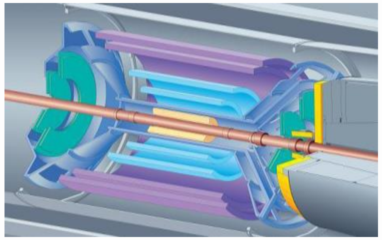
Outline

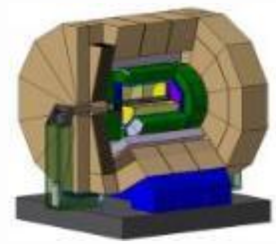
- Introduction
- Description of the design
- Measurement results
- Next prototypes
- Summary

Requirements for pixel layers

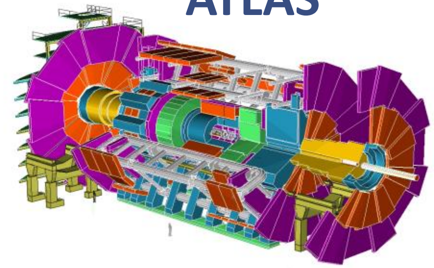
ALICE-LHC



ILC



ATLAS



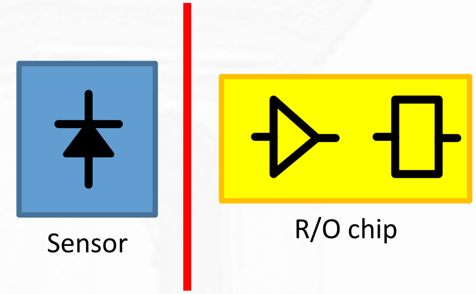
	ALICE-LHC	ILC	ATLAS-LHC	ATLAS-HL-LHC	
				Outer	Inner
Timing [ns]	20 000	350	25	25	25
Particle rate [kHz/mm²]	10	250	1000	1000	10000
Fluence [n_{eq}/cm²]	> 10^{13}	10^{12}	2×10^{15}	10^{15}	2×10^{16}
Ion. Dose [Mrad]	0.7	0.4	80	50	>500

Monolithic CMOS (ALICE-LHC, ILC) **Not decided** (ATLAS-LHC, ATLAS-HL-LHC)

CMOS Demonstrator Program

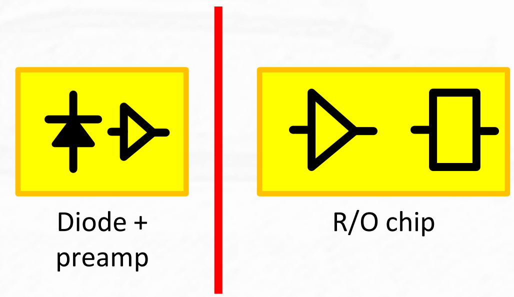
Passive CMOS sensor + R/O chip

- Study charge collection
- Passive sensor for hybrid detector
- Possible cost advantage if performance is the same as traditional sensor



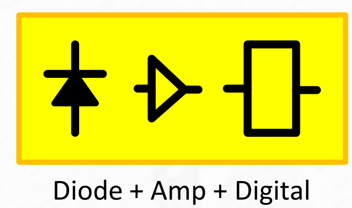
Active CMOS sensor + R/O chip

- CCPD hybrid detector
- Possible on-sensor functionality like subpixel encoding

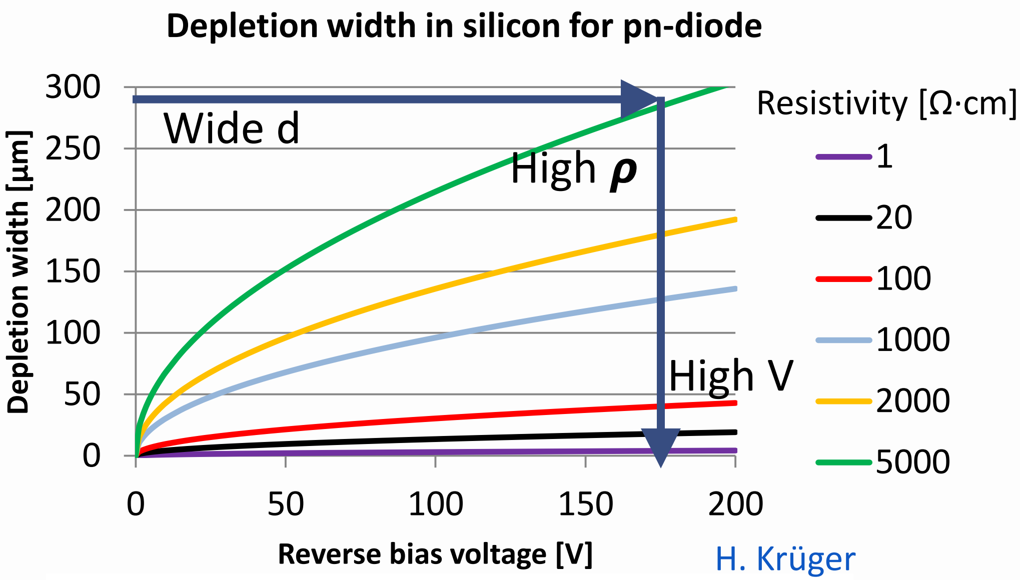


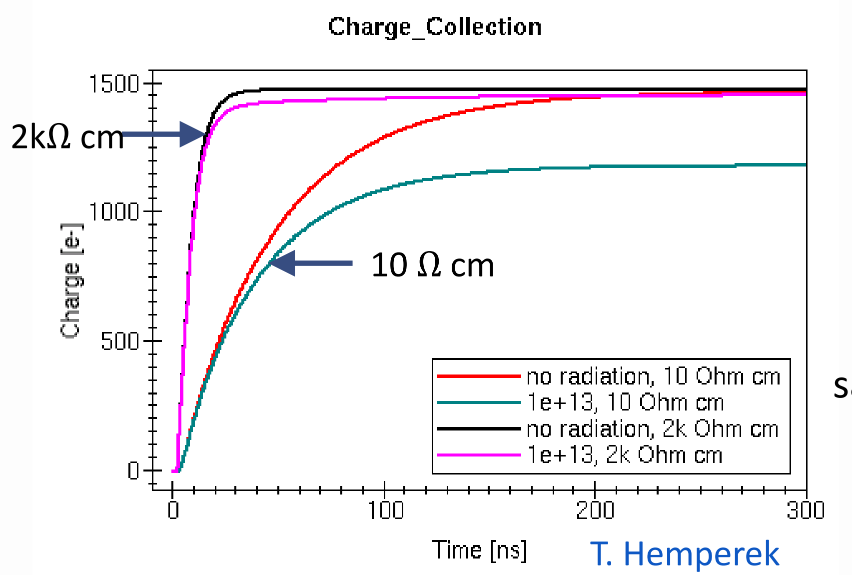
Active CMOS sensor with standalone R/O

- DMAPS – Depleted Monolithic Active Pixel Sensor
- Significant cost reduction
- Suitable for outer layers



Depletion depth





ATLAS requires fast and radiation tolerant sensor with good SNR, which makes wide depletion zone desirable.

Depletion width **d** $\propto \sqrt{\boldsymbol{U_{bias} \cdot \rho_{substrate}}}$

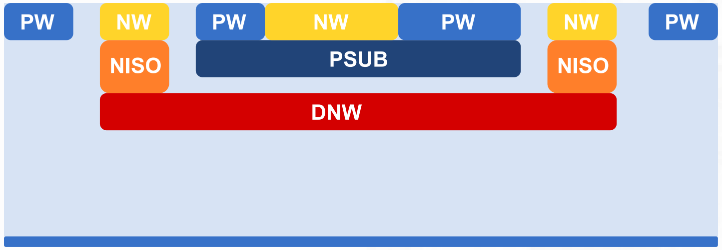
- $Q_{collected} \propto d$
- $C_{det} \propto \frac{1}{d}$ (important for CSA)
- Wider depletion zone → more drift, less diffusion

TCAD simulation assuming the same bias voltage and 20µm of Si.

Technology and designed sensors

LFoundry CMOS3E:

- 150nm CMOS
- 2kΩcm p-type bulk
- Deep NWell available
- HV process
- Thinning and back size metallization possible



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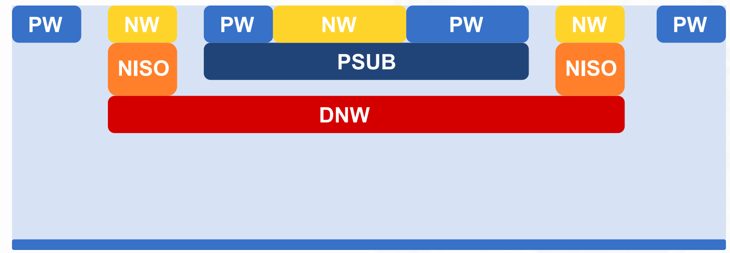
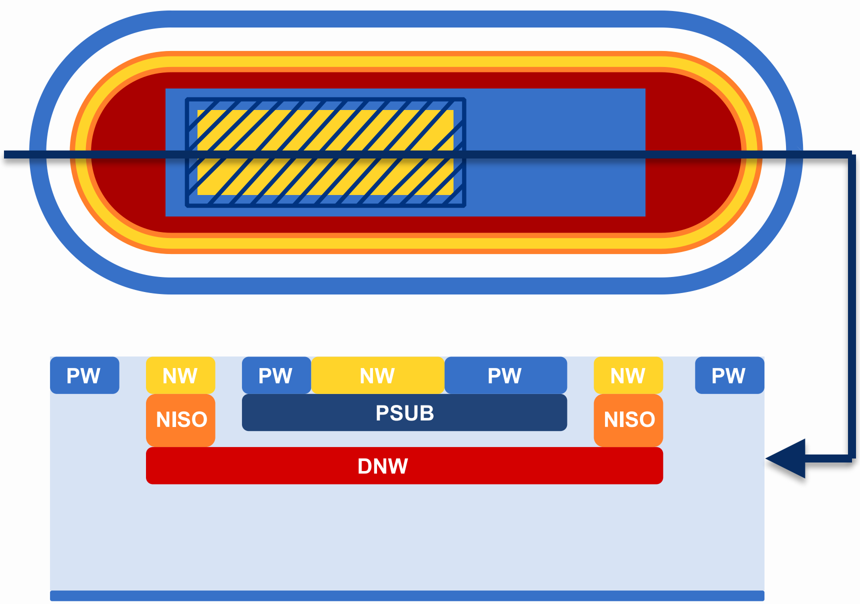


Sensors:

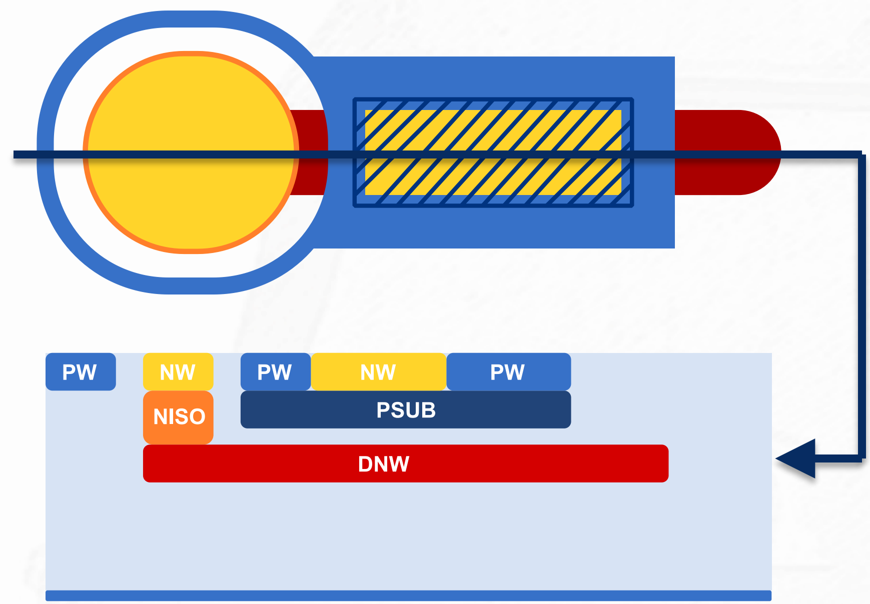
Version A

Larger fill factor , larger sensor capacitance



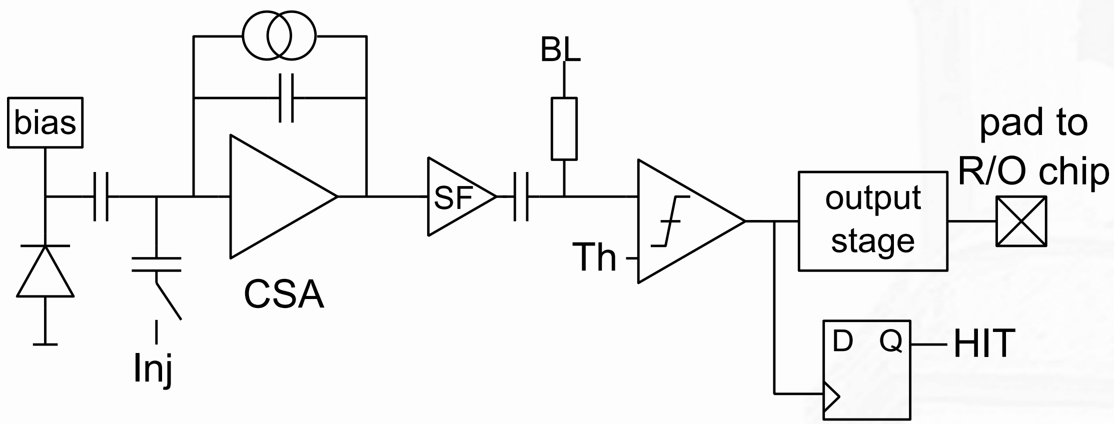
Version B

Smaller fill factor , smaller sensor capacitance



In-pixel electronics

- All pixels have the same electronics
- Pixels can be tuned using:
  - Local DAC for Th
  - Global DACs and bias voltages (CSA current, comparator current, output signal amplitude, etc.)



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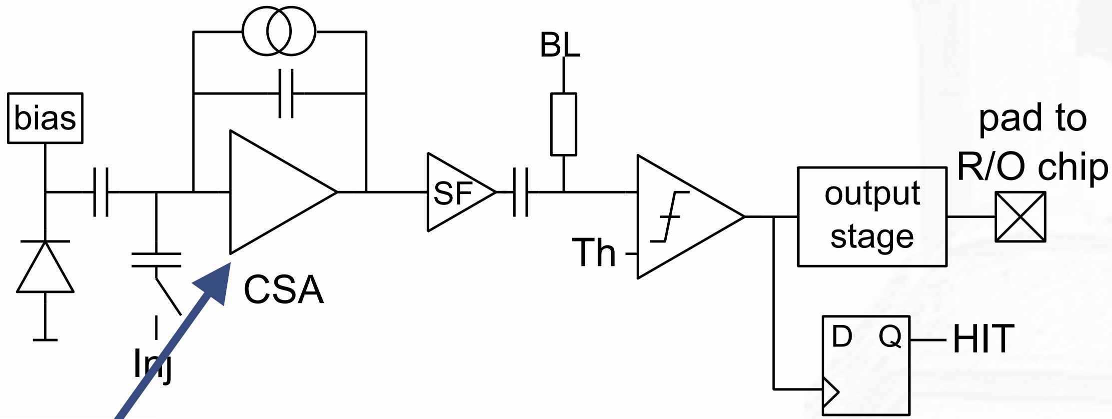
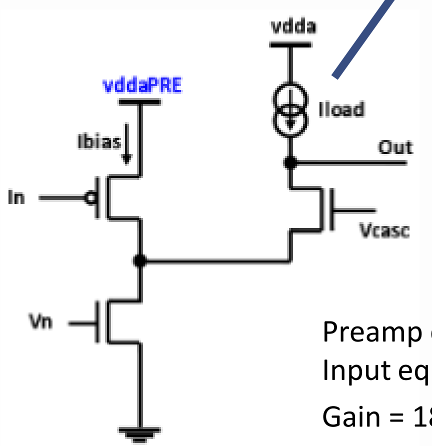
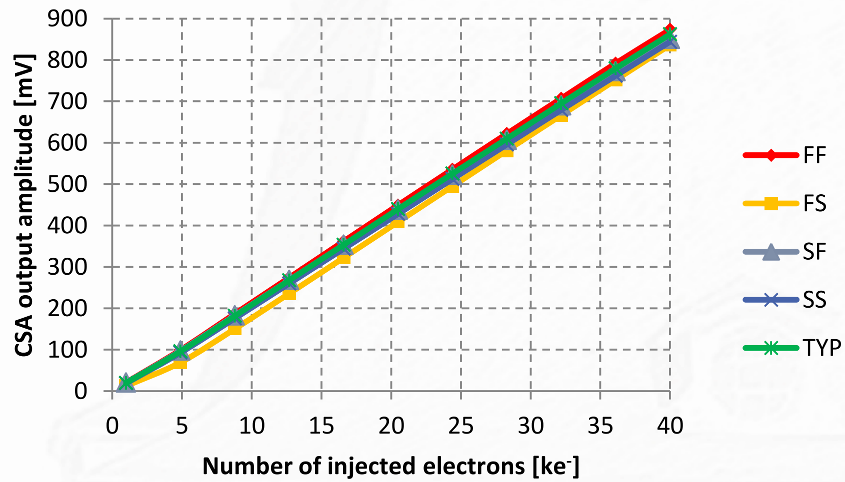




Preamp current = 10µA
Input equivalent noise = 124 e^-
Gain = 18 $\frac{\mu V}{e^-}$
T_{peak} (for 4ke^-) = 31.2 ns



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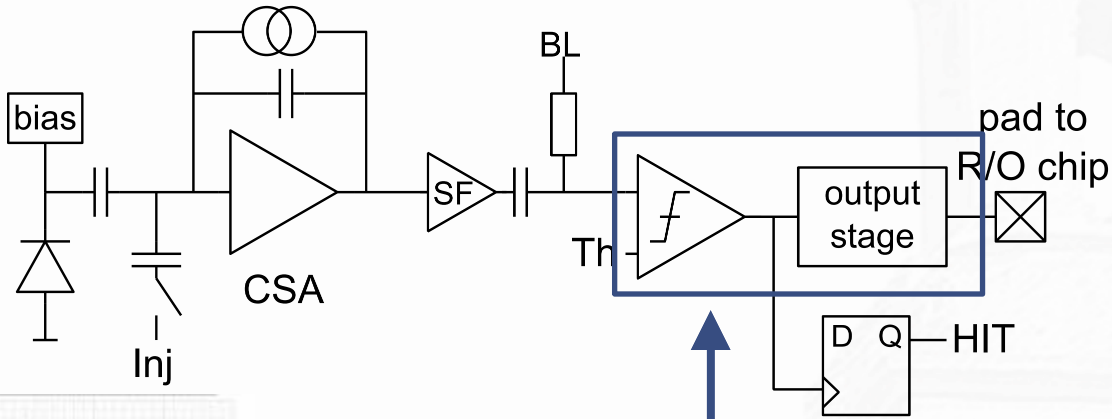
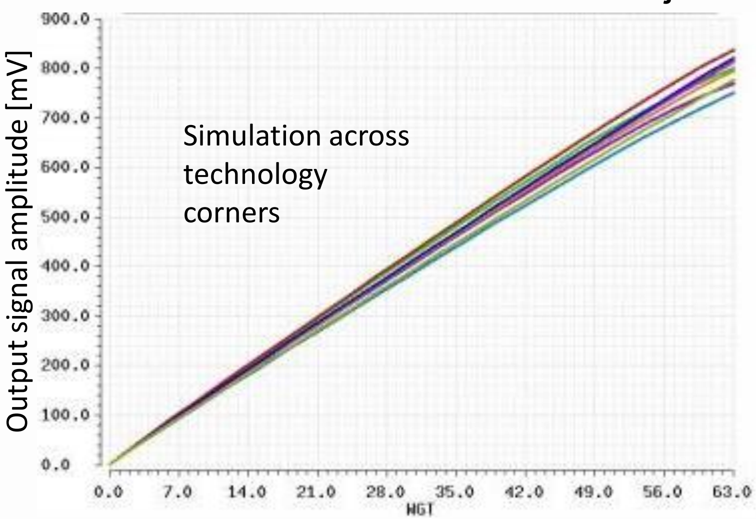
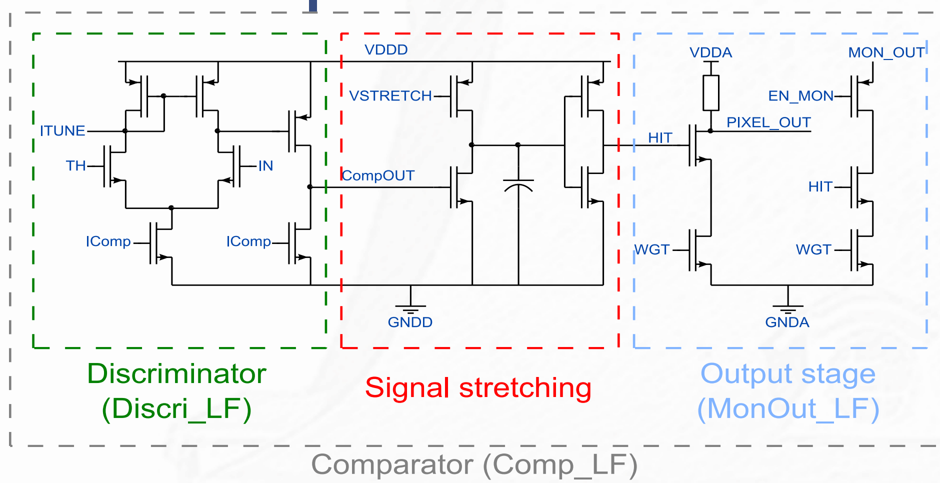
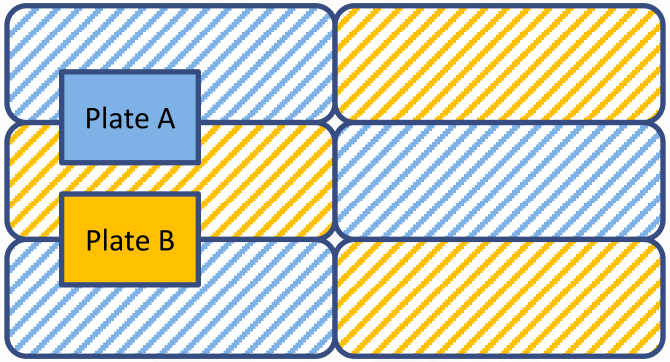






Pixel matrix

- Pixel size is 33µm × 125µm (FEI4 pixels are 50µm × 250µm)
- Pixels organised into groups of 6
- Each group is connected to 2 pixels of FEI4
- Distinction between pixels in group through amplitudes of output signals



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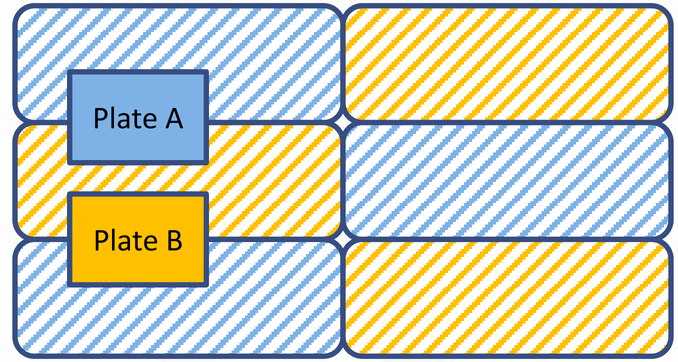
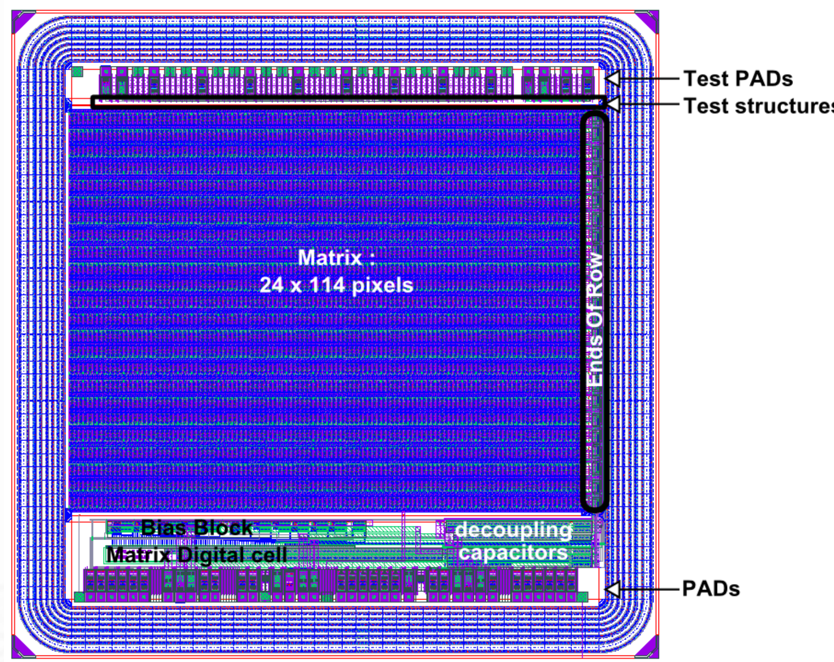
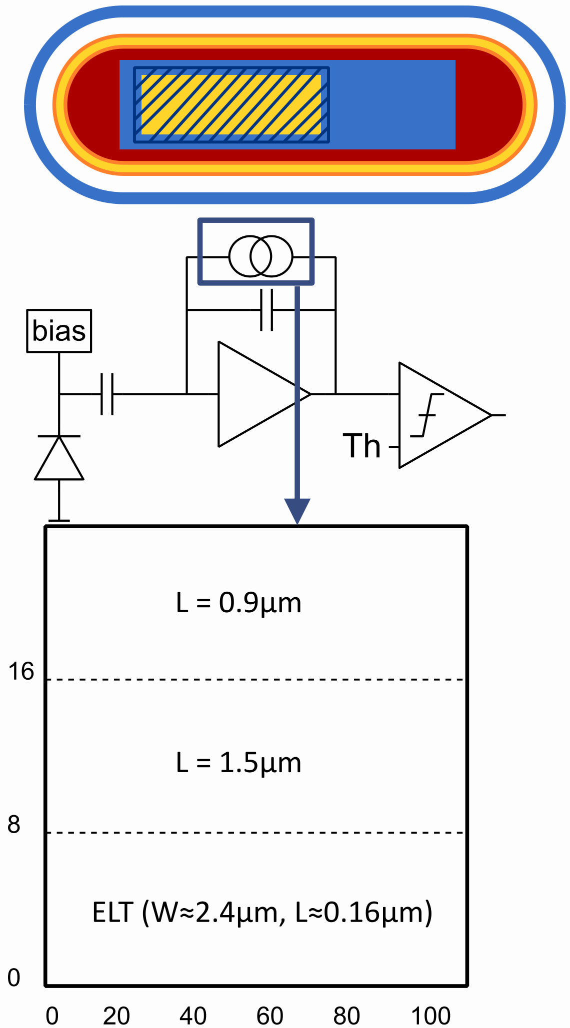


- Chip size is 5mm × 5mm
- Configuration of global DACs and pixels done via shift register
- Pixels can be readout with R/O chip or standalone using the shift register
- Output of each pixel's CSA and comparator can be monitored (one pixel at a time)
- Two chip versions (one for each sensor type) with different flavours of pixels
- Submitted in September 2014

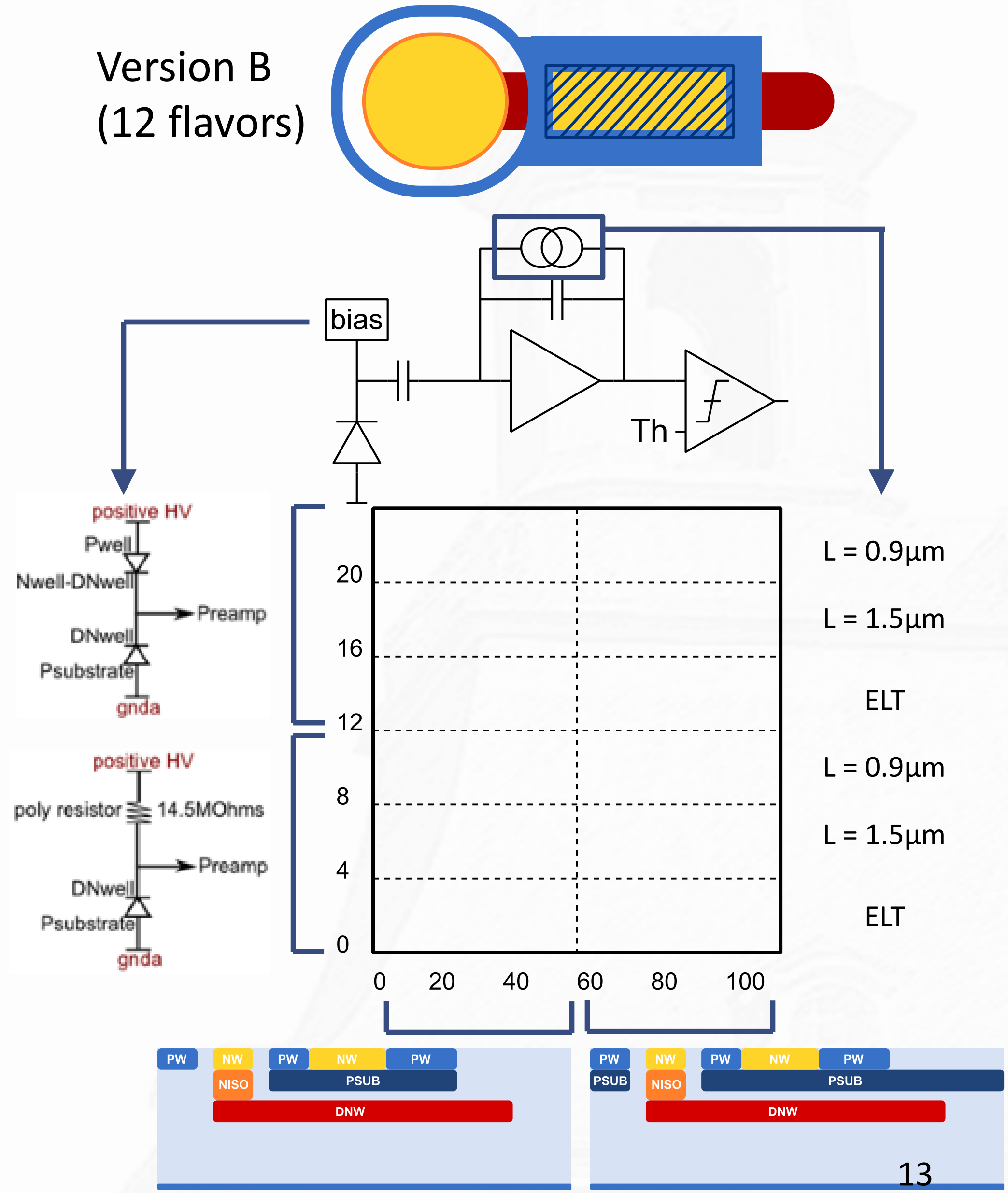


Pixel matrix – versions A and B

Version A
(3 flavors)

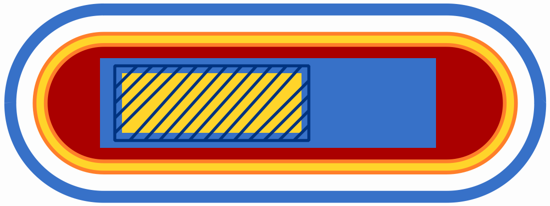


Version B
(12 flavors)

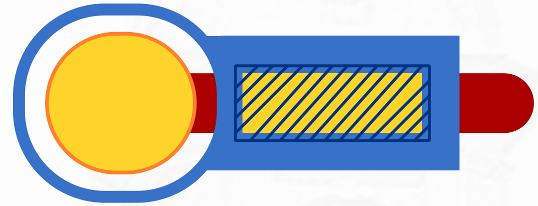


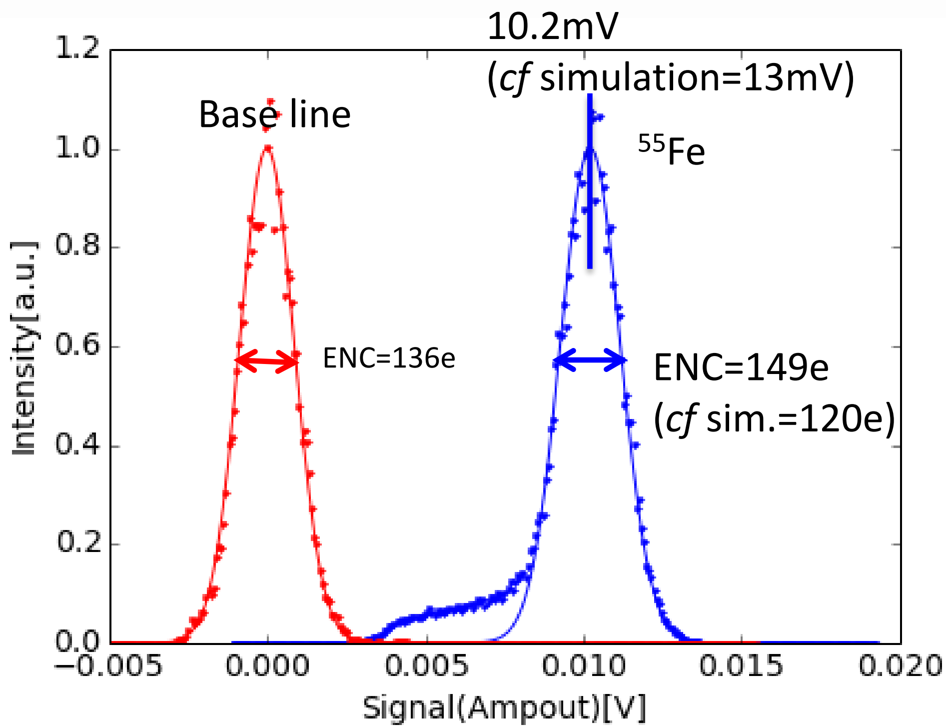
Single pixel gain and noise

Version A
- Bias: -111.8V
- Source: ^{55}Fe



Version B
- Bias:20V
- Source: ^{55}Fe





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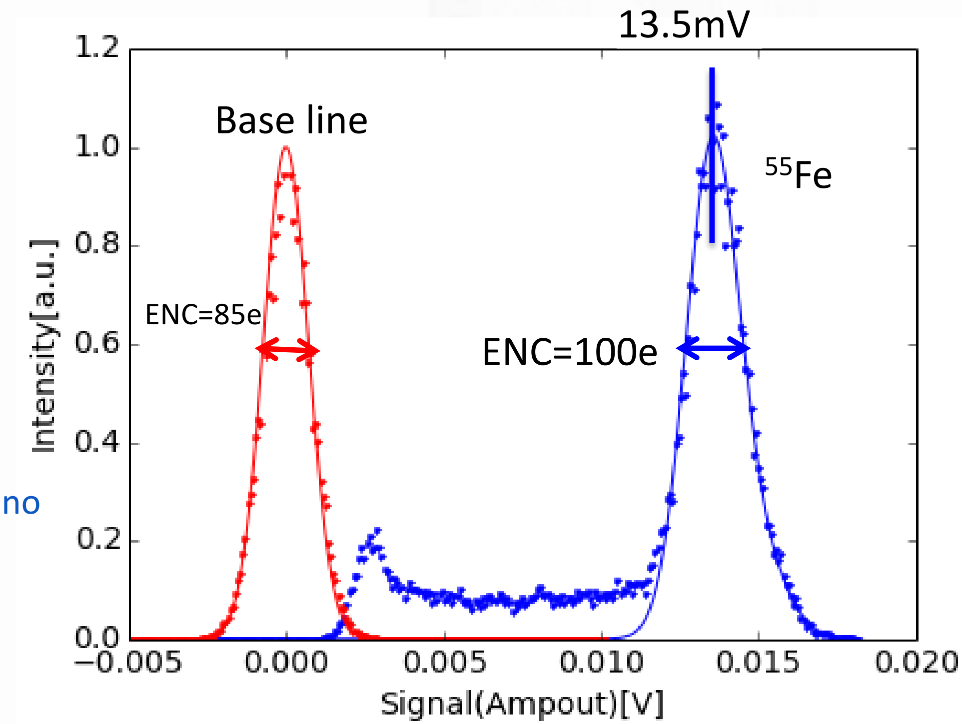
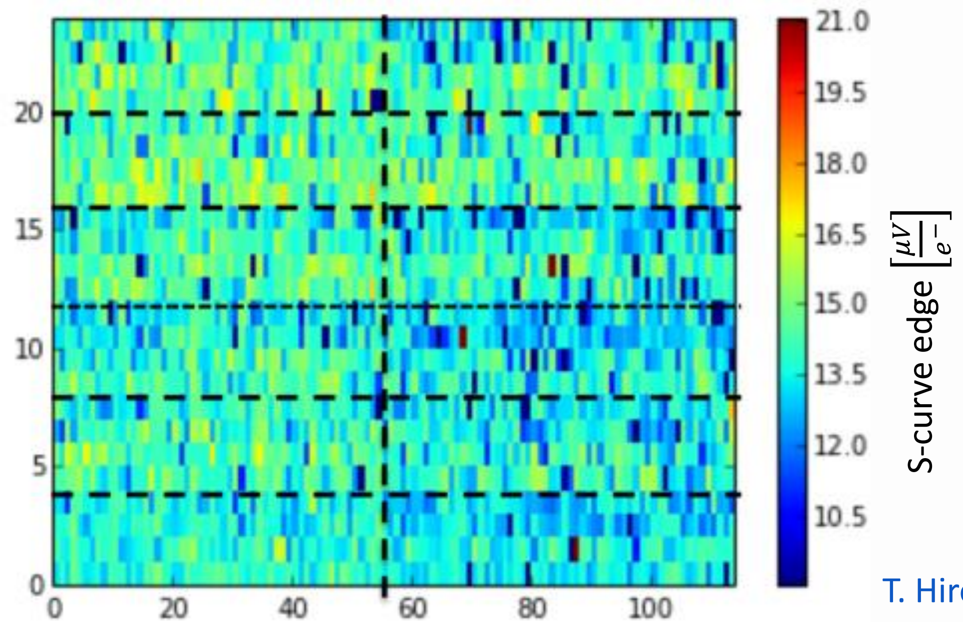


Noise and gain were comparable with the simulation results.

Gain and noise maps of version B

- Measured with pulse injection (250 mV ≈ 3000 e^-)
- No significant difference between flavors in terms of gain
- Pixels with resistor bias are noisier (before irradiation)



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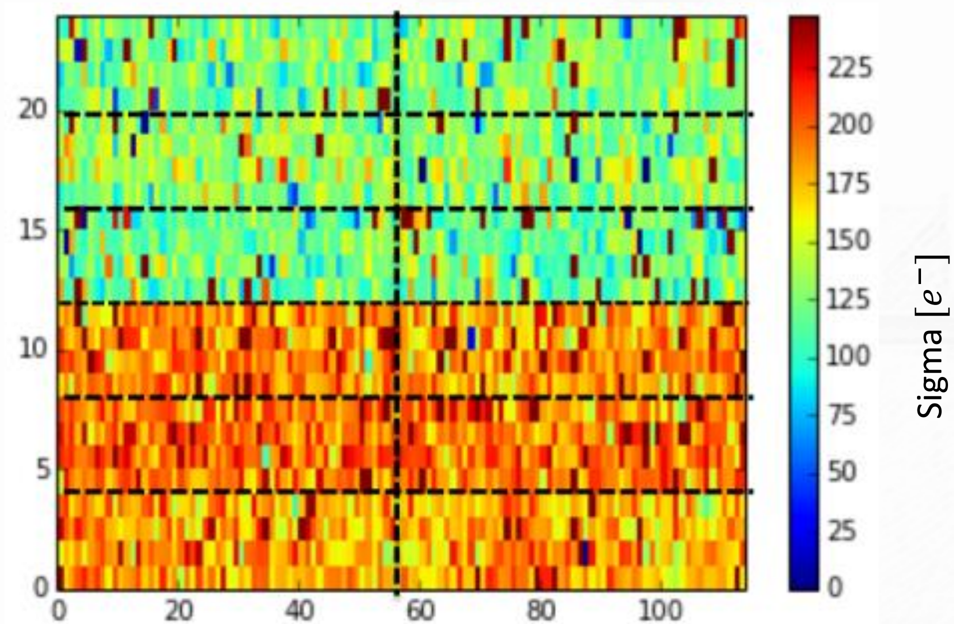
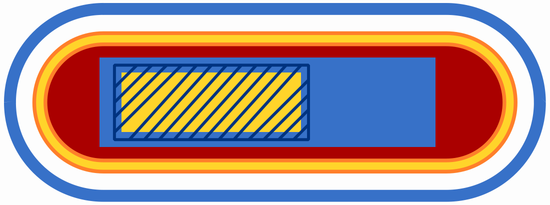


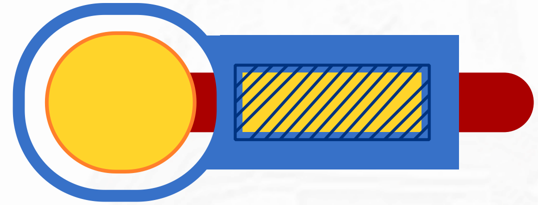
Charge spectra (3.2 GeV e^- beam)

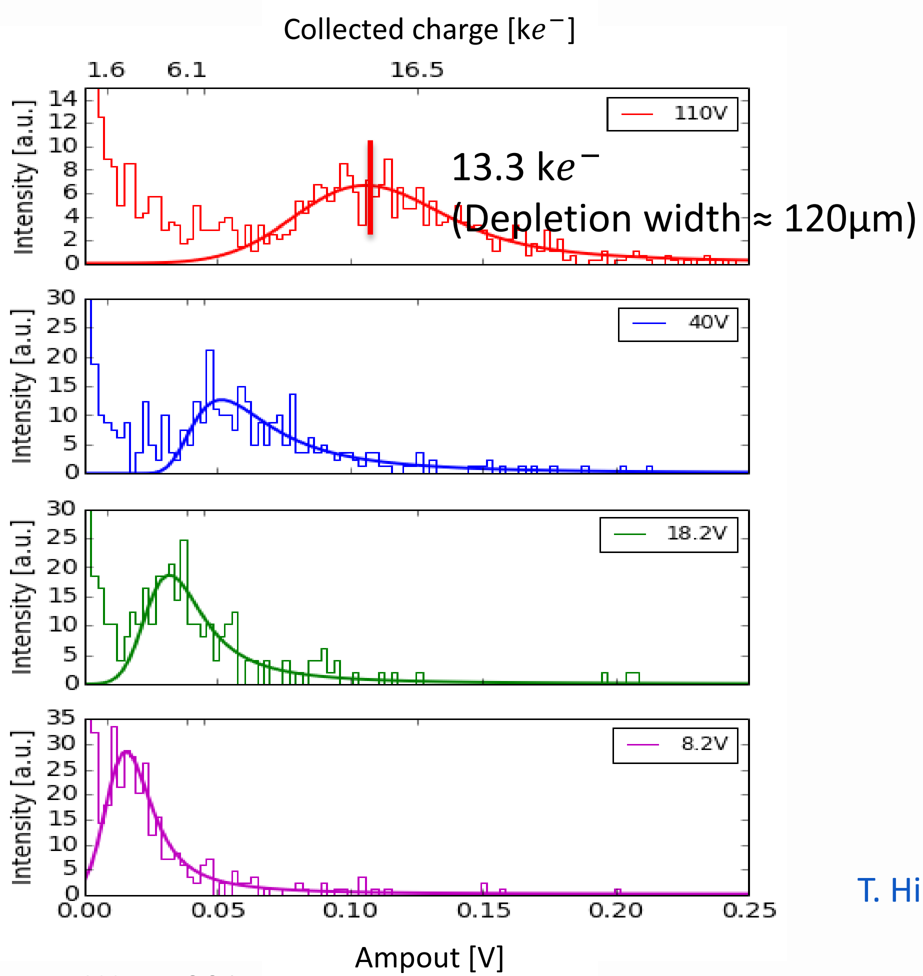
universitätbonn

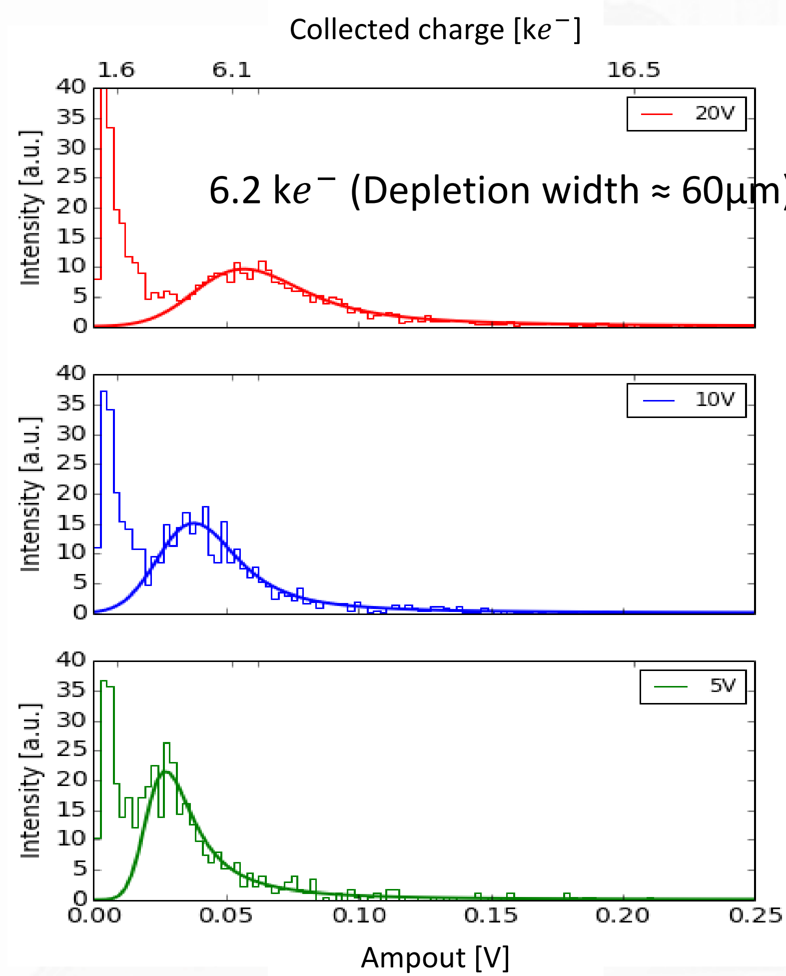
Version A



Version B







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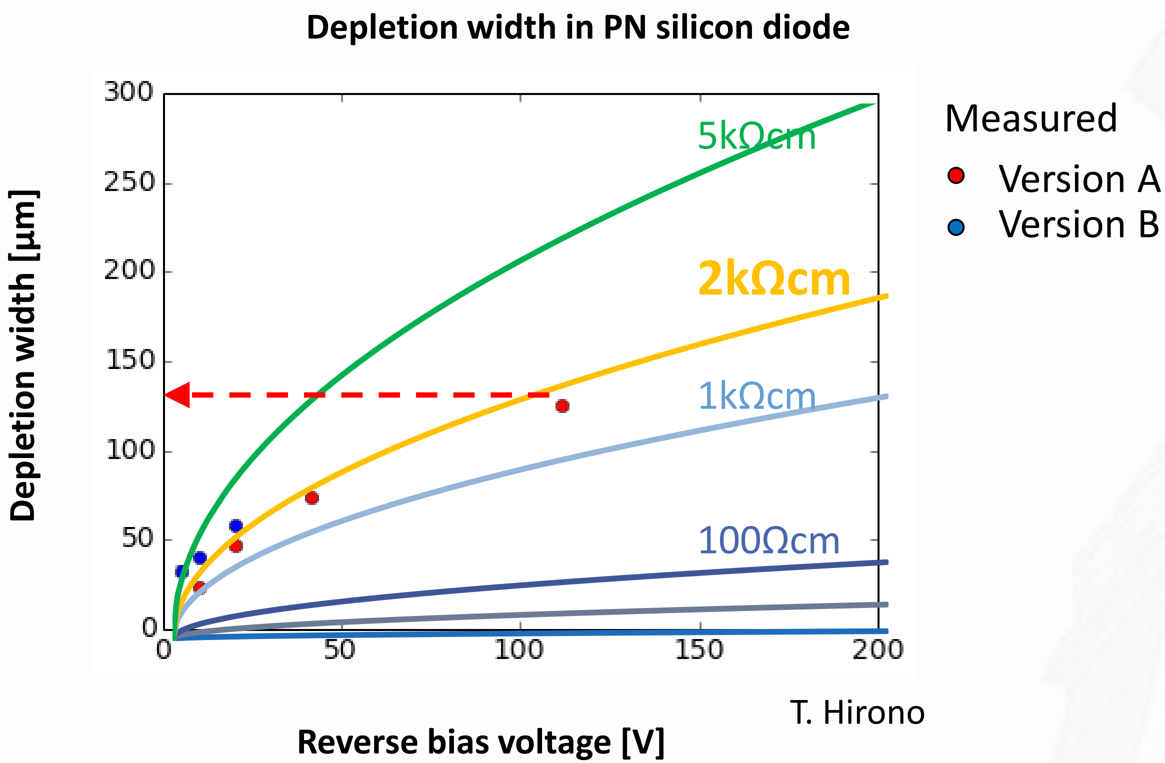
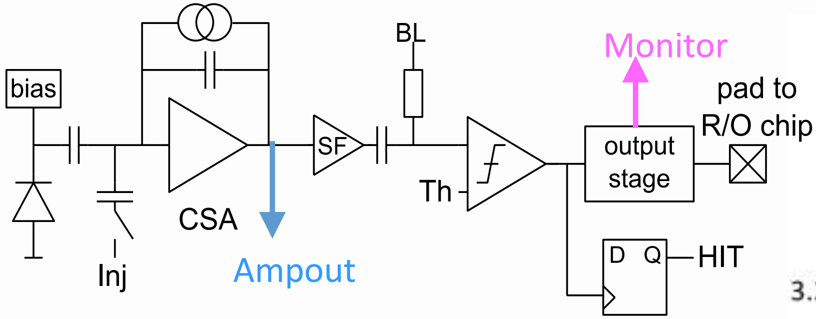
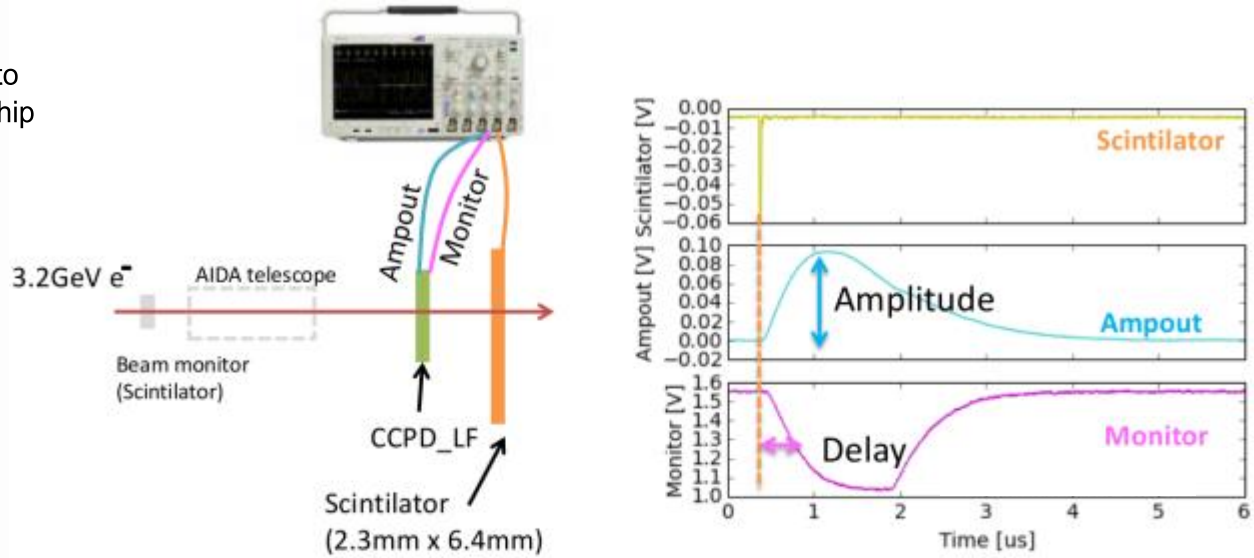
Depletion width



- Version A matched to the calculation of a simple p-n silicon diode of 2kΩ cm
- Depletion of Version B behaves differently because of its complex structure

Time walk measurement





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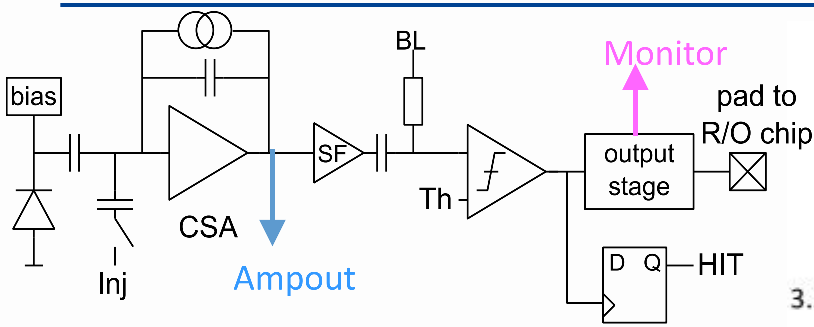
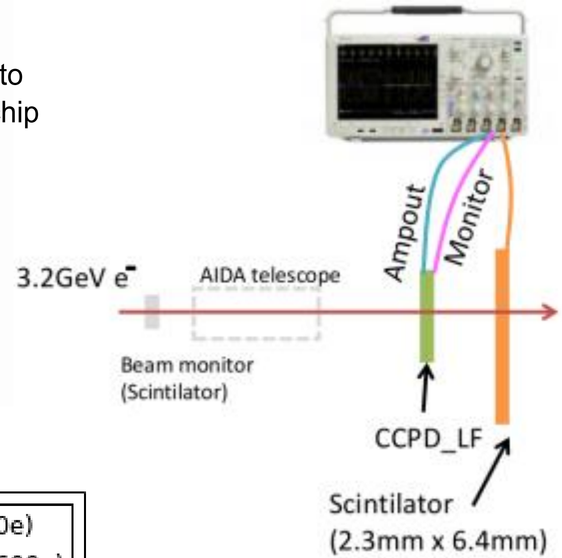
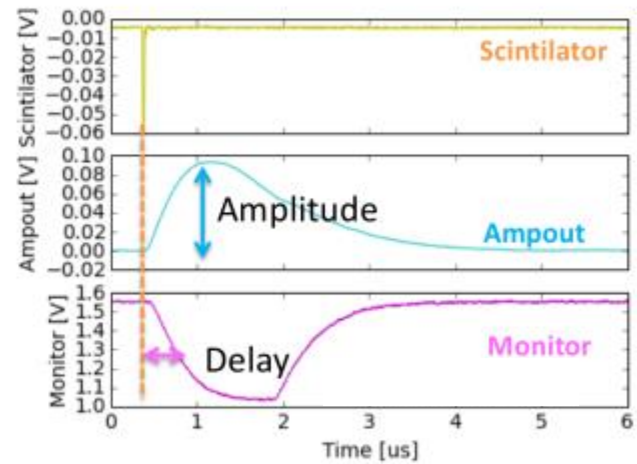
- Time walk of version B was measured using 3.2 GeV electrons

Time walk measurement







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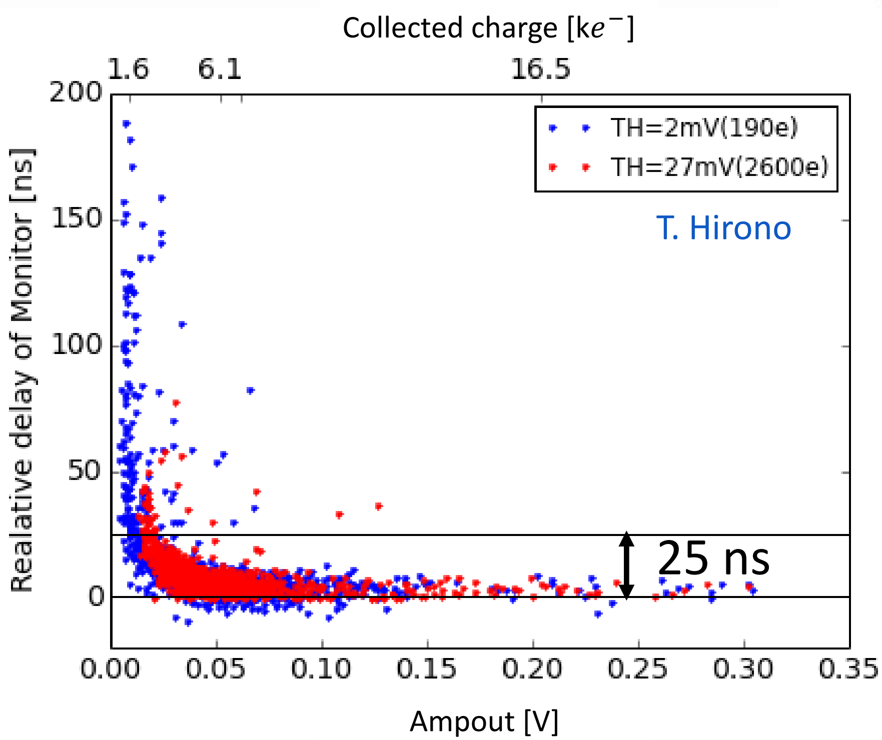
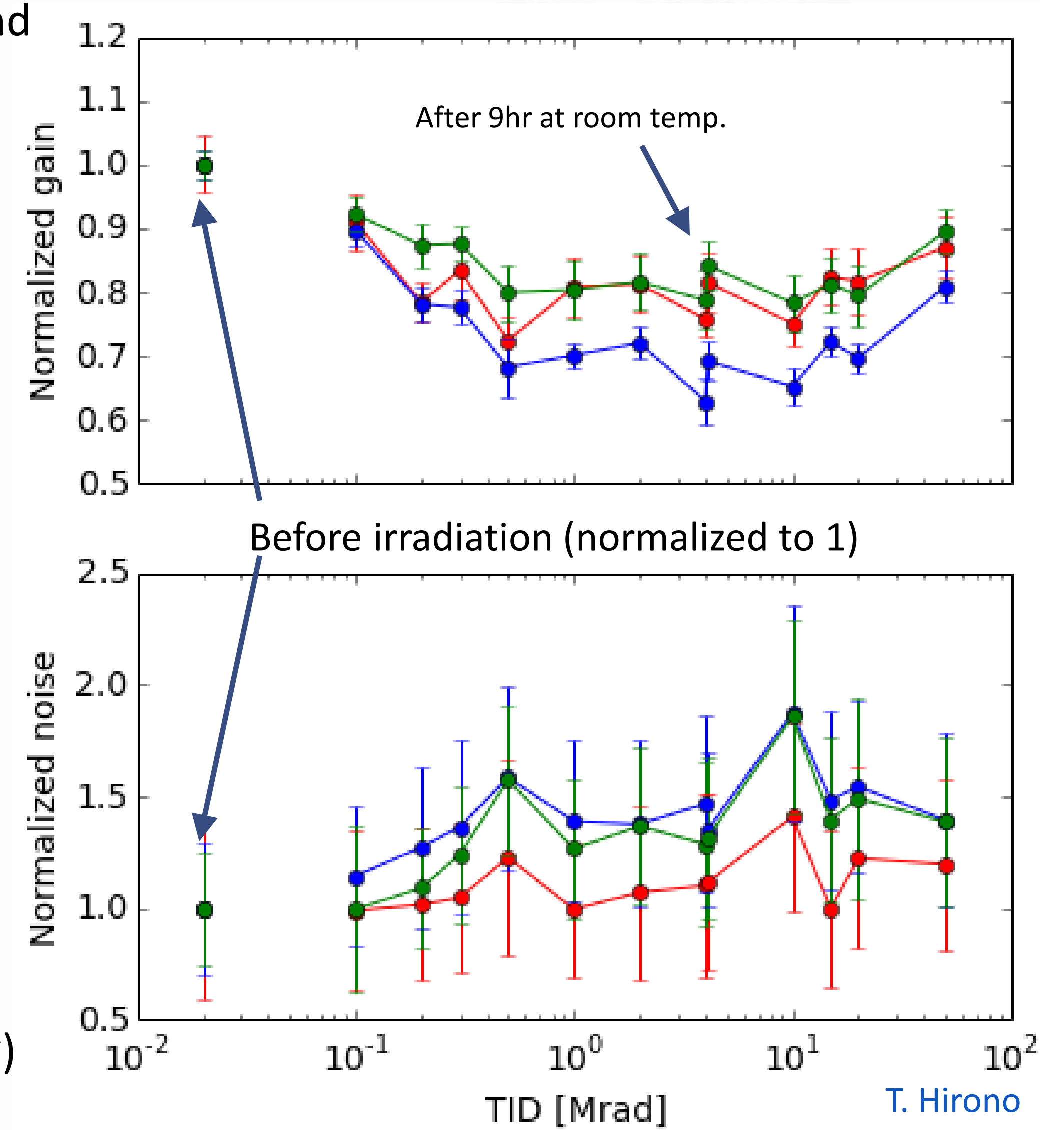


- Time walk of version B was measured using 3.2 GeV electrons
- Fraction of "in-time (25ns)" hits
  - Low threshold : 79%
  - High threshold : 91%
- Needs to be improved in next prototype

Radiation tolerance (TID)

- Gain and noise of readout measured before and after X-ray (~60keV) irradiation
- TID: 50Mrad (outer layer of ATLAS-HL-LHC)
- Flavors of CSA feedback (version A)
  - Normal (L=0.9µm)
  - Long (L=1.5µm)
  - ELT (W≈2.4µm, L≈0.16µm)
- Readout works after irradiation
  - Gain degraded to 70-80%
  - Approx. twice larger noise
- No significant differences between flavors
- More irradiation studies are coming (24GeV p^+)



Next prototypes

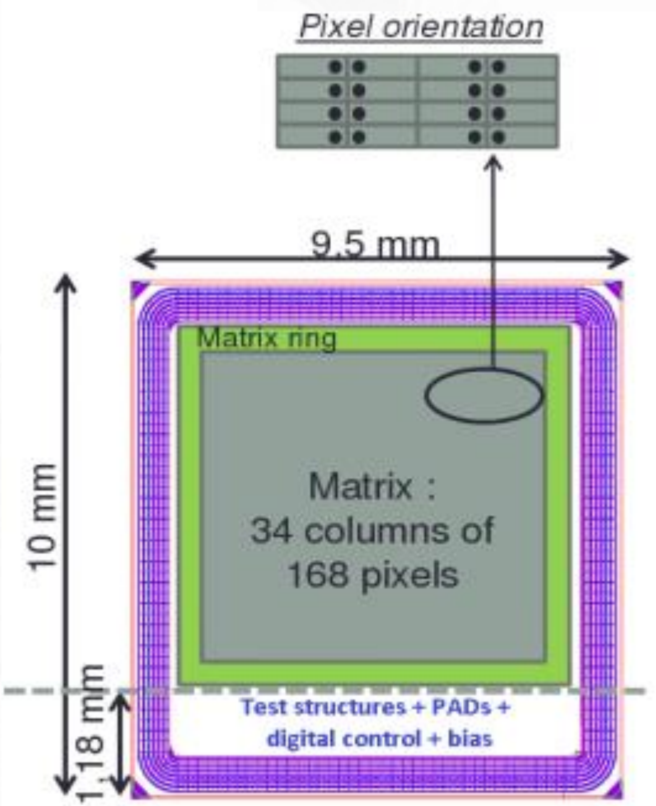
Two more prototypes based on experience gained with CCPD-LF are planned:

- LF-CPIX – an improved version of CCPD-LF
- Fully monolithic design

LF-CPIX

Project's overview:

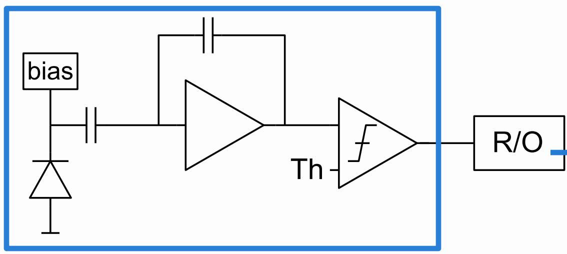
- Common design effort: CEA/IRFU, CPPM, University of Bonn
- Pixel size of 50µm × 250µm (no subpixel encoding)
- Matrix composed out of few different pixel types (complying with CMOS Demonstrator guidelines):
  - Passive pixels
  - "Analog-only" pixels (diode + front-end)
  - "Analog-digital" pixels (diode + front-end + comparator)
- Main improvements over the first prototype
  - New CSA (faster rise time)
  - Reduction of comparator's threshold dispersion
  - Reduction of parasitic coupling to sensitive nets
  - Optimization of sensor and guardrings layout



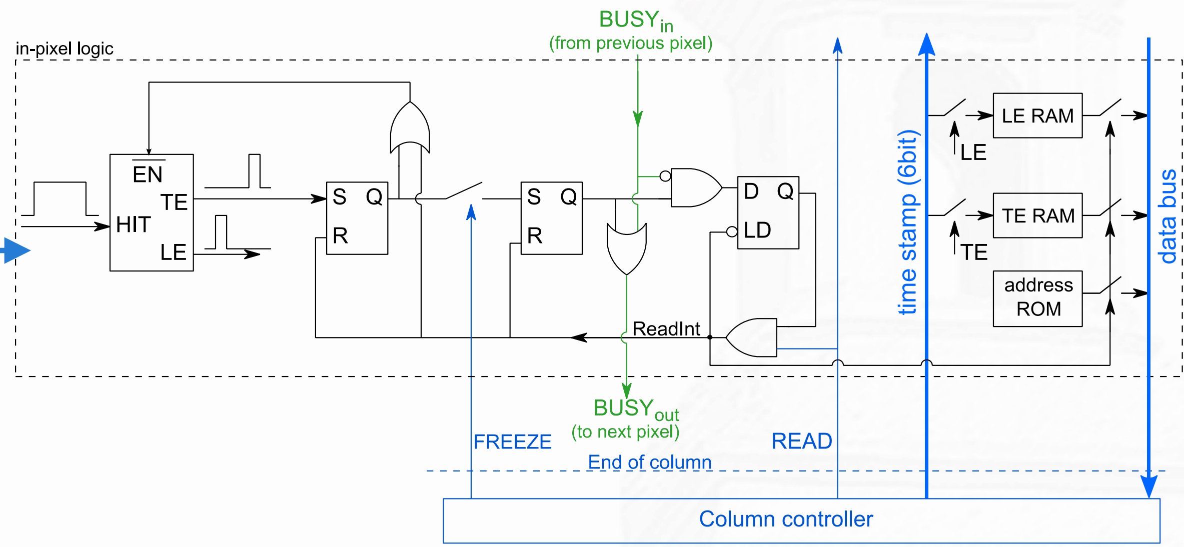
Preliminary chip layout plan

Monolithic design

- Aiming at ATLAS outer layers – moderate occupancy and radiation damage
- Combination of LF-CPIX sensor and analog FE with digital readout (column drain architecture, similar to FEI3)



Same as for CCPD-LF/LF-CPIX

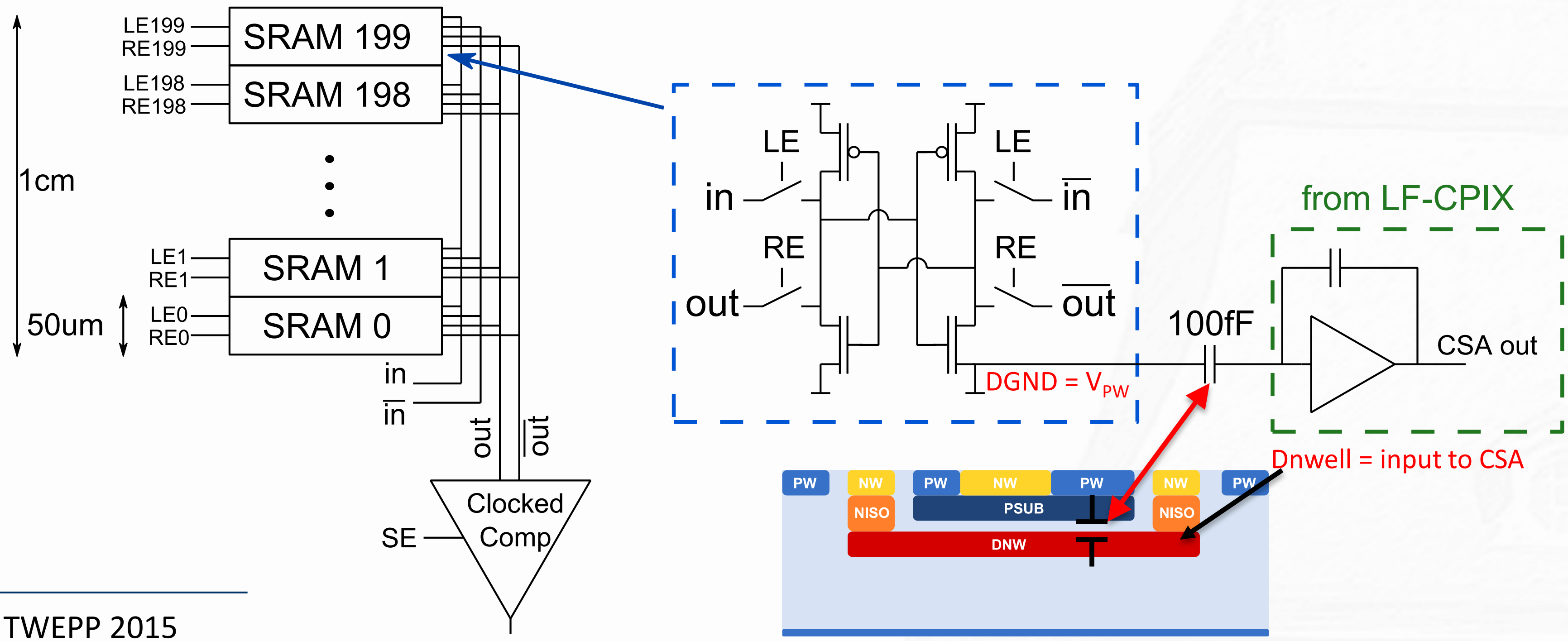


- Main challenge is keeping low noise operation while distributing, storing and reading time and token information along the column

Monolithic design

- Junction capacitance between charge collecting DNW and PWell of digital part O(100fF)

- Worst case scenario – PWell not isolated from DGND
  - $dV_{PW} = 1mV, C_{PW-DNW} = 100fF \rightarrow Q_{crosstalk} = 624e^{-}$



Monolithic design

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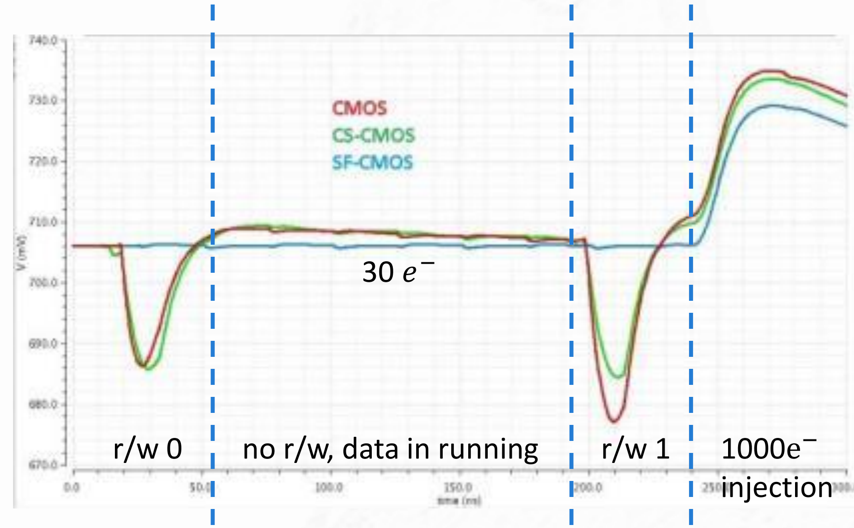
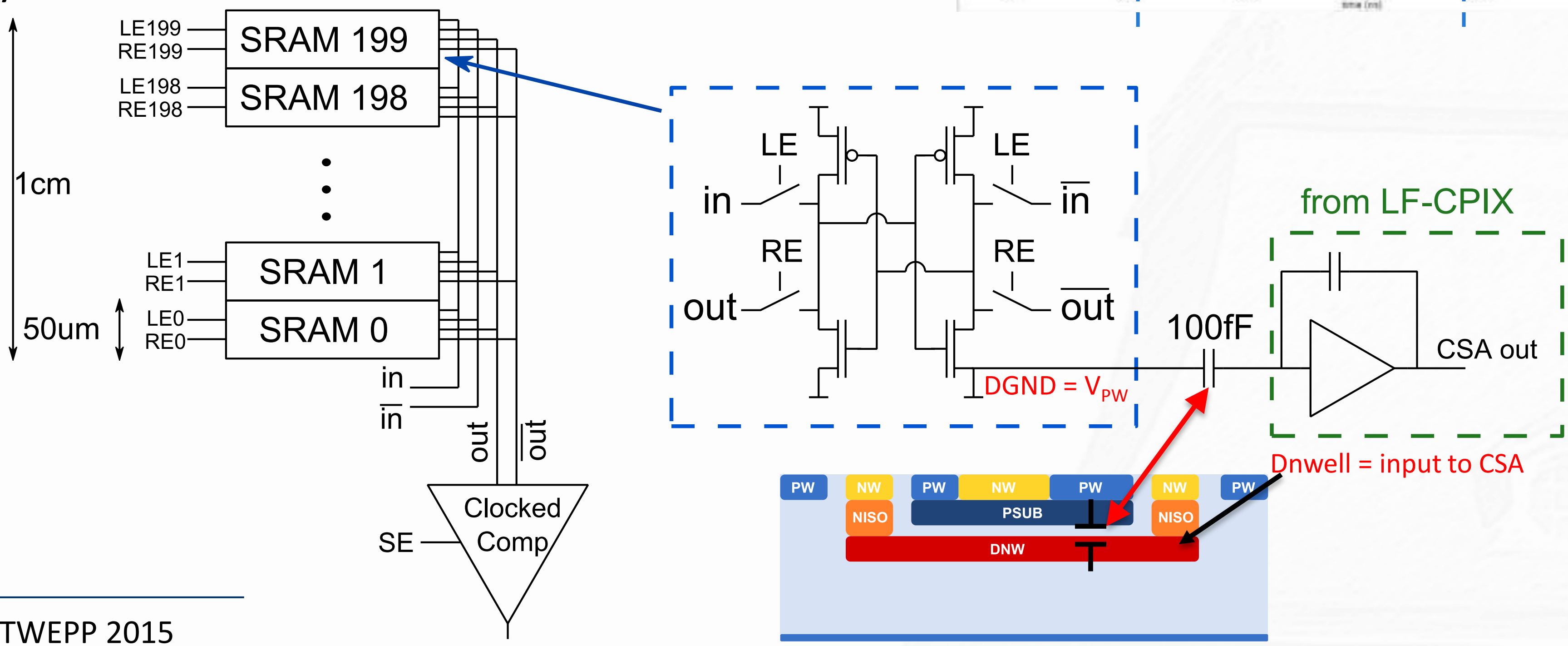
- Worst case scenario – PWell not isolated from DGND
  - $dV_{PW} = 1mV, C_{PW-DNW} = 100fF \rightarrow Q_{crosstalk} = 624e^-$
- Low noise circuits (e.g. CS-CMOS) and very careful layout needed





Summary

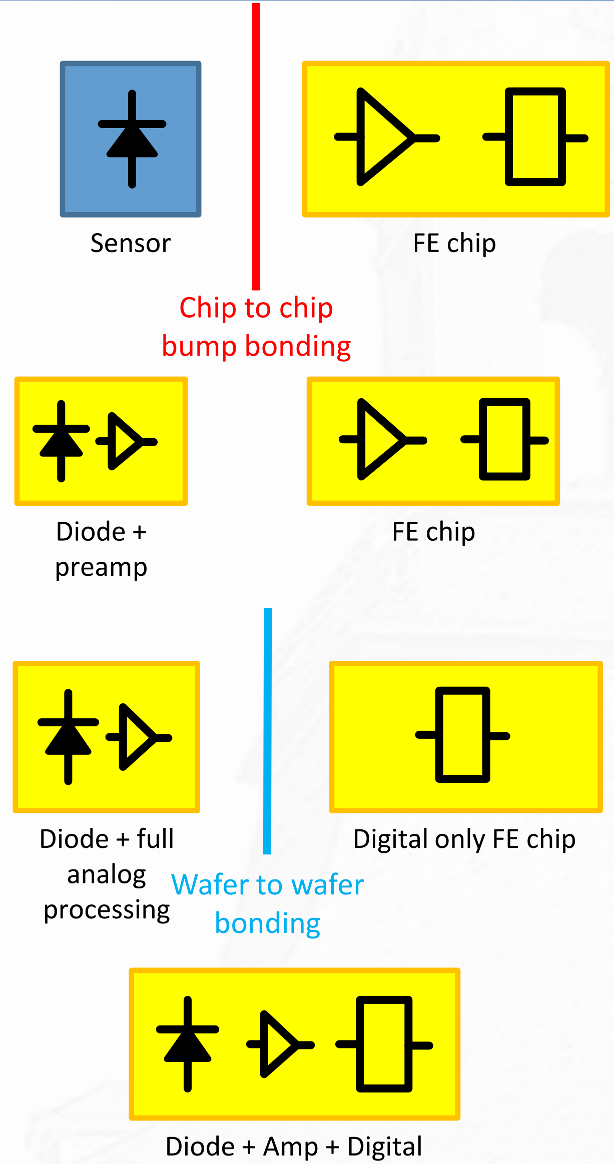
- A prototype CCPD was designed in LFoundry 150nm HV CMOS process and manufactured on a HR wafer
- Chip was tested and measurement results are in agreement with simulation predictions
- Radiation tolerance and readout with FEI4 tests are starting now
- Based on gained experience two more prototypes are being designed now:
  - LF-CPIX – an improved, larger version of CCPD-LF to be submitted in October 2015
  - Fully monolithic design – still in early stage, submission planned for the end of this year or beginning of next year

Thank you

Backup

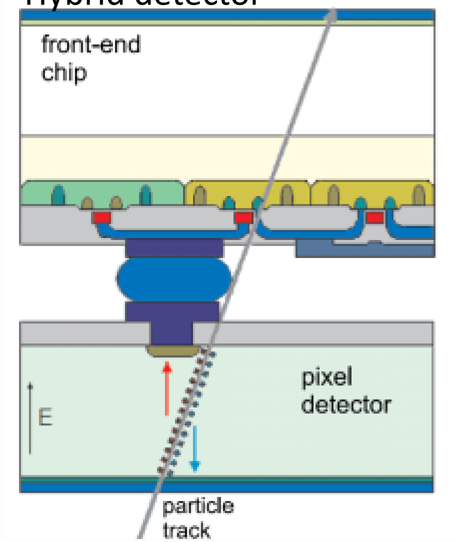
Concepts & classification of silicon detectors

- Standard Hybrid Pixels:
  - Planar or 3D sensor, fully depleted
  - Mixed signal r/o chip
- Hybrid Pixels with “smart” diodes:
  - HR- or HV-CMOS as a sensor (8”)
  - Standard r/o chip
  - CCPD (HVCMOS) with FE-I4
- CMOS Active Sensor + Digital R/O chip
  - HR- or HV-CMOS sensor + CSA (+Discriminator)
  - Dedicated “digital only” FE chip
- Monolithic Active Pixel Sensor (MAPS)
  - usually on epi substrate → diffusion signal, not suited for HL-LHC
  - HR- material (charge collection by drift) → fully Depleted MAPS (DMAPS)

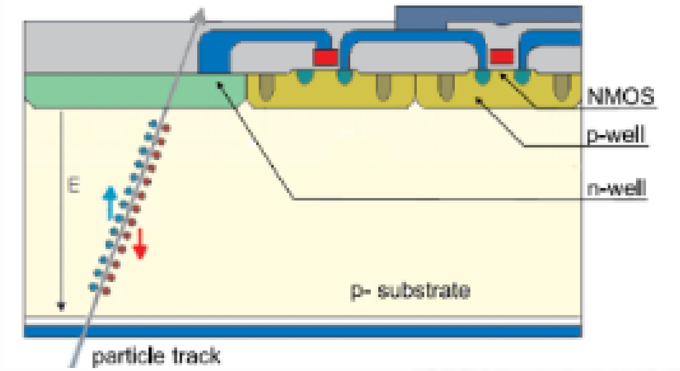


Particle detectors

Hybrid detector



Depleted Monolithic
Active Pixel Sensor

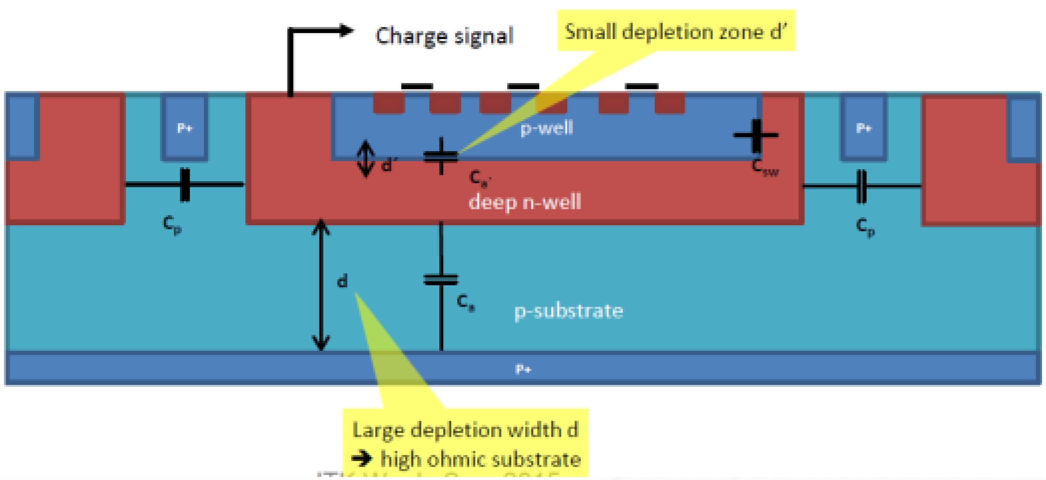


	Hybrid	Depleted Monolithic
charge collection time	fast (drift)	fast (drift)
cost	high	low
material	high	low
pixel size	medium	small
signal	high	high
possible readout complexity	high	low/medium

Pixel capacitance

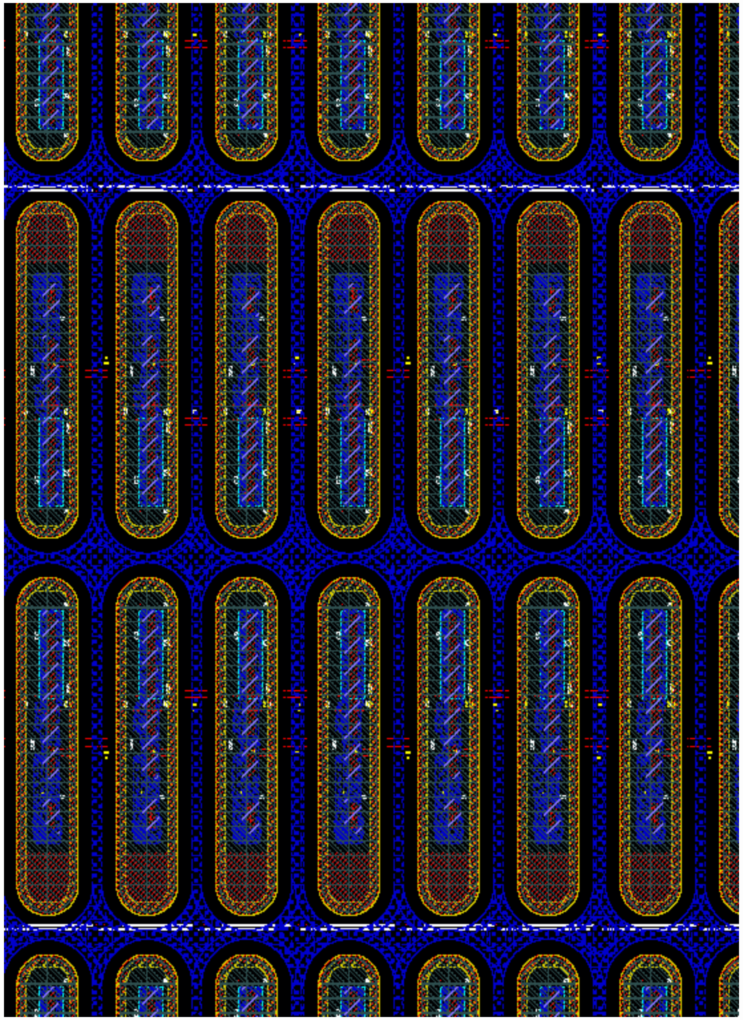
MAPS Pixel Capacitance

- Large fill factor MAPS total pixel capacitance Cd = Ca + Ca´ + Cp+Csw
  - Collecting node has a double junction
  - Capacitance to backplane $C_a \approx \varepsilon_r \frac{A}{d}$
  - Area capacitance between deep n-well and p-well Ca´ $\approx \varepsilon_r \frac{A'}{d'}$
  - Sidewall capacitance between deep n-well and p-well Csw
  - Capacitance to neighbor pixels C_p

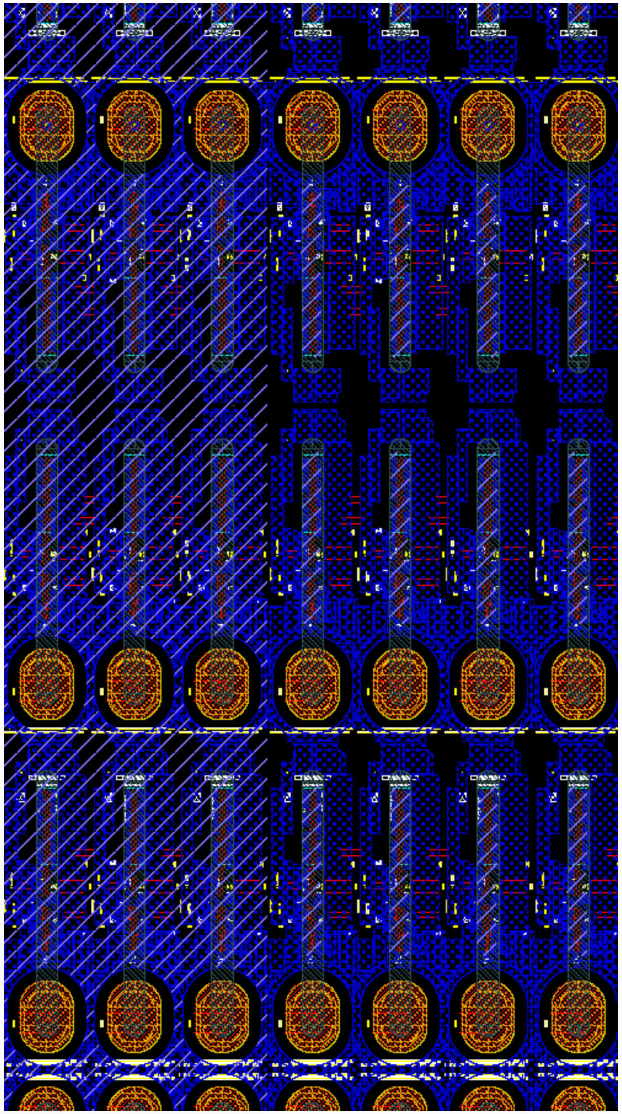


CCPD-LF matrix layout

Version A



Version B

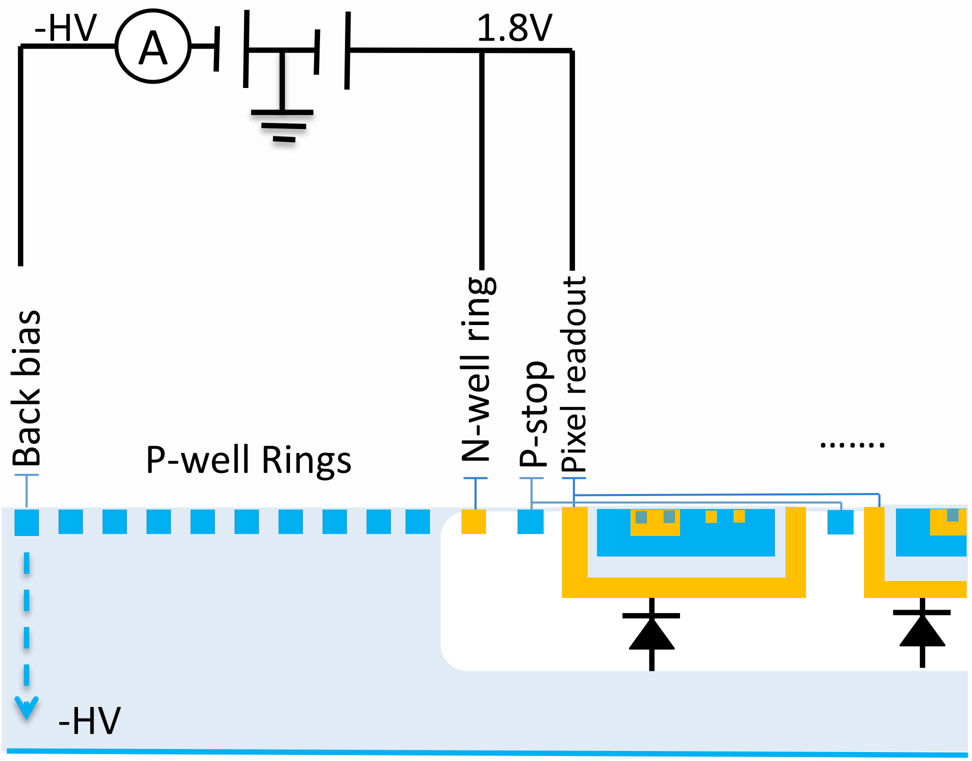


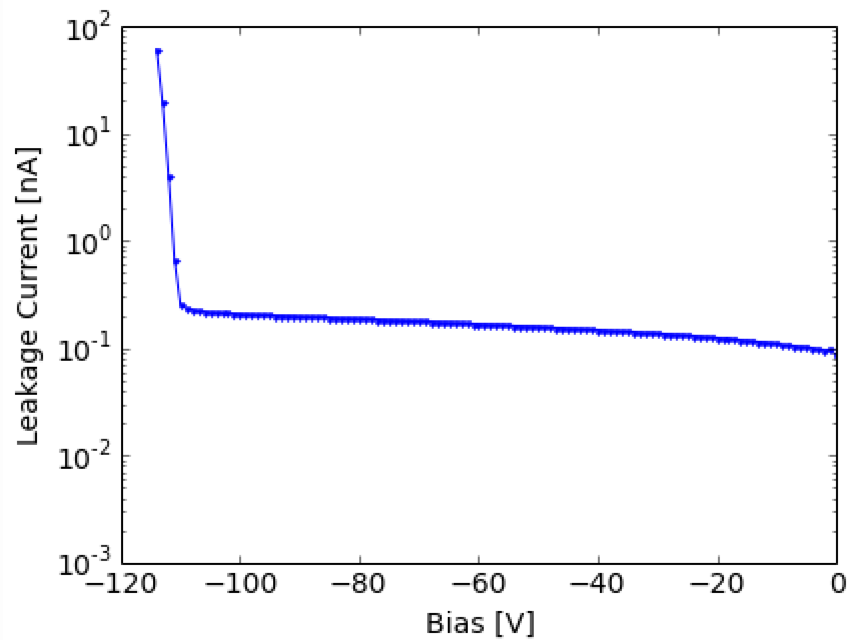
Measurement results – breakdown voltage

- IV curves (Version A)

  1.8V on collection well

  negative high voltage on "Back bias"



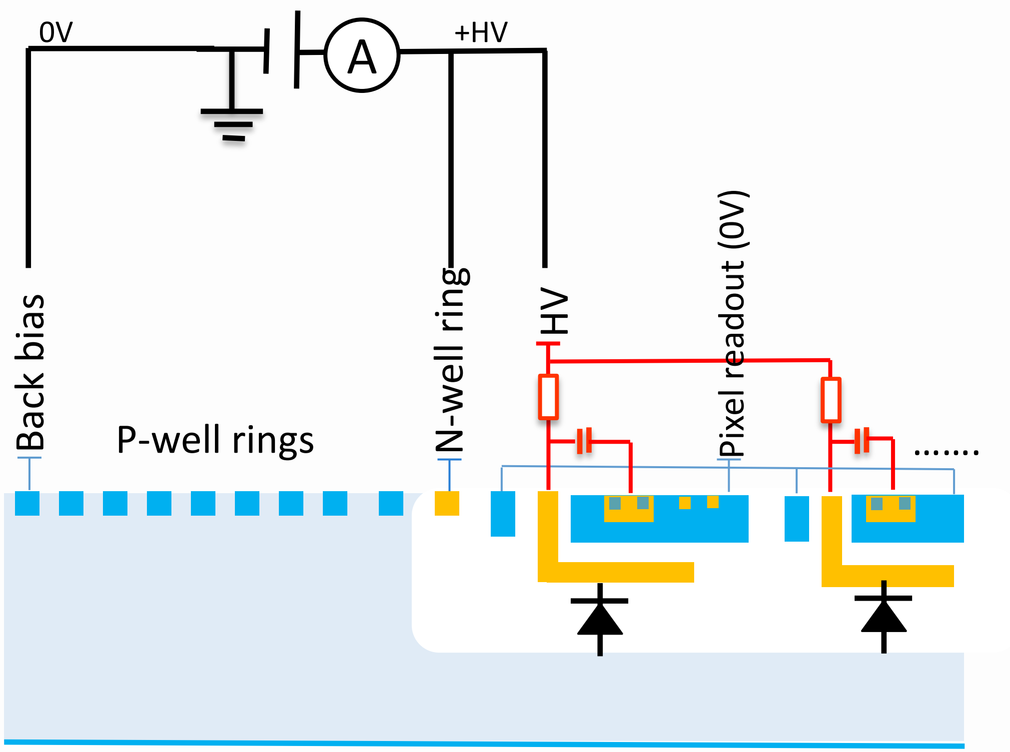


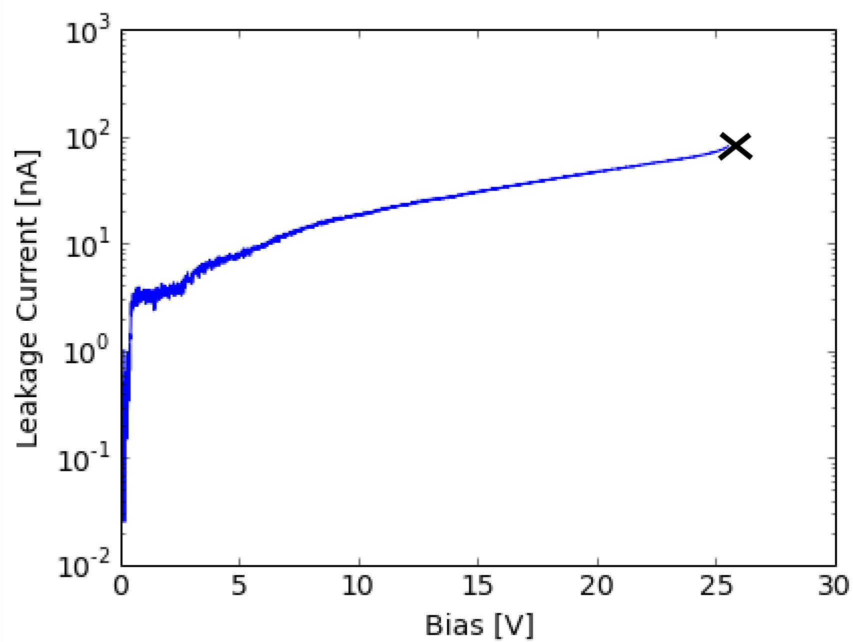
Breakdown = -114V

Measurement results – breakdown voltage

- IV curves (Version B)

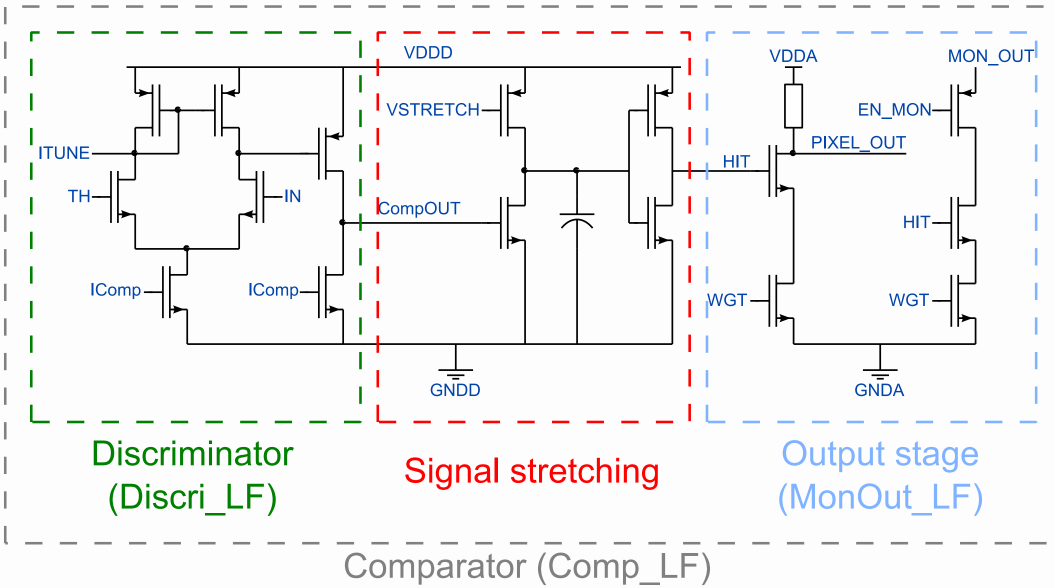
positive high voltage on collection well, “HV”
HV and electronics are coupled with C

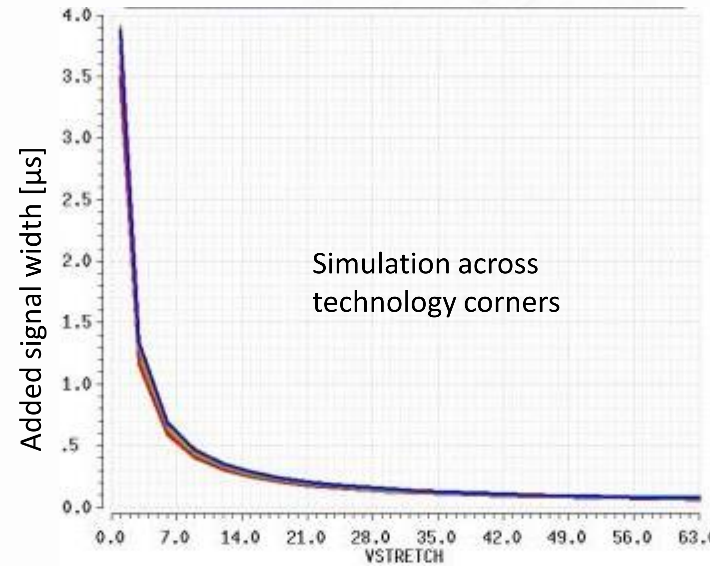


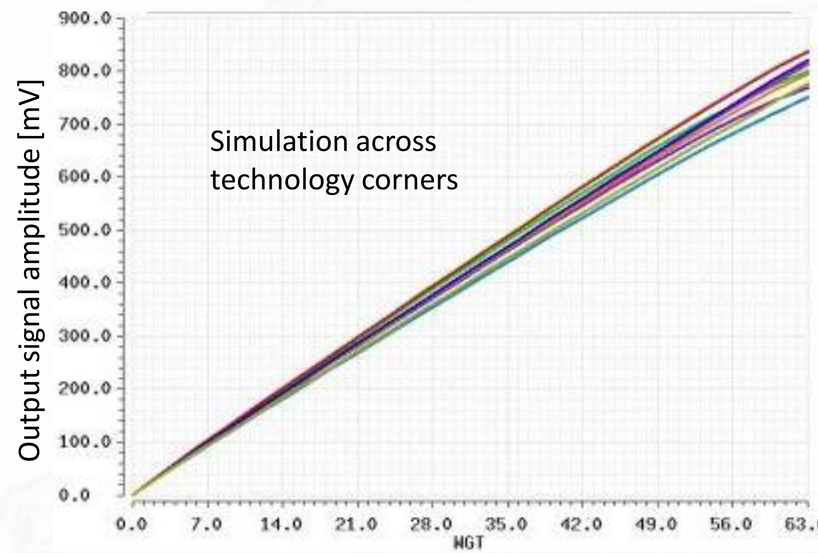


High voltage was applied without breaking the capacitor

In-pixel comparator and output stage

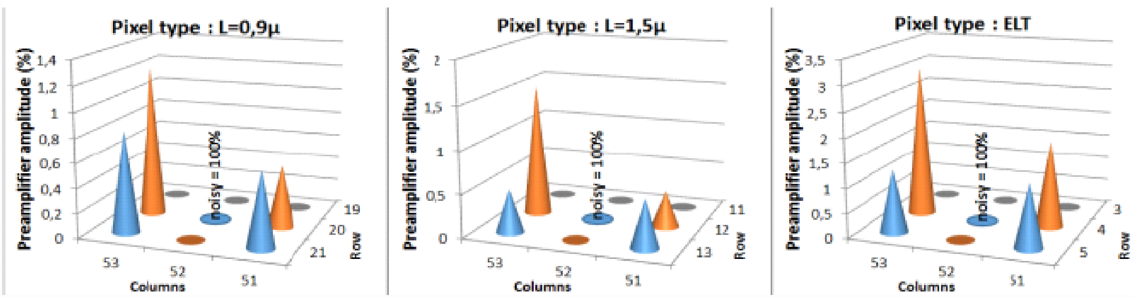




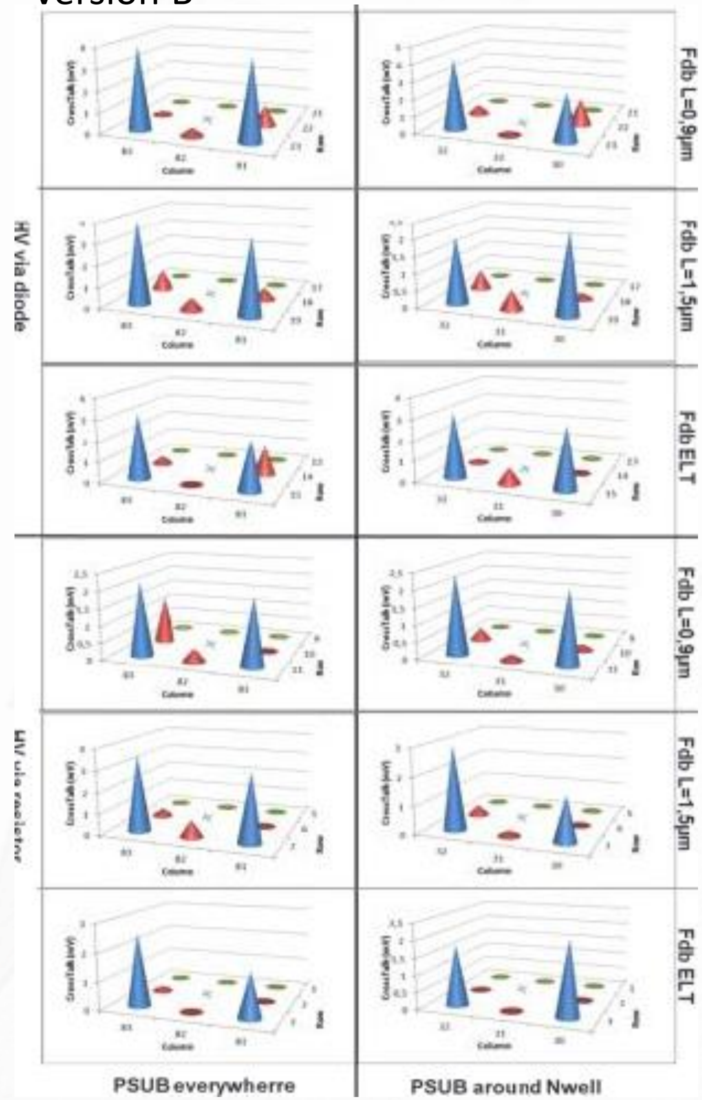


Crosstalk between pixels

Version A



Version B

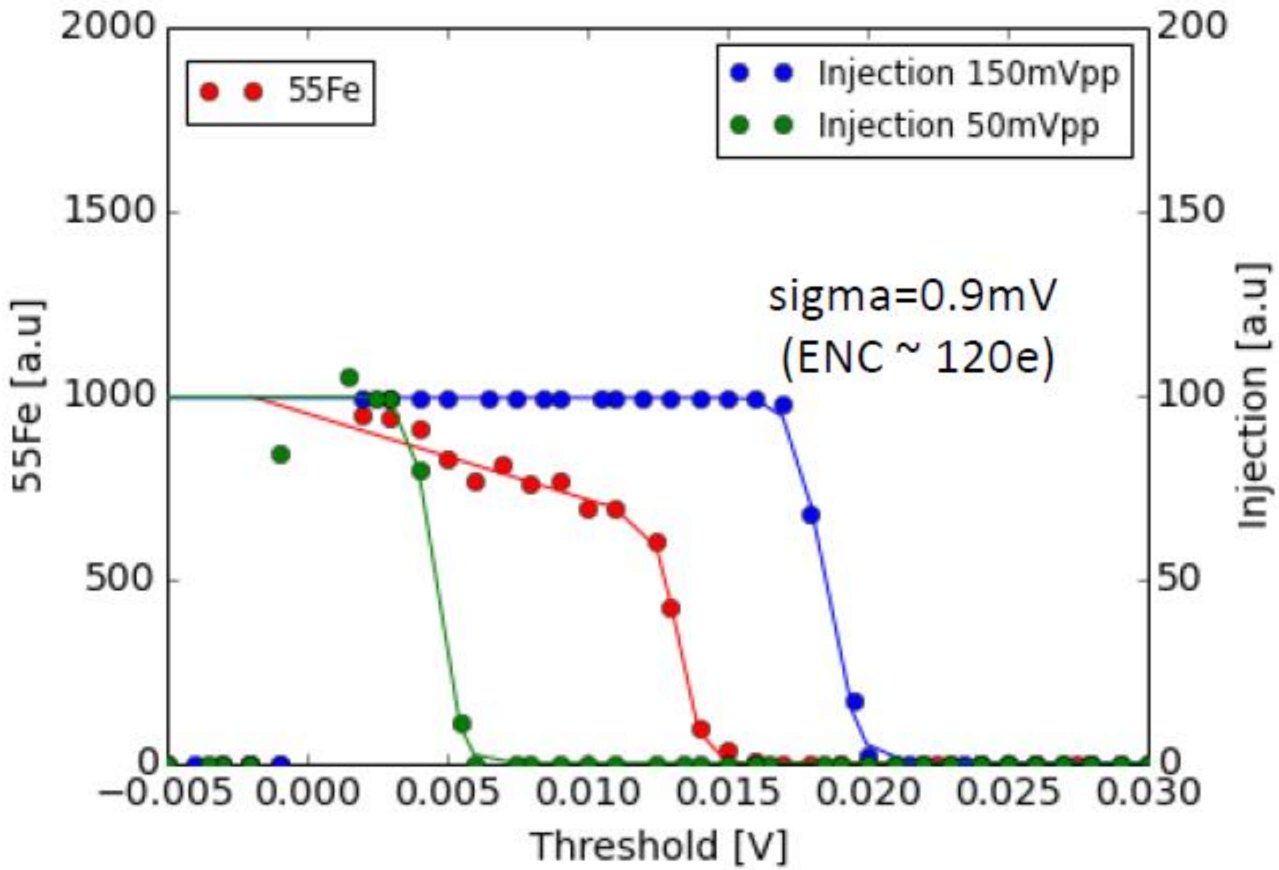


S. Godiot

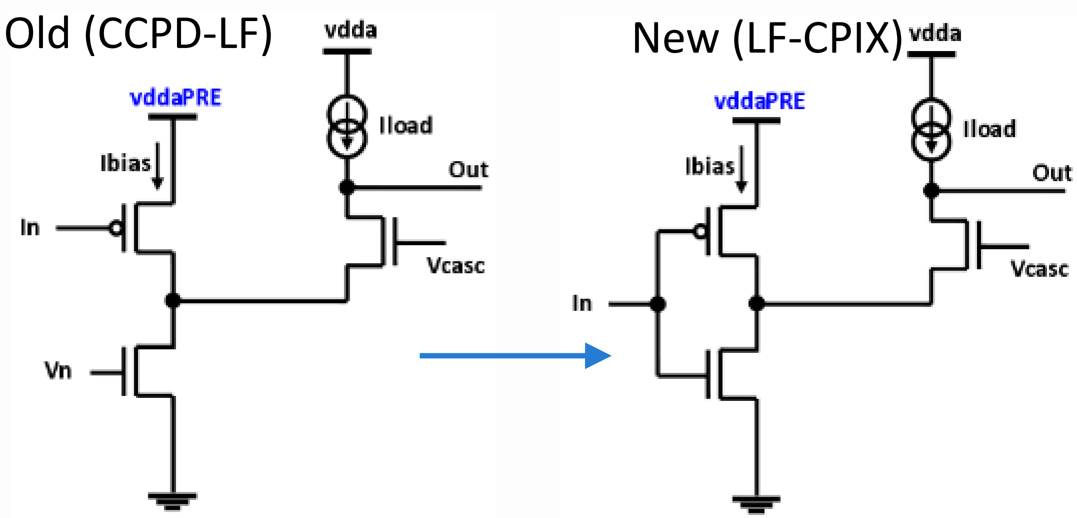
- Measured on a submatrix of 3 × 3 pixels
- Pixel in the middle is injected (1V ≈ 12 ke^-), Th = 1V, BL = 0.75V
- Crosstalk is very small and comparable between versions A and B

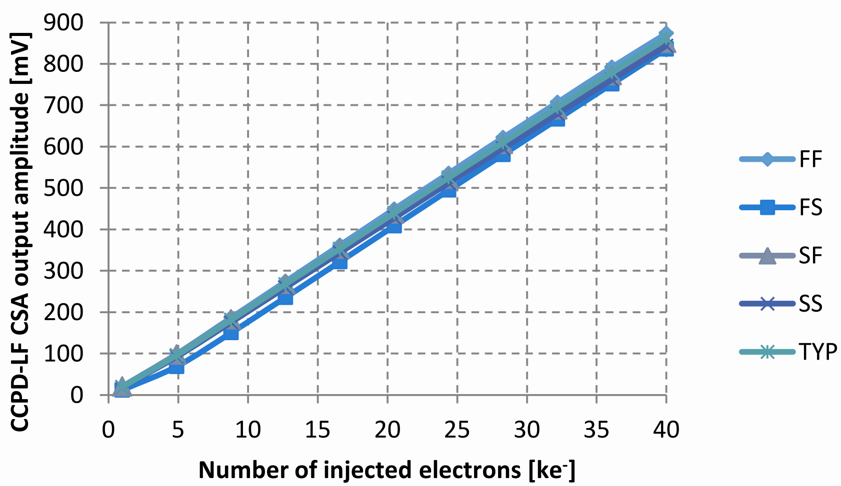
Threshold scan

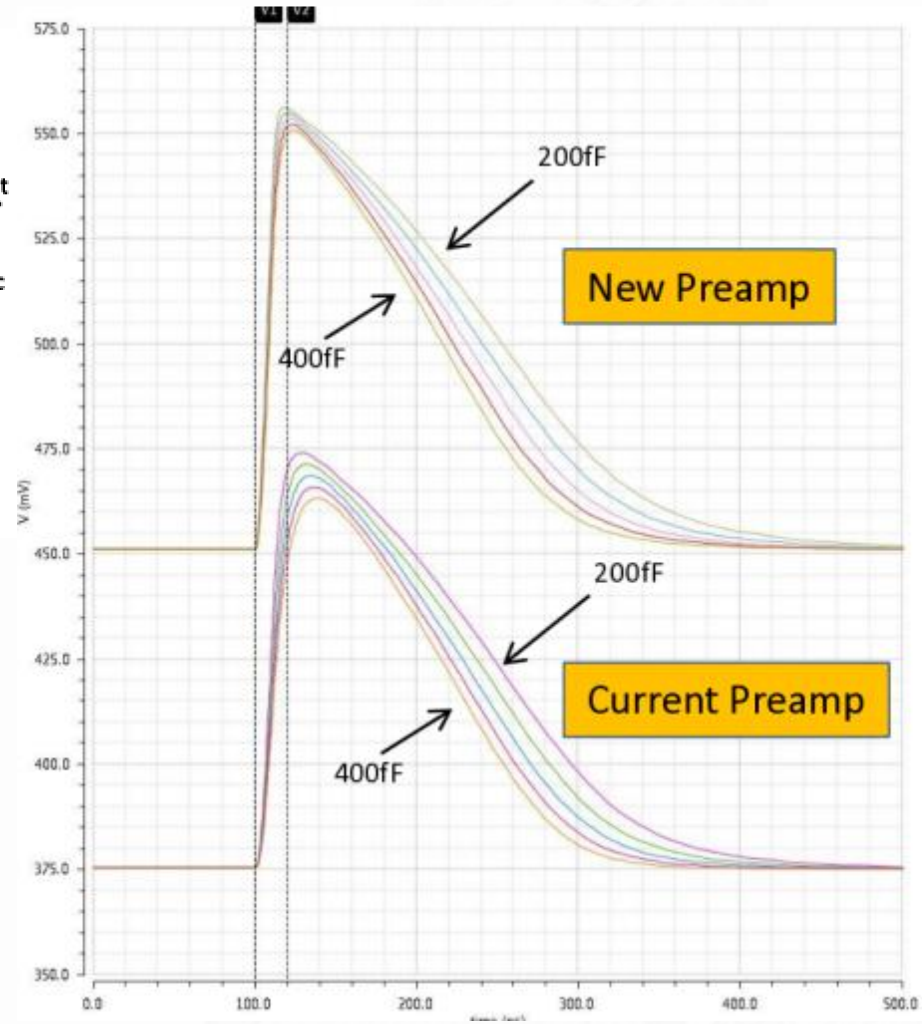
Chip: CCPDLF B
Pix: [14,14]
preamp [14,14] ON
mon [14,14] ON
inj [14,14] ON
Global DACs: default
HV: 20V (19nA)
Injection: Agilent 33250A
Freq. 1kHz



CSA – old and new

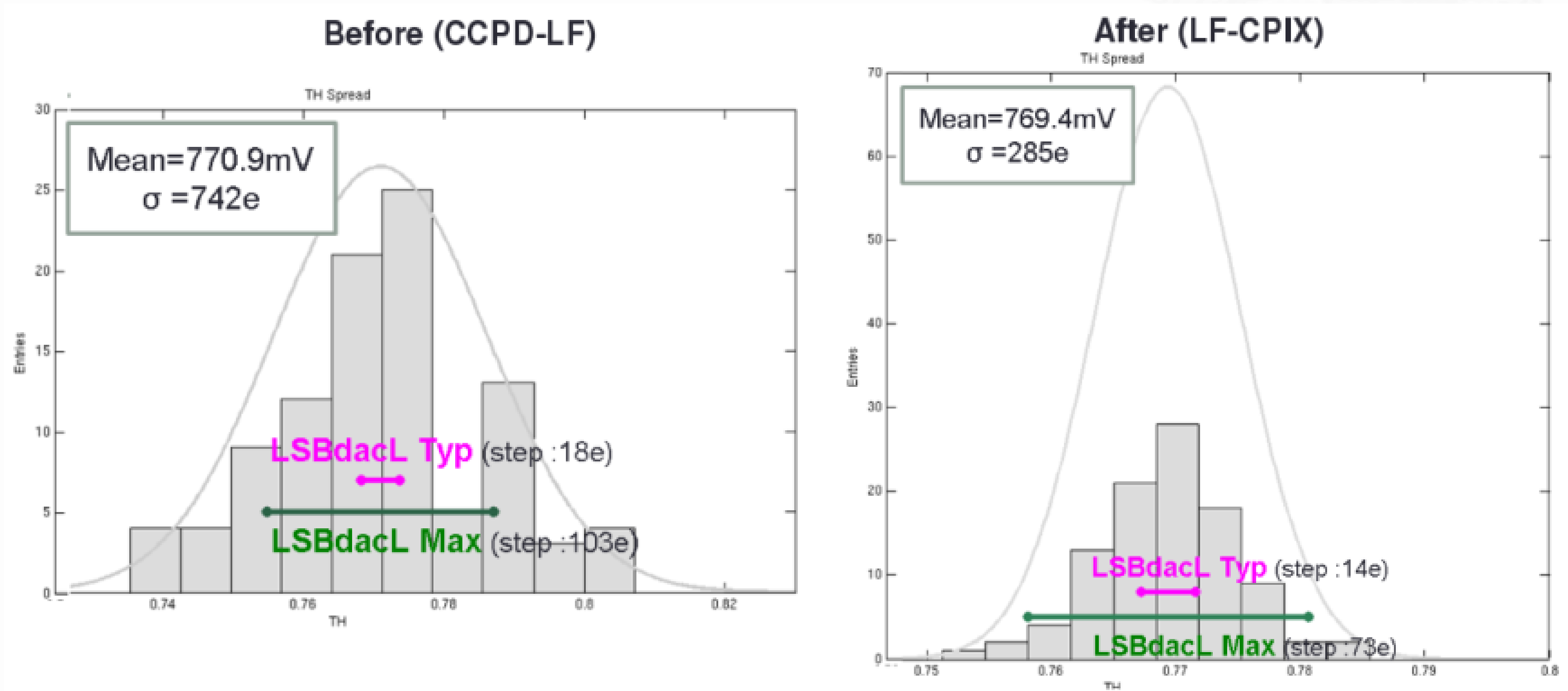






LF-CPIX - improved comparator

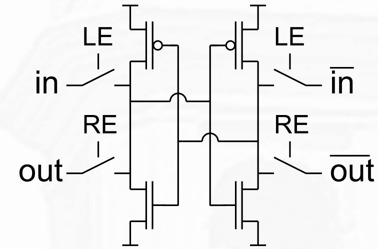
- Comparator's architecture remained the same, but re-scaling transistors allowed to significantly reduce threshold dispersion



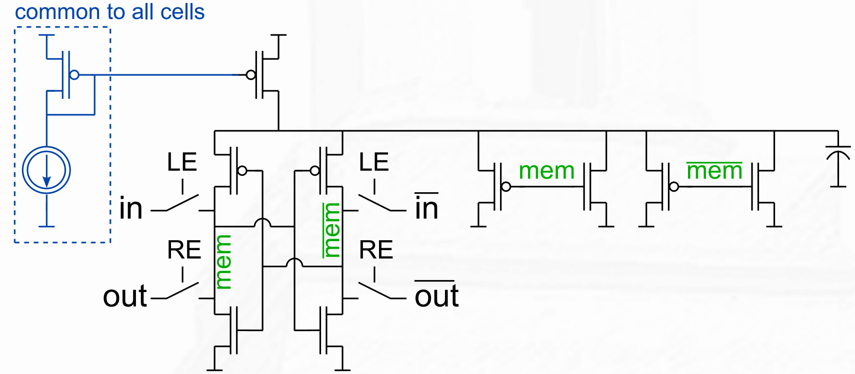
CPPM (S. Godiot, S. Kipfer, P. Pangaud)

SRAM – other kinds

- Standard CMOS SRAM
  - Smallest area
  - No control over slew rate



- Current steering CMOS (CS-CMOS)
  - Nearly constant current consumption
  - Lower noise due to slew rate control with mirror bias
  - Each cell consumes constant current ($1\mu A$)
  - Twice bigger area than standard CMOS



- CMOS SRAM with source follower
  - SF drives bit line (big, common to all pixels), not the memory element itself
  - Only two current mirrors ($\approx 20\mu A$) per column