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Versatile Routing Unit for Measurements of Time-Dependent Pulse-Height Spectra

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VERSATILE ROUTING UNIT FOR MEASUREMENTS OF TIME-DEPENDENT PULSE-HEIGHT SPECTRA

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A routing unit for the sorting of pulse-height spectra into 16 different time groups is described. The widths of the time groups can be chosen independent of each other in increments of 10^{-4} of the total time range. Possible group widths are 10 μs to 10 s for use with the built-in 100 kHz oscillator and 100 ns to infinity using a suitable external pulse train generator.

1. Introduction

The rapid progress in nuclear particle detectors and low-noise amplifiers and the availability of faster, cheaper, more compact and more reliable electronic components have led to the development of high-resolution analog-to-digital converters which require large amounts of memory space for optimum equipment utilization. Large memories, in turn, offer a wide variety of possibilities in addition to the straightforward accumulation of a one-parameter spectrum.

Manufacturers of fixed-wired multichannel analyzers usually provide sophisticated programmer units for the adaptation of their systems to the needs of the experimenter. Little attention, however, has so far been given to the problem of storing a series of pulse-height spectra taken at different times. A real-time clock equipped computer can, in principle, do the job, but the generation of the time group number keeps the computer busy for a sizeable fraction of total time and thus considerably reduces the acceptable event rate.

A routing unit was therefore developed for use with both fixed-wired and computer-served systems that allows repetitive accumulation of pulse-height spectra in different time intervals. The problem has been solved previously by McCarthy et al.[1]) who generated the interval address by feeding a dc voltage from a suitably triggered ramp generator into an additional ADC, and by Demuynck and Uyttenhove[2]) who essentially used the output of two successive univibrators to drive a chain of binary scalers the states of which are directly used for the addressing. Both these methods require some effort for obtaining ultimate accuracy and stability, and both generate intervals of equal duration.

2. Principle of operation

A different method was therefore chosen which, for accuracy and stability, depends only on the repetition frequency of a pulse generator. The widths of the intervals can be chosen independently, but for ease of operation the end of each interval coincides with the beginning of the next.

Fig. 1 shows the block diagram of the instrument; the timing can be seen from fig. 2. A pulse train P from a quartz-controlled oscillator (or, if another frequency is desired, from an external pulse train generator) is gated on or off by an externally generated gate signal G. If, e.g., the primary timing unit of the experiment is an accelerator, the gate will be opened by the trigger pulse T and closed by the pretrigger pulse R which is

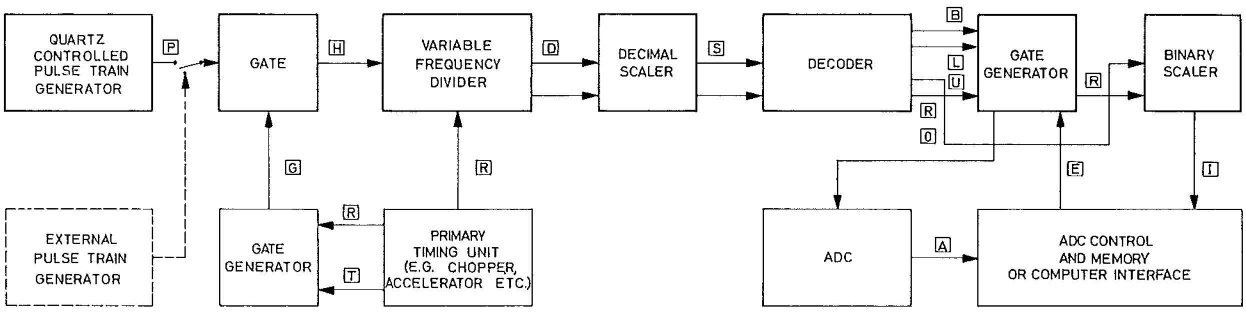

Fig. 1. Block diagram of routing unit (heavy boxes) and interconnections with primary timing and data acquisition equipment (light boxes) in a typical experiment.

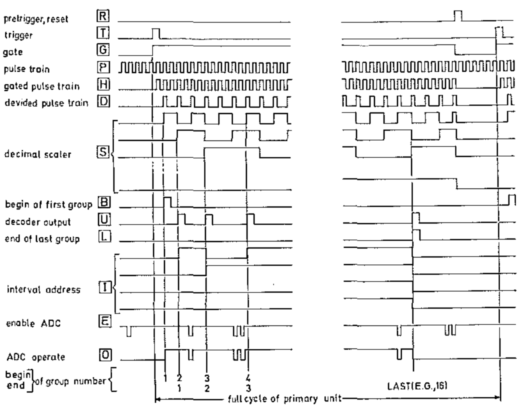

Fig. 2. Timing diagram. Settings are as follows: frequency divider = 2, start 1st interval = 1, 2nd interval = 2, 3rd interval = 4, 4th interval = 7.

also used to reset the whole unit. The frequency of the gated pulse train H is reduced by a frequency divider and the output D scaled in a decimal scaler. Whenever the state S of the scaler equals one of a series of preset values, a decoder delivers an output pulse U. The interval address I being equal to the number of U pulses minus one, all U pulses except the first are fed to a binary scaler whose output is the desired address. The enable signal E from the ADC control unit is gated according to the state of a flipflop which is set by the begin pulse B of the first interval and reset by the end pulse L of the last interval or the reset signal R, whichever occurs first. The resulting operate signal, O, prevents analysis by the ADC and transfer of amplitude data A to the memory unit before the begin of the first and after the end of the last time group.

3. Description of the instrument

The present version of the instrument is equipped with a 100 kHz oscillator, a frequency divider variable from 1 to 100 in 1–2–4–8 steps, a four-digit decimal scaler and a 16-group four-digit decoder. There is no reason, however, why any of these specifications could

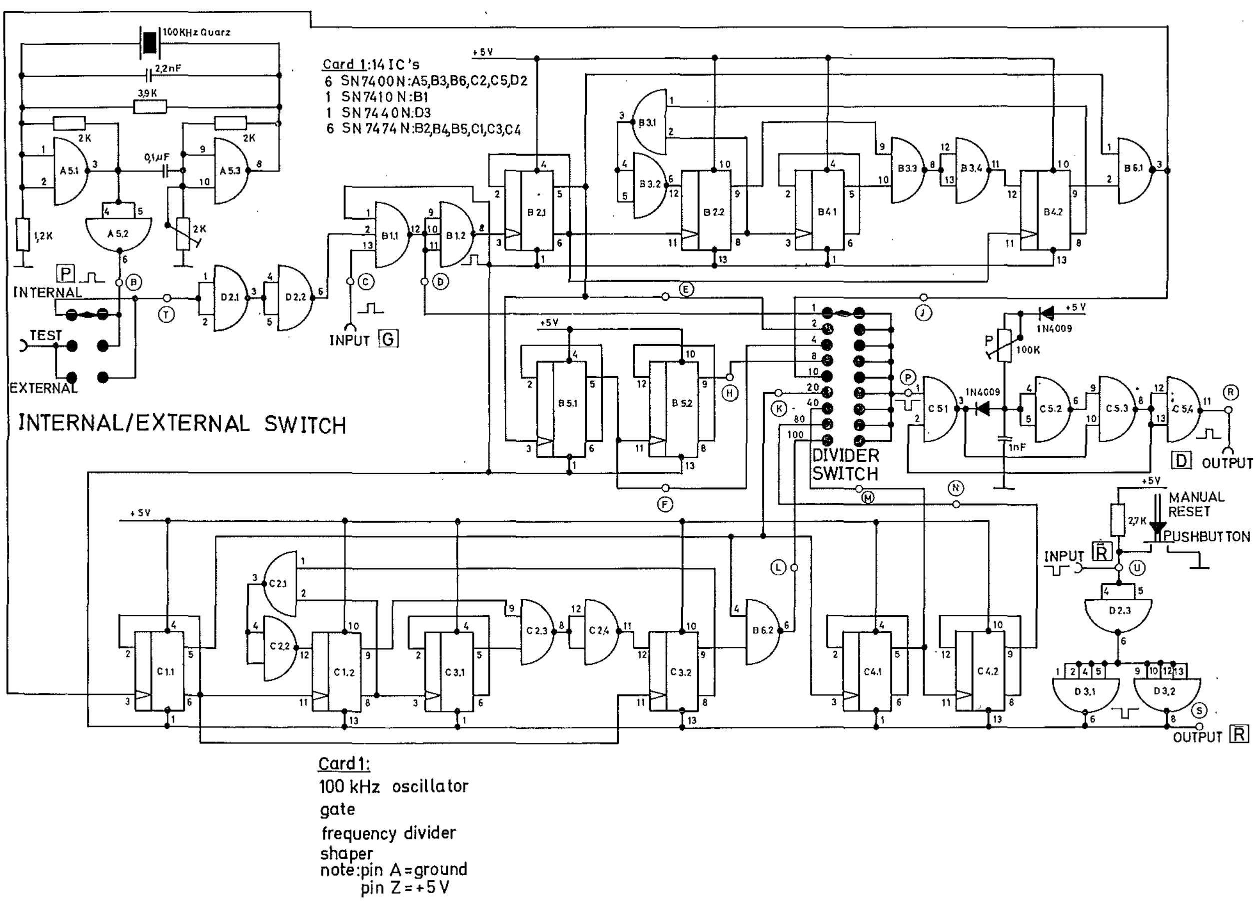

Fig. 3. Circuit diagram: card 1.

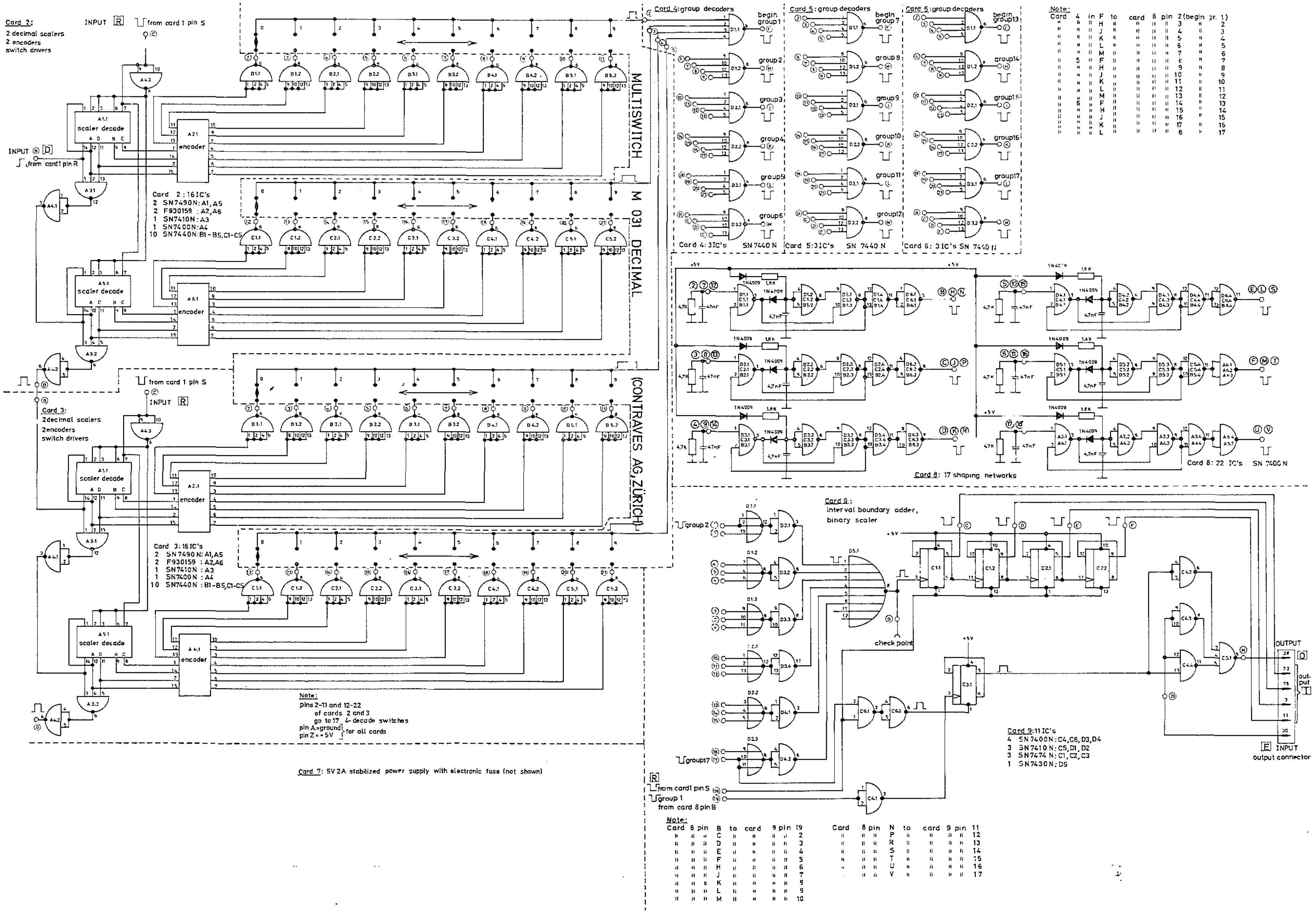

Fig. 4. Circuit diagram: cards 2 through 6, 8 and 9.

not be changed in a straightforward way according to the needs of a particular application. The whole unit is built from TTL integrated circuits. The frequency divider will accept pulse train frequencies up to 30 MHz, but its output should not exceed 500 kHz without modification of the shaping network (C5 on card 1), or 10 MHz with pins 12 and 13 of C5 directly connected to the divider switch output.

The details of the circuit are shown in figs. 3 and 4. The whole unit is arranged on 9 cards; circles denote connector pins, squares denote signals (note that complementary signals are often used), and the position of each logic unit is characterized by a letter corresponding to the row of the IC on the card (from top to bottom), by a number corresponding to the column (from left to right), and by another number corresponding to the number of the system within the IC. Card 1 contains the quartz oscillator, the gate, the frequency divider with output shaper, and the power gate for the R signal. Each of cards 2 and 3 contain two scaler decades, encoders, and group selection switch drivers. Cards 4 through 6 contain the decoders for the generation of the 17 interval boundary pulses, card 7 (not shown in the diagram) the 5V 2A power supply, card 8 shaping networks for the 17 outputs of cards 4 to 6, and card 9 the adder for the interval boundary pulses 2 through 17, the binary scaler, and the gate generator for the O signal.

4. Performance

The instrument has been used for several months in a variety of applications including spectroscopy of short-lived nuclides and tests of stability and temperature dependence of electronic quipment. A short error analysis is given below.

As can seen from fig. 2 the interval boundary time t and associated absolute uncertainty Δt (relative to the opening time of the G signal)

$$t \pm \Delta t = \begin{cases} f^{-1}(\tfrac{1}{2}-\tfrac{1}{2}x) \pm f^{-1}(\tfrac{1}{2}-\tfrac{1}{2}x)\Delta f/f \\ \pm f^{-1}(\tfrac{1}{2}-\tfrac{1}{2}x)(1 \pm \Delta f/f) \quad \text{for } g = r = 1 \\ \\ f^{-1}(gr-\tfrac{1}{2}-x) \pm f^{-1}(gr-\tfrac{1}{2}-x)\Delta f/f \\ \pm \tfrac{1}{2} f^{-1}(1 \pm \Delta f/f) \quad \text{for } g \text{ or } r \neq 1 \end{cases} \tag{1}$$

depend on the oscillator frequency $f+\Delta f$, the width

$$w = x/f \qquad (0 < x < 1) \tag{2}$$

of the D signal, and the settings r and g of the frequency reduction and interval boundary controls. The absolute inaccuracy, long term instability, and temperature walk of the frequency f were measured to be

$$f \pm \Delta f = 100 \text{ kHz} (1 + 0.1000 \times 10^{-3} \pm 0.0013 \times 10^{-3}/\text{day} - 0.0020 \times 10^{-3}/^\circ\text{C}). \tag{3}$$

Thus the time error Δt associated with the third and fourth term in the expression (3) for f is of the order of a few ppm under normal operating conditions. If $\Delta f/f$ is negligible only the systematic error from the opening of the gate at some random phase of the oscillator remains, and eq. (1) reduces to

$$\Delta t/t = \begin{cases} \pm 1 & g = r = 1 \\ \\ \pm 1/(2gr - 2x - 1) \approx \pm 1/(2gr), & g \text{ or } r \neq 1, \end{cases} \tag{4}$$

i.e. for best accuracy gr should be made as large as possible. For the present setup the maximum values of r and g are 100 and 9999; thus an error $\Delta t/t$ of 10^{-3} or less is achieved for time interval boundaries between 5 ms and 10 s. Clearly, a higher oscillator frequency and larger reduction ratio extend this range to shorter and longer times.

Another possible source of error may arise from the pulse-height dependence of the conversion time of some (e.g., Wilkinson type) ADC's. In cases where neither the error nor the counting losses due to the introduction of a constant (maximum) ADC deadtime can be tolerated, this problem is easily solved by adding another register which is only updated while the ADC is not busy. However, because for present-time ADC's (100 MHz oscillator frequency, 8k channels) and interval widths $\geqq 50$ ms less than 10^{-3} counts would, on the average, be stored in the wrong interval, this feature was not included in the present instrument.

I gratefully acknowledge the help ot Mr. H. Schreiber.

References

[1]) A. L. McCarthy, B. L. Cohen and L. H. Goldman, Phys. Rev. **137** (1965) B 250.

[2]) J. Demuynck and J. Uyttenhove, Nucl. Instr. and Meth. **74** (1969) 97.